SiTRA brief status report to the EUDET S.C., August 31st 2009

Members:

Helsinki University and VTT(Helsinki), LPHNE-UPMC/CNRS-IN2P3 (Paris), Charles University in Prague (Prague), IFCA-CSIC/U. of Cantabria (Santander)

Associated Institutes:

IMB-CNM (Barcelona), KIT (Karlsruhe), Obninsk State University (Obninsk), INFN-Torino University (Torino), IFIC /CSIC (Valencia), HEPHY (Vienna)

Outline

- More t.b. infrastructures
- Alignment
- Combined test beams: achieved or achievable
- Transnational access
- Contributions to conferences & EUDET memos

More test beam infrastructures

This year SiTRA members and associated collaborators have been developing more test beam infrastructures.

⇒ Test infrastructure to host new alignment system test beam at the SiLC test beam at SPS H6b test beam: 15-31 August. (HEPHY, IFCA) (see alignment section)

⇒ Upgrade of an existing Faraday cage and associated readout and full DAQ system (LPNHE) (see next slide)

⇒Preparation of new modules for combined test beam with calorimeter expected in 2010 (LPNHE)

⇒Preparation of the mechanics for a combined test with the Mechanical EUDET prototype (End Cap) (LPNHE with EUDET calorimeter colleagues).

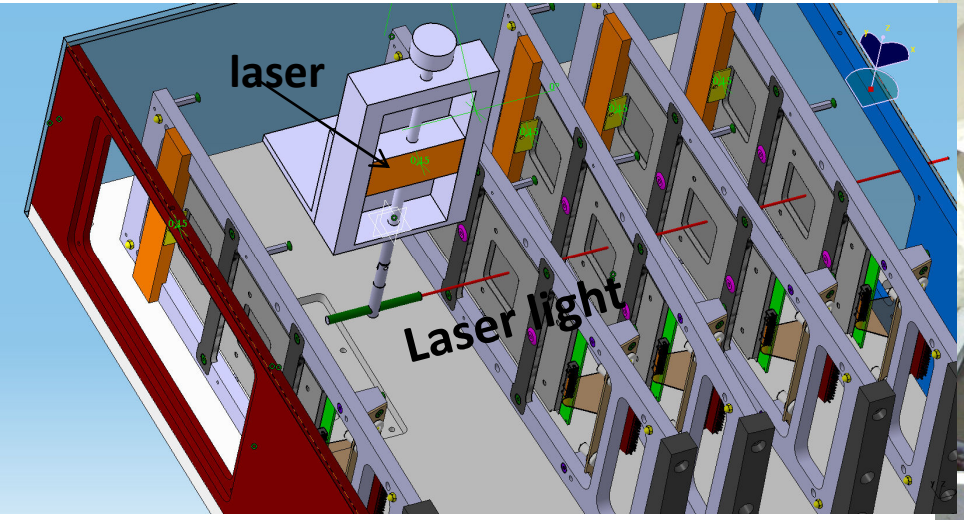
=> Latest on the mix mode FEE chip

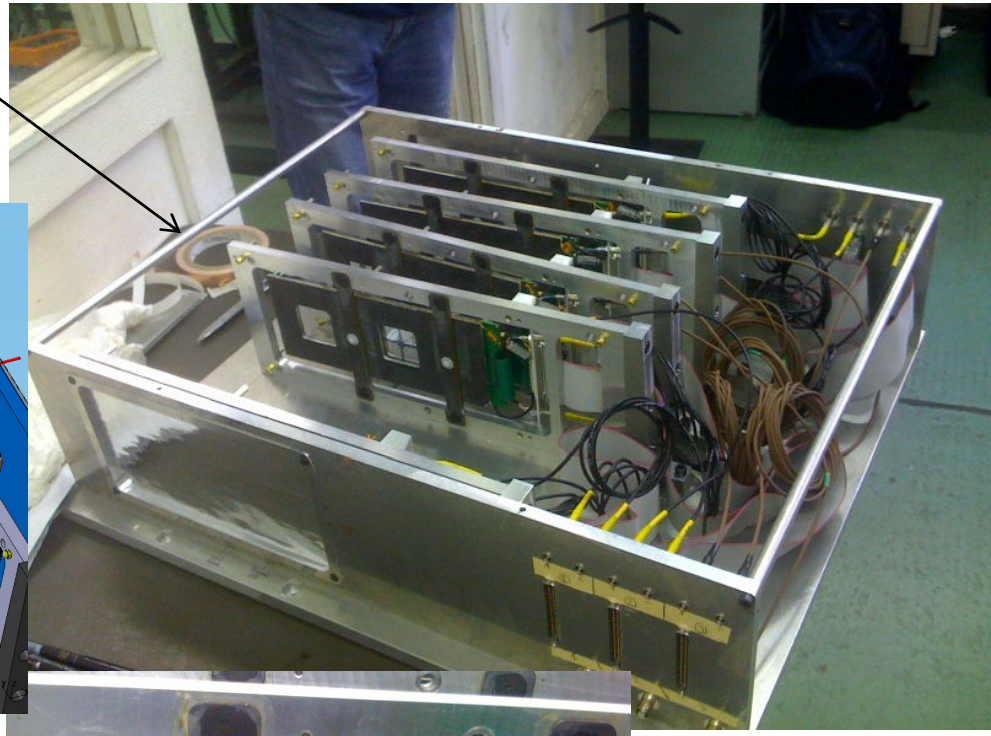
The preliminary results on the August test will be reported at the Forthcoming Annual EUDET Meeting. The status and some results on the last 4 points will be presented at this meeting as well.

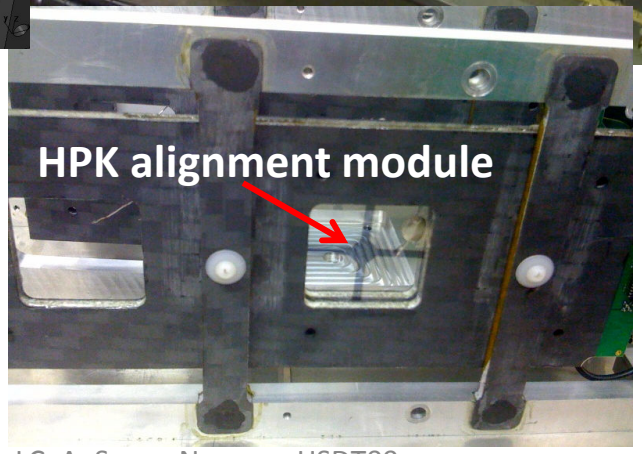
Ex: Upgrade of an existing Faraday cage (LPNHE)
(here with HPK friendly alignment equipped modules)

The Faraday/Cooling cage developed last year as test infrastructure has been upgraded with the main following features:

- IR laser included on the" roof "with vertical displacement







- New FE boards and related FPGA and cabling, adapted both for ref readout based on VA1' and new FEE chips.
- New VHDL and C++-ROOT based readout package.

Ready for test beam (see later)

Alignment

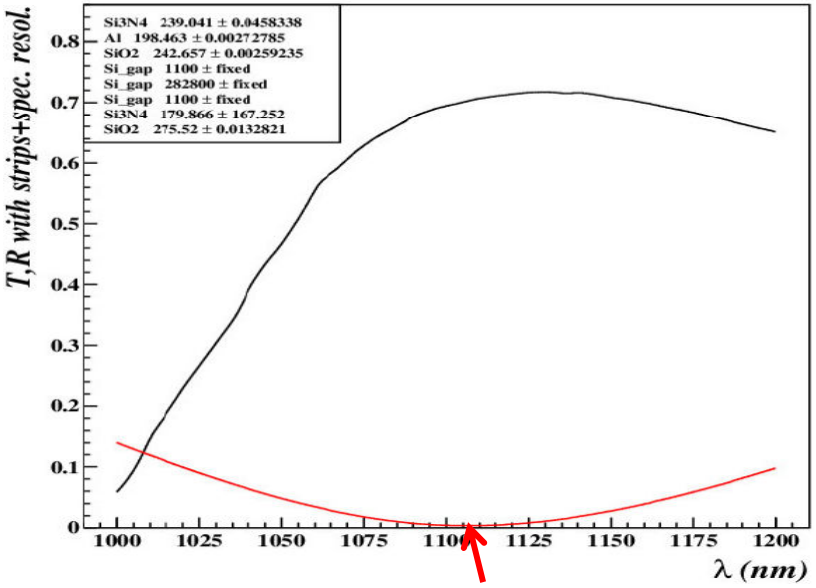
EUDET Work-package under the responsability of IFCA-Santander

R&D on new IR transparent detectors

Goal: Transmittance up to 70%

In the framework of SiLC & EUDET, an R&D is conducted for developing IR transparent sensors with transmittance T up to at least 70% (*20% for usual alignment sensors*). The higher transmittance the more sensors can be aligned with a single beam.

A detailed simulation study (*the most complete in the field so far*) was performed by ***M. Fernandez-Garcia (IFCA and former EUDET fellow***) for determining the key parameters to increase T.



Key parameters defined by Marcos

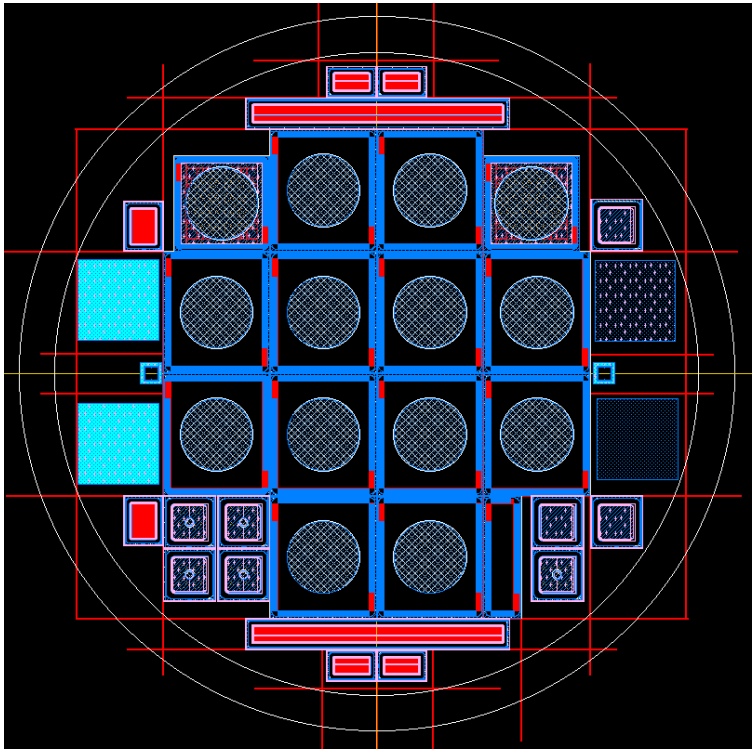
1) No need for 3rd party antireflection coating. (ARC). Passivation layers are used as ARC
2) Metal strip width chosen to minimize reflectance (10% of pitch)
3) Thickness of different layers optimized to achieve maximum transmittance. Outcome depends mostly on thickness of outermost passivation layers.

Followed by the fabrication of these new sensors **by IMB-CNM** (M. Lozano et al.) , before going to industrial transfer. Next slide show the production of the 1st batch

R&D on IR transparent detectors

Goal: Transmittance up to 70%

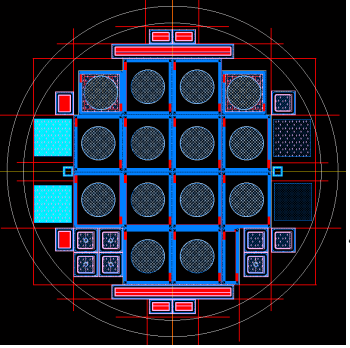
Tests on these new sensors were performed on a preliminary batch end of July at the IMB-CNM production line. The wafers include:



- 12 different detectors
- Common parameters:
- active area= 1.2x1.5 cm^2
- circular window in the back metal (r=0.5 cm)
- 256 readout strips with 1.5 cm length
- 9 guard rings and scribe line with n-well
- 6 detectors completed with floating intermediate strips for improved spatial resolution using the capacitive charge division principle.
- Optical test structures needed to characterize each material

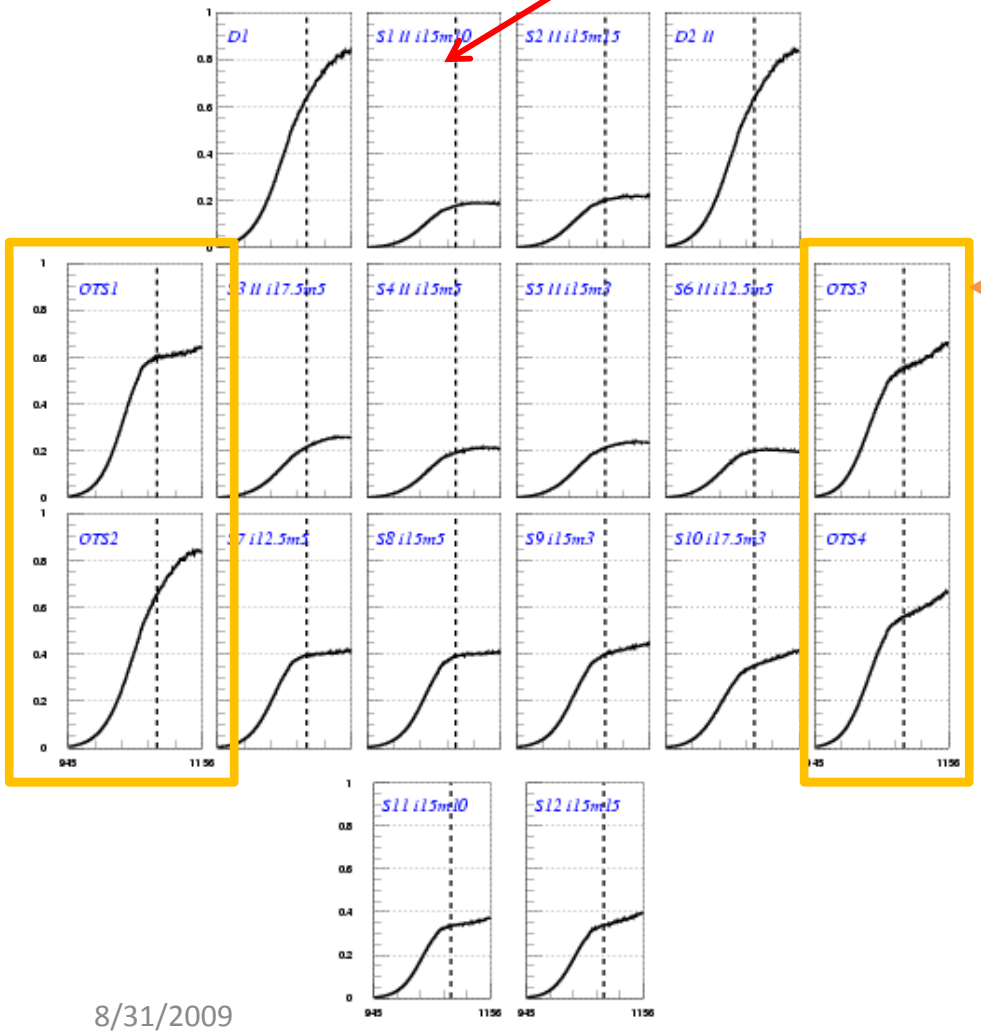
Goals:

Study of effect of intermediate strip on optical transmittance
Characterization of T,R versus metal and/or implant width

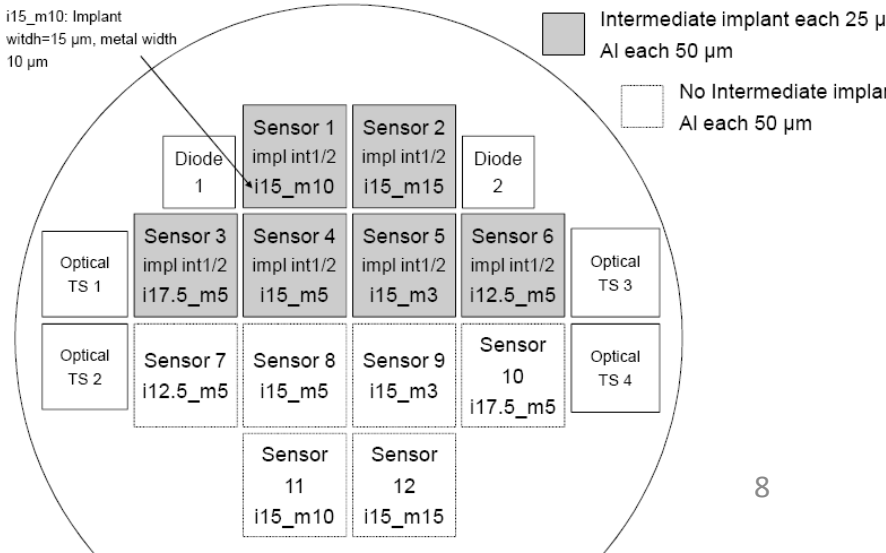


Intermediate results from photometric measurements July09

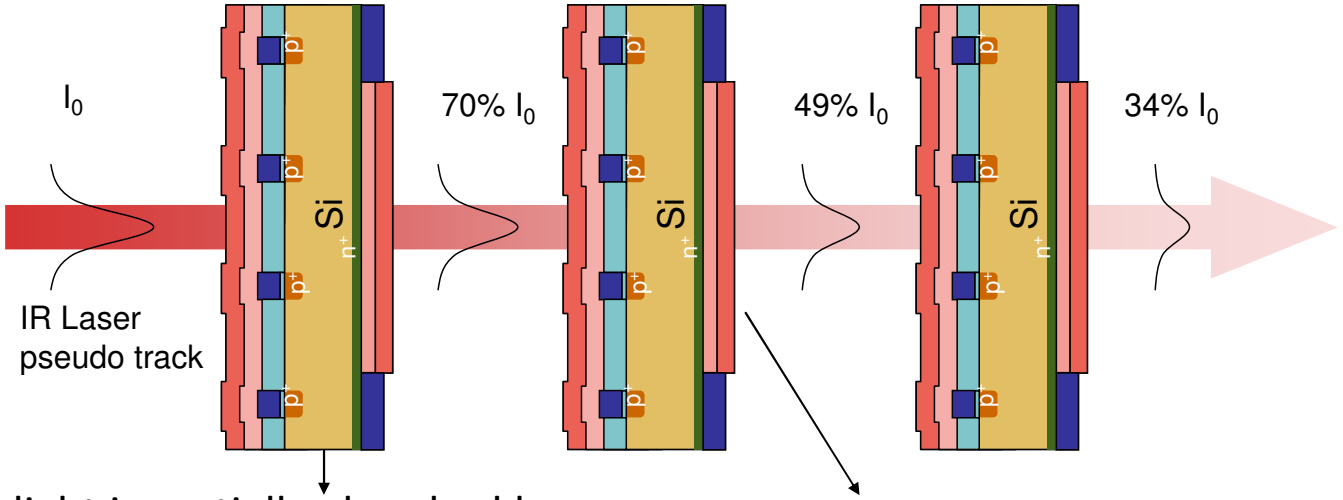
S1 ii i12.5 m5 = Sensor 1, intermediate implant, implant width 12.5, metal width 5

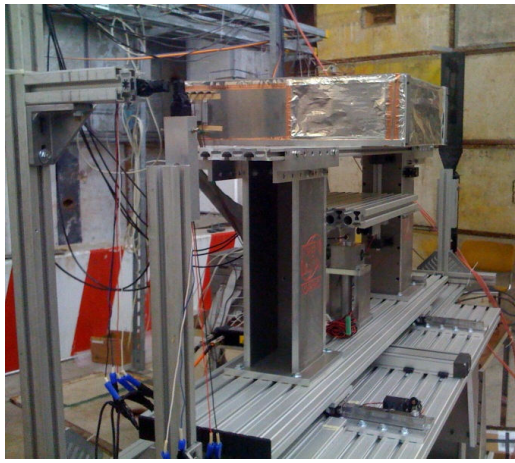


- Intended as "control" measurements. Two layers still missing (so absolute %T is not representative)
- First in-situ measurements during production of wafers.
- Analysis of optical test structures agrees very well with simulations.
- Analysis is ongoing. Outcome will be the thickness of the 2 missing layers to have 70% transparency



IR transparent detectors (IRTP)





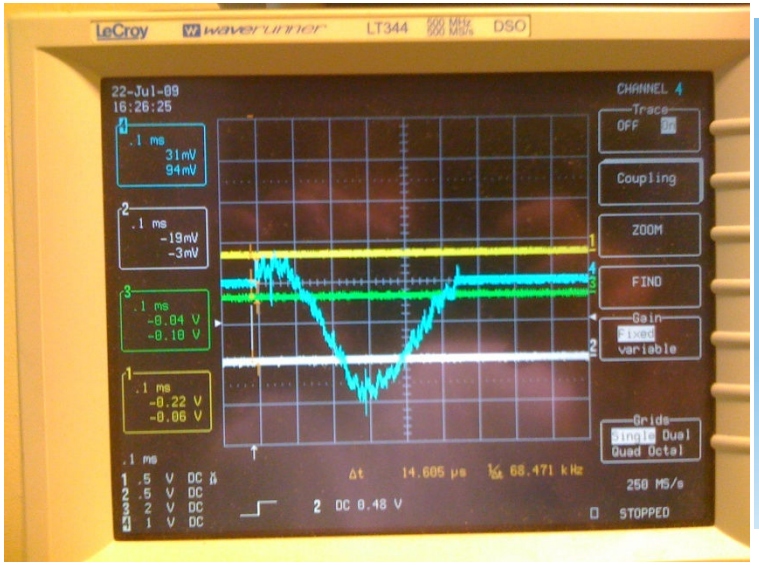
IR light is partially absorbed by Si detectors

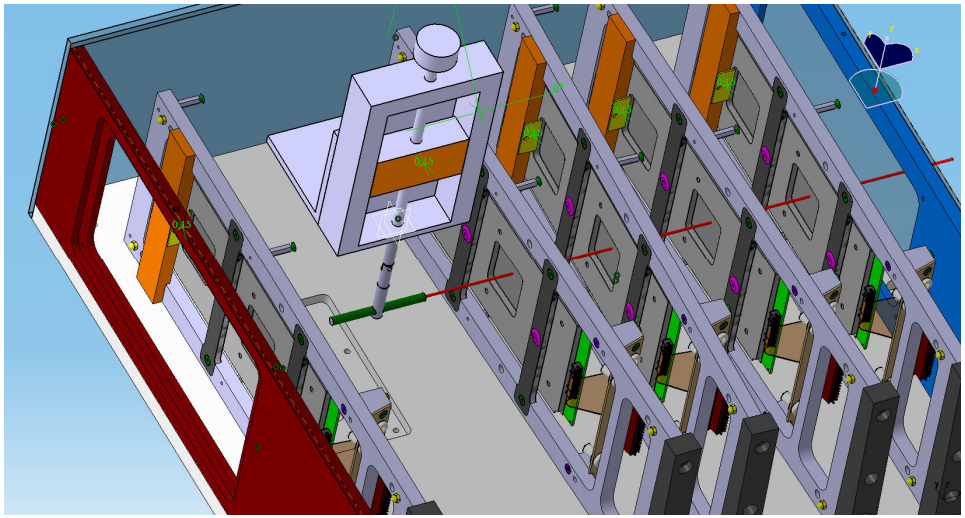
Φ≈1mm open in the Al allows beam-through

Expected transmittance ≈ 70% (HPK alignment sensors ≈ 20%); Tests on 3 consecutive modules equipped with IRTP with IR laser and at the SPS test beam in 2010-2011.

The aim of this development was to find the best optimized design with “standard materials” (SiO2, Si3N4, Si), followed by a *technological transfer* to an industrial firm for large production => **in good shape**: Full production in October 2009

Alignment preliminary Measurements





Preliminary response to IR laser of the HPK friendly alignment as measured with the upgraded faraday/cooling cage (LPNHE)

Much more to come from SiLC CERN test beam and related alignment measurements at the Annual Meeting.

Combined test beams:

1. SiLC test beam at SPS CERN combined with MAPS EUDET telescope
   Combines alignment system test including 2 modules made with friendly alignment sensors produced by HPK for SiLC (HEPHY)
   Just finished today August 31st at SPS CERN . Report on preliminary results expected for the Annual EUDET meeting.
   (HEPHY, IFCA and CU Prague)
2. Combined test beam with LCTPC at DESY
   Installed in June 2009, run by HEPHY and KIT with LCTPC collab.
3. Preparation of combined test beam with CALICE calorimeter
   Started at the mechanical level (LPNHE with Grenoble, LLR and LAL CALICE mechanical team). Report at the Annual Meeting
4. Under study: request for a combined test beam with Dual Readout
   More at the Annual meeting.

Transnational Access

2009:

- Torino: system tests in a Si infrastructure test setup in Paris

2010:

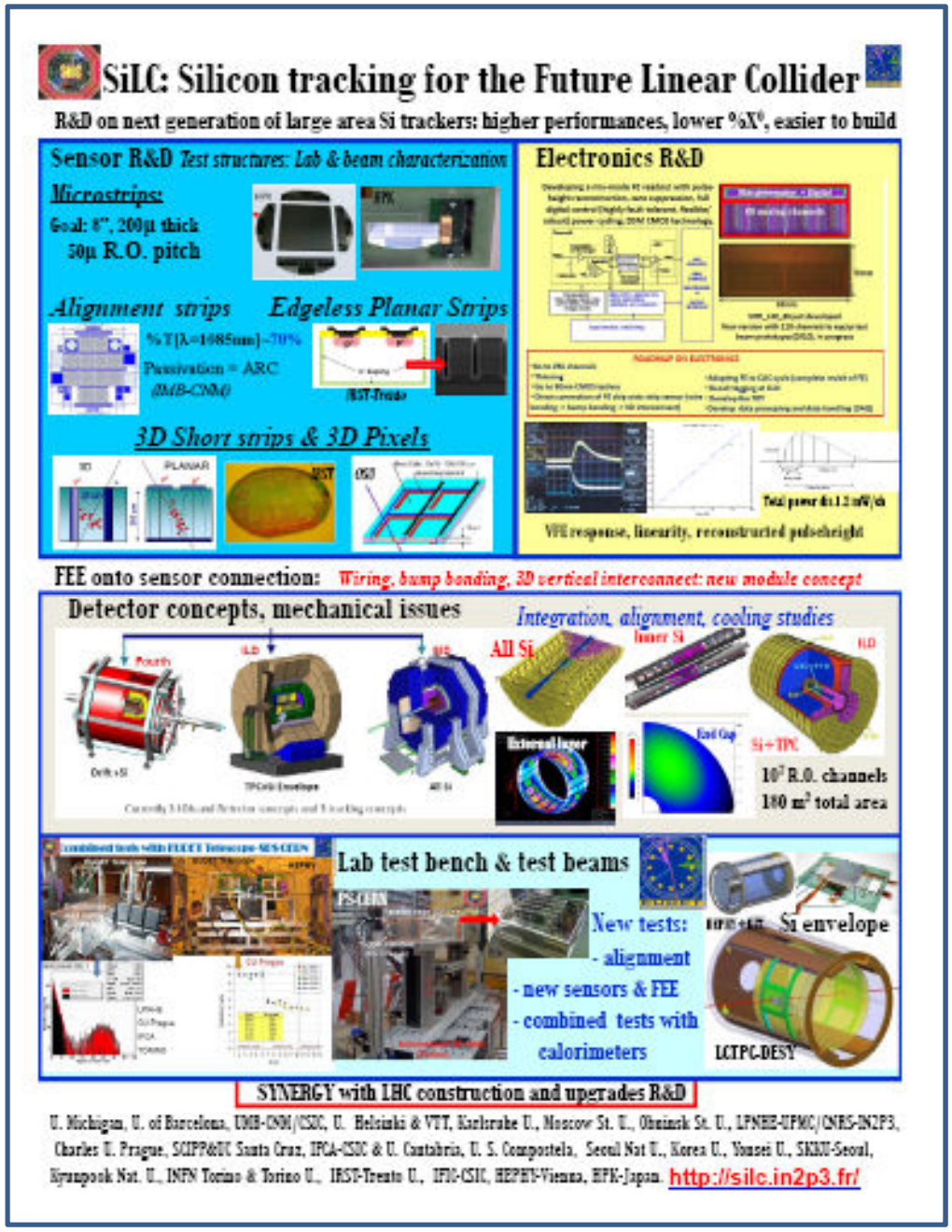
- The request to use our test infrastructure for the dual readout (Pisa and several other Italian teams)

Conferences, EUDET memos

Presentations given this year and publications:
-Papers submitted to the **Proceedings of LCWS08** on LCTPC (Stefan Haensel-HEPHY), Alberto Ruiz (Alignment) , Aurore Savoy-Navarro (FEE mix mode chip), A. Savoy-Navarro (Test beams results with Si prototypes); to be published.
-**TIPP09,** Tsukuba, March 2009, Than Hung Pham (LPNHE), mix mode FEE chip for strip Readout for LC (presentation) paper submitted to NIMA, accepted.
Poster presented by Thomas Bergauer
-**TiLC09**, Tsukuba (April 2009): A. Savoy-Navarro (mix mode FEE chip),
- **Lepton-Photon, DESY (**August 2009): Poster presented by A. Charpy
- **Symposium on Semi Conductors Tracking**,(August 29-Sept 1st) invited talk: A. Savoy-Navarro (including the developments and results from SiTRA) (see next slide)
More to come until end of the year....

- Contribution to **the ILC LOIs, March 2009** and related updates on:
SiD concept (mainly on alignment related issues)
and **ILD concept**: full responsibility on Silicon tracking section.

EUDET Memos in 2009: We expect to produce about 8 to 9 memos for 2009.
(under preparation)



Ex: Poster presented at Lepton Photon 2009