# FCAL: Status Report: (FEE)

M. Idzik for FCAL Collaboration

Department of Physics and Applied Computer Science
AGH University of Science and Technology

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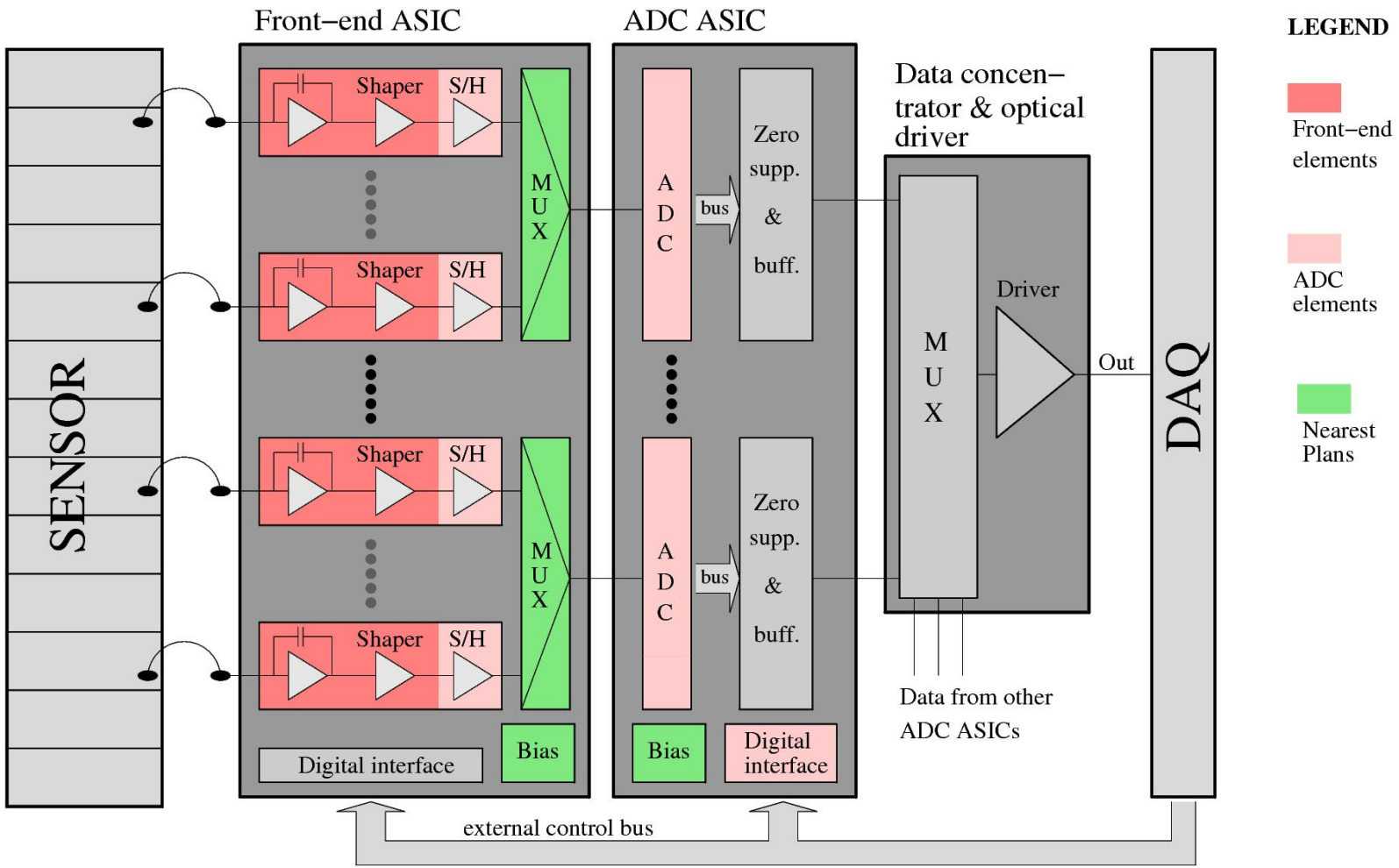
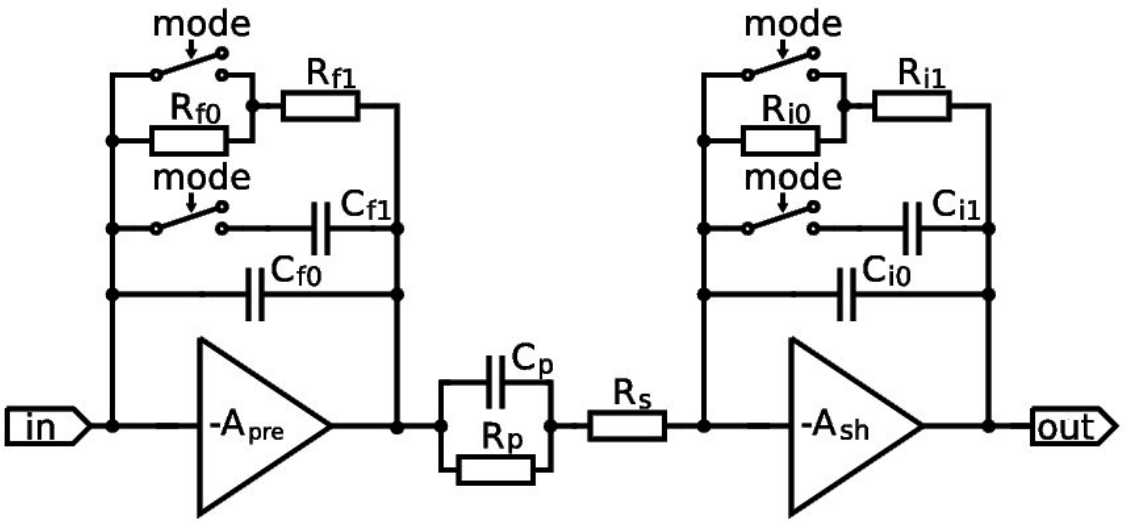
# Outline

# LumiCal Readout System



# Front-end requirements (old)



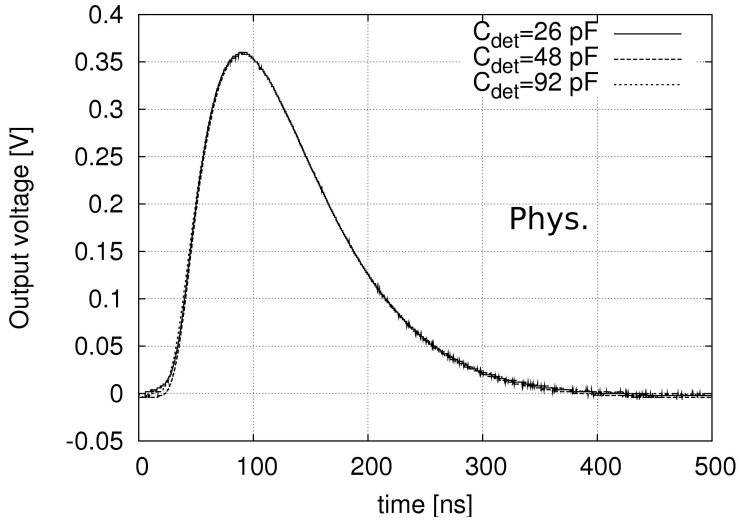

## Components

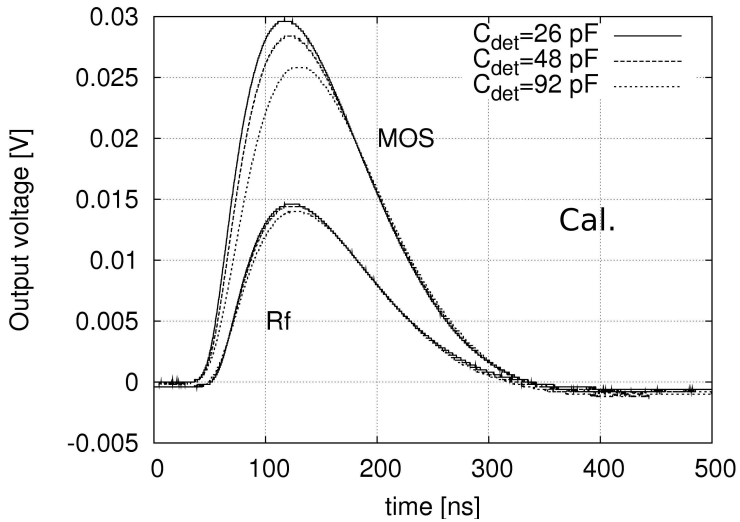
- Charge amplifier
- Pole zero cancellation
- 1st order shaper

- $C_{det} = 10 \div 100$ pF $\rightarrow$ charge sensitive amplifier
- $\Delta t \simeq 300$ ns $\rightarrow$ $T_{peak} \simeq 60$ ns
- Two independent modes: physics and calibration (MIP) $\rightarrow$ gain switched as a configuration option
- Physics mode: $Q_{max} \approx 10$ pC $\rightarrow$ $C_f \approx 10$ pF
- Calibration mode: $S/N > 10$ for MIP

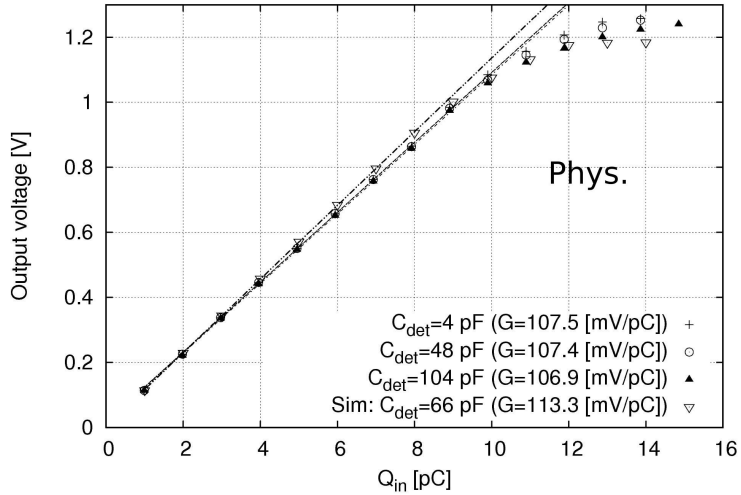
# Example pulse shape and linearity

## Pulse shape




## Gain




- For physics mode $Q_{in} = 3.3$ pC (upper left)
- In calibration $Q_{in} = \approx 10$ fC (left)
- Linear up to 10 pC

# Front-end parameters summary

| Mode | Gain [mV/fC] | Noise@50pF [fC] | Linearity [pC] | Rate [MHz] | Crosstalk [%] |
|---|---|---|---|---|---|
| Physics | 0.107 | 0.62 | 10 | 3 | ≈1 |
| Calibration | ≈20 | 0.28 | 0.035 | 2.5 | ≈0.1 |

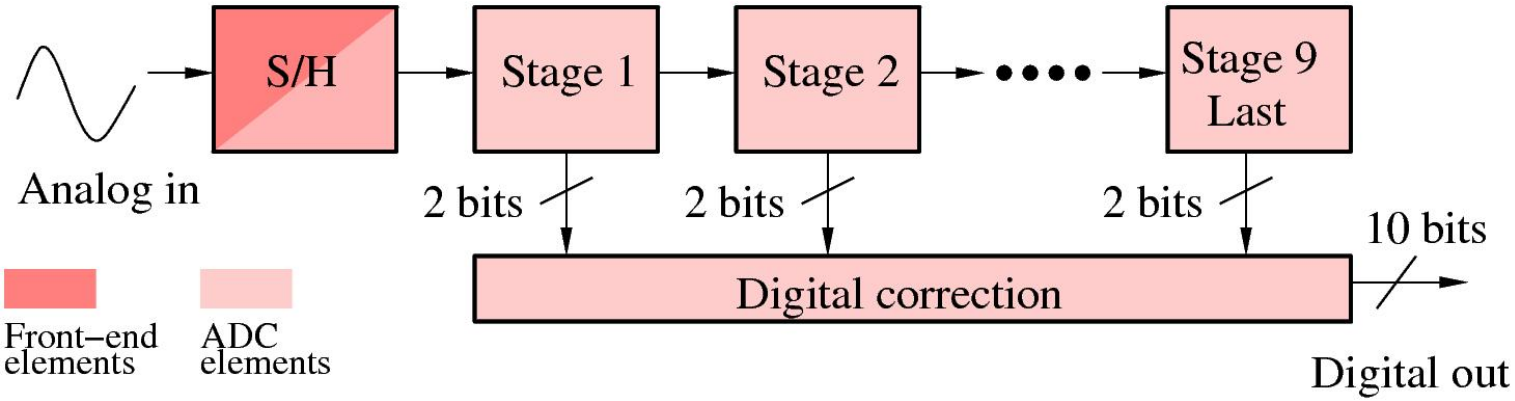
- Similar results for both $R_F$ and *MOS* configurations (MOS slightly better)
- Crosstalk needs to be measured with sensor fanout
- Power consumption per channel is 8.9 mW
- Noise in details:
  - $\mathrm{Noise}_{\mathrm{phys}}[\mathrm{aC}] = 522 + 2.08 \cdot C_{in}[\mathrm{pF}]$
  - $\mathrm{Noise}_{\mathrm{cal}}[\mathrm{aC}] = 48 + 4.65 \cdot C_{in}[\mathrm{pF}]$

# Front-end status and future plans

- Status
  - First prototype tested and ready for tests with sensor
  - Single prototype ASIC comprises of 8 channels
  - Parameters meet specifications
- Future plans
  - Tests with sensor and fanout
  - Measurements on test beam
  - Will we need new prototype ?, are there still some parameters to be fixed ? (Switching on/off needs to be added)

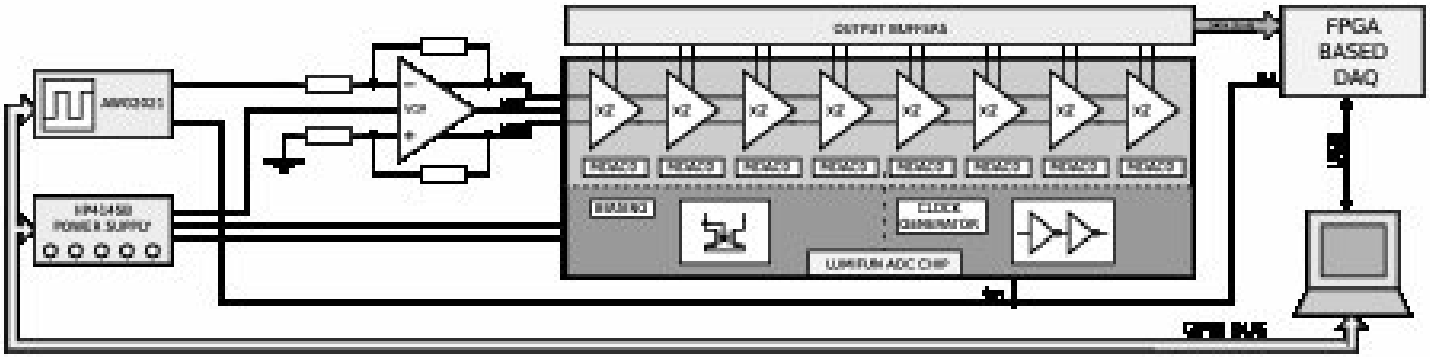
*M. Idzik, Sz. Kulis, D. Przyborowski, "Development of front-end electronics for the luminoisty detector at ILC" Nucl. Instr. and Meth. A 608 (2009) pp.169-174*

# ADC Requirements

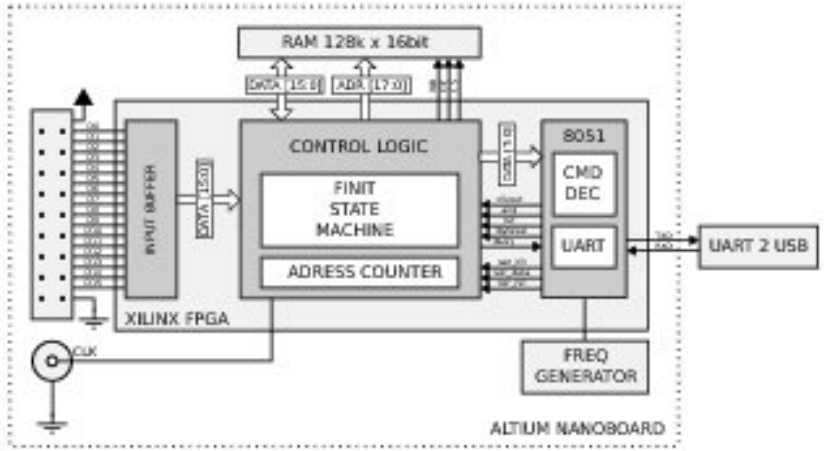



- Speed or clock frequency
  - 3MHz when one ADC per channel ← *most probable conf.*
  - 30MHz when one ADC per ∼8 channels
- 10 bits at the moment
- Power efficient & small area
- Fully differential pipeline architecture
- S/H can be a part of ADC or front-end channel → two prototypes with and without S/H designed

# ADC Test Setup



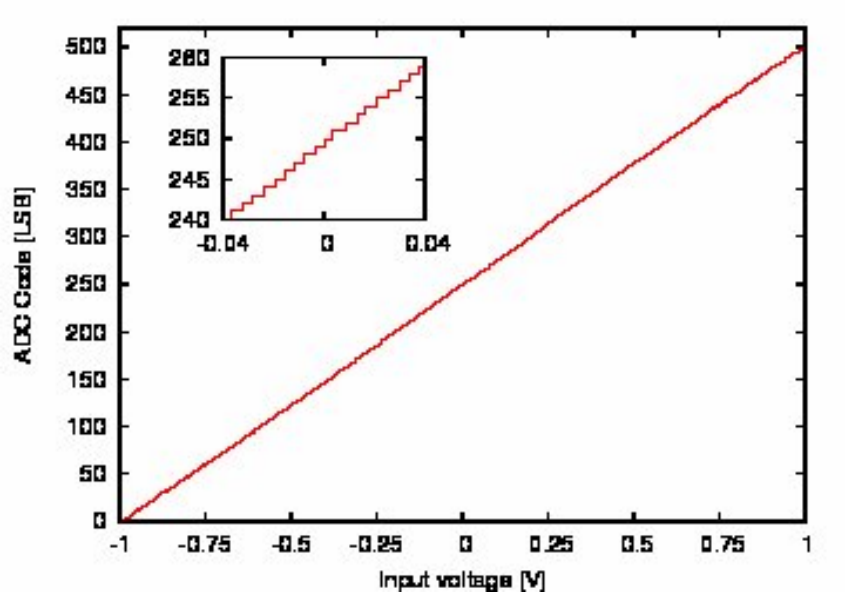

- Signal from AWG2021 generator
- External single-ended to differential converter
- Software digital correction (first prototype)
- FPGA based (Altium nanoboard with Xilinx Spartan2E) DAQ




FPGA based DAQ

# ADC - First prototype

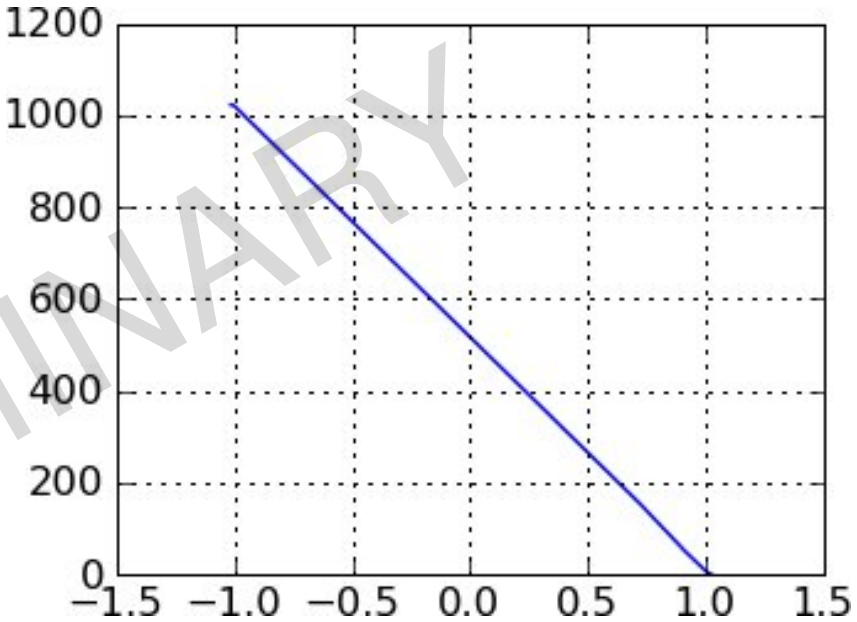
- Only 8 pipeline stages
- No digital correction
- Fully functional
- Works up to 35 MHz
- max INL < 3 LSB
- max DNL=-1 (few missing codes)




*M. Idzik, K. Swientek, S. Kulis, "Development of Pipeline ADC for the Luminosity Detector at ILC", Proc. 15th Int. Conf. "Mixed Design of Integrated Circuits and Systems" MIXDES 2008, Poznan, Poland, 19-21 June 2008, IEEE Xplore database*

# ADC - Second prototype

- All 9 stages + S/H
- Digital correction
- Clock and power switching
- No reference voltages yet
- Fully functional

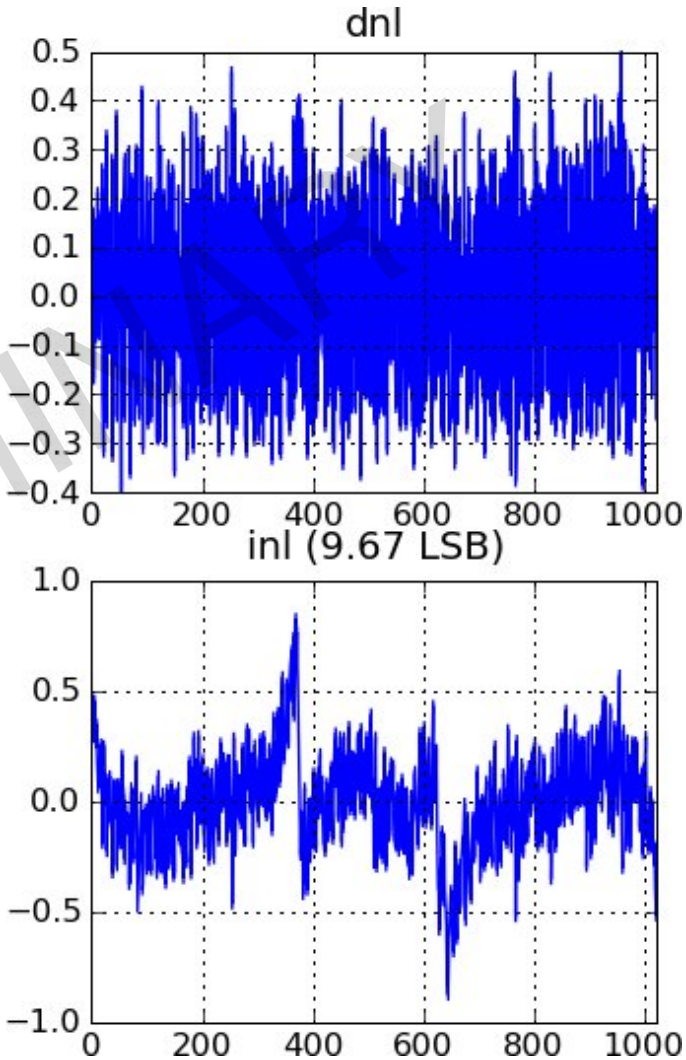





*M. Idzik, K. Swientek, S. Kulis, "Design and measurements of 10 bit pipeline ADC for the Luminosity Detector at ILC", will be presented at TWEPP2009, Paris september 21-25 2009, http://twepp09.lal.in2p3.fr*

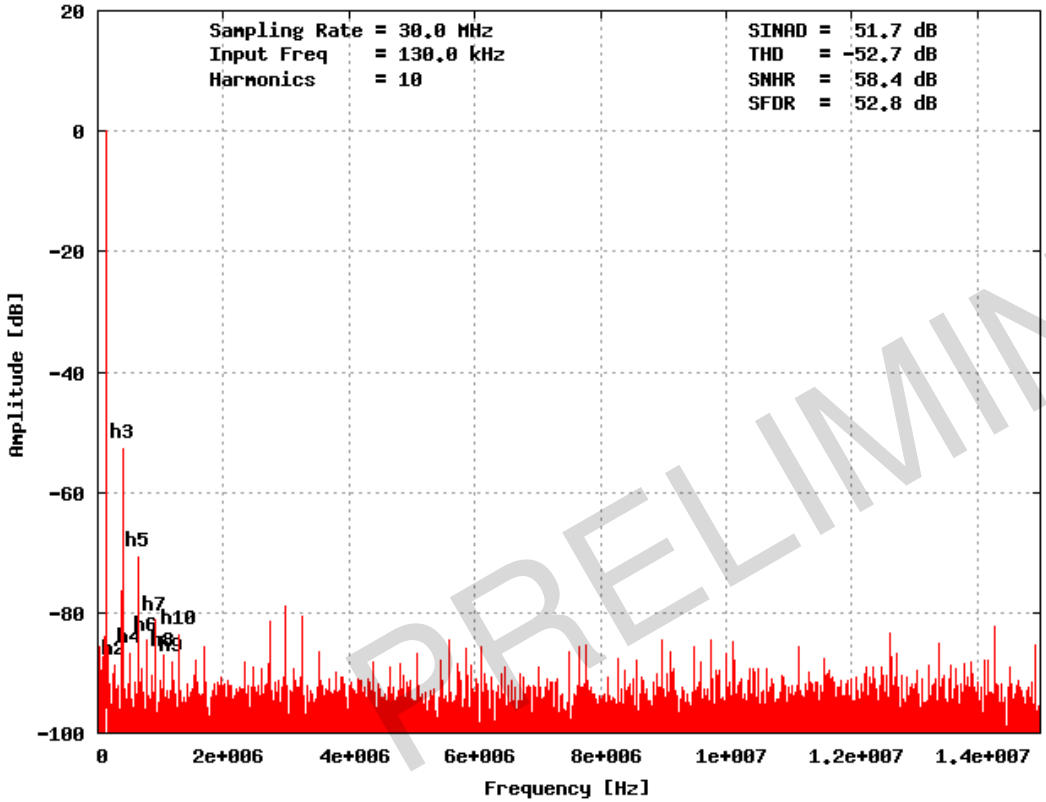
# ADC - Second prototype - linearity

- Good INL (<1LSB)
- Good DNL (<0.5LSB)
- Works up to 35 MHz



# Dynamic measurements 30 MHz

FFT spectre






- SINAD = 51.7 dB
- THD = -52.7 dB
- SNHR = 58.4 dB (9.4 bits)
- SFDR = 52.8 dB

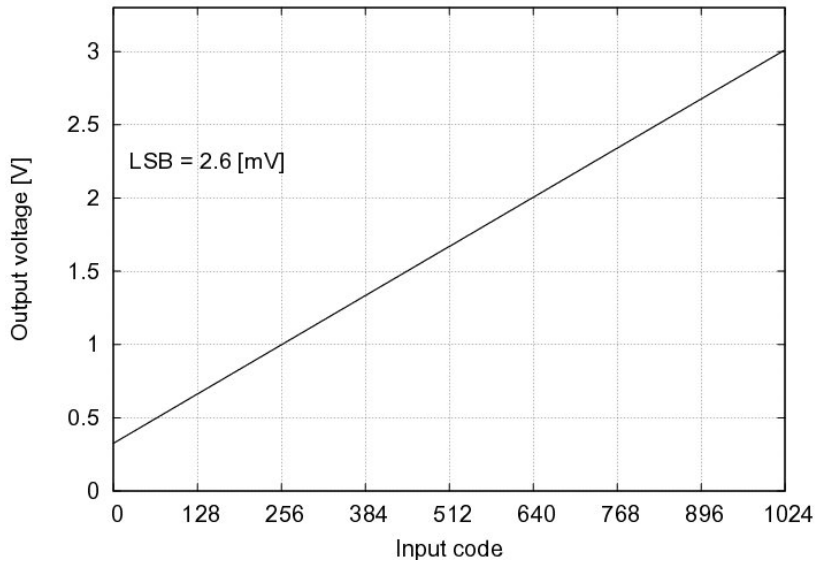
- Very preliminary, first measurements
- SNHR (noise) is good
- SINAD affected by harmonic distortions which may come from setup; pure differential sine signal generator needed...

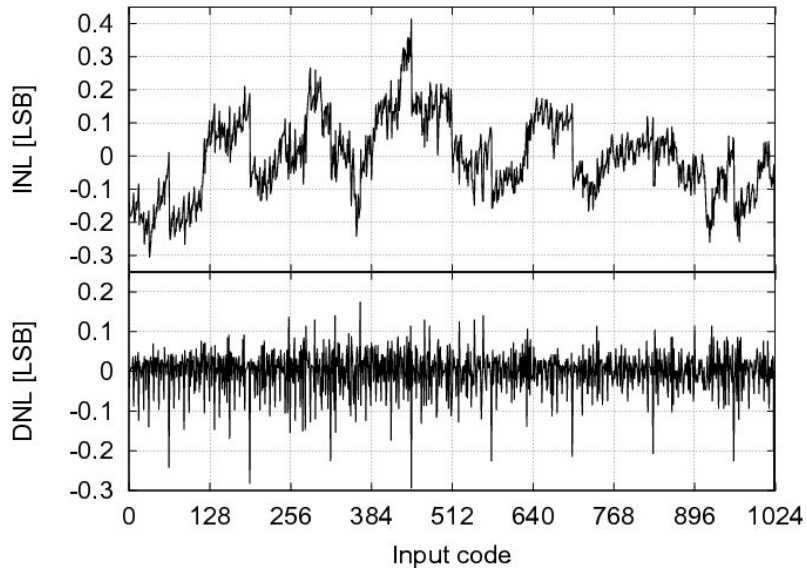
# ADC summary and future plans

- Summary
  - New 10-bit ADC prototypes are fully functional
  - They work up to about 35 MHz as expected
  - Static measurements show good DNL, INL & ENOB
  - Dynamic measurements need setup improvements
  - Power consumption can be scaled with frequency
- Future plans
  - Measurements
    - Continue static and power measurements
    - Precise dynamic measurements
    - Clock and power switching tests
  - Prepare multichannel version

# 10 bit general purpose DAC design

- Designed, fabricated and tested
- Fully functional
- High-swing voltage output
- Core area 0.18 $mm^2$
- Power cons. < 0.6 mW
- max INL < 0.42 LSB
- max DNL < 0.42 LSB




*D. Przyborowski, M. Idzik, "Development of a General Purpose Low-power Small-area 10 bit Current Steering CMOS DAC", Proc. 15th Int. Conf. "Mixed Design of Integrated Circuits and Systems" MIXDES 2009, Lodz, Poland, 25-27 June 2009, IEEE Xplore database*

# Other designs

- Bandgap reference voltage designed and fabricated, to be tested
- Fast (>500 MHz) LVDS transmitter and receiver designed and fabricated, to be tested

# Digital processing & data concentrator

- Waiting for better detector specification $\rightarrow$ data flux
- Pure digital design so can be done fast in comparison to front-end and ADC
- Will first be designed and tested with FPGA
- After FPGA tests ASIC implementation should be fast (mounth or two)

# Test setup (beam) preparation

- Silicon sensors from Hammamatsu ready and preliminary I-V and C-V measurements performed
- First fanout structures designed and fabricated
- Prototype front-end (8 channels) ASICs will be used
- External ADC will be used since the prototype ADC ASIC is not yet multichannel
- PCB board for test setup designed and produced

# Summary

- Front-end prototype ready for test beam
- New almost complete ADC prototype under tests, preliminary results promising
- Peripheral circuits (DAC, Bandgap, LVDS) designed, fabricated and partially tested
- Data concentrator will be first implemented as FPGA circuit, so no need for ASIC prototyping
- Full chain Test setup (beam) preparation in progress