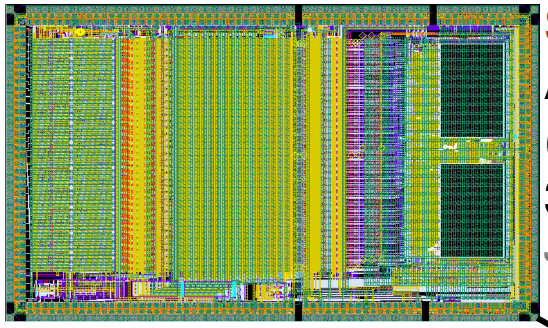
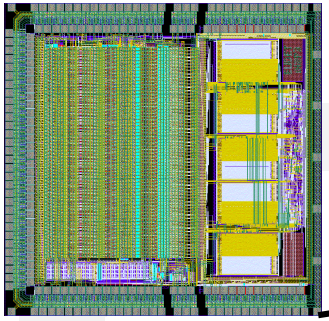
CALICE/EUDET FEE status

C. de LA TAILLE

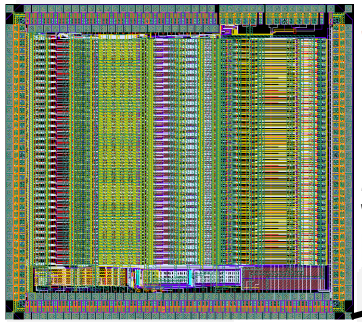
ILC front-end ASICs : the ROC chips



SPIROC
Analog HCAL
(SiPM)
36 ch. 32mm²
June 07

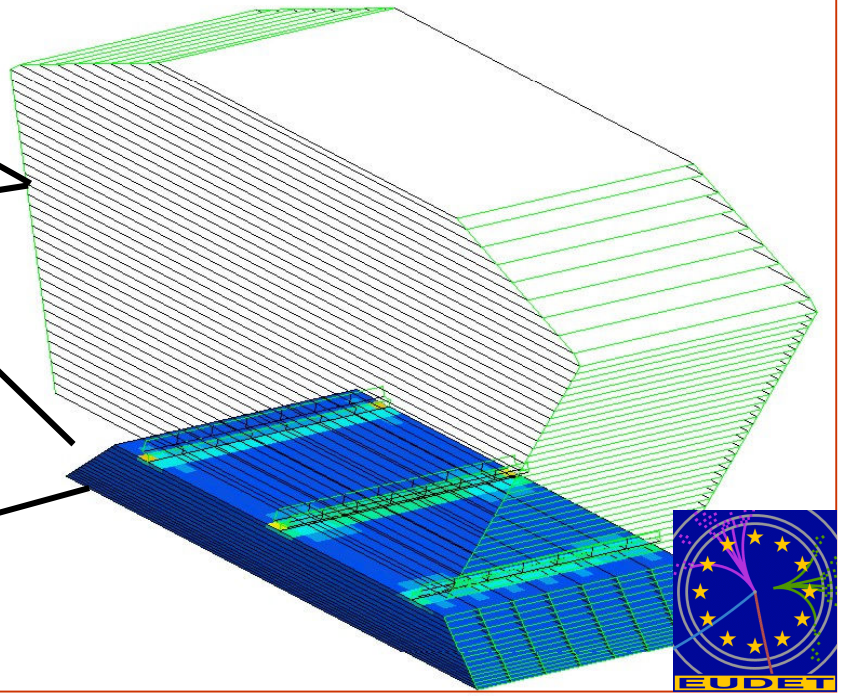


HARDROC
Digital HCAL
(RPC, µmegas or GEMs)
64 ch. 16mm²
Sept 06



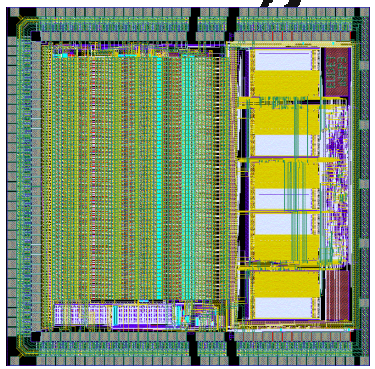
SKIROC
ECAL
(Si PIN diode)
36 ch. 20mm²
Nov 06

- Technological prototypes : full scale modules (~2m)
- EUDET EU funding (06-09)
- ECAL, AHCAL, DHCAL
- B=5T

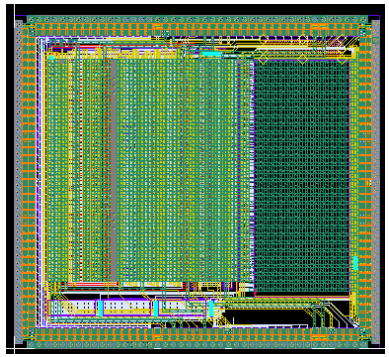


HaRDROC status

- 240 chips HARDROC1 produced in june 2007 to equip 4-chip and 24-chip RPC and Micromegas detectors
  - Package PQFP240
  - Not completely power-pulsed



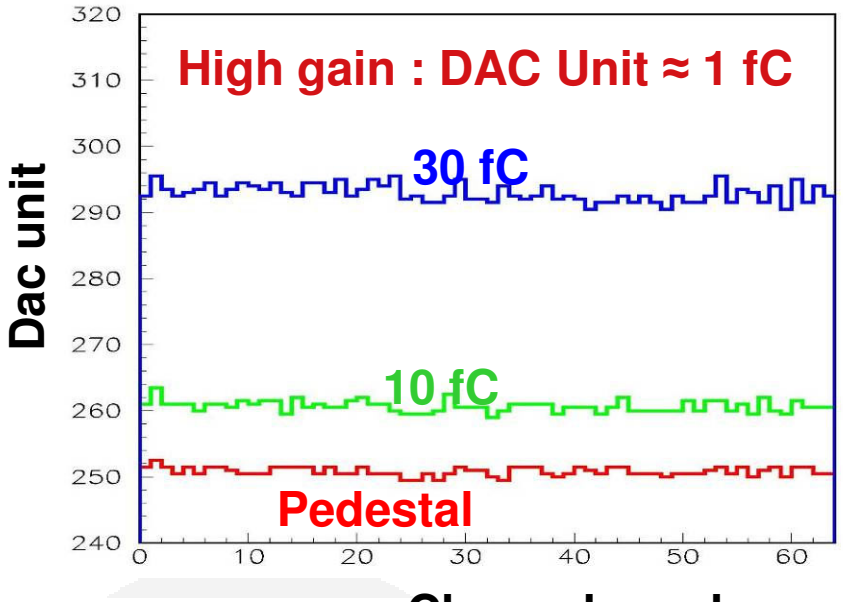
- 400 chips HARDROC2 produced in june 2008 to equip 24-chip RPC and Micromegas for square meter
  - 3 thresholds (0.1-1-10 pC)
  - Power pulsed to 5-8 µW/ch
  - Package TQFP160

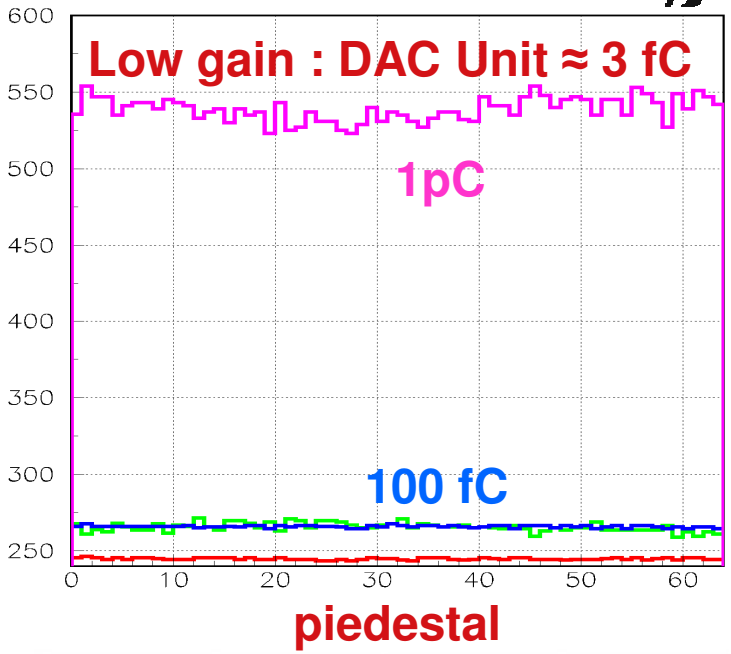


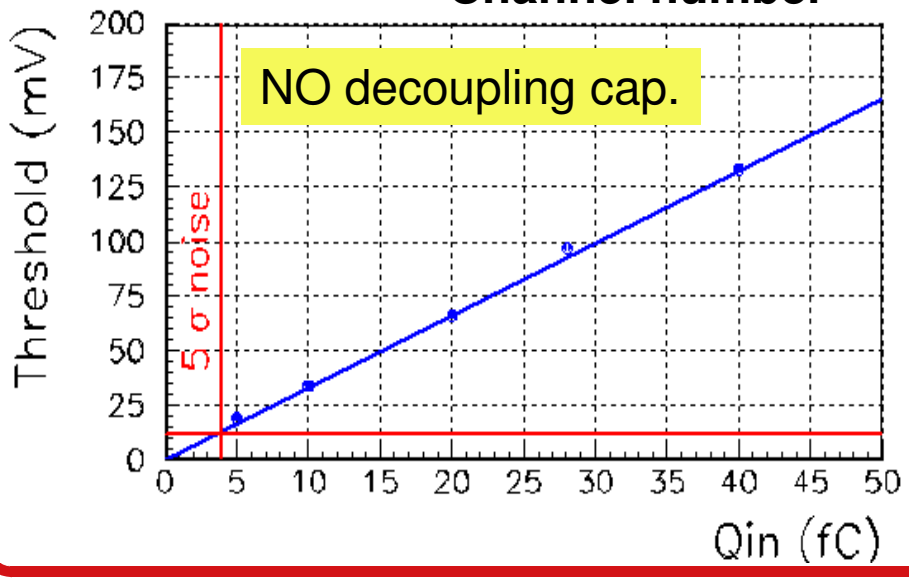
- Essential for readout + DAQ2 validation
- Full production run : end 2009
  - After validation on detector

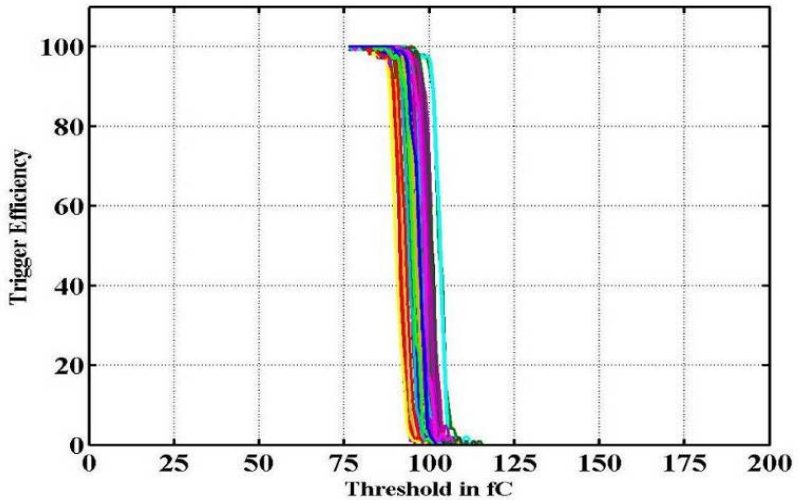
TQFP: t=1.4 mm

Trigger efficiency measurements



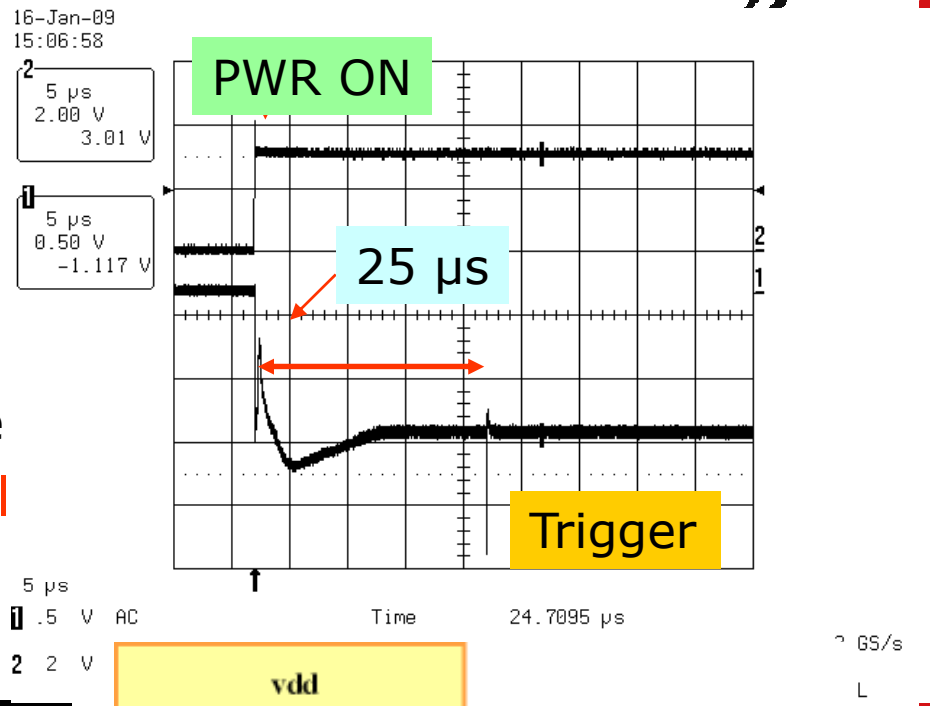




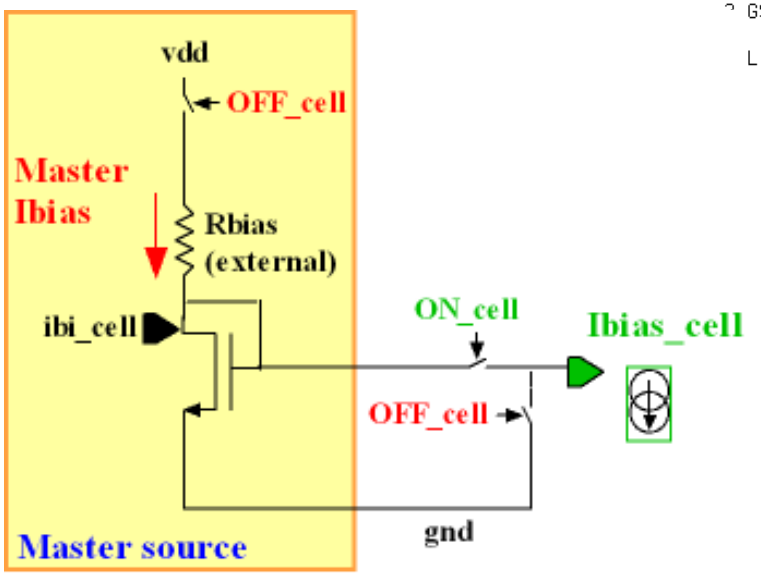


Power pulsing

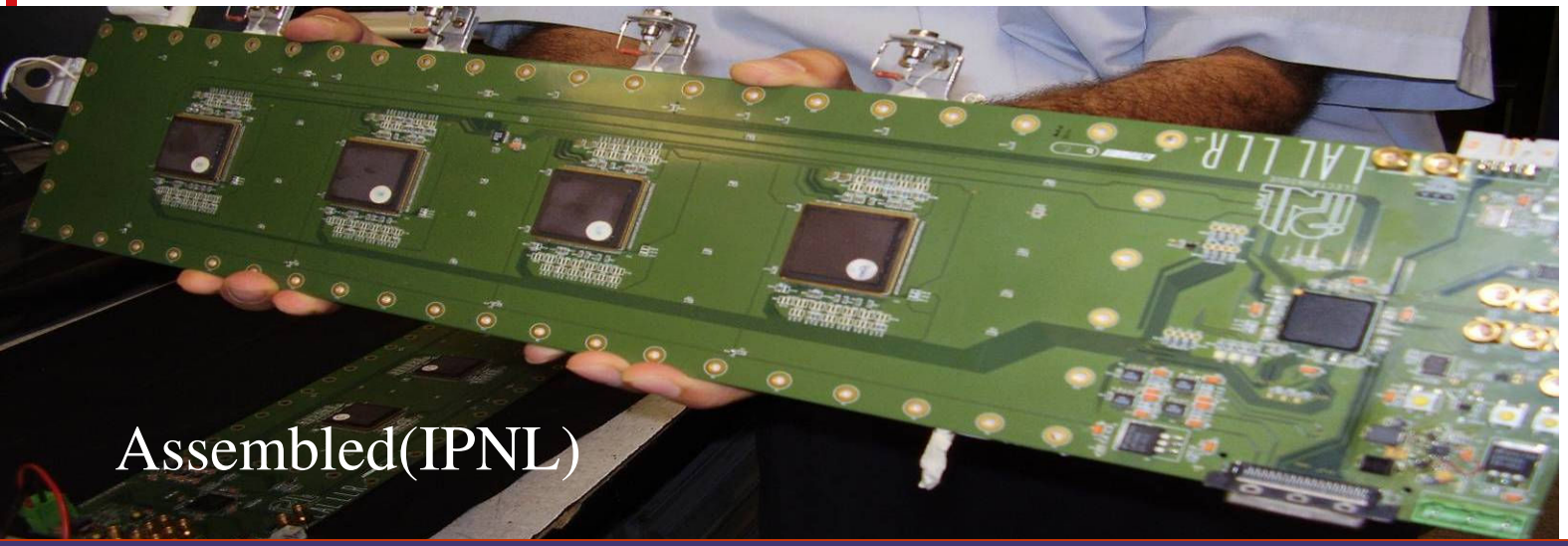
- Total power on : 100 mW
- Total power off : 10 µW
- Power dissipation
  - 1.5 mW/ch continuous
  - 25 µs awake time
  - 7.5 µW/ch with 0.5% duty cycle
- 10 µW/ch = 24h operation of ful slab with 2 AAA batteries !

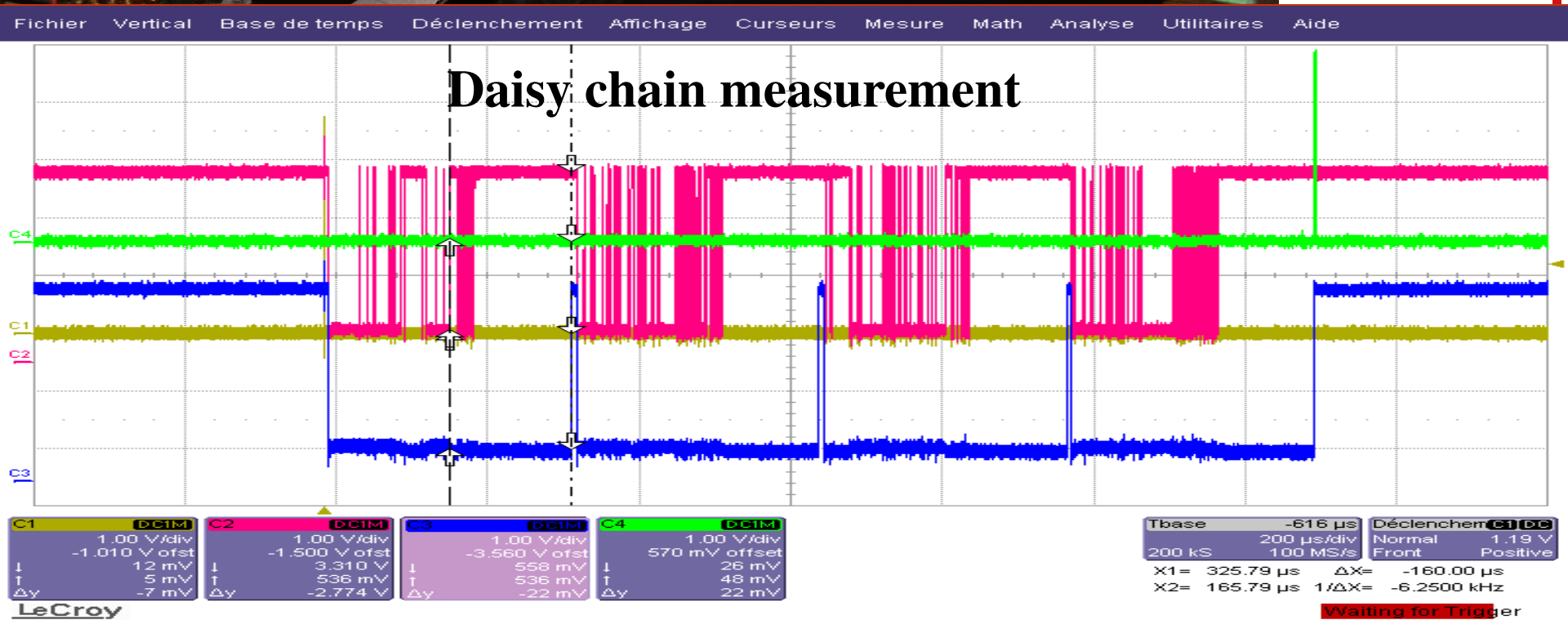


PA	5.46mA	DAC	0.84mA
3 FSB	12.3mA	BG	1.2mA
SS	*9.3mA*	vddd	0.67mA
3 Discris	7.3mA	vddd2	0.4mA (=0 if 40MHz OFF)
TOTAL	38mA		



Readout validation with HARDROC





Towards technological prototype

GRPC

Slab #1

DIF #1

Slab #2

DIF #2

DIF #3

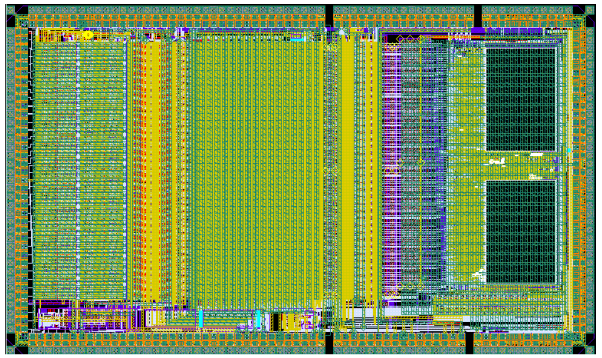
Fully equipped large scalable detector to be soon tested in cosmic rays bench and in test beam at CERN in **summer 09** [I. Laktineh et al.]

Similar development with µMEGAS [C. Adloff et al.]

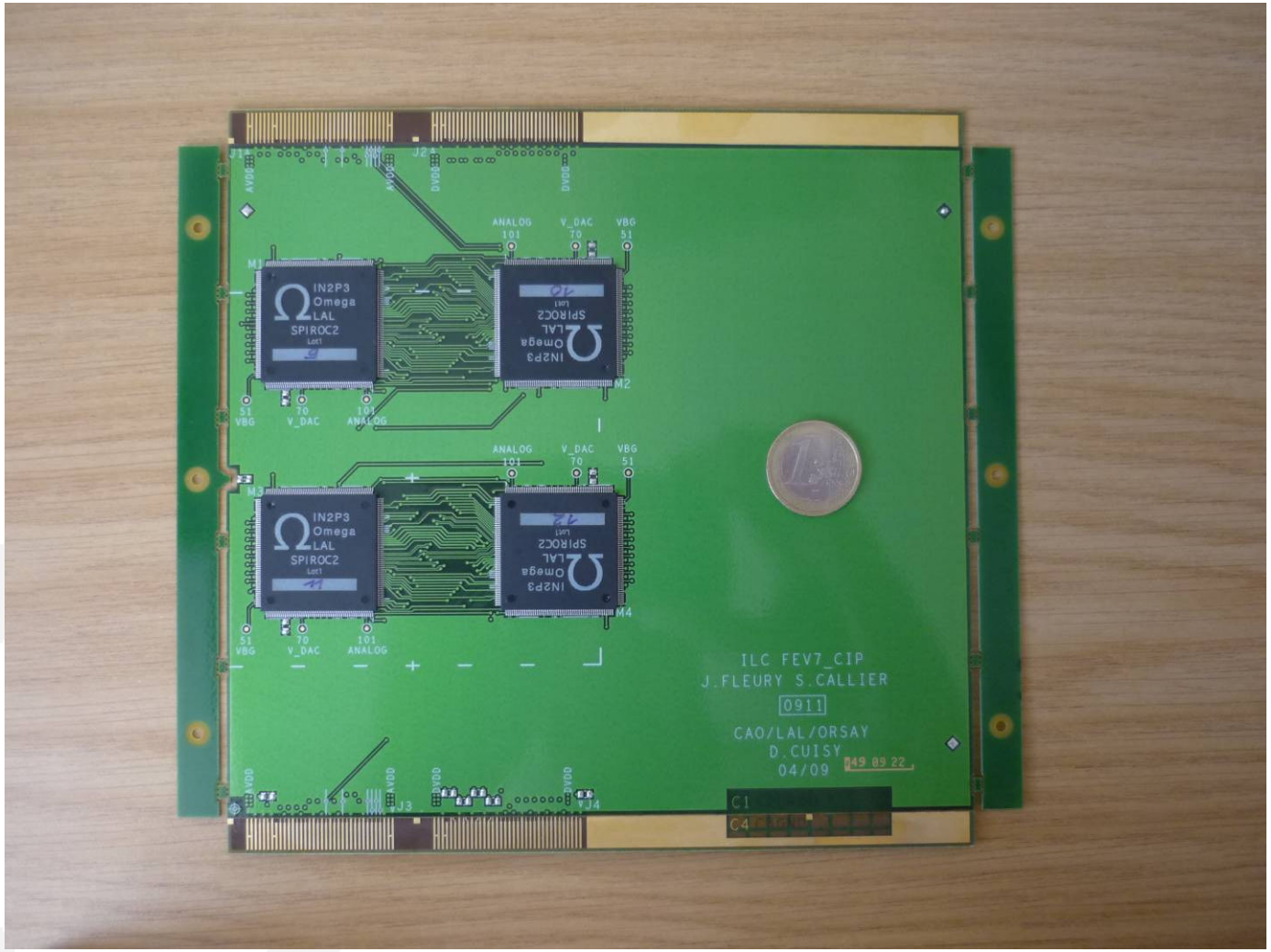
A NICE PROOF of INFRASTRUCTURE

SPIROC for AHCAL

- Internal input 8-bit DAC (0-5V) for individual SiPM gain adjustment
- Energy measurement : 14 bits
  - 2 gains (1-10) + 12 bit ADC 1 pe → 2000 pe
  - Variable shaping time from 50ns to 100ns
  - pe/noise ratio : 11
- Auto-trigger on 1/3 pe (50fC)
  - pe/noise ratio on trigger channel : 24
  - Fast shaper : ~10ns
  - Auto-Trigger on ½ pe
- Time measurement :
  - 12-bit Bunch Crossing ID
  - 12 bit TDC step~100 ps
- Analog memory for time and charge measurement : depth = 16
- Low consumption : ~25µW per channel (in power pulsing mode)
- Individually addressable calibration injection capacitance
- Embedded bandgap for voltage references
- Embedded 10 bit DAC for trigger threshold and gain selection
- Multiplexed analog output for physics prototype DAQ
- 4k internal memory and Daisy chain readout



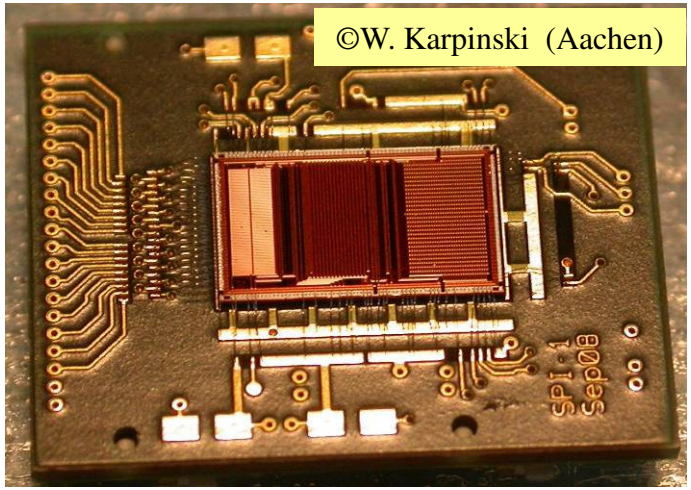
ECAL board FEV7 with SPIROC2



SPIROC status

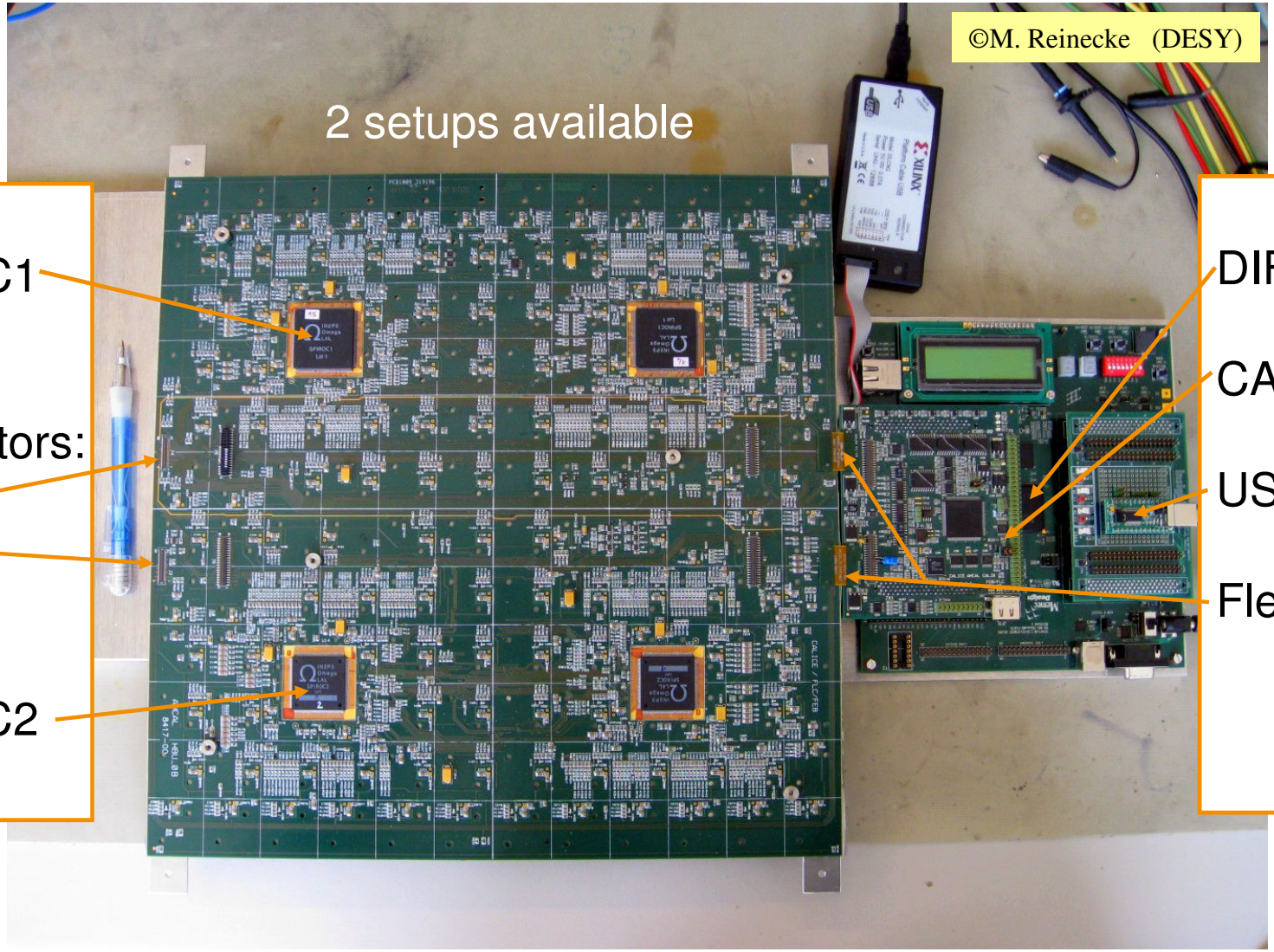
- 200 chips SPIROC1 produced in nov 2006
  - Package PQFP240
  - Good analog performance
  - Bug in ADC ramp : no digital data out !

- 50 chips **SPIROC2** produced in june 2008 to equip AHCAL and ECAL EUDET modules
  - **Fulfiled EUDET milestone**
  - Package TQFP208
  - Difficult slow control loading
  - Measurements (slowly) coming in
  - Complex chip
  - Collab LAL, DESY, Heidelberg

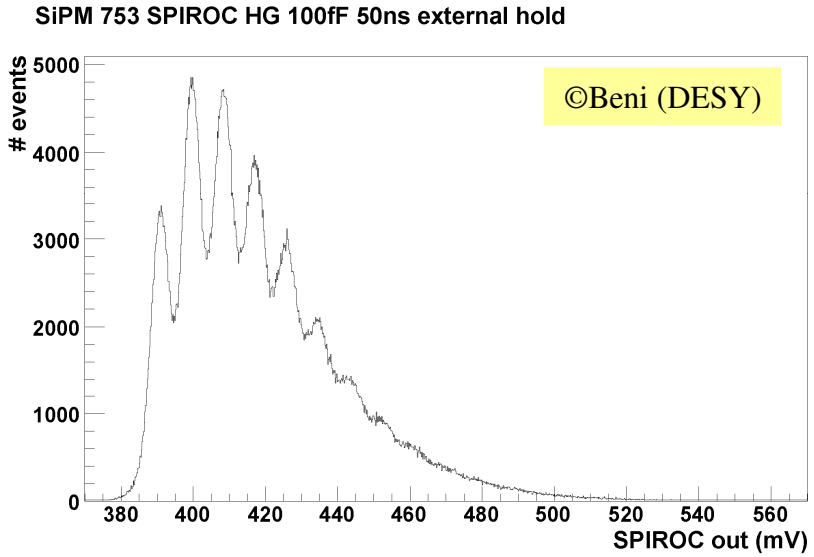


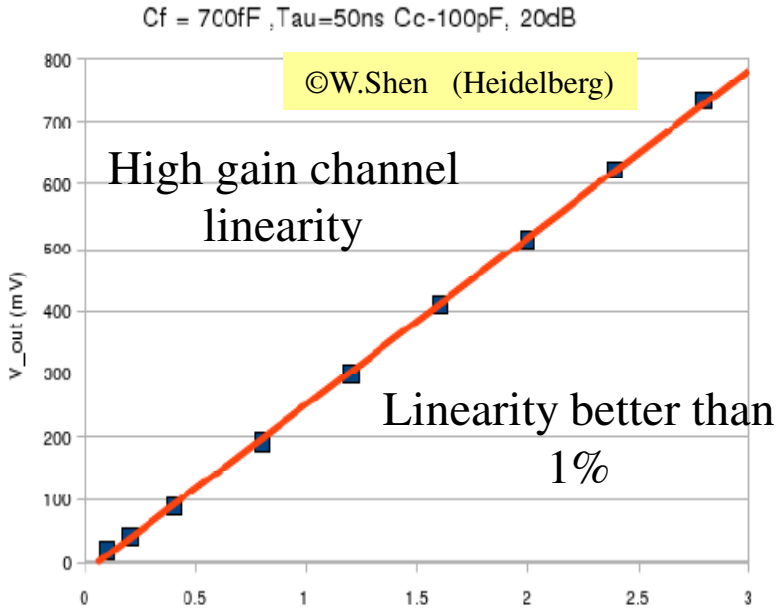
- External requests :
  - astrophysics PEBS (Aachen), medical imaging (Roma, Pisa, Valencia…), nuclear physics (IPNO), Vulcanology (Napoli)

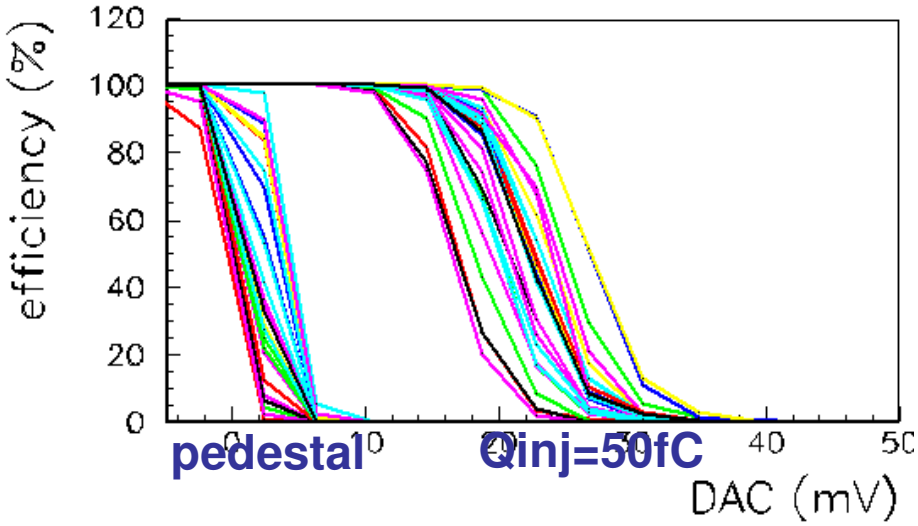
HBU0 status

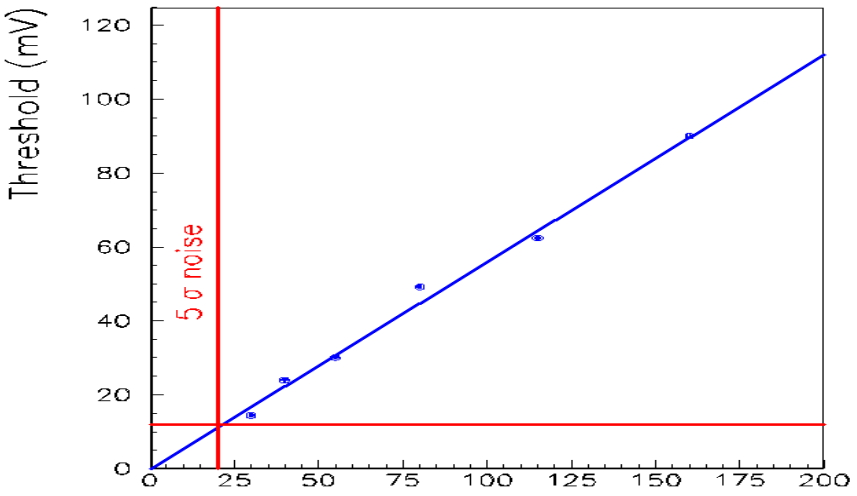

©M. Reinecke (DESY)
2 setups available
SPIROC1
Connectors:
Signal
Power
SPIROC2
DIF FPGA
CALIB
USB / DAQ
Flexleads

Performance

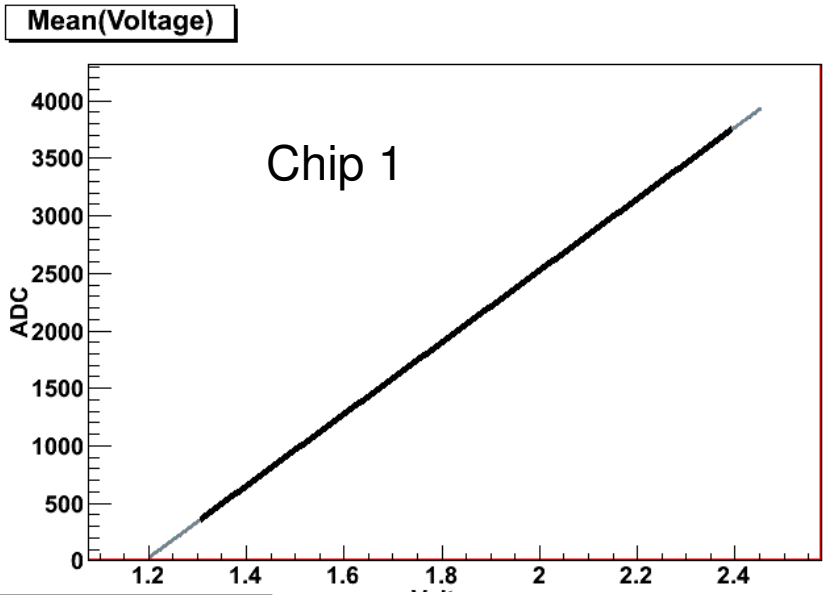


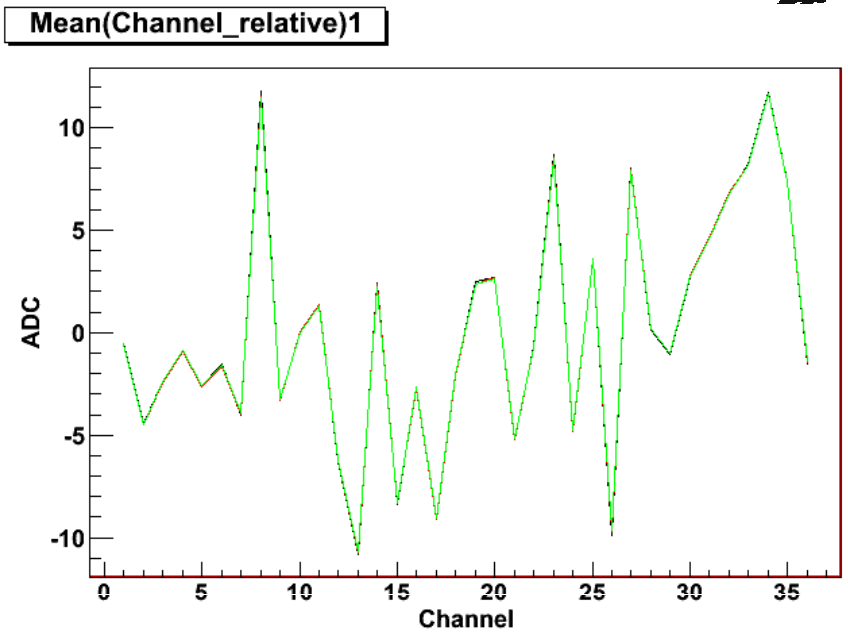


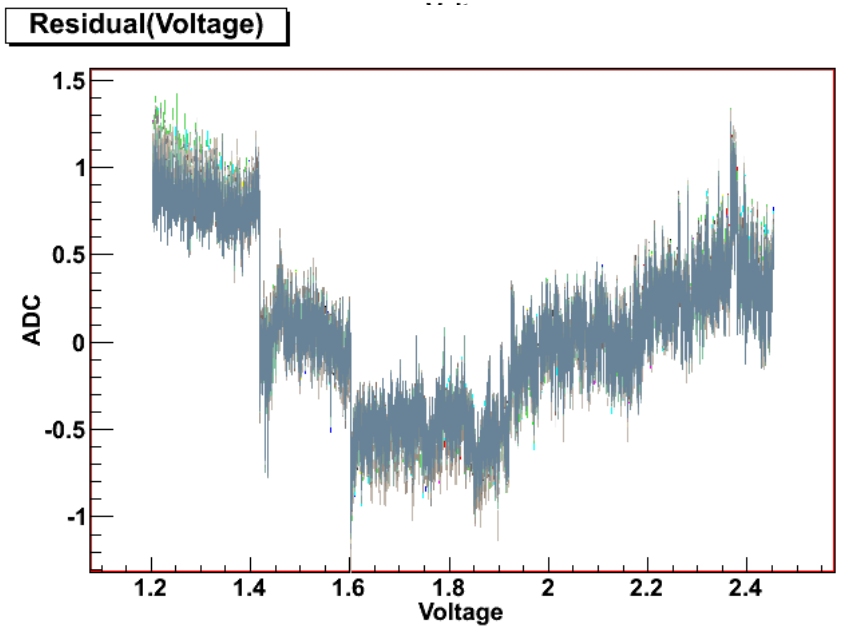


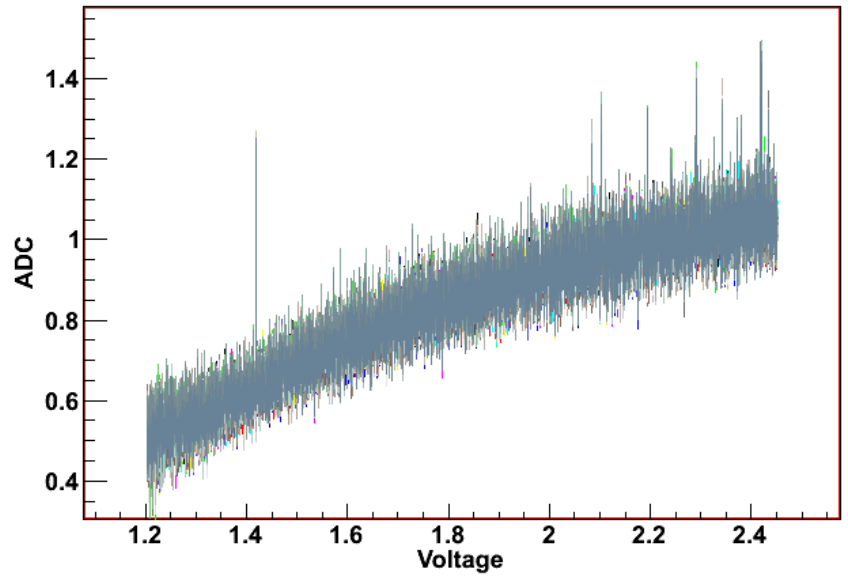


Internal 12-bit ADC performance



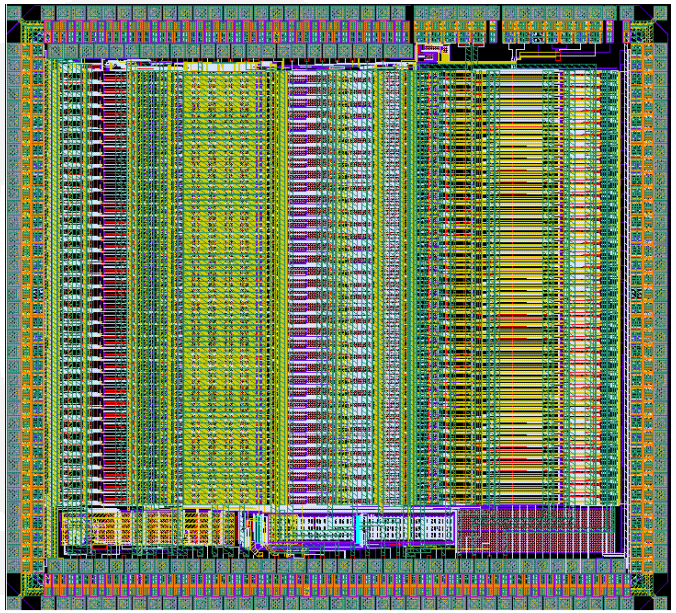


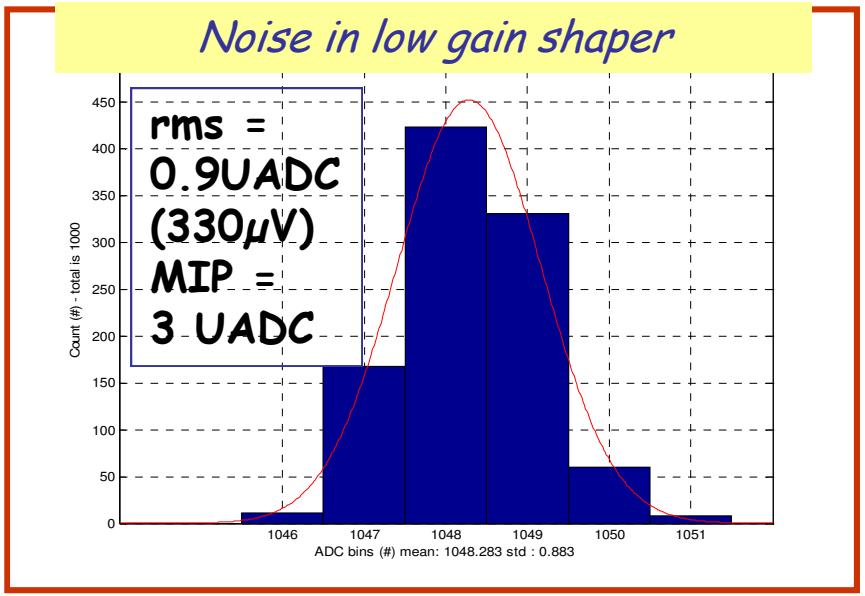




SKIROC for W-Si ECAL

- Silicon Kalorimeter Integrated Read Out Chip (Nov 06)
  - 36 channels with 15 bits Preamp + bi-gain shaper + autotrigger + analog memory + Wilkinson ADC
  - Digital part outside in a FPGA for lack of time and increased flexibility, but cannot be used on an ASU or FEV
  - Collaboration with LPC Clermont





SKIROC status

- SKIROC1 useless with detector (no readout)
- SPIROC2 used as SKIROC emulator
  - 36 channels only
  - Limited dynamic range (~500 MIPs)
  - Tests starting with FEV7
  - Noise tests on testboard proceeding (ENC ~ 1 ke-)
- R&D will continue within CALICE
  - SKIROC2 to be submitted with production run
  - Expensive ASIC (70 mm2 = 70 k€) => MPW not worth it
  - 64 channels
  - 95% identical to SPIROC (only preamp differs)

Test beam with technological prototype

- Data rate (Spiroc/Skiroc) : naive estimate
  - Volume : 36ch*16sca*50bits=30 kbit/chip
  - Conversion time : 16*80 µs = 1.5 ms
  - Readout speed 5 MHz (could be increased to 10-20 MHz)
  - 8 chips/DIF line (one FEV only)
  - Total : 1.5ms + 30000*200ns*8 = 50 ms/16 events = 3 ms/evt => 300 Hz during spill

- Overall readout rate
  - « Add » 1-10% power pulsing : 3-30 Hz effective rate
  - Pessimistic as assuming all chips full

- Note : readout electronics designed for ILC low-occupancy, low rate detector **≠Testbeam** !!

Summary

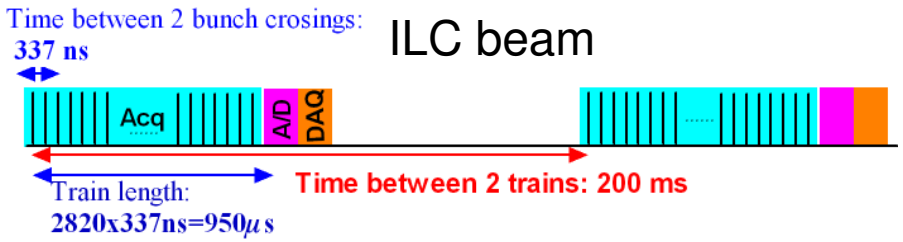
- 2nd prototypes of HARDROC (DHCAL) and SPIROC (AHCAL+ECAL) submitted in june 08
- DAQ part being validated with HaRDROC
- Power pulsing tests essential now at system level
- Front-end boards first prototypes coming in
- DAQ interface (DIF boards) prototyped

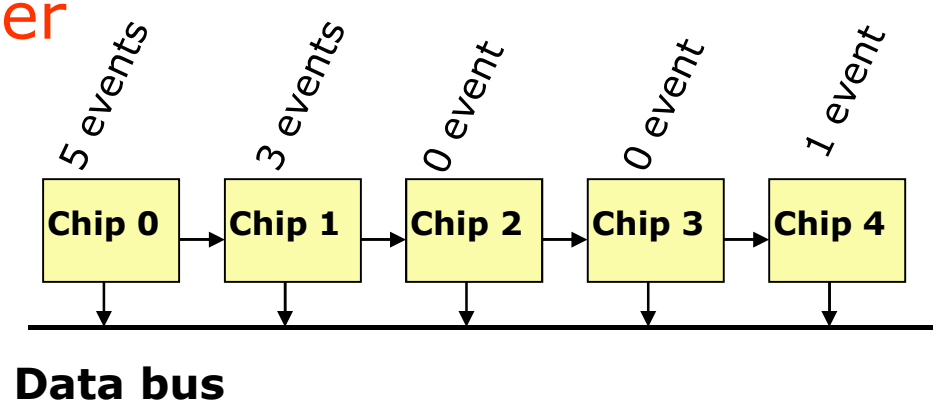
- Tests are very complex and essential
- Still need to validate noise, autotrigger, ADC, power pulsing with detector.

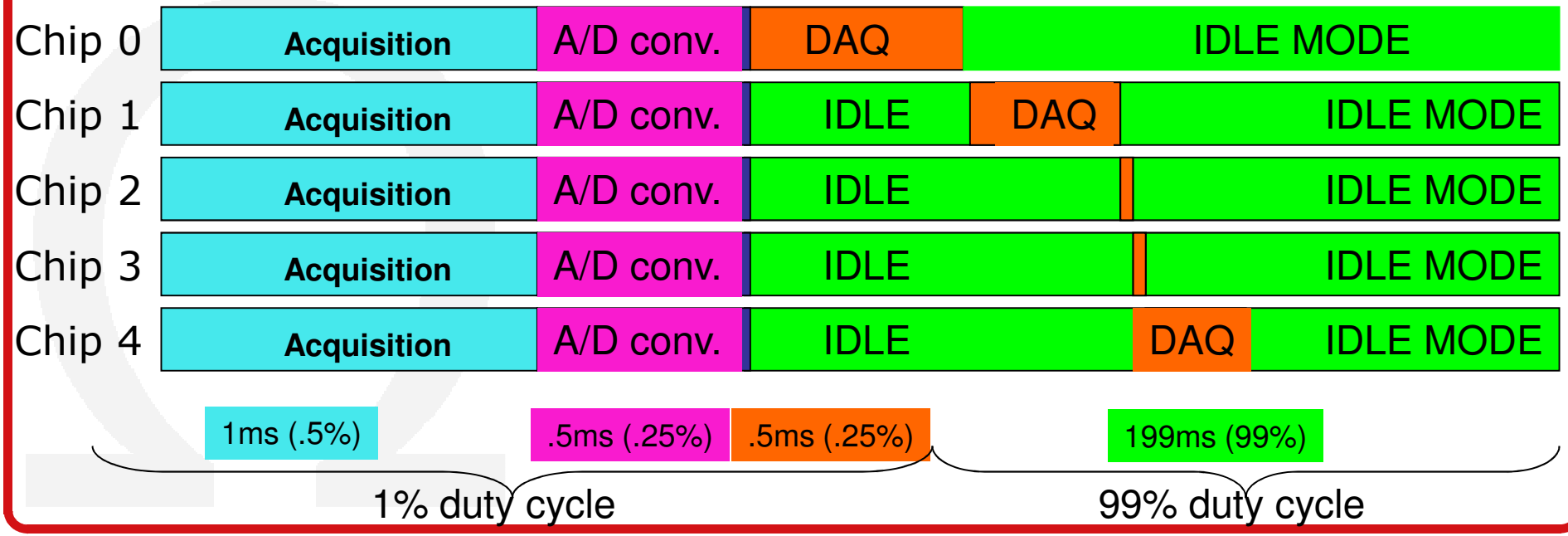
Backup slides

Read out: token ring

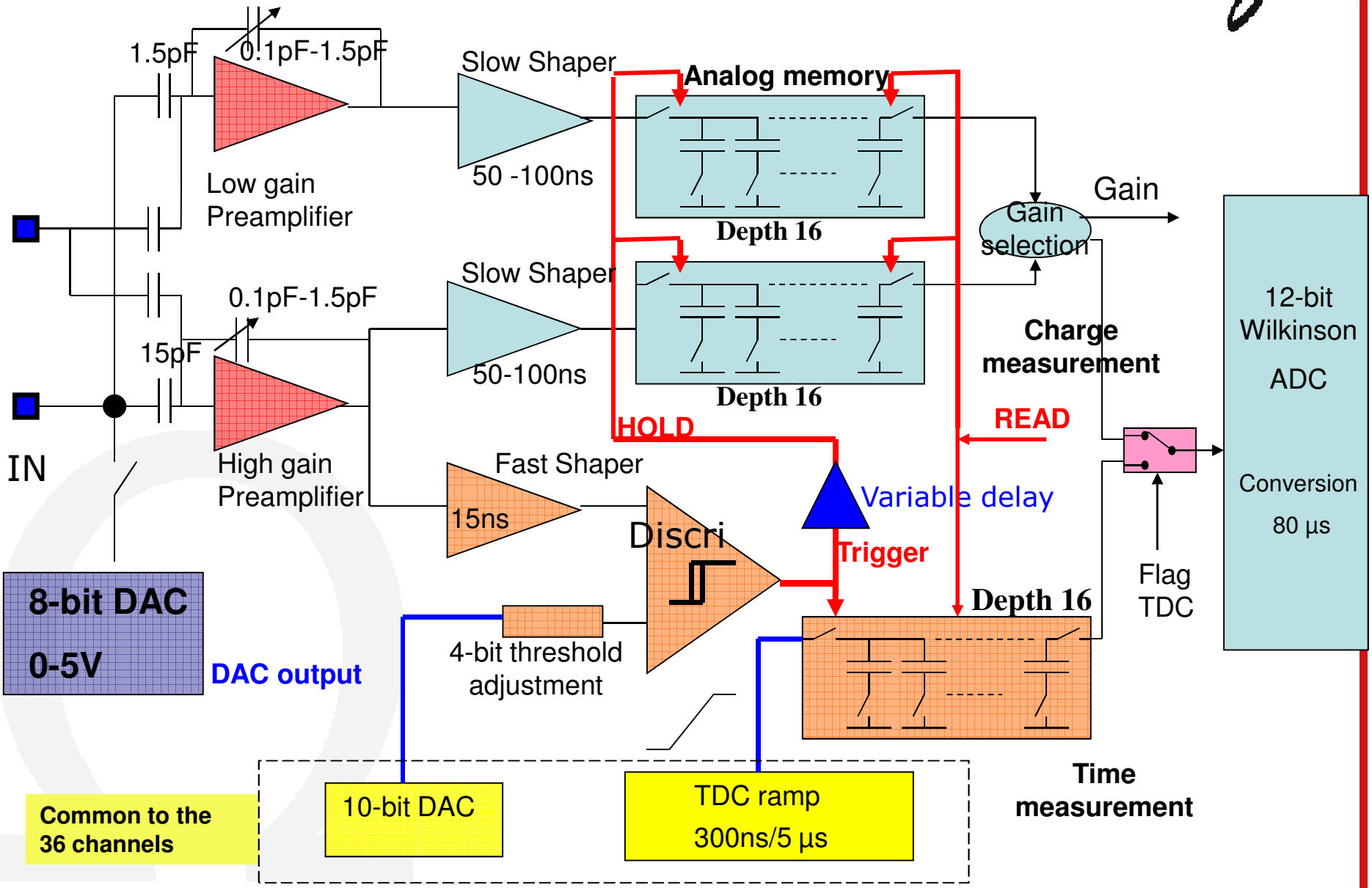
- Readout architecture common to all calorimeters
- Minimize data lines & power



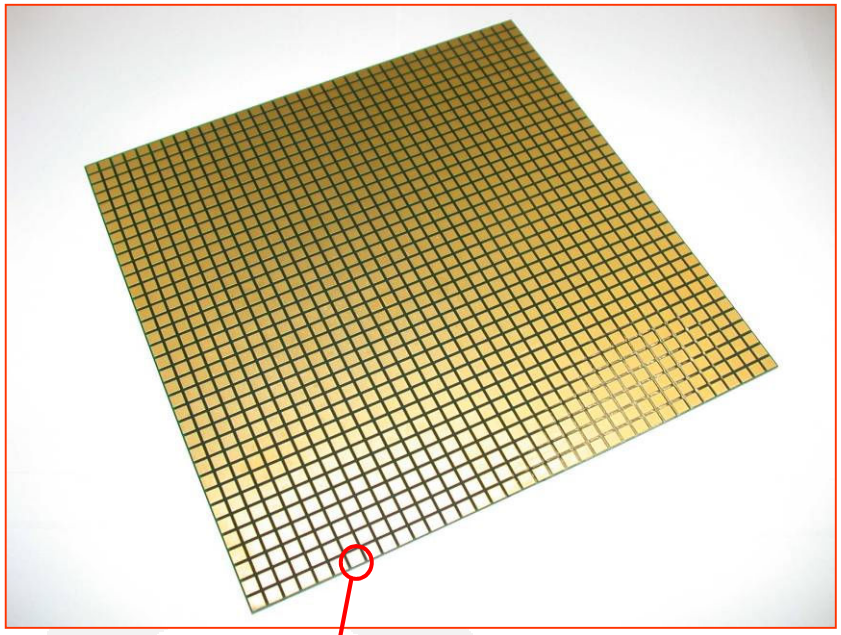


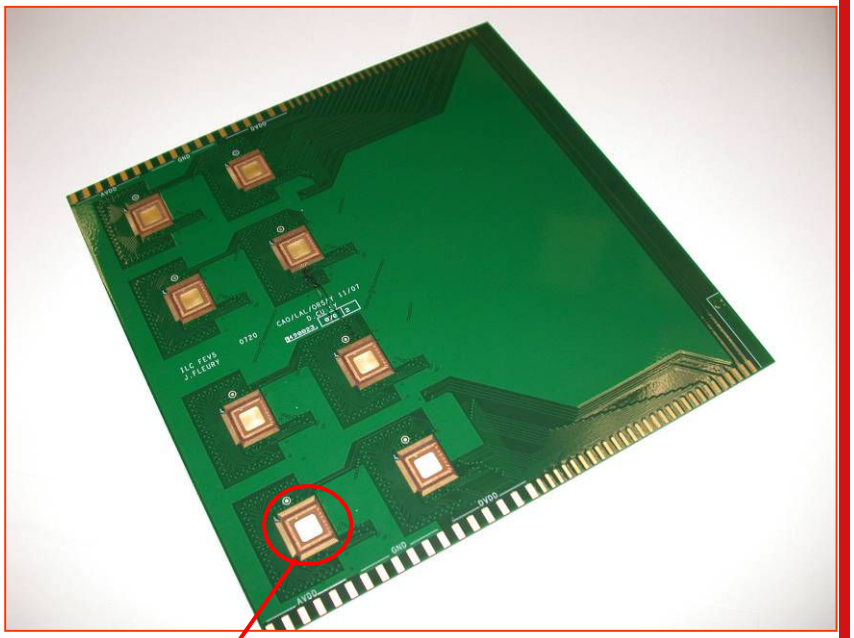


SPIROC : One channel schematic

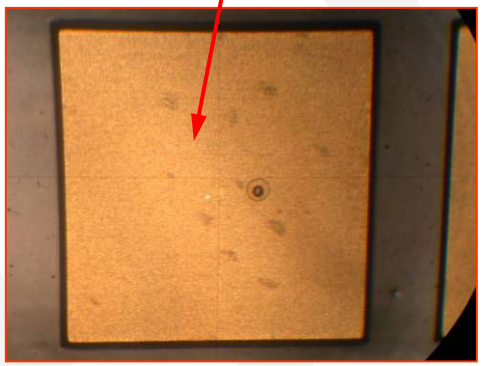


FEV5 : new PCB for ECAL

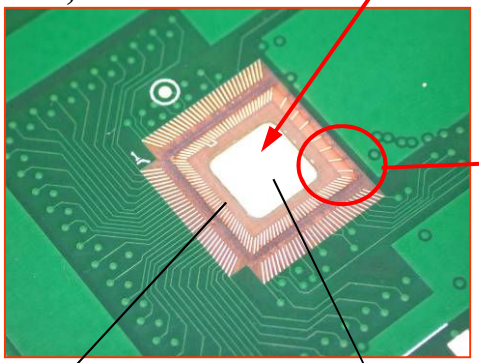


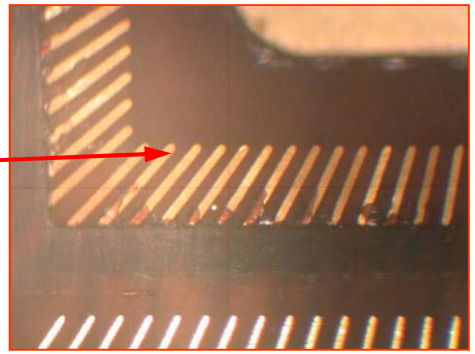


Global dimensions :
*180*180 mm, thickness 1.2mm*



*pixel dimensions : 4*4 mm*





0.15mm <depth<0.17mm

0.6mm< depth<0.7mm