TPC Task Status Report

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DESY

EUDET Annual Meeting 2009

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EUDET JRA2/TPC

Main objective: Large Prototype (LP) of a TPC.

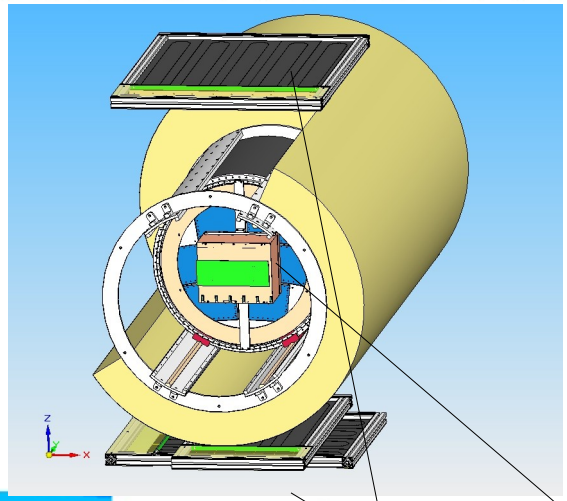
Consisting of

- **Field cage**
- **Readout electronics**
- **DAQ and Monitoring**
- **Gas-/HV-system**
- **Common Software**
- **SiLC envelope**
- **End plate**
- **MPGD detector modules**
- **Cosmic/beam trigger**

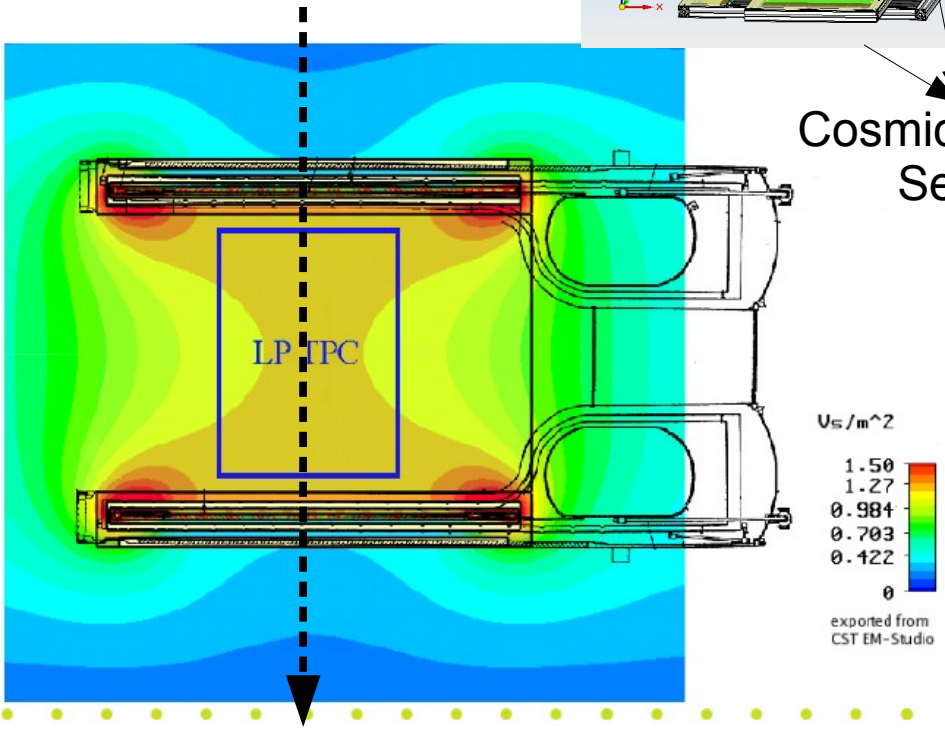
JRA1:
Magnet (PCMAG) + infrastructure
T24 Test beam

DESY Setup

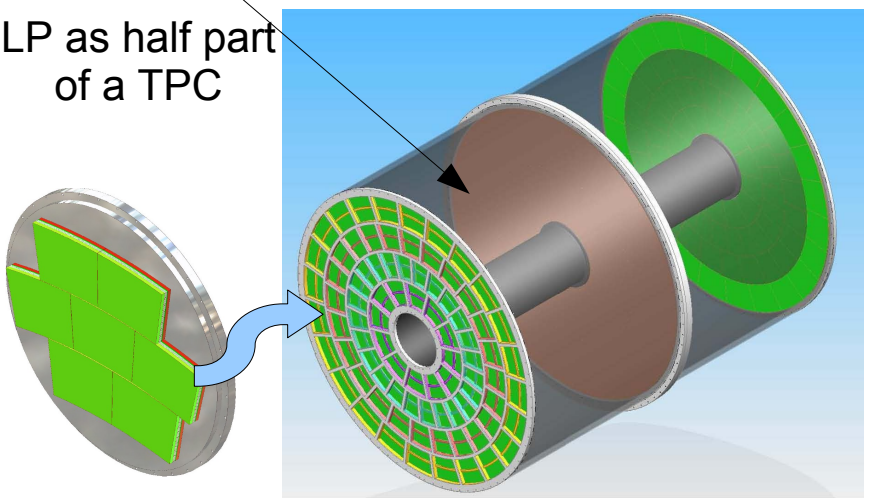
- *PCMAG:* superconducting magnet, up to 1.25 T
- e^- test beam @DESY (1GeV/c<p<6GeV/c)



Cosmic Trigger Setup



LP as half part of a TPC



EUDET JRA2/TPC

DESY-FLC TPC group / University of Hamburg is responsible for constructing and delivering a Field Cage (FC) for the Large Prototype (LP) of a TPC.

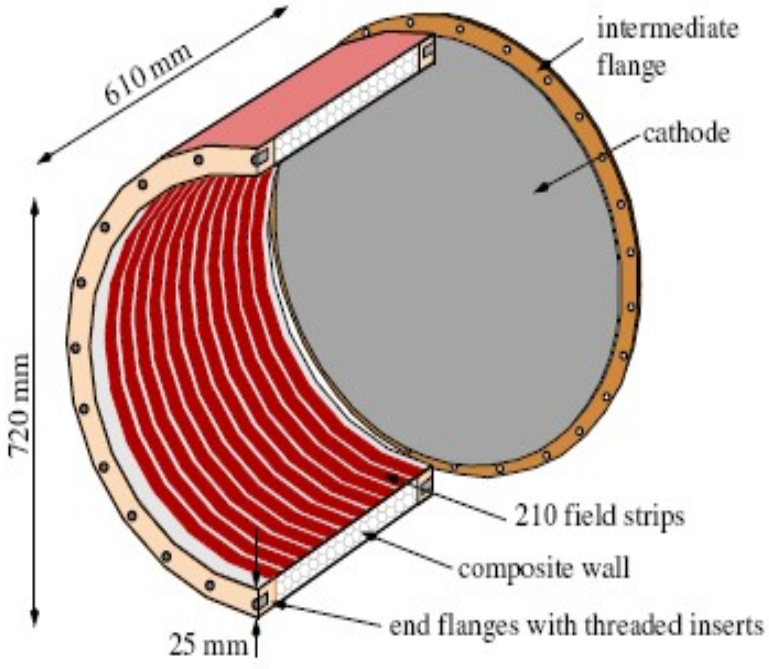
LUND University in collaboration with CERN is responsible for the development and supply of a 2000 channel electronic ADC readout system based on ALTRO electronics + DAQ/monitoring system.

Rostock University is responsible for supplying a TDC based electronic readout system.

The TPC Large Prototype

- Requirements:
  - **Dimensions**
    - diameter = *O*(800 mm), length = *O*(600 mm)
  - **Lightweight field cage, though stable and flexible to use**
  - **Homogeneous electrical field**

The Field Cage

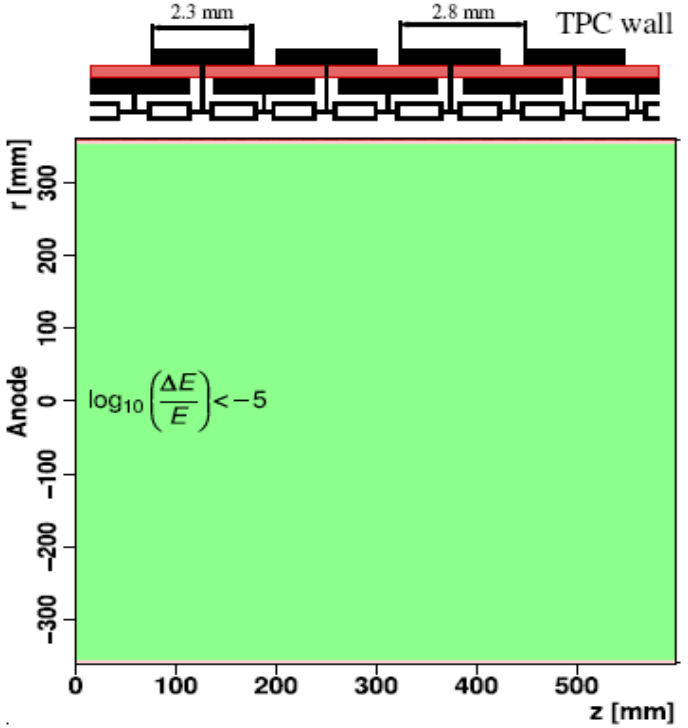


parallel plate capacitor

external shiedling (gnd)

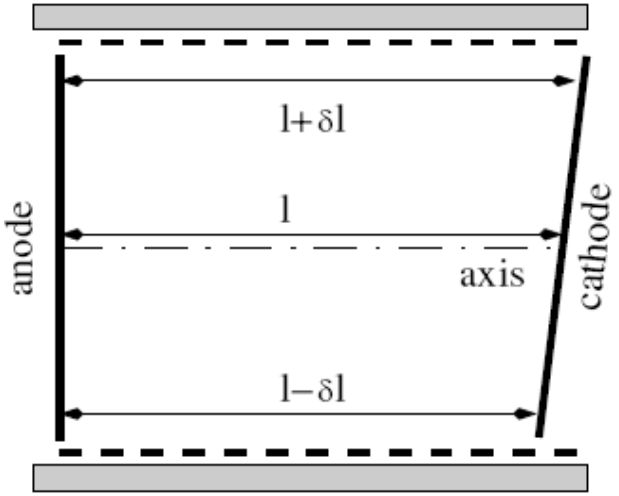
field strips

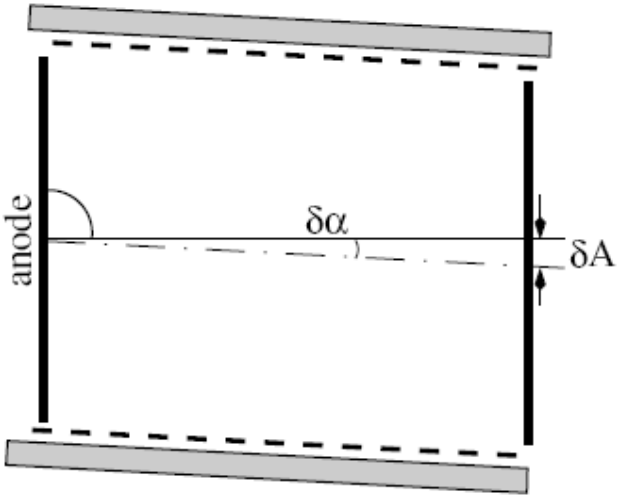
mirror strips

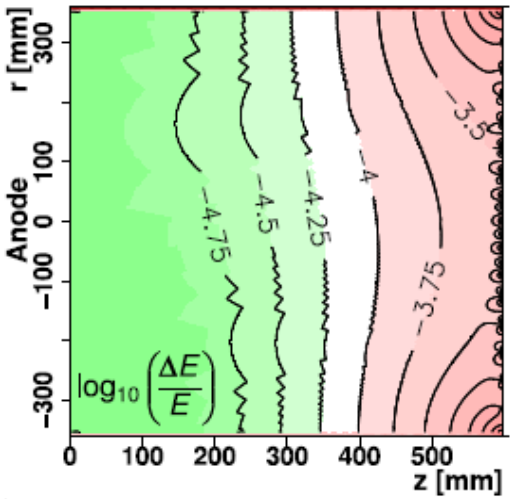


P. Schade, DESY

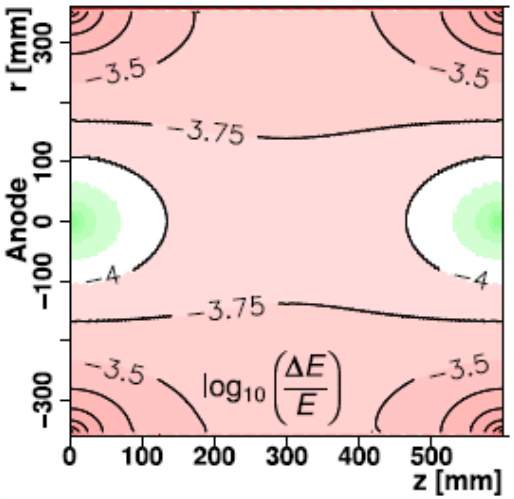
The Field Cage





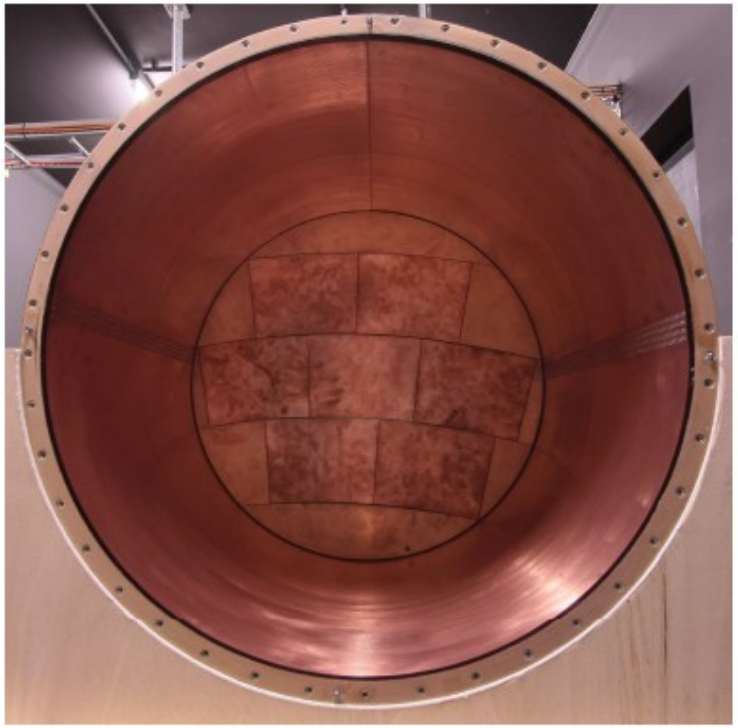


$\delta l = 100\,\mu\mathrm{m}$

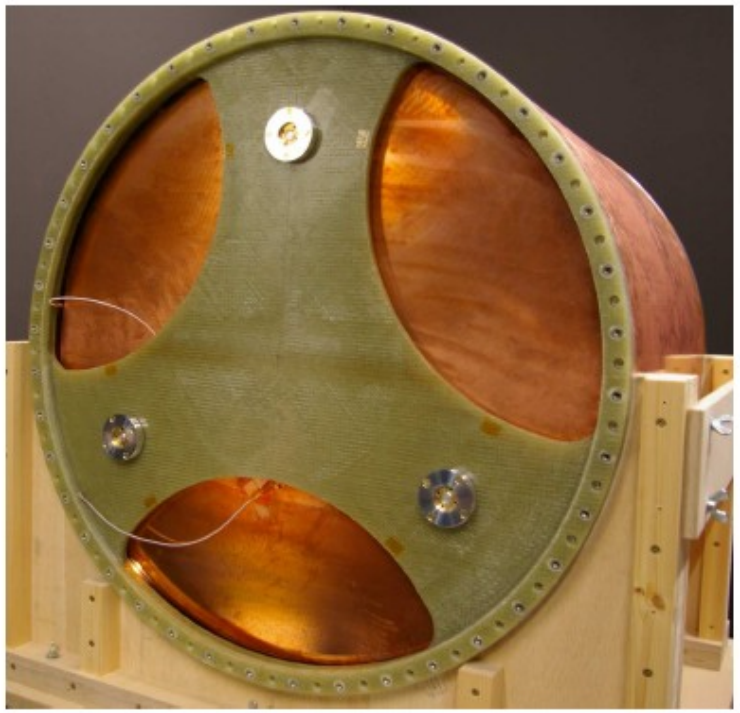


$\delta A = 100\,\mu\mathrm{m}$

The Field Cage



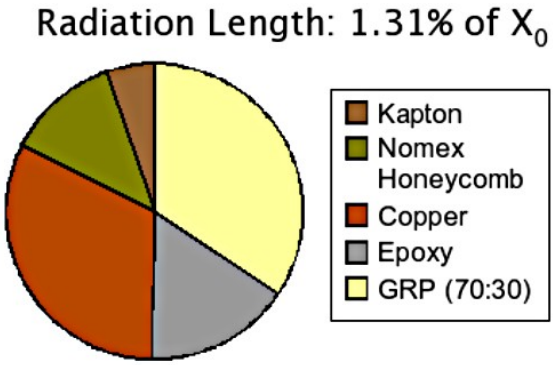
field cage with anode end plate

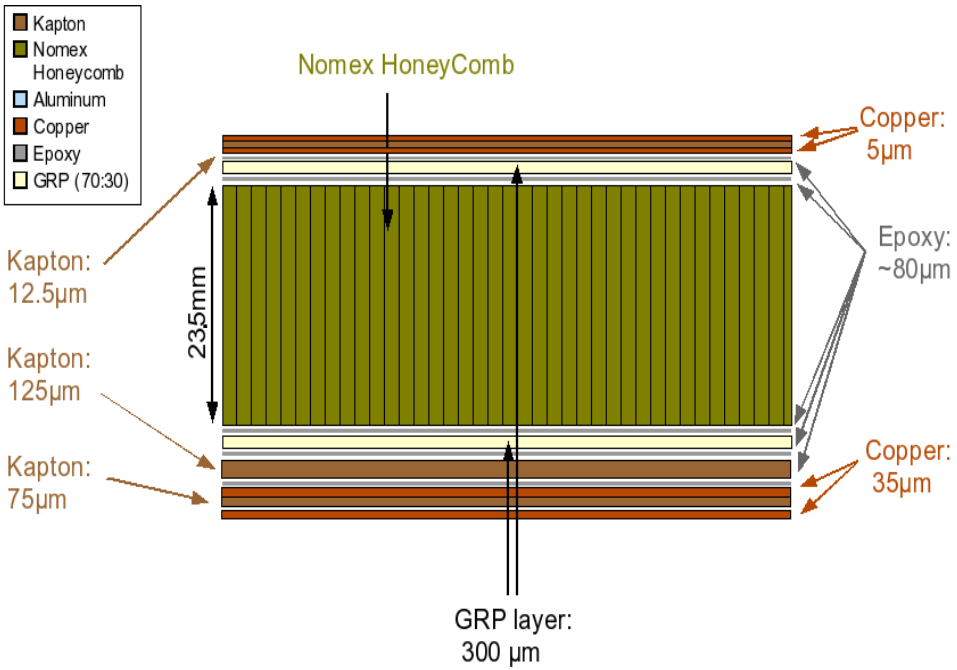


field cage with cathode end plate

P. Schade, DESY

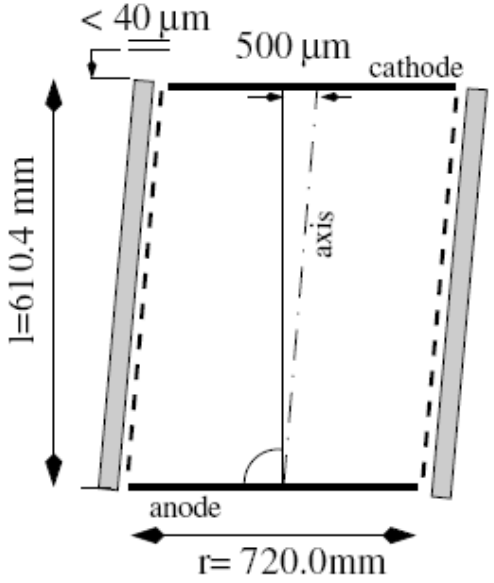
The Field Cage

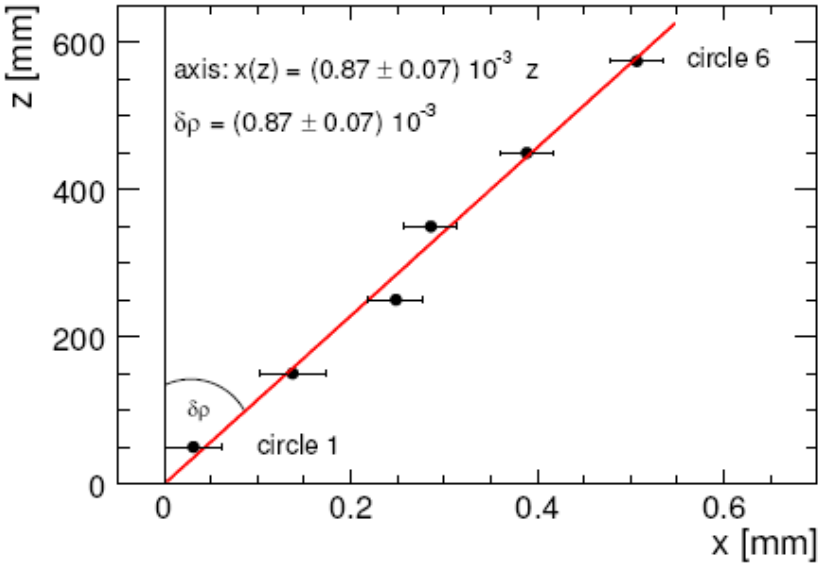


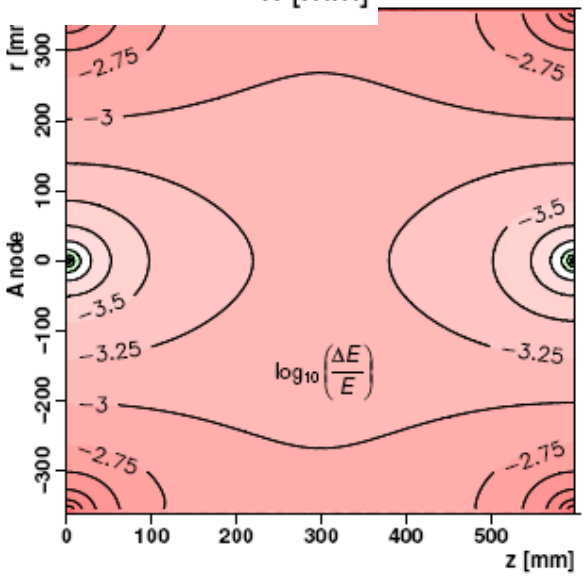


Diameter: Inner 720 mm,
Outer 770 mm
Wall thickness 25 mm
Length 610 mm
HV to be applied: up to 20 kV

The Field Cage





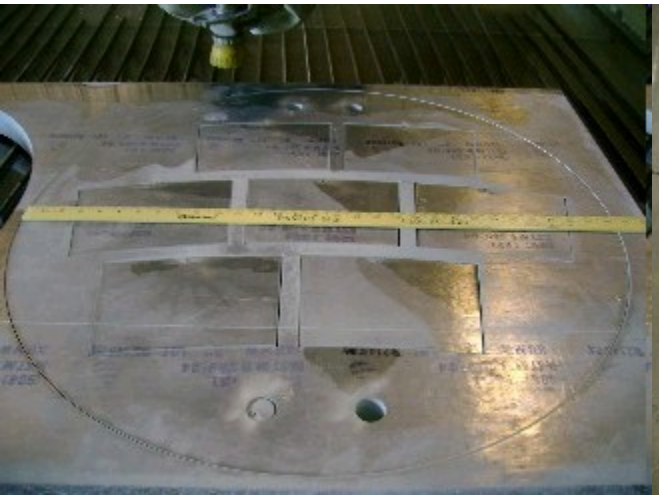
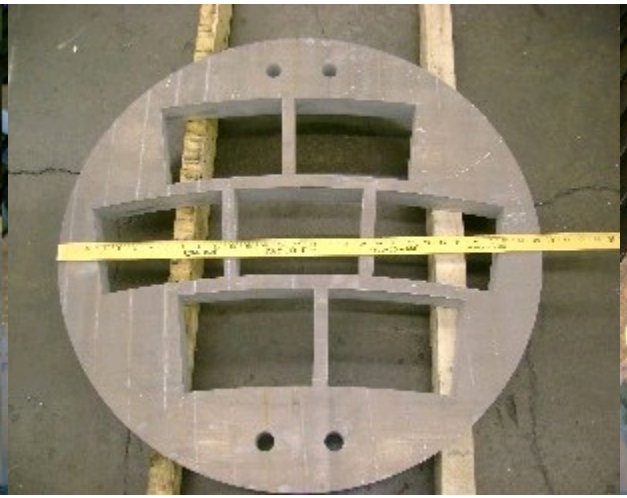


Achieved mechanical accuracy:

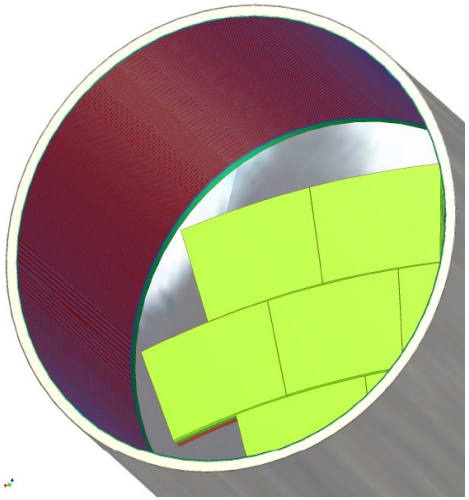
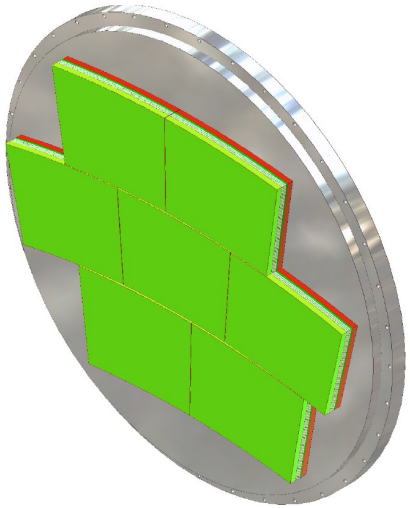
- Aligment of the end faces: $\delta l < 40\ \mu m$
- Alignment of field cage axis: $\delta A \sim 500\ \mu m$
- Field quality $10^{-4} \lesssim \Delta E/E \lesssim 10^{-3}$

P. Schade, DESY

The End Plate

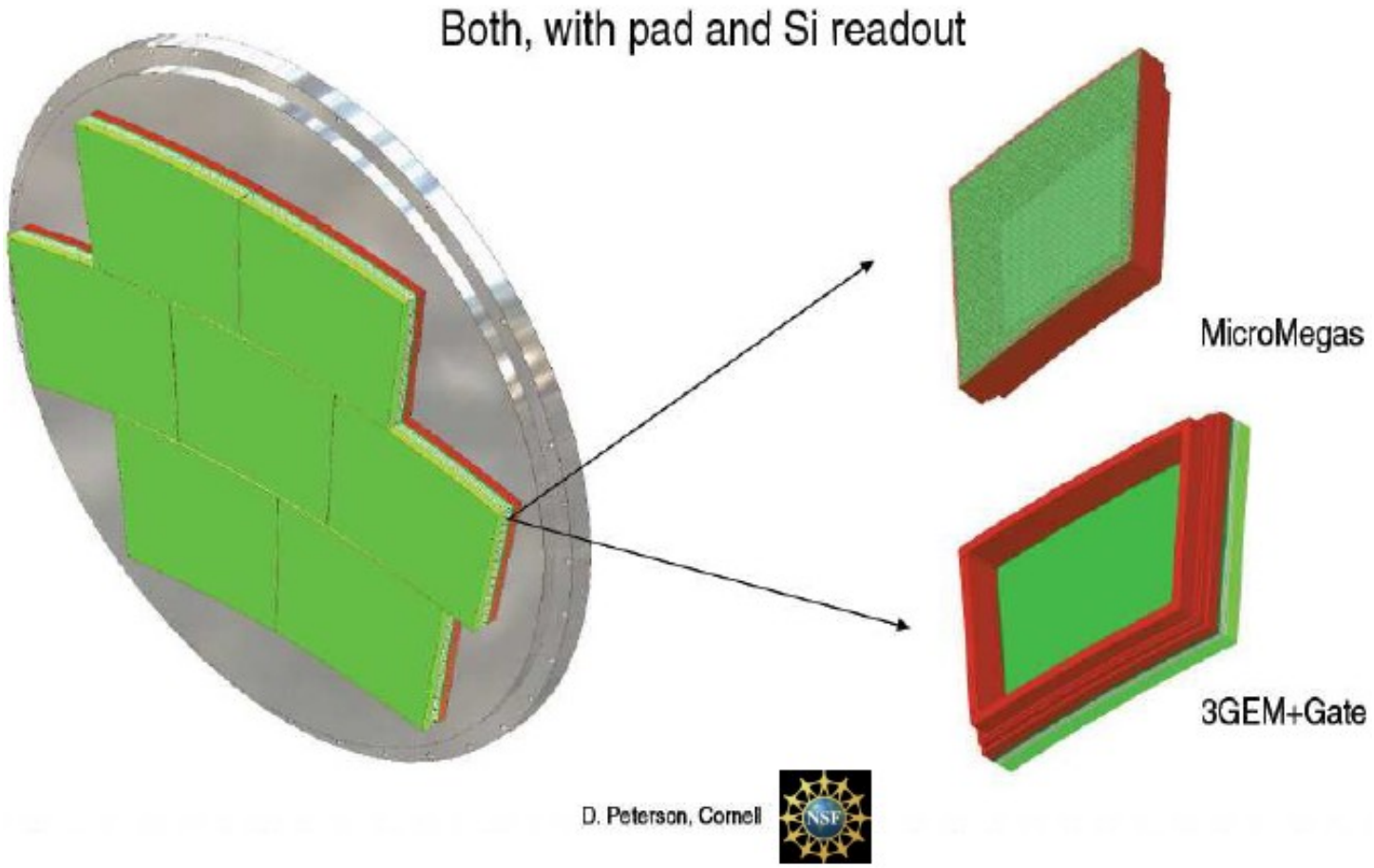





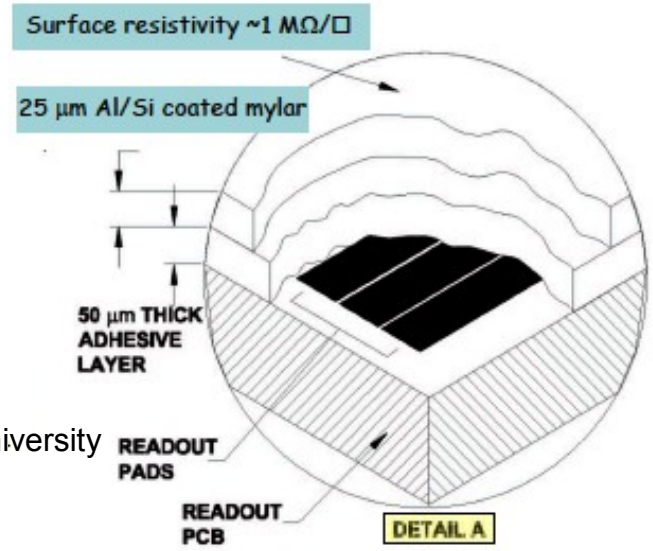
D. Peterson, Cornell

The End Plate



MicroMeGaS Structure

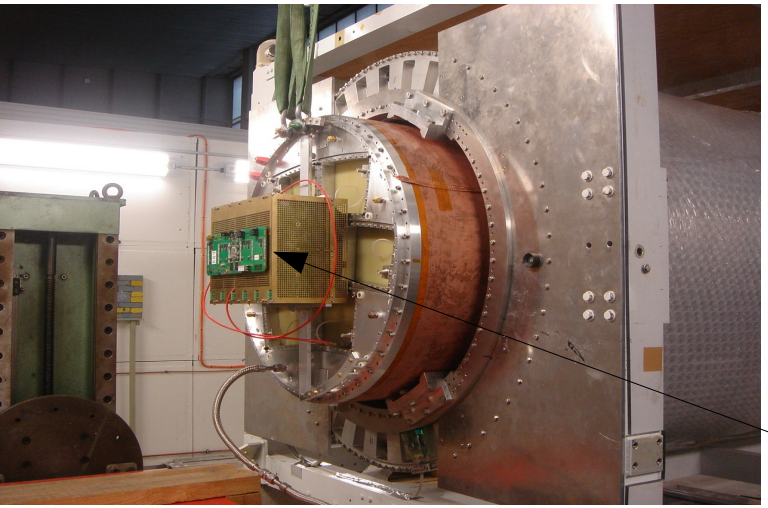
'Bulk Micromegas' panels, without resistive foil and with resistive carbon-loaded kapton, have been produced at CERN (Rui de Oliveira)

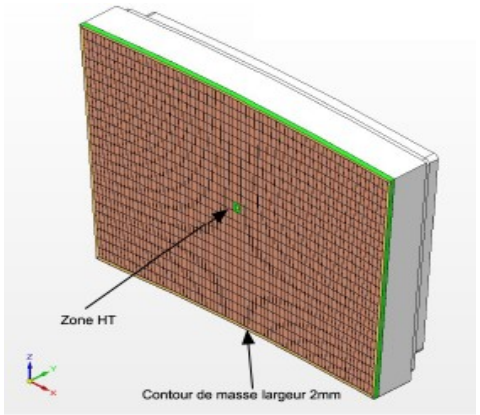


MicroMeGaS for LP:

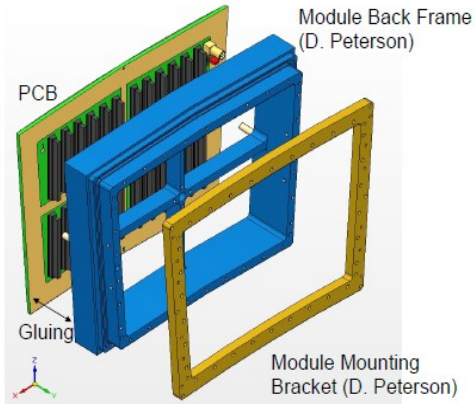
24 rows x 72 pads
Av. Pad size: 3.2 x 7mm²

P. Colas, CEA Saclay
M.S.Dixit, Carleton University





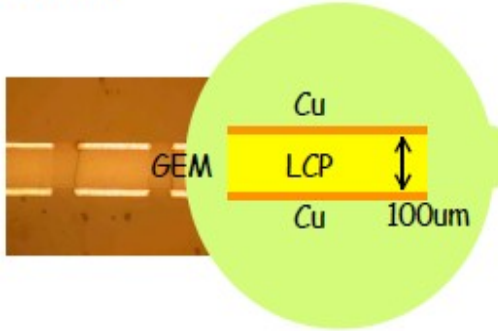
Detector side

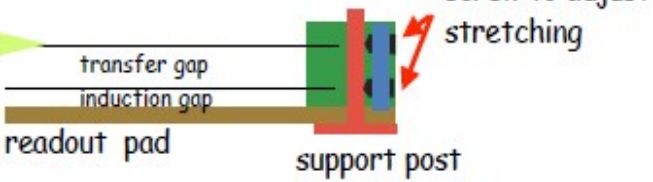


Readout electronics: AFTER (T2K TPC)

Double GEM Structure

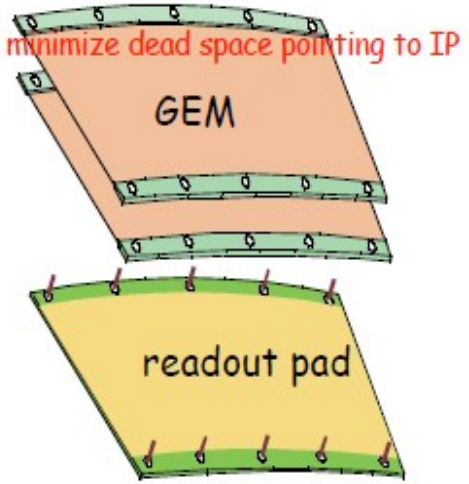
GEMs

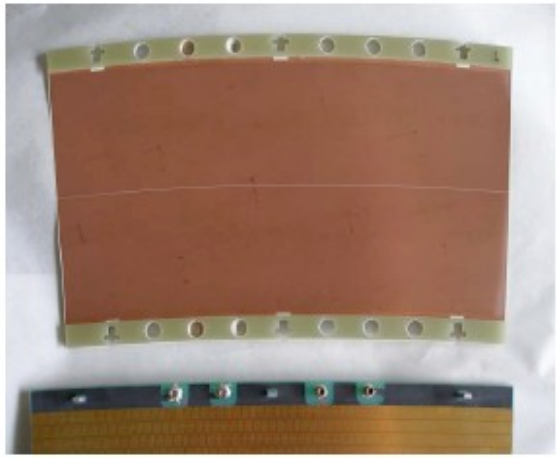




Transfer gap ~ 4mm (+2mm) : enlarge signal distribution width > 0.3* pad pitch

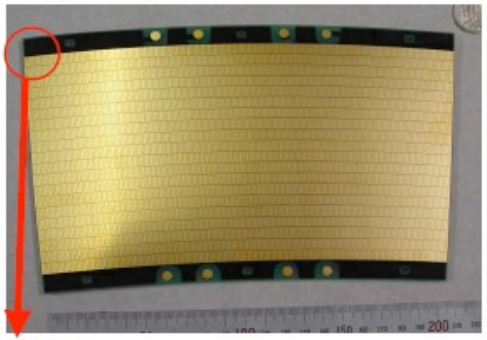
frame : top & bottom frame.
no side frame

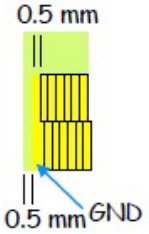




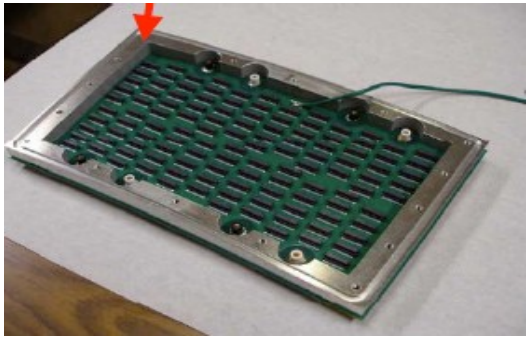
28 pad raws (176/192 pads/raw)
~1.2(w) x 5.4(h) mm^2
staggered every each layer

Total 5,152 ch/module





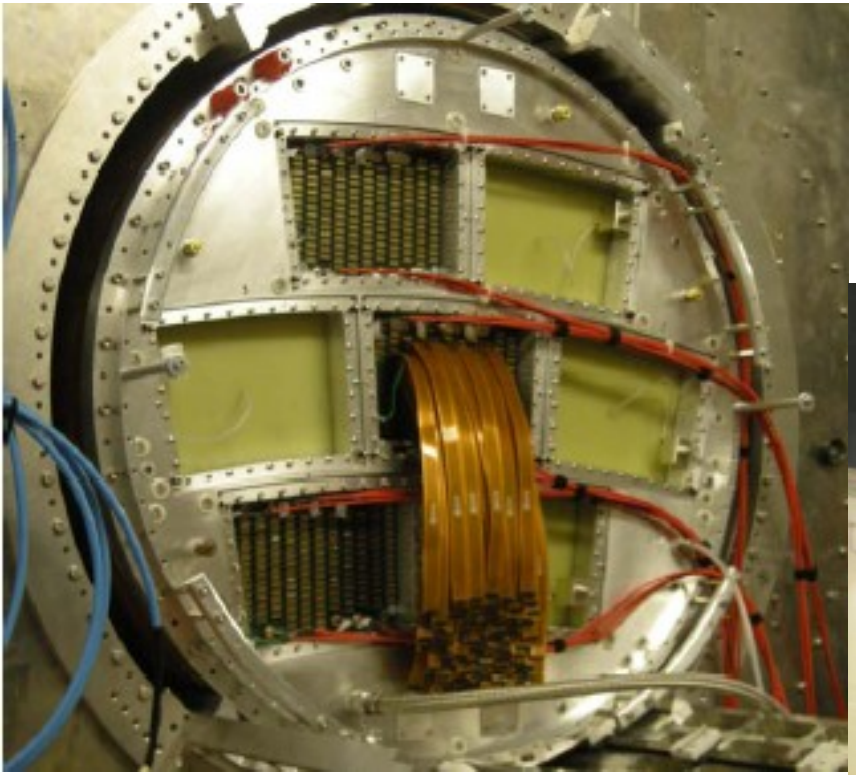
6 layers PCB
one GND layer



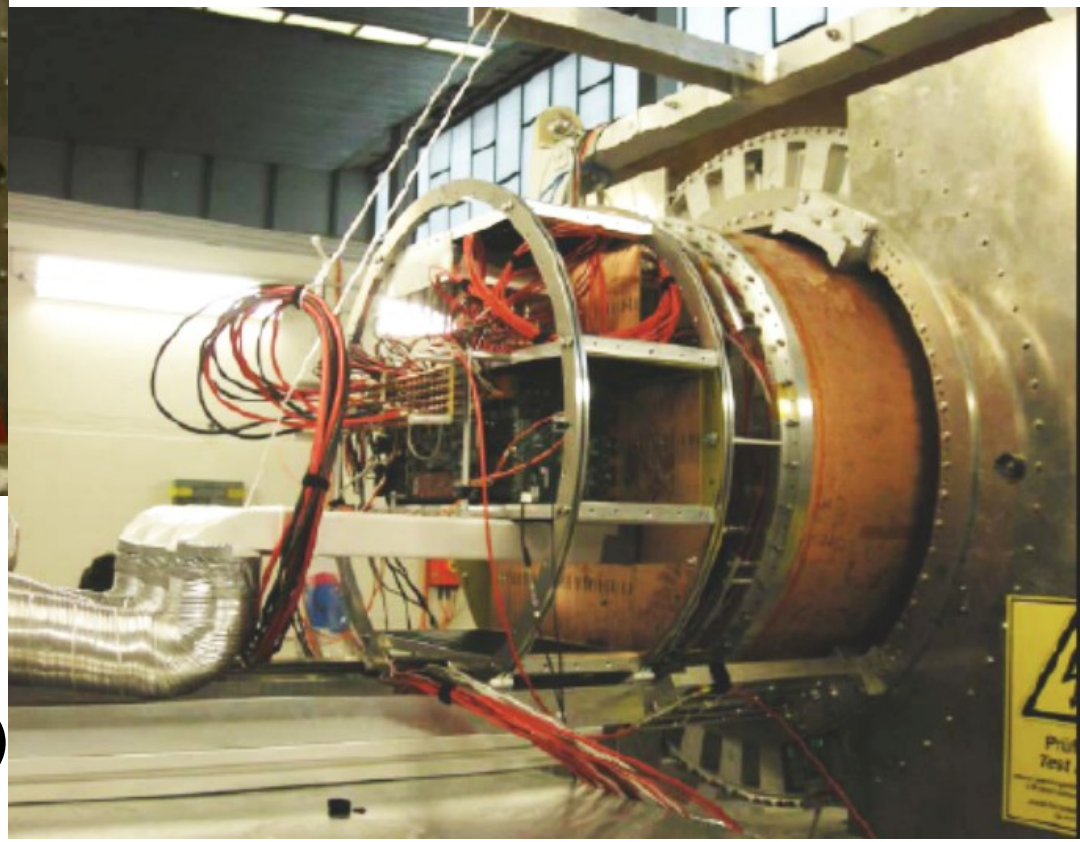
Optional: gating GEM

A. Sugiyama, Saga Univ.

Double GEM Structure



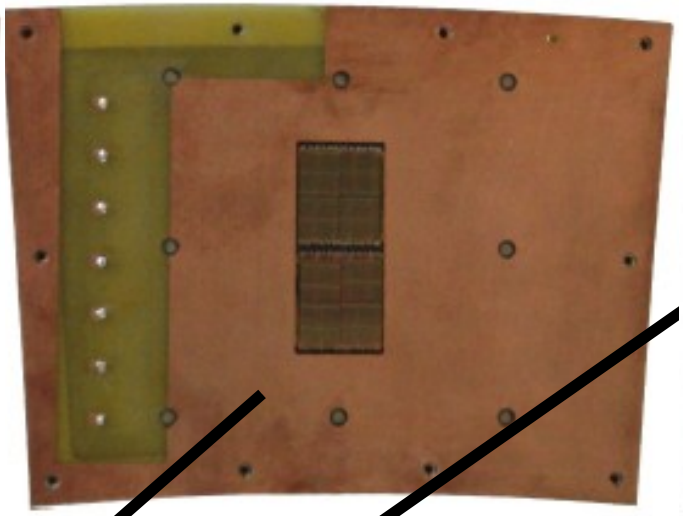
About 3200 channels
readout electronics

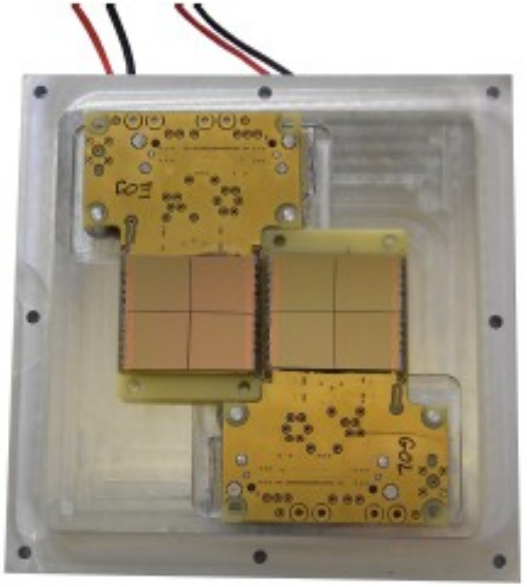


Readout electronics:
Based on ALTRO (ALICE TPC)

L. Joensson, LUND University

3-GEM Structure & TimePix





anode plane

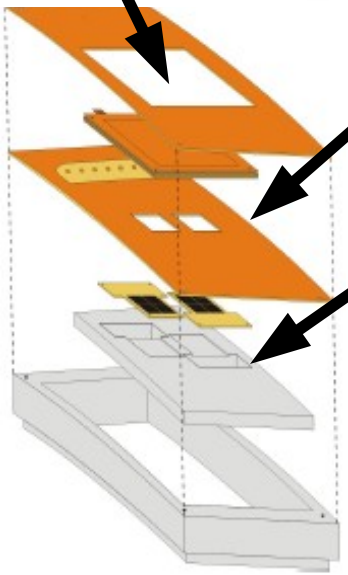
GEMs

readout plane

quad-boards

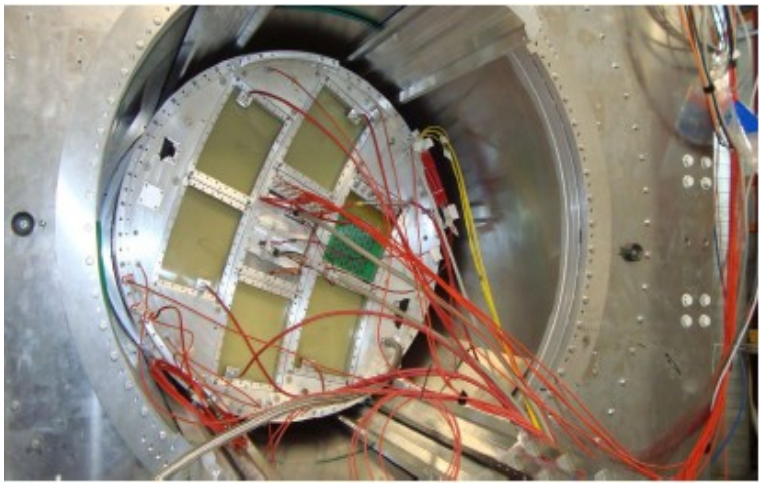
reinforcement of anode plane

redframe



Readout:
2 quadboards
(4 TimePix
Chips each)

J. Kaminski, Univ. of Bonn



Readout Electronics

Three-fold readout electronics:

- ALICE based:
  new PCA16 amplifier chip + ALTRO chip (EUDET & LCTPC) → adopted to ILC environment; designed within EUDET DAQ scheme

- T2K based:
  AFTER electronics for T2K TPC (CEA Saclay)

- TDC based:
  ASDQ chip + TDC (EUDET & Uni Rostock)

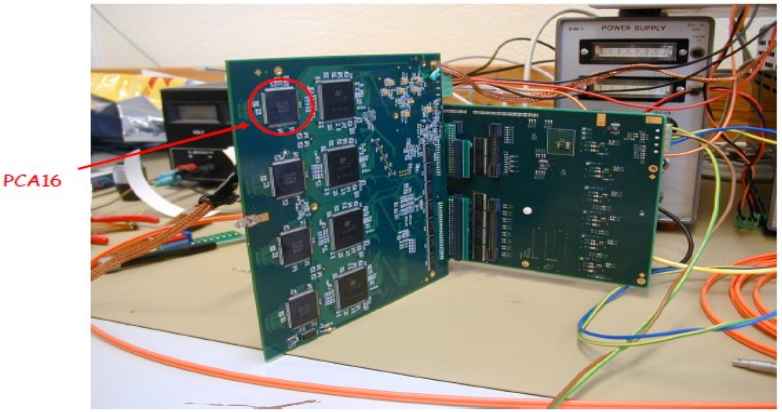
AFTER electronics for MicroMeGAS (resistive anode readout)
ALTRO and TDC based electronics will be hooked to the GEM detector modules (connector compatibility)

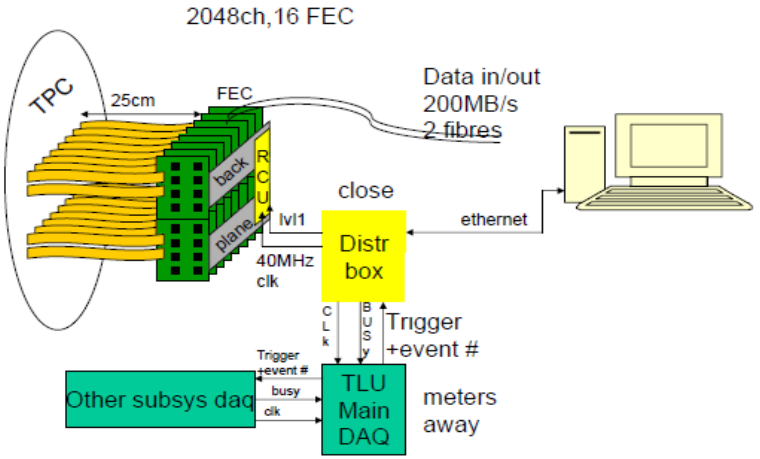
Readout Electronics: ALTRO

PCA16:

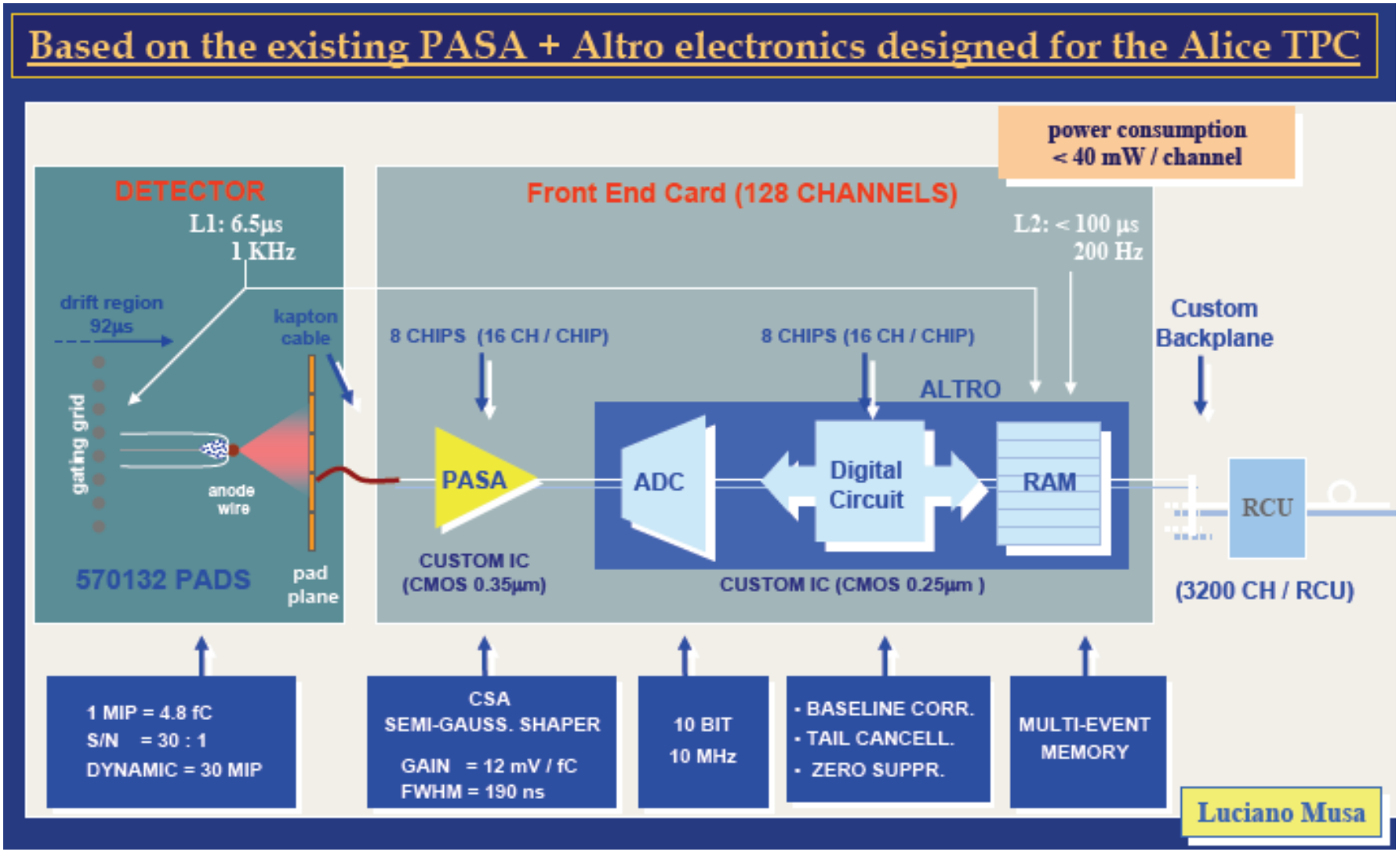
1.5 V supply; power consumption <8 mW/channel
16 channel charge amplifier + anti-aliasing filter
Fully differential output amplifier
Programmable features
signal polarity
Power down mode (wake-up time = 1 ms)
Peaking time (30 – 120 ns)
Gain in 4 steps (12 – 27 mV/fC)
Preamp out mode (bypass shaper or not)
Tunable time constant of the preamplifier
Basically pin-compatible with PASA

The test set up with a fully equipped front end board





Readout Electronics: S-ALTRO



P. Aspell, CERN

Readout Electronics: S-ALTRO

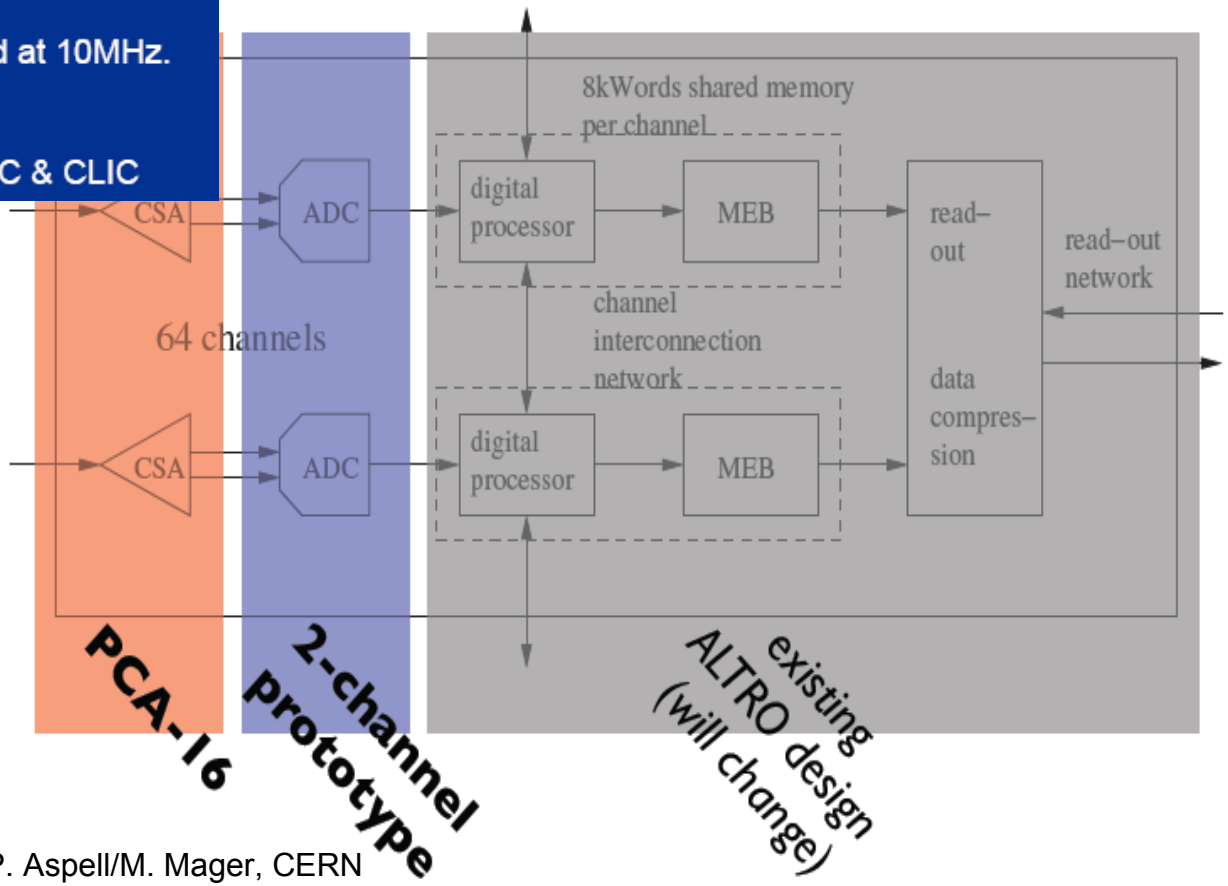
Goal :

To demonstrate integration per channel of an analog front-end, an ADC and digital signal processing in a single chip.

Data processing of 100us of data sampled at 10MHz.

Prepare ideas for TPC readout in the ILC & CLIC

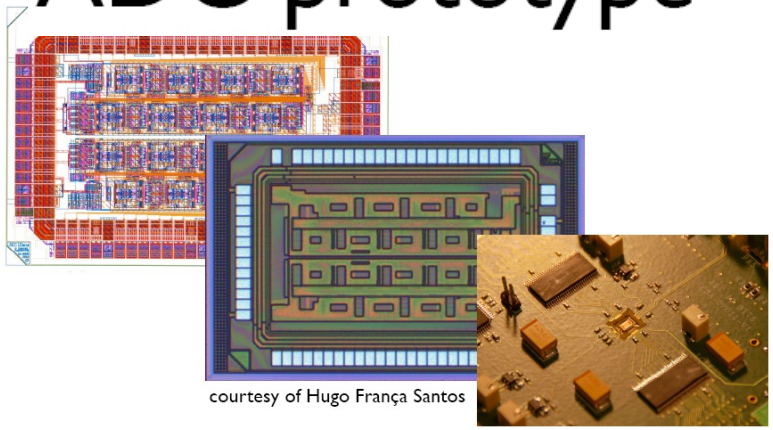
Current Design



P. Aspell/M. Mager, CERN

Readout Electronics: S-ALTRO

ADC prototype

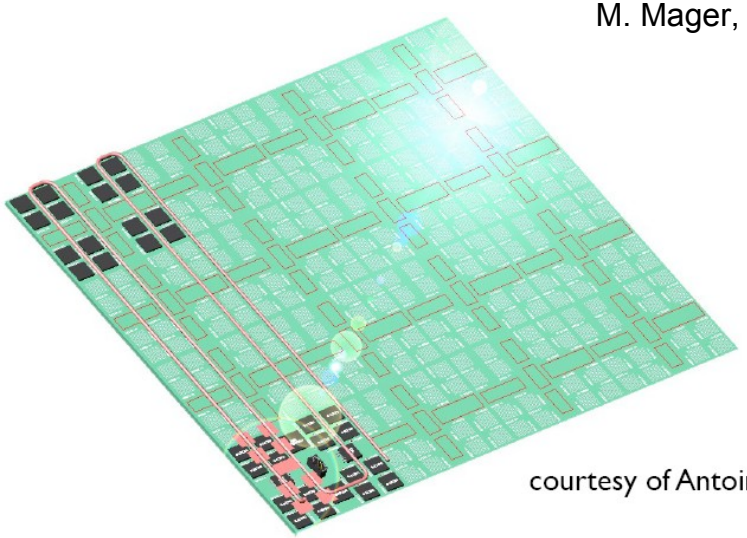


courtesy of Hugo França Santos

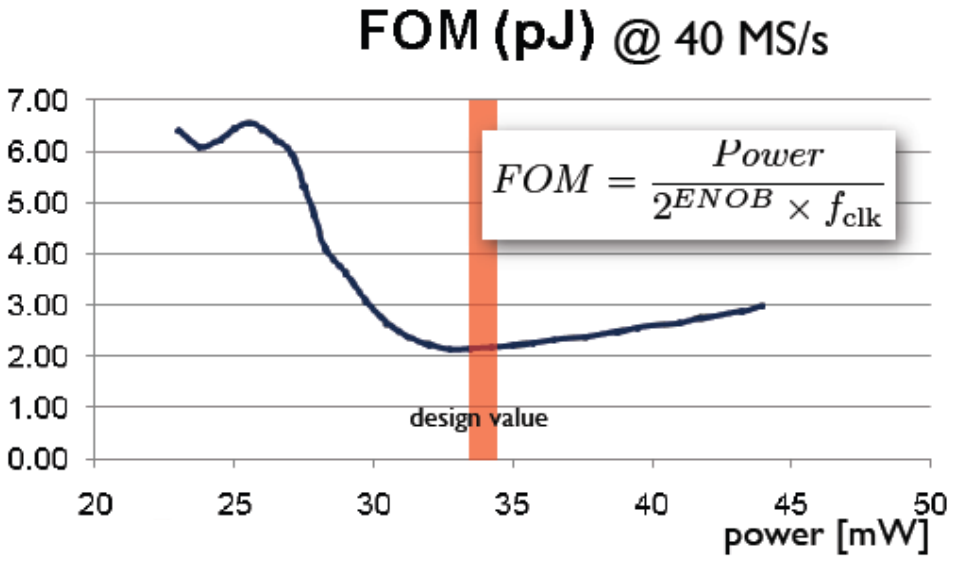
Single ADC area: 1.57 X 0.45 = 0.7 mm²

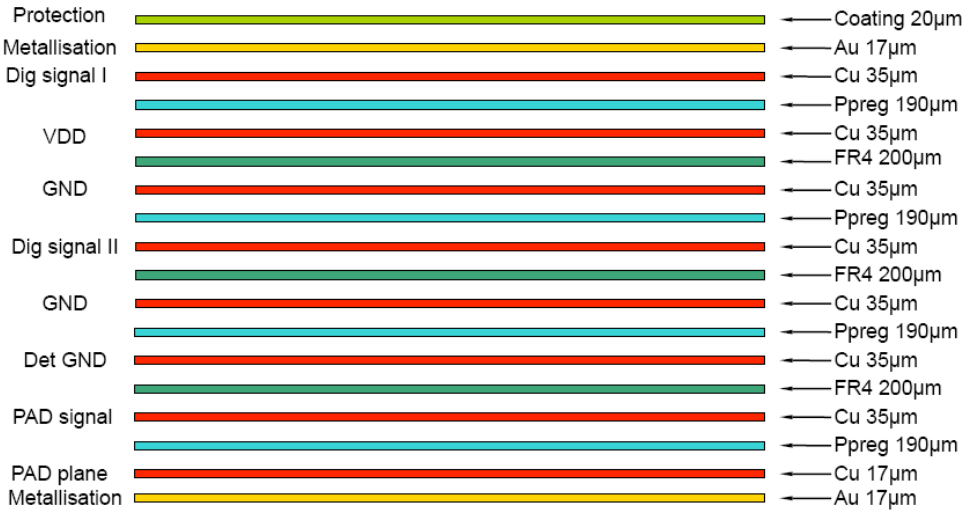
Prototype area: 2.35 X 1.6 = 3.76 mm²

M. Mager, CERN



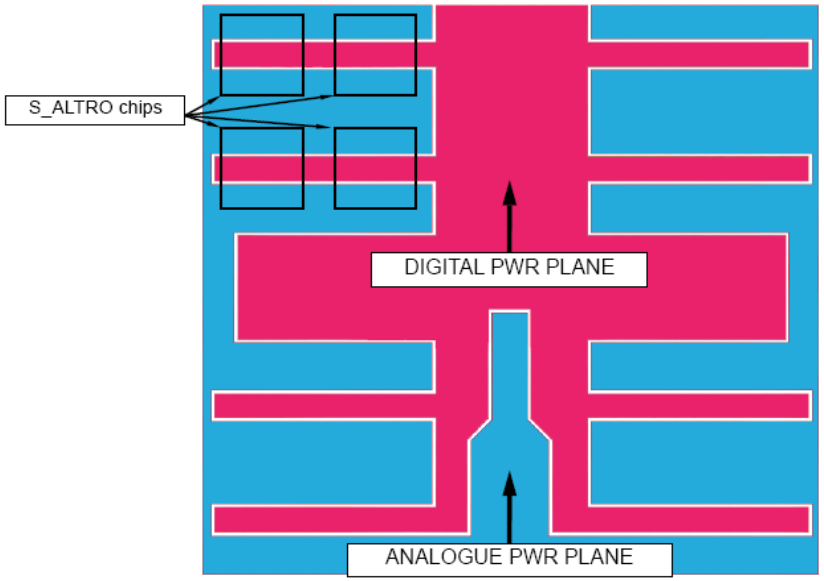
courtesy of Antoine Junique



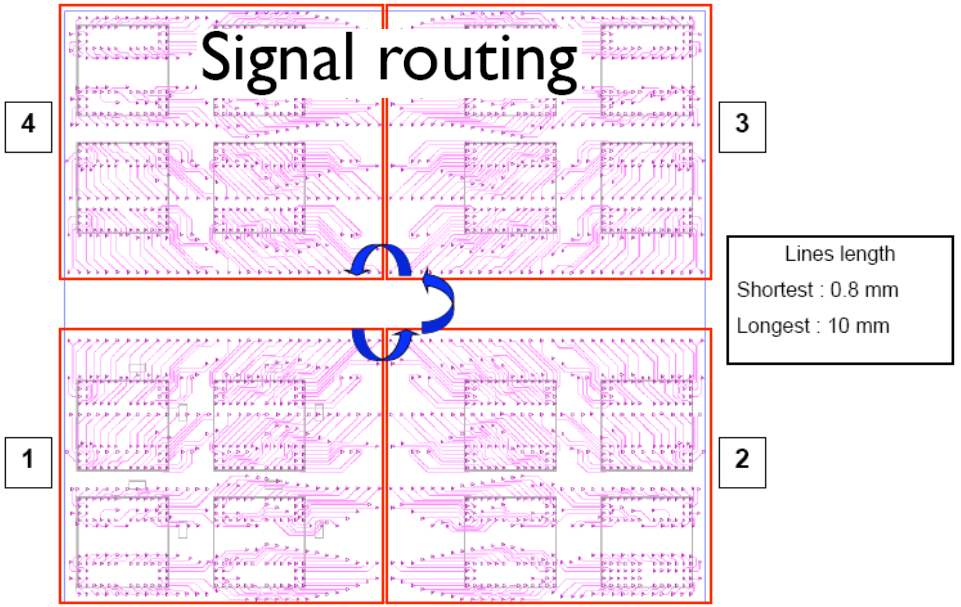


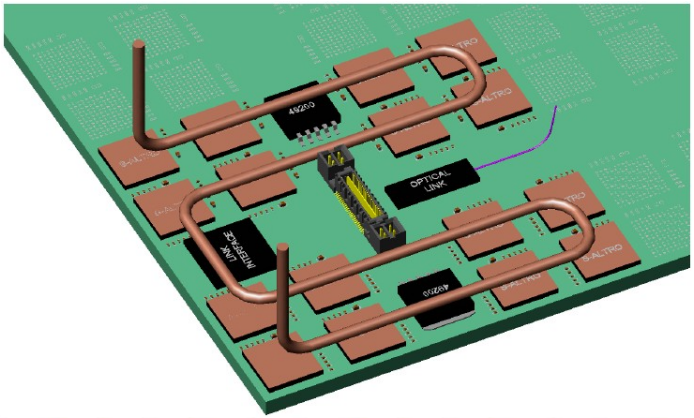
Readout Electronics: S-ALTRO

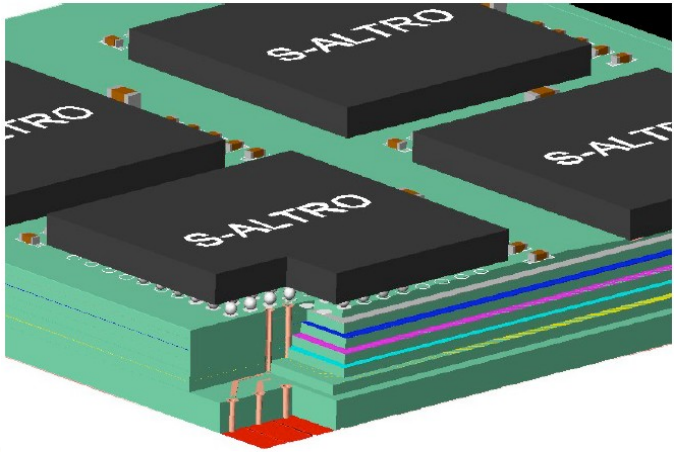
Power distribution



M. Mager, CERN







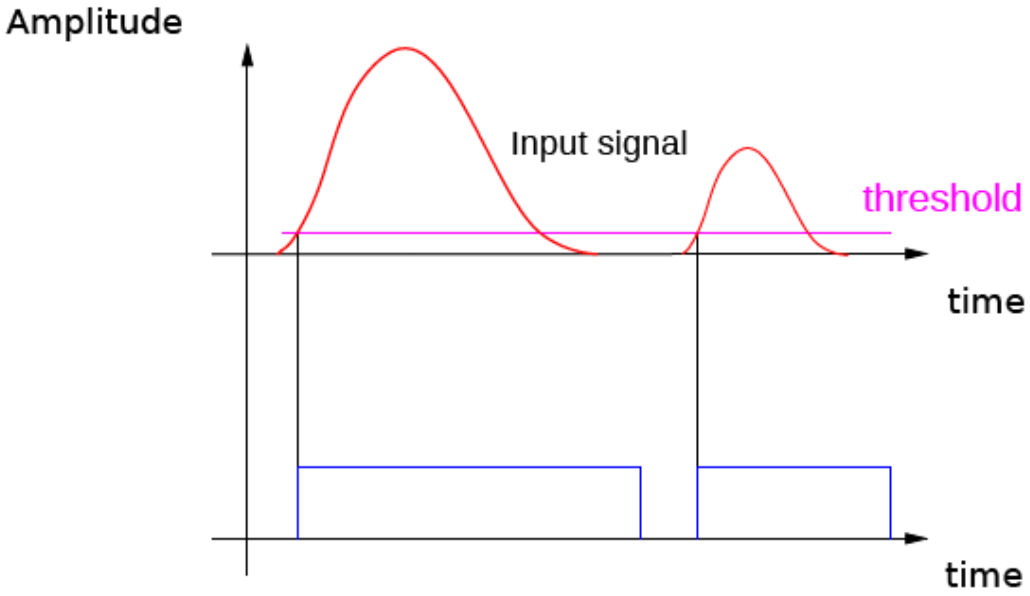
Readout Electronics: S-ALTRO

Plans

- Adopt design to real geometry, in particular:
  - non-quadratic shape of chamber
  - mounting margins
- Understand heat production and cooling
  - 40mW/ch
- Power pulsing
  - FPGA prototype by Japanese group

M. Mager, CERN

Readout Electronics: TDC



Output digital signal from QTC

Data zero suppression by analogue data processing.

Here example with threshold timing and charge-to-time conversion.

- The time of arrival is derived using the leading edge discriminator.
- The charge of the input signal is encoded into the width of output digital pulse.

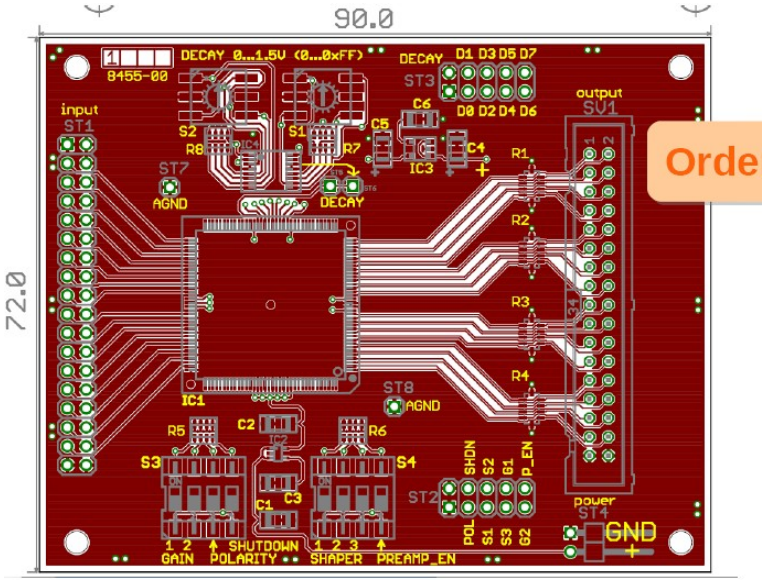
A. Kaukher, Univ. Rostock

Readout Electronics: TDC

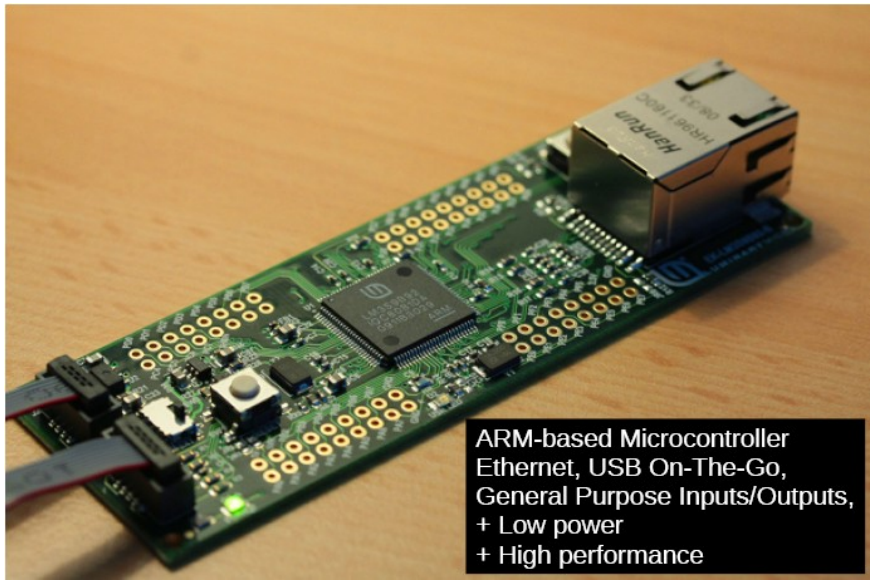
A. Kaukher, Univ. Rostock

Readout Electronics: TDC

PCA16 based readout board, to be used for study of signals from a GEM detector.



Ordered



Fast lane from a readout system (ADC/TDC) to existing industry solutions.

A. Kaukher, Univ. Rostock

Readout Electronics: TDC

No results with GEM Modules, yet. Higher gas gain is necessary.
Currently, VME crate is not prepared to work in (stray) B-field.

It is planned to use a Micromegas Module. Higher gas gains are possible. Larger area can be covered.

Next step:

- Threshold / efficiency scan,
- Charge-to-time conversion parameter (QDR) scan,
- Z-scan in LPTPC.

Signal simulation for a GEM detector is being prepared.
Last milestone (31.12.2009) to be reached in time.

A. Kaukher, Univ. Rostock

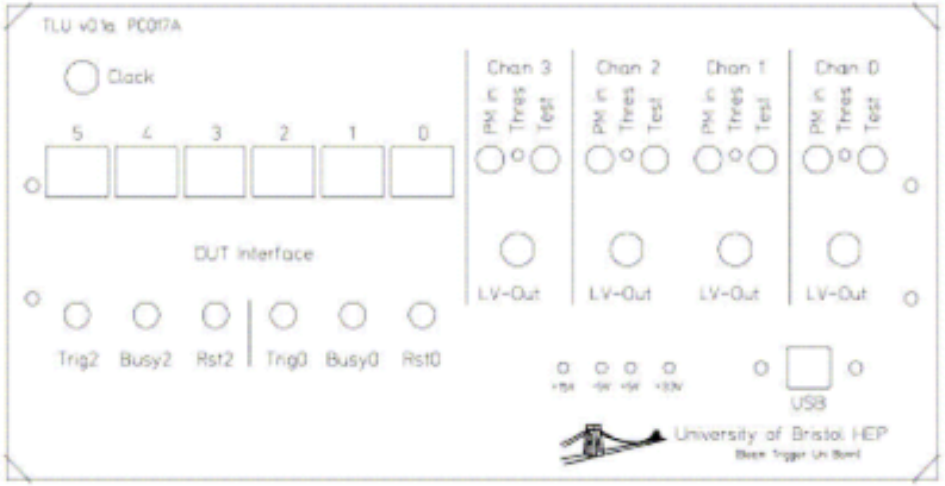
DAQ Trigger System

Trigger Logic Unit (TLU) provided by University of Brussels:

- 4 comparators
- Beam trigger with scintillators

TLU outputs:

- Trigger signal (LVDS)
- Event number (LVDS) pulled out by a data clock (LVDS)



Distributor box:

- Get event# from TLU and tag event with time
- Send event # + time to DAQ computer, assert BUSY for a fixed time: waiting for DAQ PC end of r/o
- Provide common clock

Monitoring

Monitoring via DOOCS:

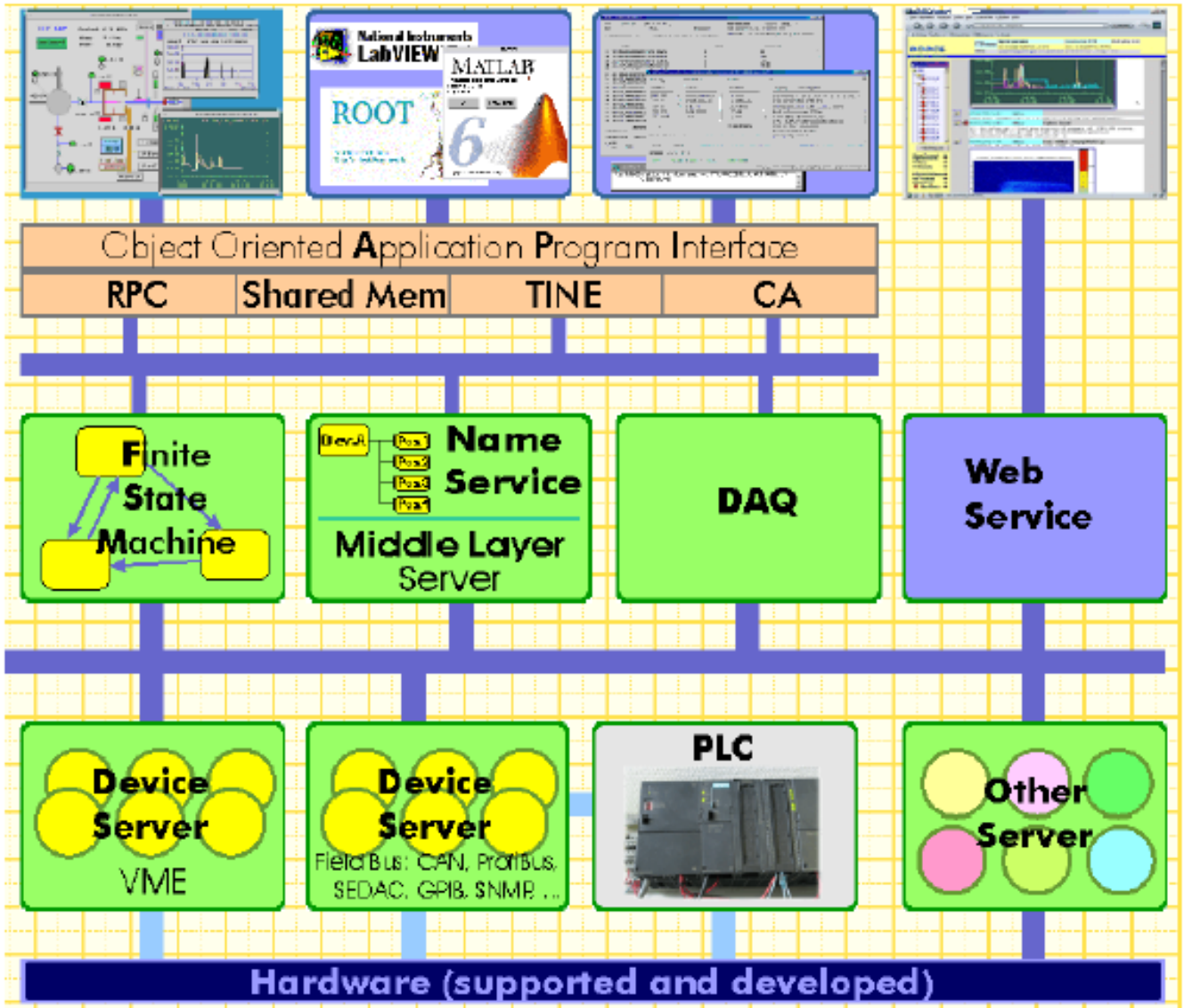
Distributed Object Oriented Control System; output as LCCD stream in LCIO format

hardware is connected to control system with Beckhoff devices

Monitored parameters (so far)

- Temperature
- Gas pressure
- Gas flow
- Impurities
- HV control

Monitoring

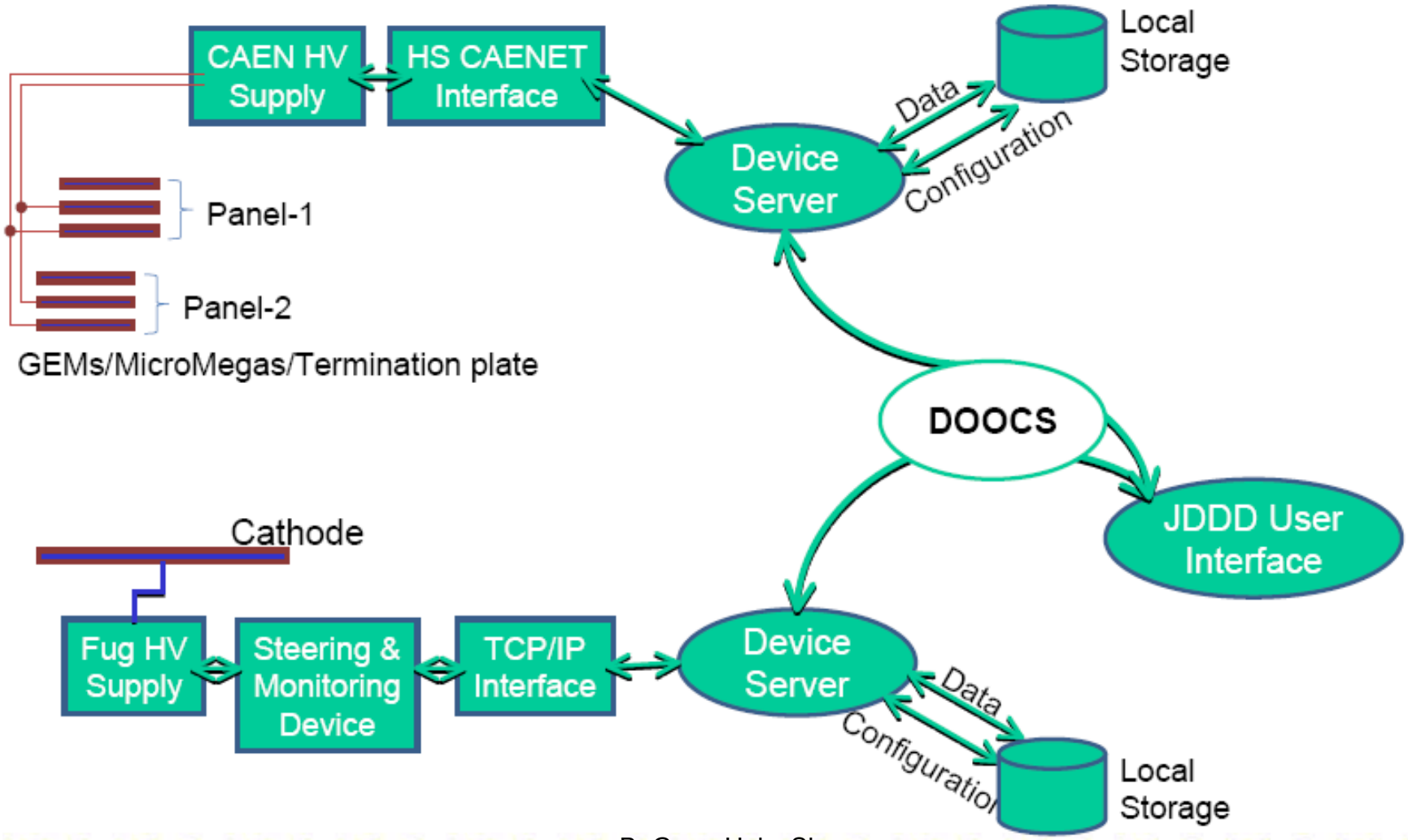

Application Layer
Object Oriented Application Program Interface
RPC
Shared Mem
TINE
CA
Communication
Finite State Machine
Name Service
Middle Layer Server
DAQ
Web Service
Middle Layer
Device Server
VME
Device Server
FieldBus: CAN, ProfiBus, SEDAC, GPIB, SNMP, ...
PLC
Other Server
Device Layer
Hardware (supported and developed)

Gas-/HV-System

Basic gas system installed:

- Mass Flow Controller → gas pressure regulation
- Stainless steel flexible tubing
- Monitoring of pressure, temperature and H_2O/ O_2
- Safety valve

Gas-/HV-System



B. Gaur, Univ. Siegen

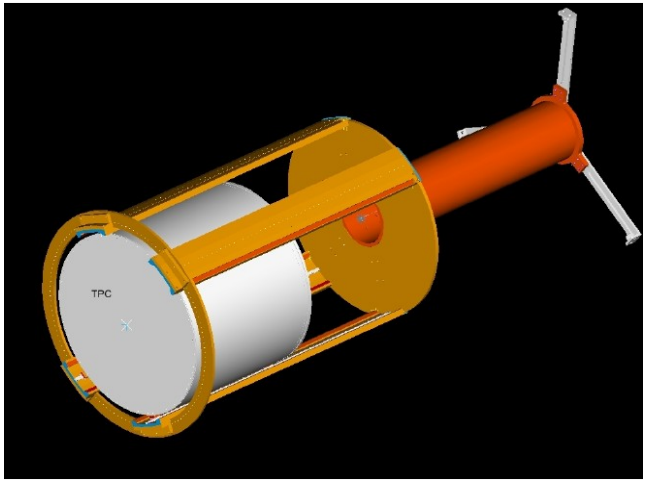
Common Software

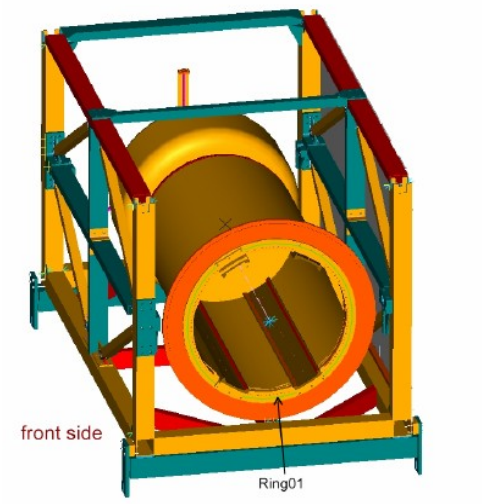
Goal:
- Common data taking
- Common data stream
- Common data format
- Unified reconstruction and analysis

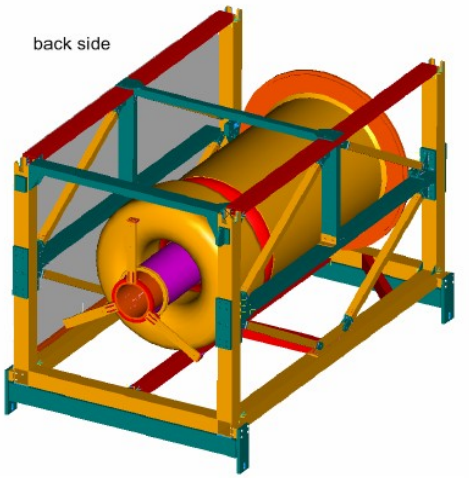
Modular **A**nalysis & **R**econstruction for the **L I N**ear Collider

Modular MarlinTPC:
Marlin based simulation, digitization, reconstruction and analysis code for the TPC

LP Mechanics

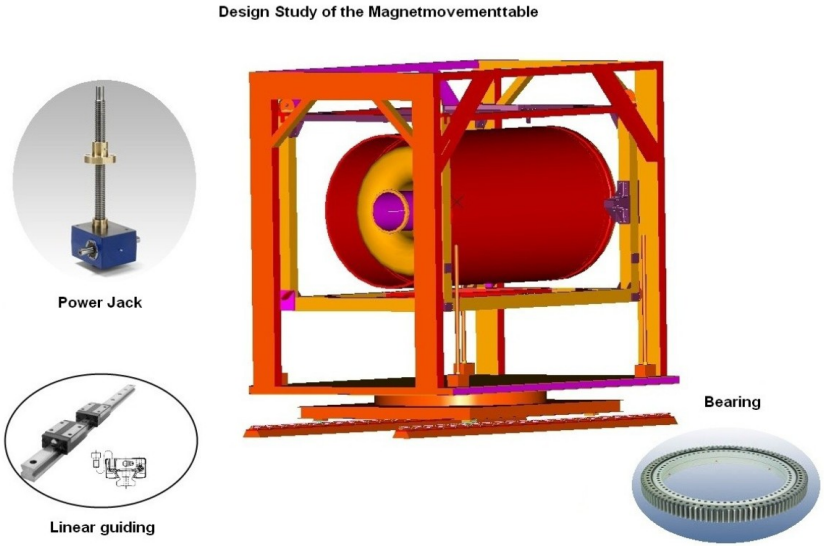






Support structures:

- TPC
- PCMAG

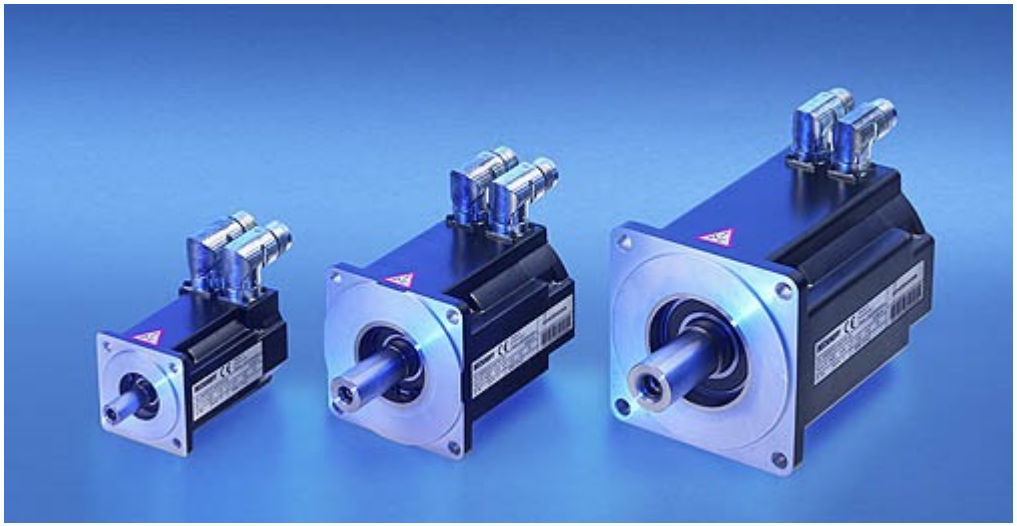


F. Hegner, V. Prahl, R. Volkenborn, DESY

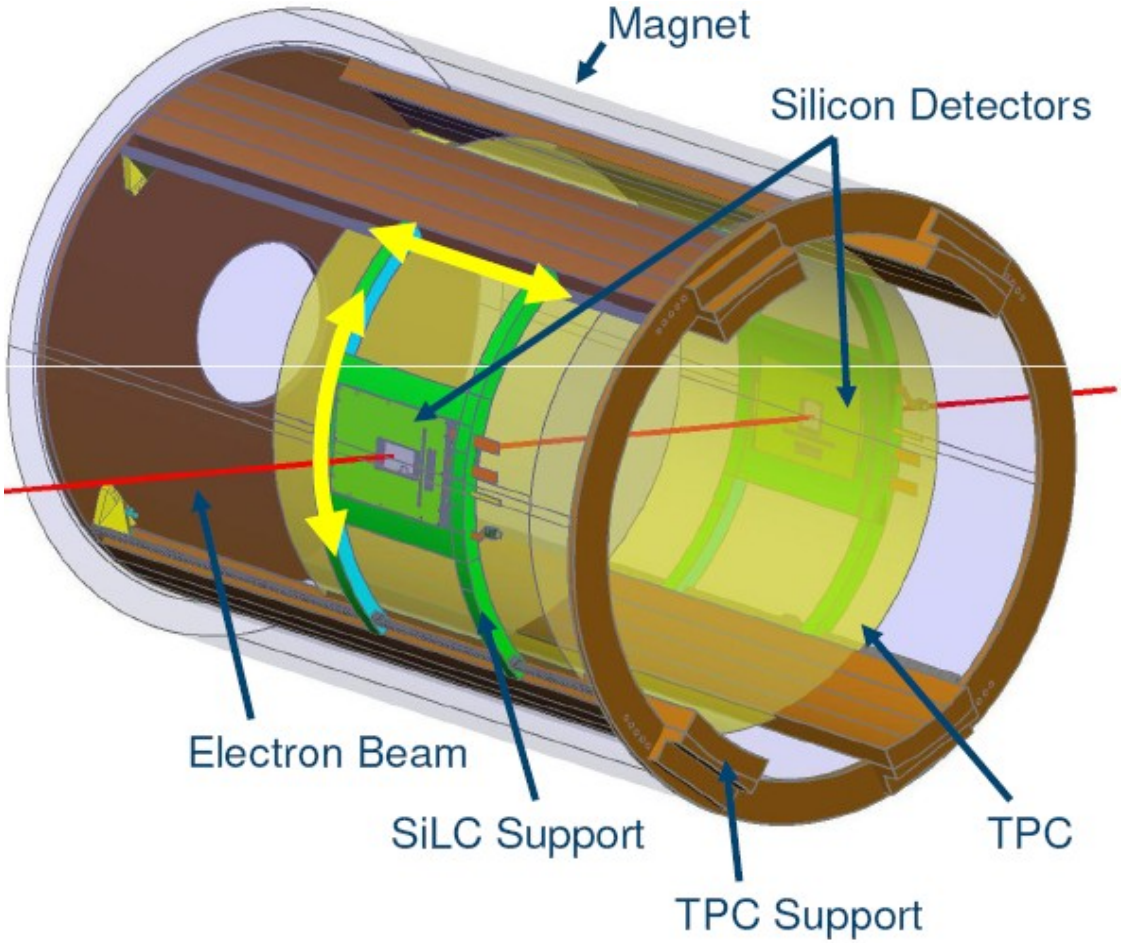
LP Mechanics

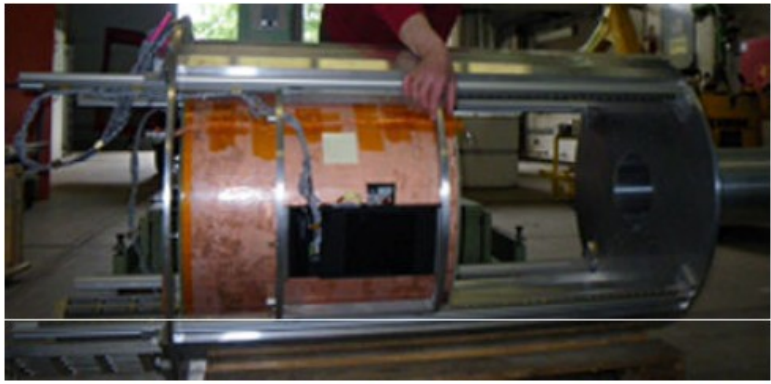
LP Mechanics

Actuation and Control



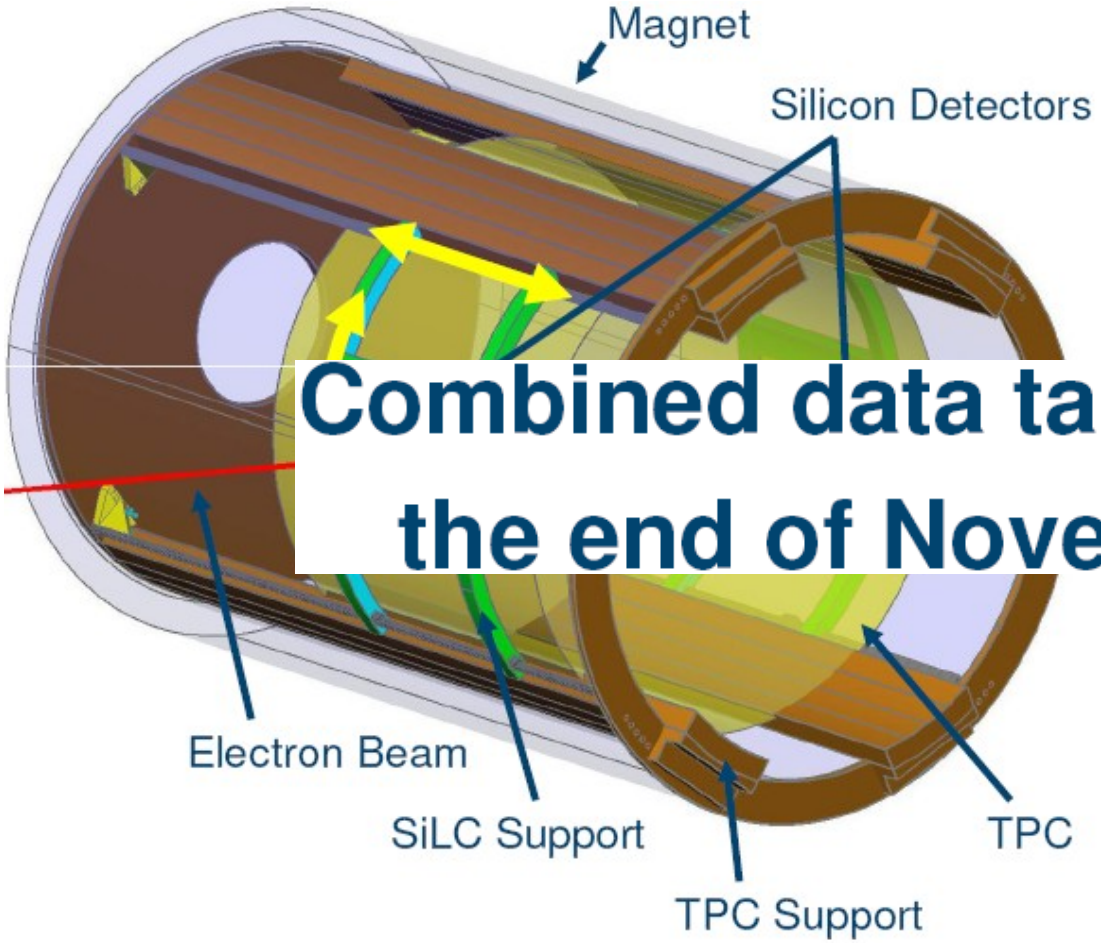
Si Envelope





S. Haensel
HEPHY Vienna

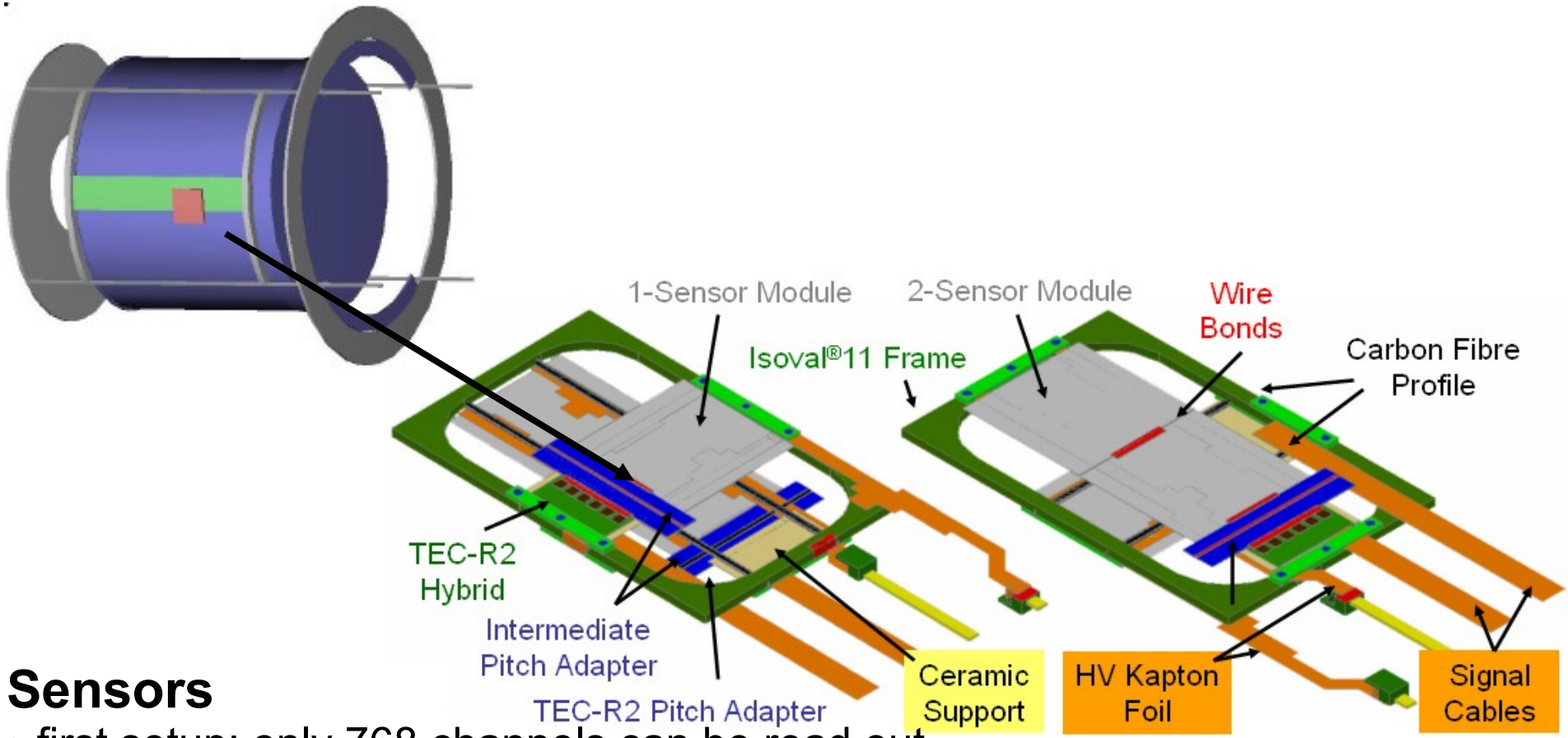
Si Envelope



Combined data taking before the end of November 09!

S. Haensel
HEPHY Vienna

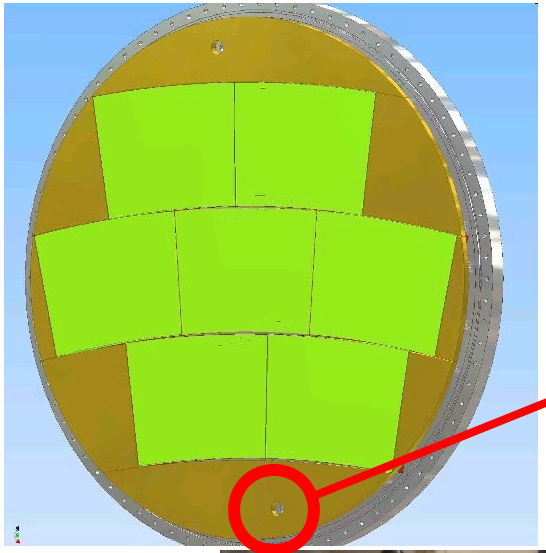
Si Envelope

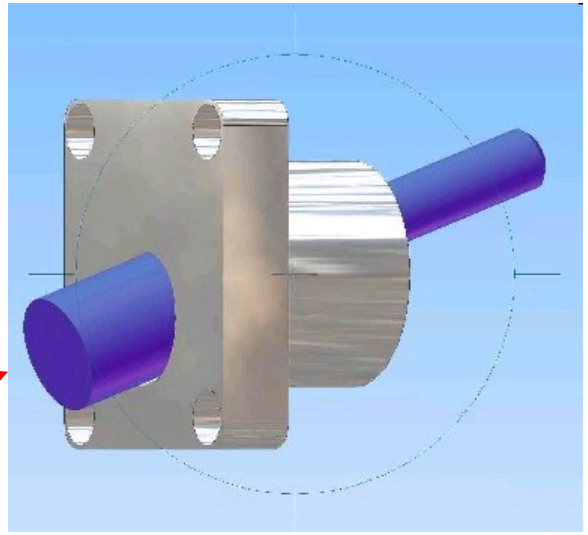


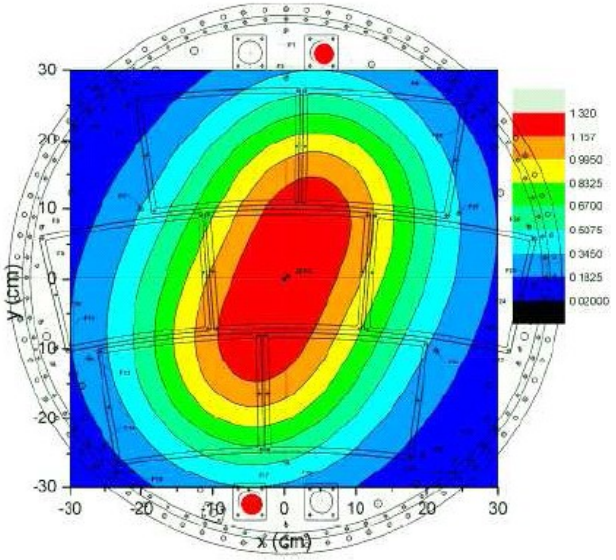
Sensors

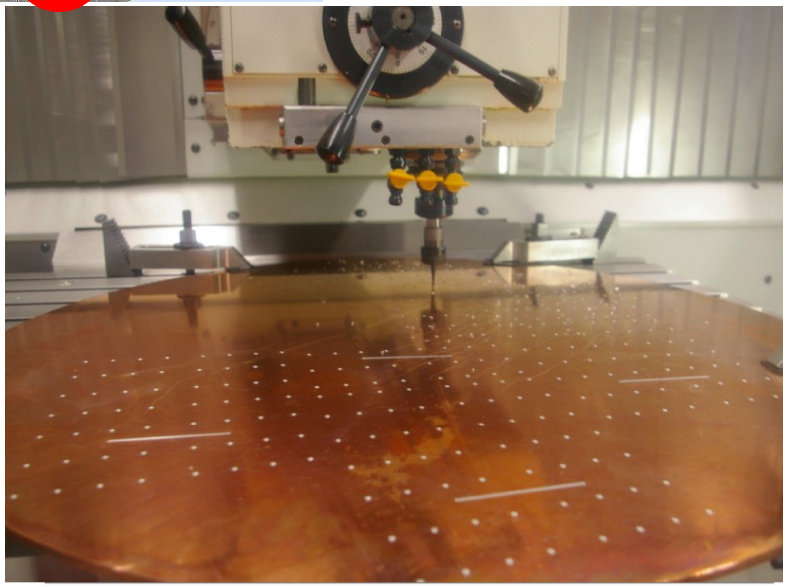
- first setup: only 768 channels can be read out
  - ➢ the readout sensitive area is reduced to 38.4 x 38.4 mm² (only the intersecting readout area of the two modules on top of each other is interesting)

Laser Calibration Setup

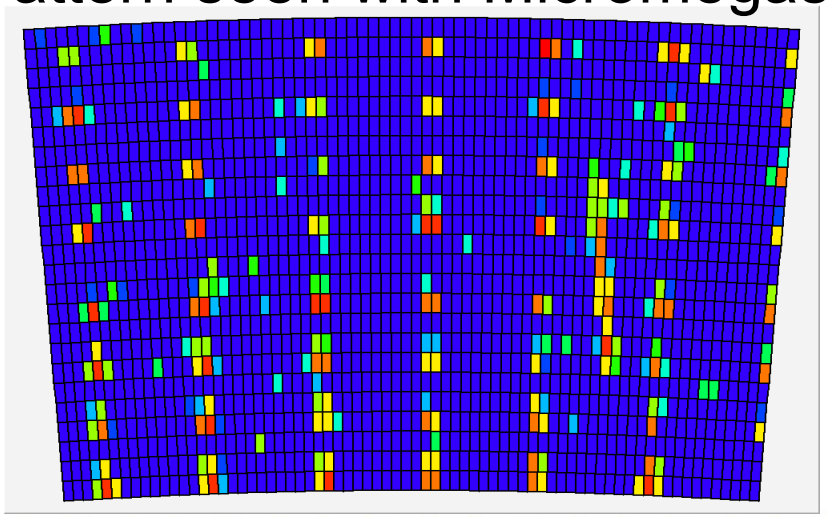








Pattern seen with Micromegas



Status

- Field cage, cathode end plate / alignment wheel, cathodes delivered, one cathode patterned
- 3200 channels of ALTRO electronics in use

  640 channels TDC electronics available → noise problems

  S-ALTRO development under way
- TLU trigger system available → synchronization problems
- Basic Gas-/HV-system in use
- Common software under construction
- Infrastructure for SiLC envelope installed
- LP with three different amplification technologies operated
- 12 weeks of test beam with LP operation so far → more to come

Summary & Outlook

- A Large Prototype of a TPC has been built and is being assembled/tested/commissioned by the LCTPC collaboration
- Two MPGD technologies (with three electronics techniques) are being tested:
  - Micromegas
  - GEM
- Infrastructure for Large Prototype has been constructed
- e^- test beam (DESY) in conjunction with PCMAG (*1T* magnet)
- Preliminary results are looking very promising
- Further test beam campaigns in the next year:
  - Backplane integrated 10,000 channel readout system, based on ALTRO electronics
  - Seven Micromegas modules with AFTER electronics attached to the modules