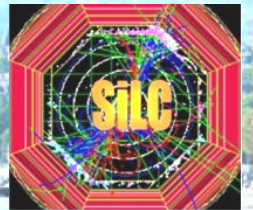


# JRA2 TA2-SiTRA - Status Report

*Helsinki U. Helsinki (Fi), LPNHE-U. Pierre & Marie Curie/CNRS-IN2P3 (Fr), Charles U. in Prague (Cz), IFCA (CSIC-U. Cantabria) Santander (Sp).*

*Also contributing to this activity the associated members:  
CNM-IMB (CSIC) Barcelona, Obninsk State U Rusia, HEPHY Vienna*

*Work also performed within the SiLC R&D collaboration  
(U. of Barcelona ,Torino INFN, ITE Warsaw)*



EUDET Annual Meeting, U. Genève 20th October '09

Iván Vila Álvarez

Instituto de Física de Cantabria [CSIC-UC]

- Introduction:
  - SITRA task scope.
- '09 Activities Report:
  - Infrastructure:
    - DAQ and FE chip.
    - Mechanics: Modules, faraday cage.
    - Alignment
    - Chip/sensor interconnections
- Transnational Access

- The SiTRA must provide:
  - => The Silicon Modules and Silicon prototypes
  - => The Faraday & cooling cage
  - => The 3D Table
  - => The alignment system
  - => The FE readout chips
  - => The DAQ system

**HERE, STATUS REPORT ON THESE ITEMS AND SOME OTHERS CLOSED RELATED R&Ds FROM ASOCIATES.**

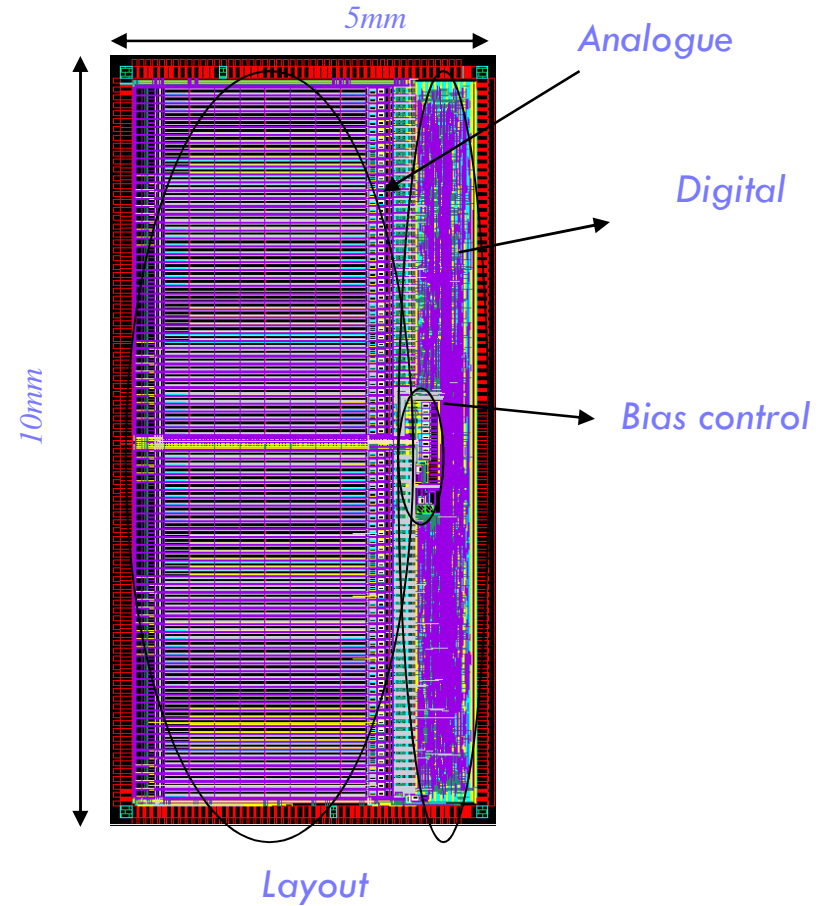
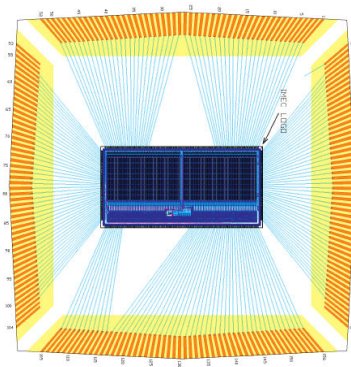
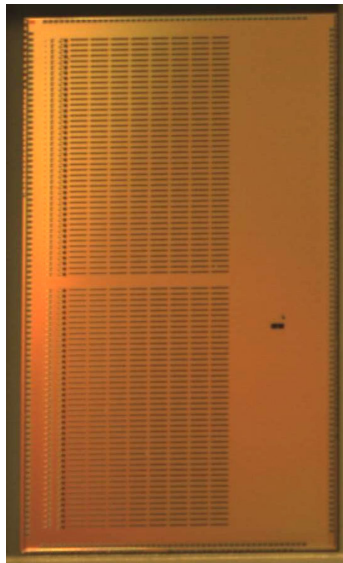


In2p3

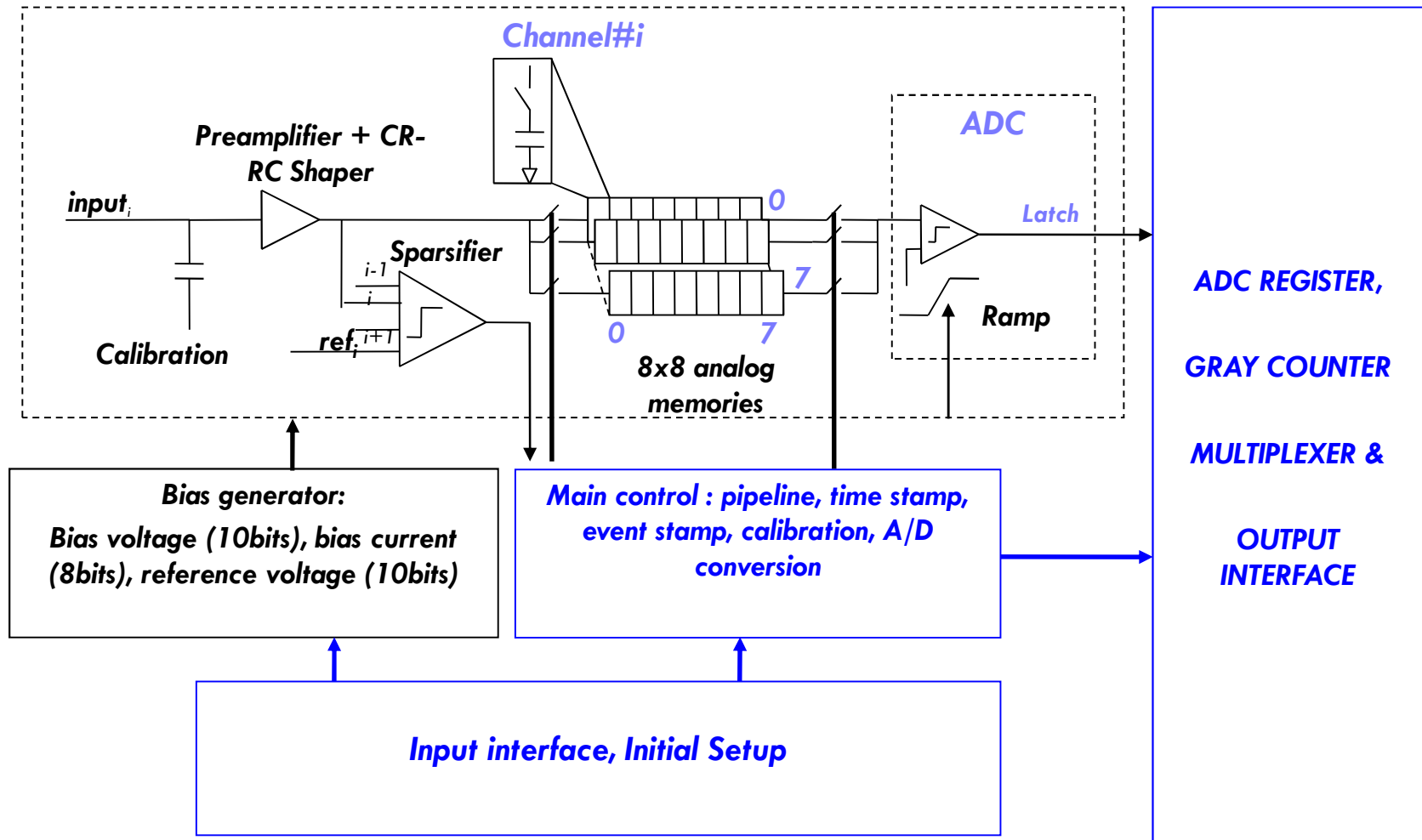


# INFRASTRUCTURE

- UMC 130nm
- 88 Channels
- Received in oct 08



# FE R/O chip 88-channel

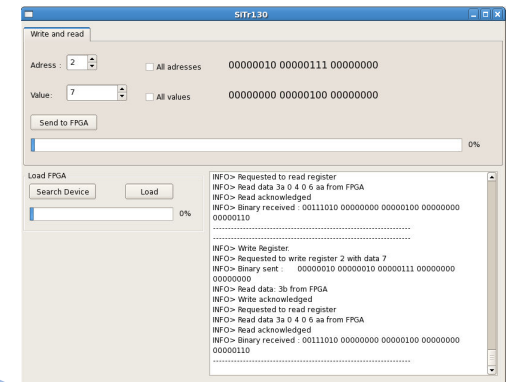
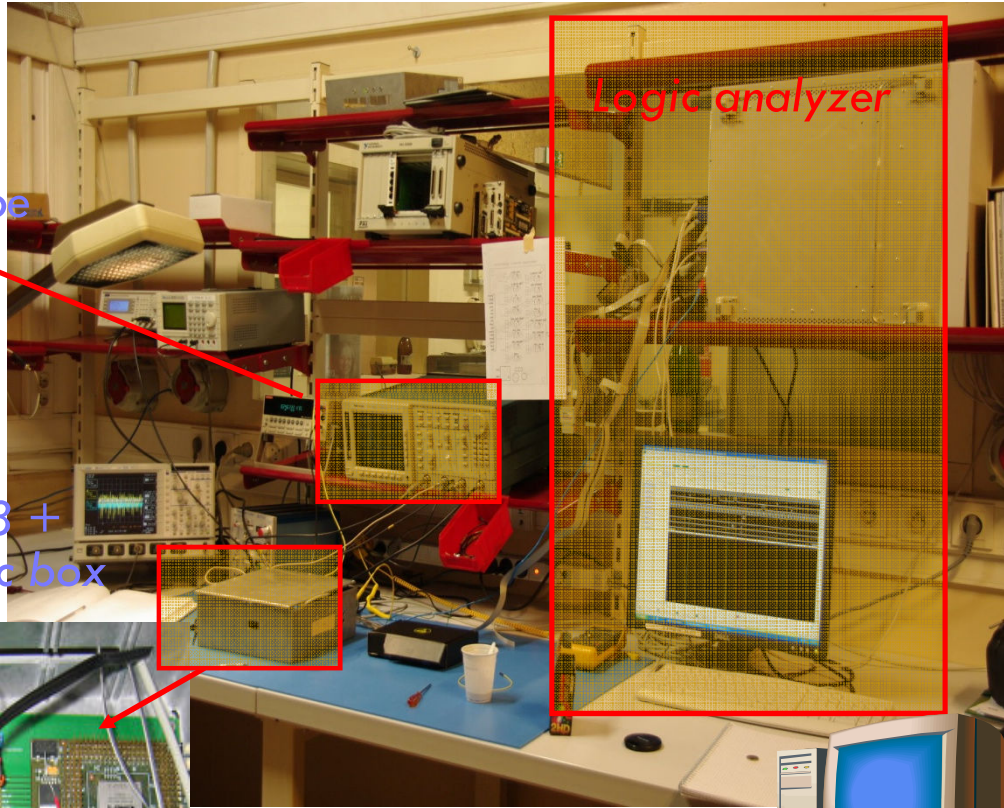
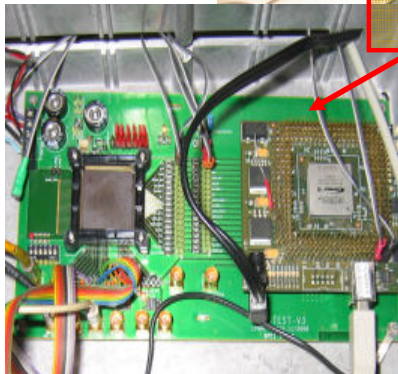


# Lab test bench of SiTr\_88

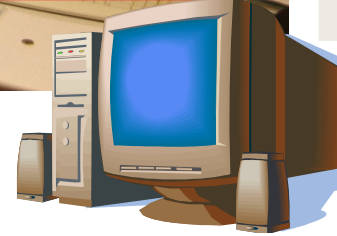
Oscilloscope

Logic analyzer

SiTR\_130-88 +  
FPGA in metallic box



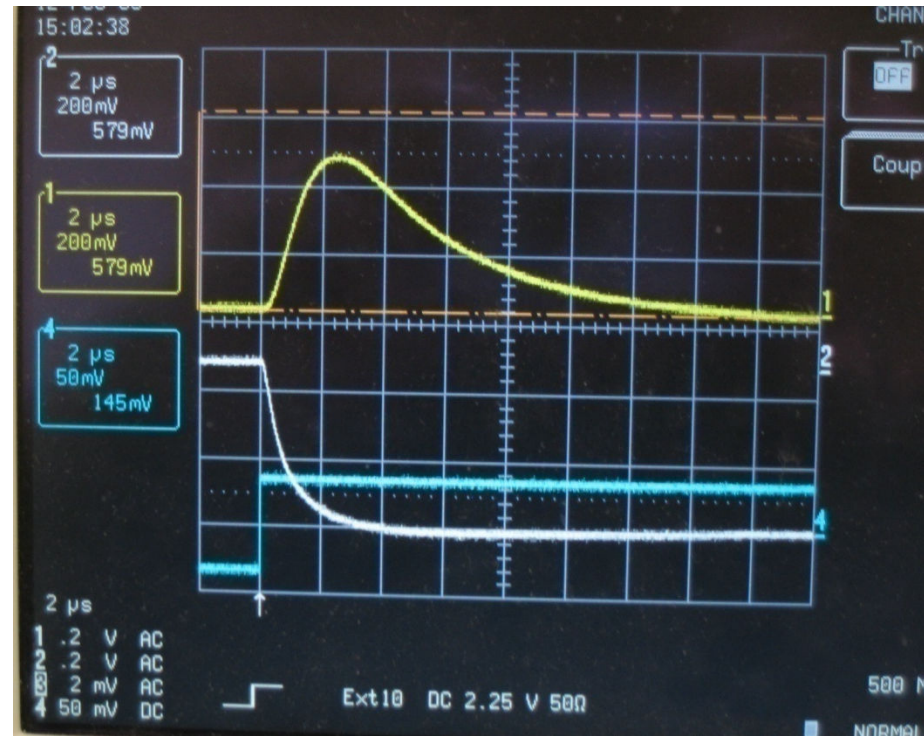
USB link



PC and C++ based  
program allows the  
control of the circuit

# Results from analogue part

- *Problem with the serial to parallel input of the digital part*
- *Analog part accessible through 88th channel fully equipped with test points*
- *Preamp → white track*
- *Shaper → yellow track*
- *Power supply → 1.3 mW/channel*
- *Linearity → 2.6% up to 24 MIP*





- *Optimized silicon surface by using  $2f/\mu\text{m}^2$  process & reduce analog memories to  $4 \times 8$*
- *Modular structure by bloc of 64-channel*
- *JTAG integration possibilities*
- *More test & calibration sub-circuit*
- *Possibility to use IBM 130nm CMOS*
- *The direct connection “bump-bonding” is under investigated*

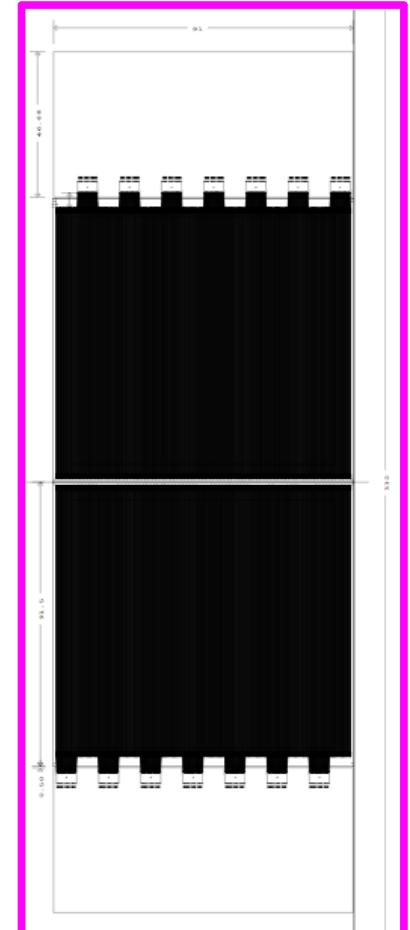
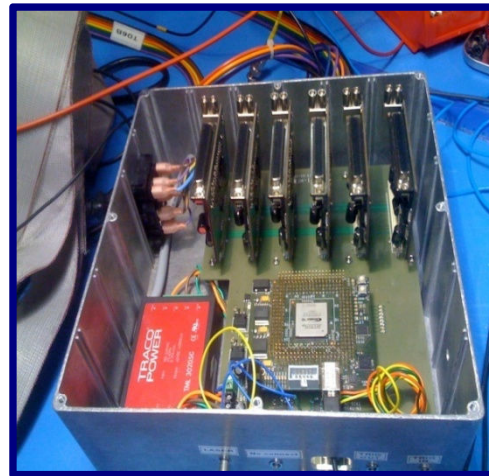
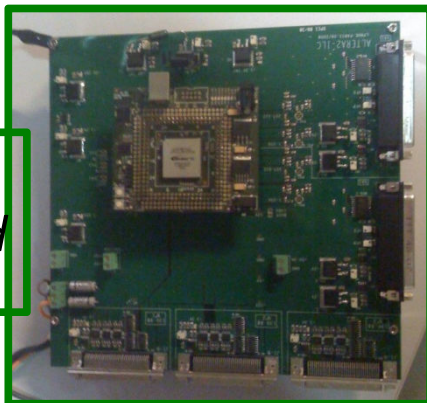
# The related DAQ system: Hardware part

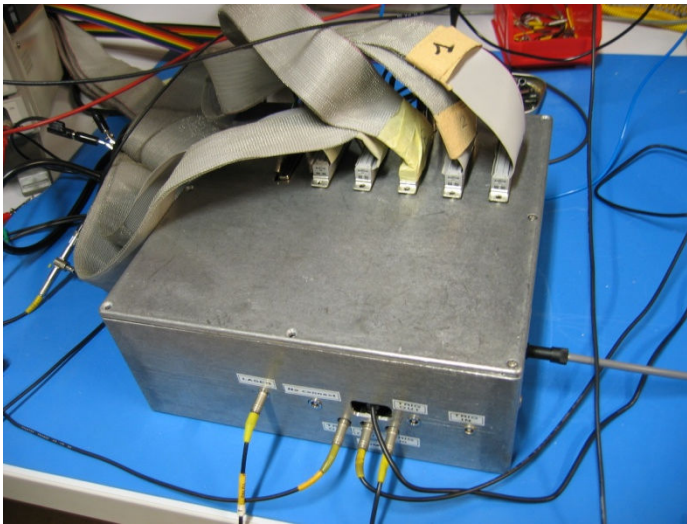
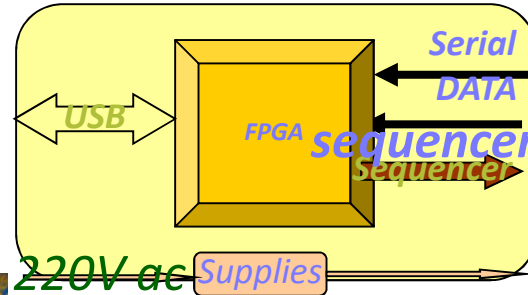
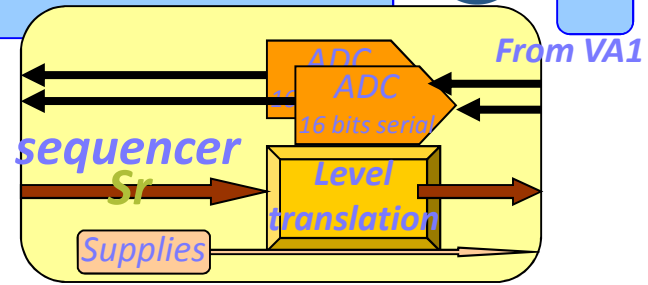
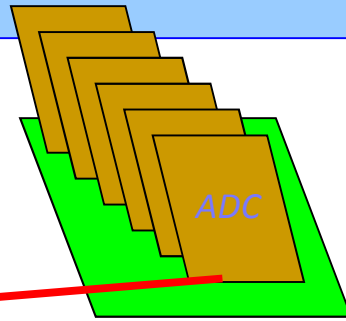
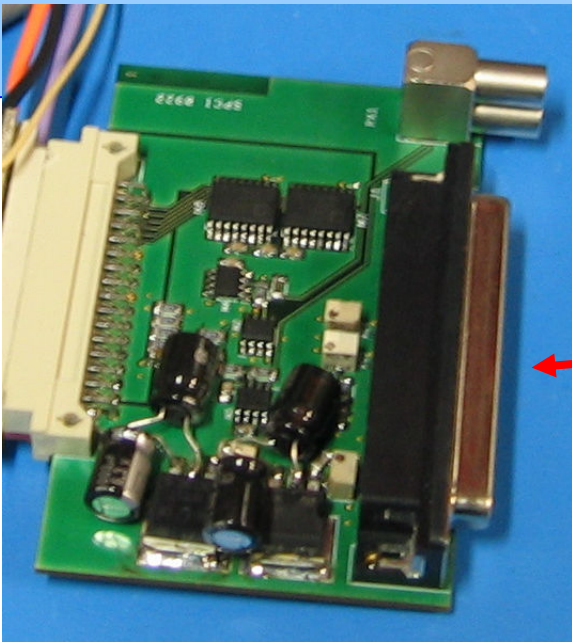
- The number of channels to read out is growing
  - Alignment tests (2009) => 2560 channels
  - Combined calo tests (mid-2010) => 15000 à 20000 ch
  - 2011-2012 -> much more !!!
- DAQ hardware “Kit” , evolutive system
  - VA1 (VFE reference), SiTR\_130 and new prototypes, mixed mode FE (Ref+SiTR\_130)
  - XILINX modules: Altera/USB (currently available → Altera/(Ethernet, USBx)? Under development

*Redesign of the module for the new SiTR\_130-128*

*FPGA system for VA1 only*

*Version For mixed FE chips*





The electronic box

## A new DAQ electronics for VA1' readout only

Only one USB link for the whole box





# INFRASTRUCTURE

# Construction of the Silicon modules

- Design of the modules

*Modules are made of two sensors bonded to each other  
(bonding performed at CERN bonding Lab)*

*Flexibility wrt the FE chip (hybrid board can be replaced)*

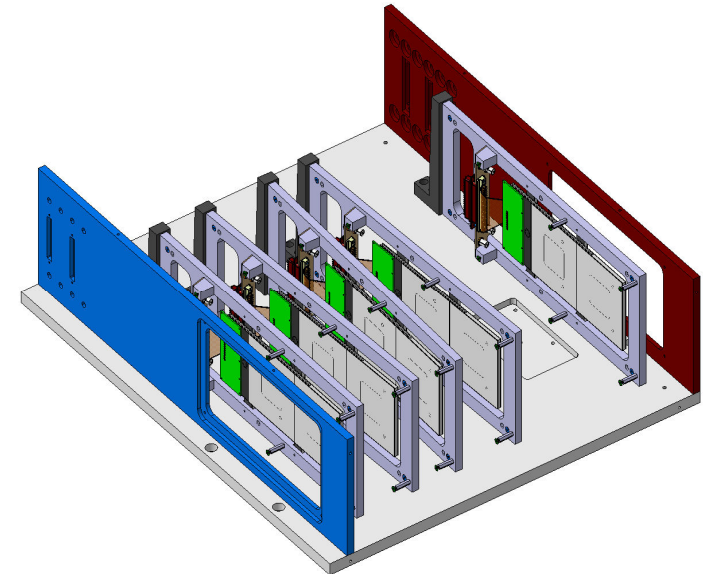
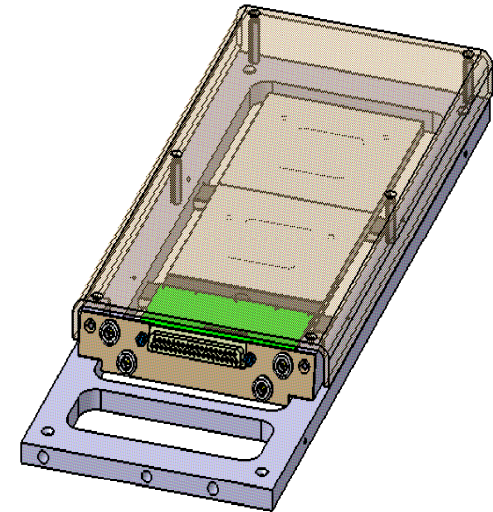
*All kinds of sensor types can be included in this structure*

*Special case are the alignment friendly modules*

*(laser IR integrated in the system)*

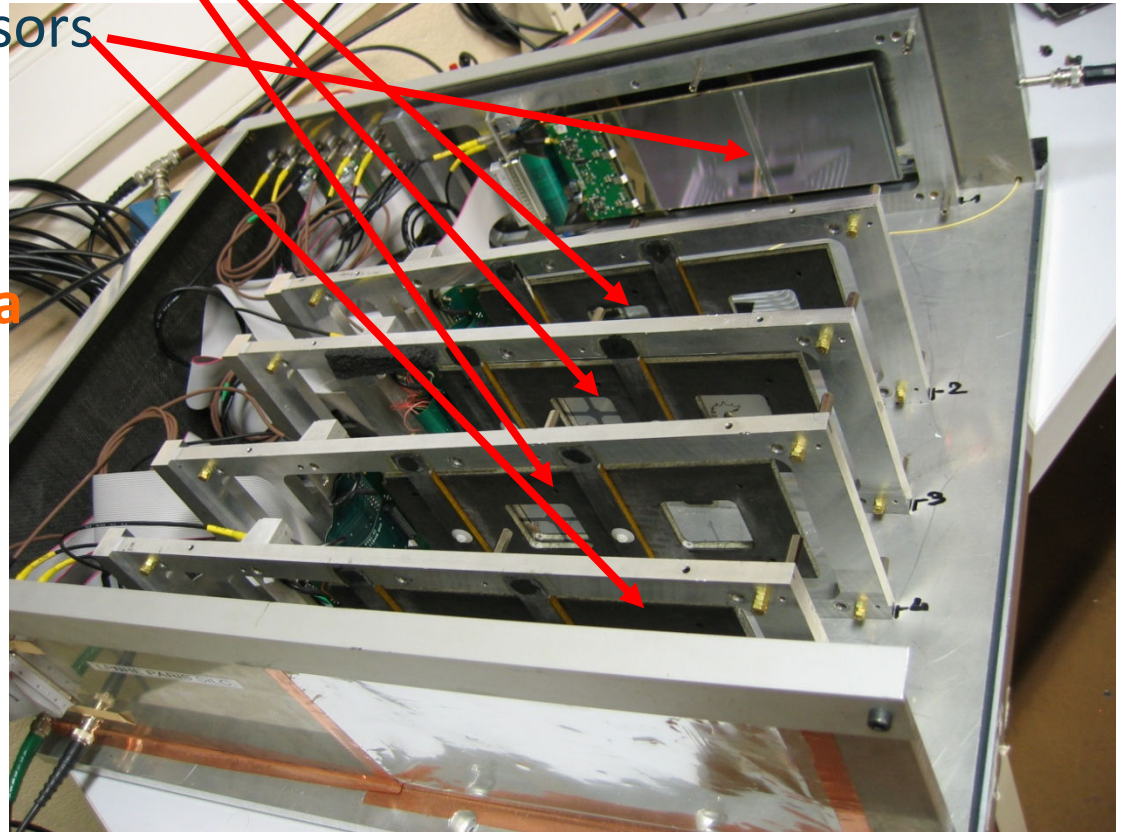
*Tests with radioactive source is integrated as well*

*Easy to manipulate -> robust support structure*



# Inside the Faraday cage

- 3 modules with friendly aligned HPK sensors
- Surrounded with 2 non AL treated HPK sensors
- Electronics from VA1<sup>®</sup>
  - 512 ch per sensor,
  - 25.4 mm active area



# *The 3D Table for test beam at CERN*



# ALIGNMENT



# INFRASTRUCTURE





## ■ Goal:

- Include a laser-based alignment on SiTRA tracking infrastructure.

## ■ Baseline:

- CMS-like HPK large area sensors with back-side Al removed. No further optical optimization.

## ■ Beyond the baseline (R&D on sensors):

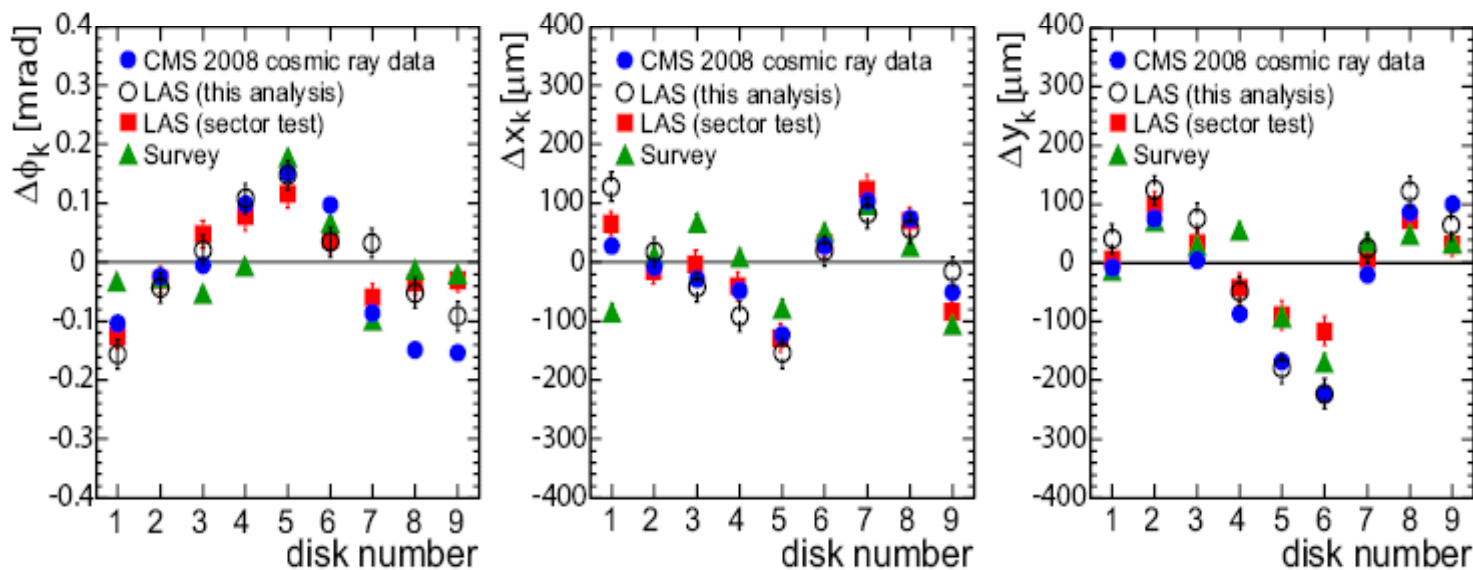
- Minimal modification of standard u-strip sensor to boost NIR light transmittance.

Optimization of sensors not included from beginning of sensor design:

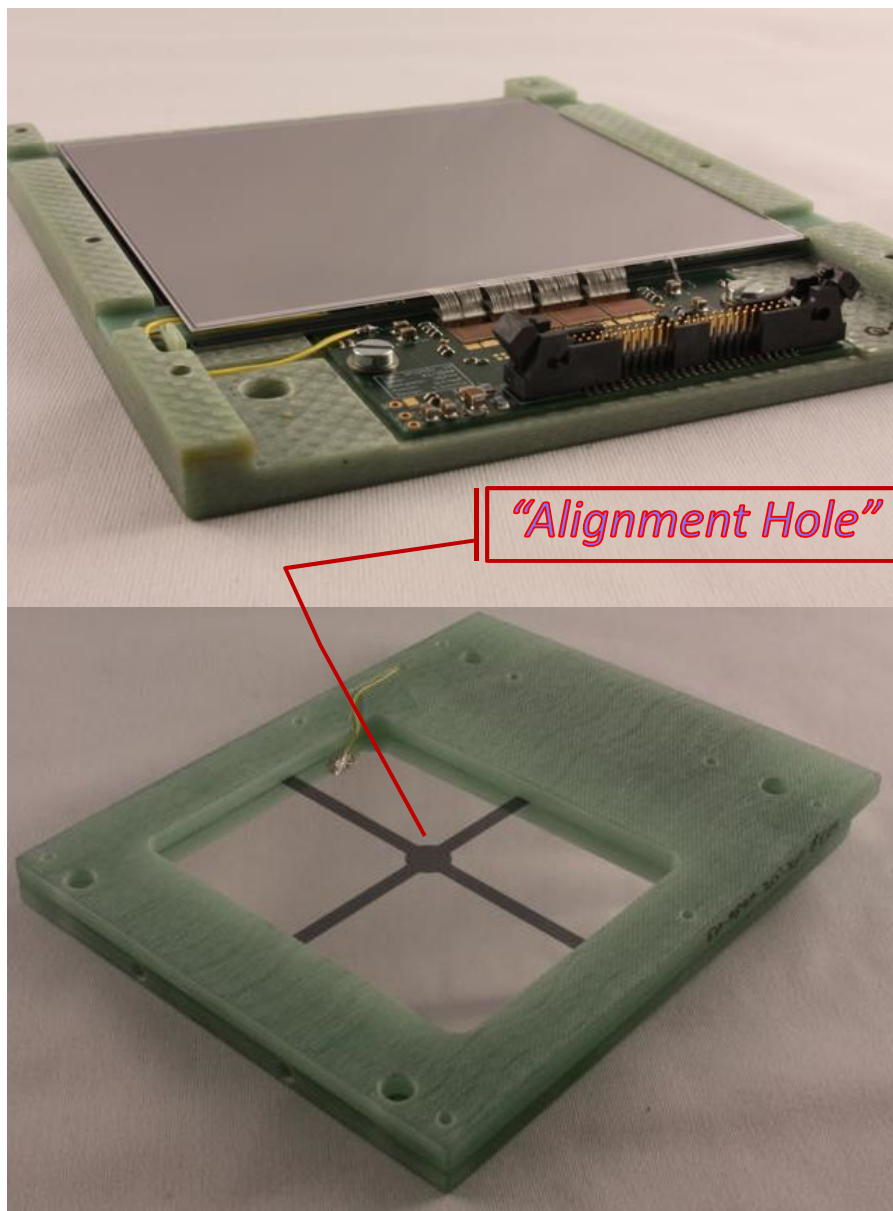
lower transmittance  $\sim < 20\%$

Some sensors need to be operated in saturation

Track-based and laser-based consistent at few tens of microns

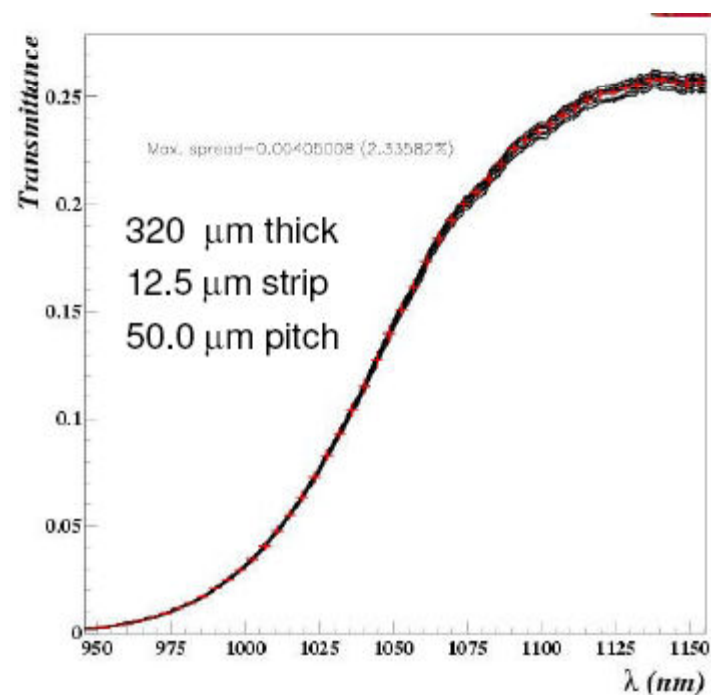


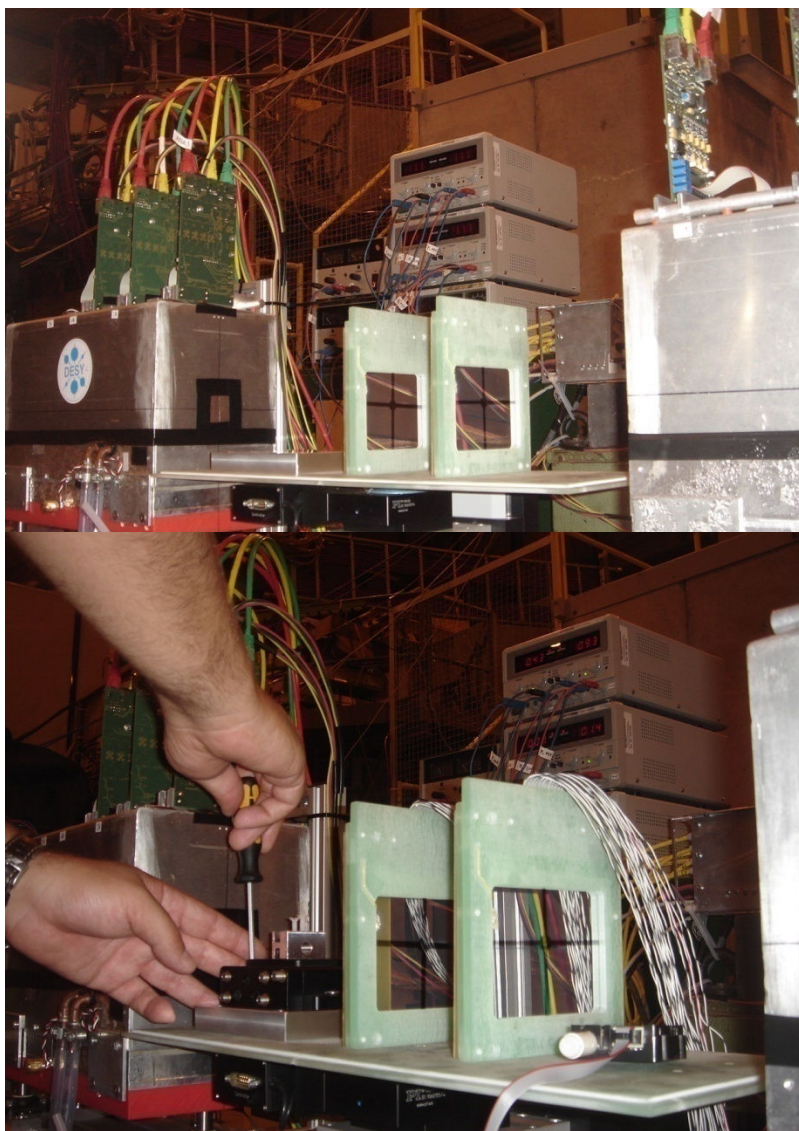
*(CMS first paper at JINST !!)*



Two single –sensor modules  
R/O with APV25 Chips  
(512ch )

NIR Transmittance ~ 15-20%





## AIM:

**Assessment of SNR for backside removed metallization.**

**Comparison between track-based and laser alignment.**

## Testbeam at CERNs SPS

(19. to 26. August 2009)

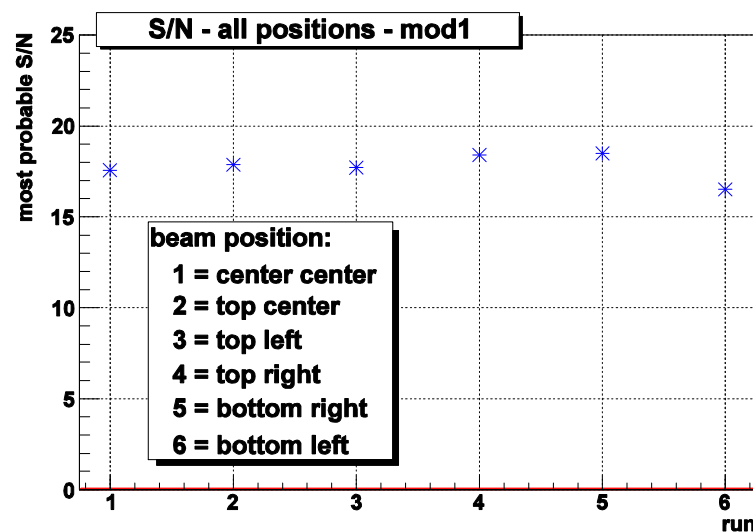
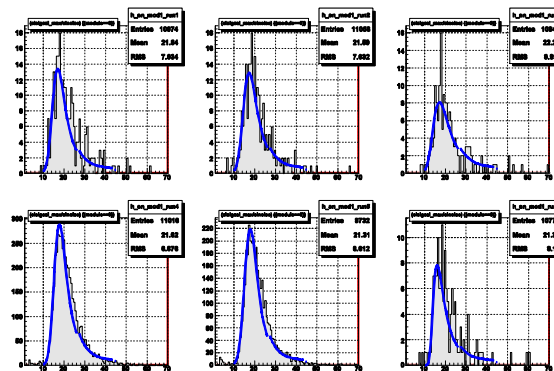
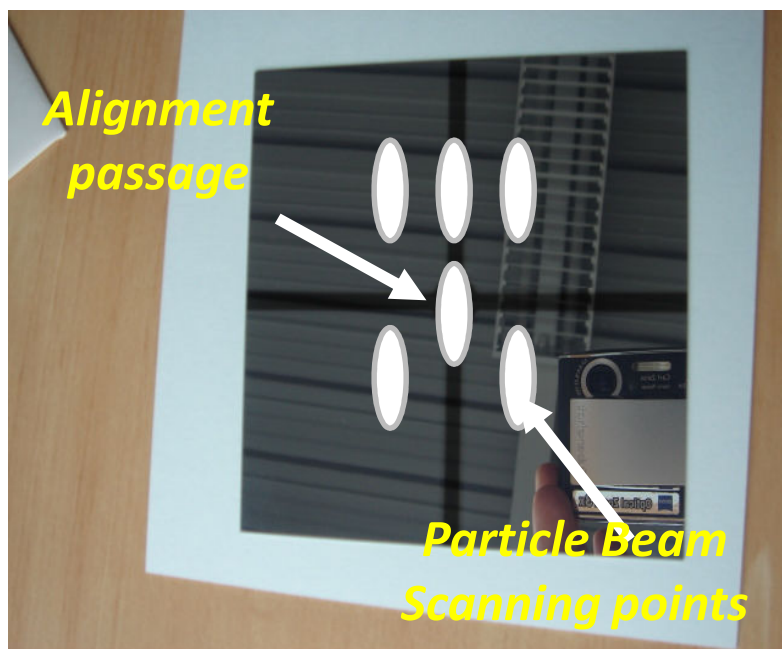
- CERN SPS North Area: H6B
- We used the *EUDET* Beam Telescope to get triggers and tracks

## Results

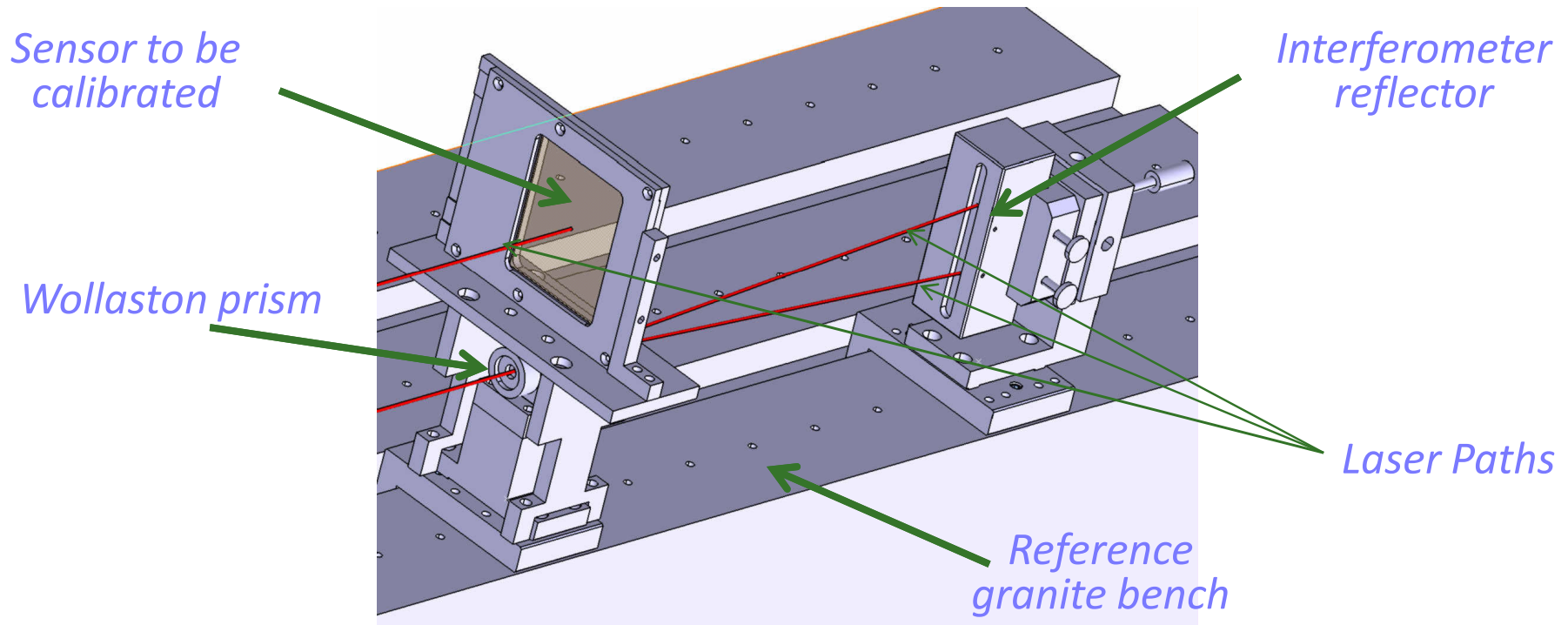
- About beam 100Kevents + laser 100Kevents.
- Analysis still in progress



- SNR sensor scanning comparing Back side with Al vs. n Back side with Al metallization



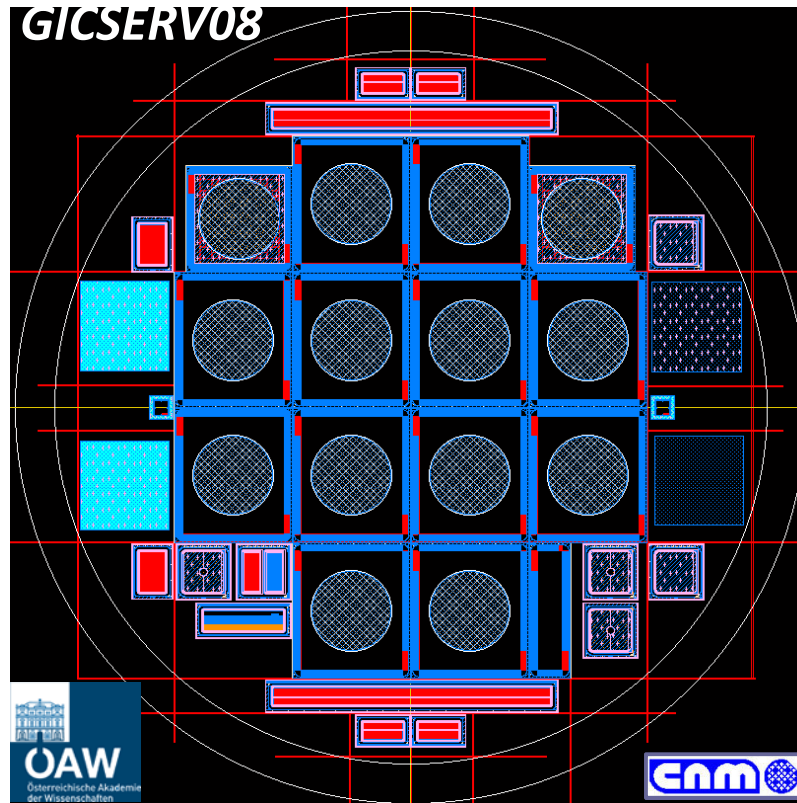
- Direct comparison with interferometric measurement (accuracy better than 1  $\mu\text{m}$ ).



- Straightness measurement configuration all parts available currently being mounted

- Prototypes built by CNM-Barcelona (Spain)

- Aims:
  - Test %T vs multigeometry
  - Use optical test structures (continuous layers) to extract refraction index and control deposition
  - Test of electrical test structures



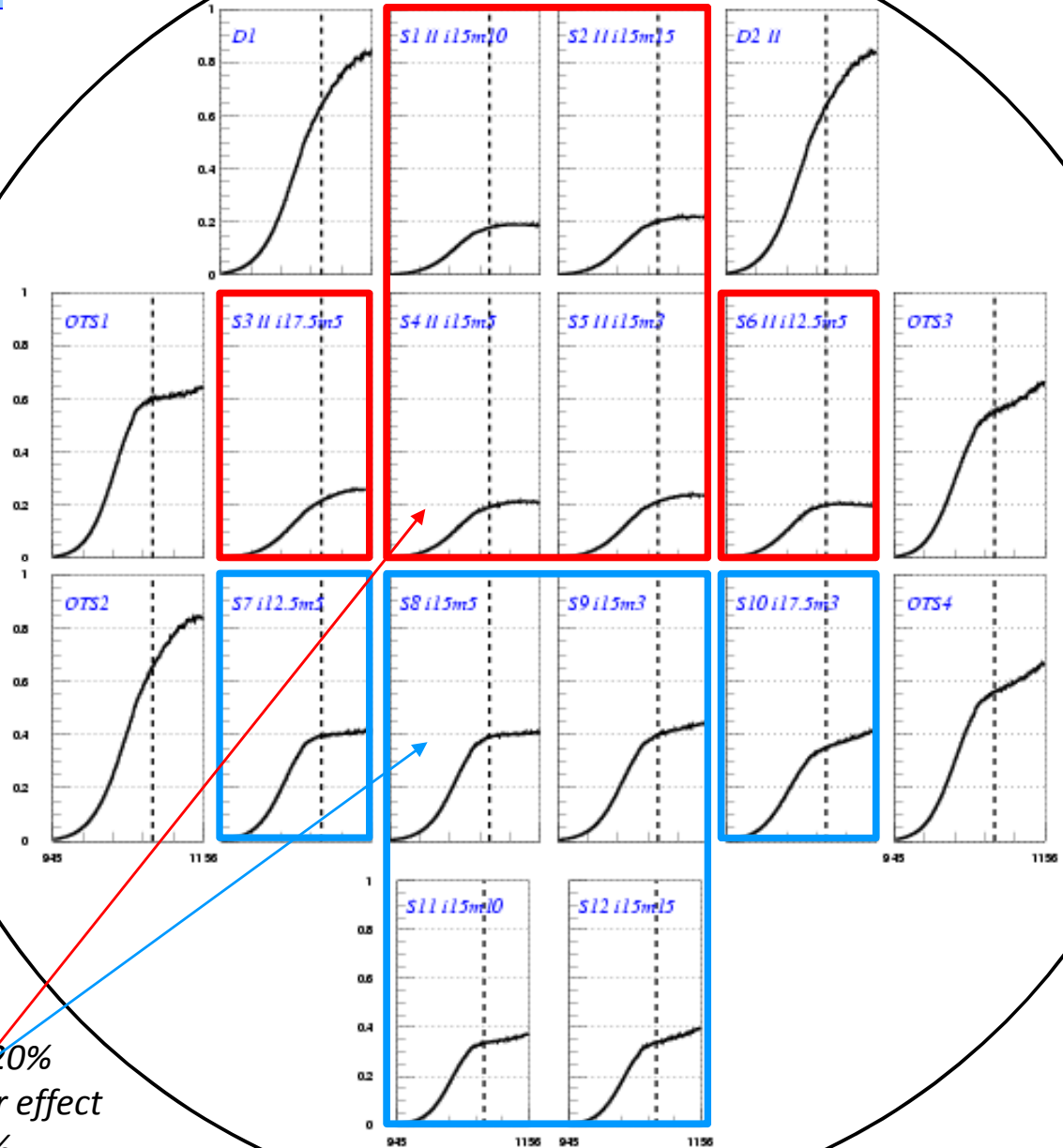
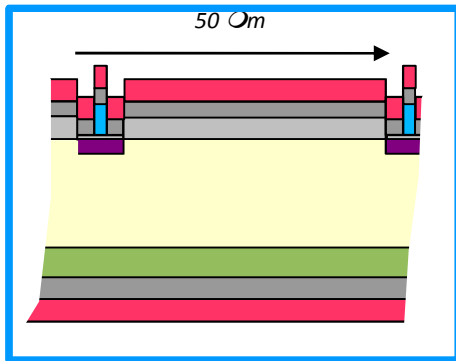
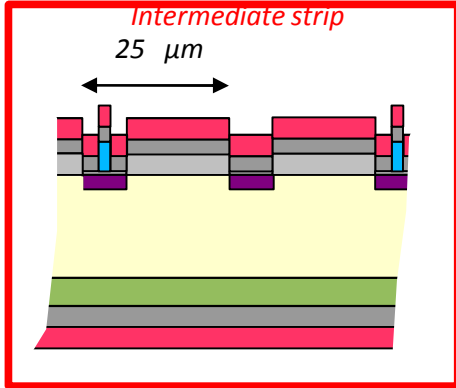
- 5+1 wafers
- 12 ustrip detectors per wafer (6 with intermediate strips, without metal contacts)
- 50  $\mu\text{m}$  RO pitch (25  $\mu\text{m}$  interm. strip)
- 256 RO strips
- 1.5 cm length varying strip width (3, 5, 10, 15  $\mu\text{m}$ )

- Mask designed by **D. Bassignana** (CNM)
- Electronic test structures designed by **M. Dragicevic** (Vienna) including:
  - CAP TS AC, CAP TS DC, CMS Diode, MOS, GCD, Sheet
- Optical test structures available (Si, Si+p<sup>+</sup>, SiO<sub>2</sub>, SiO<sub>2</sub>+passivation)

# Wafer 1:: %T



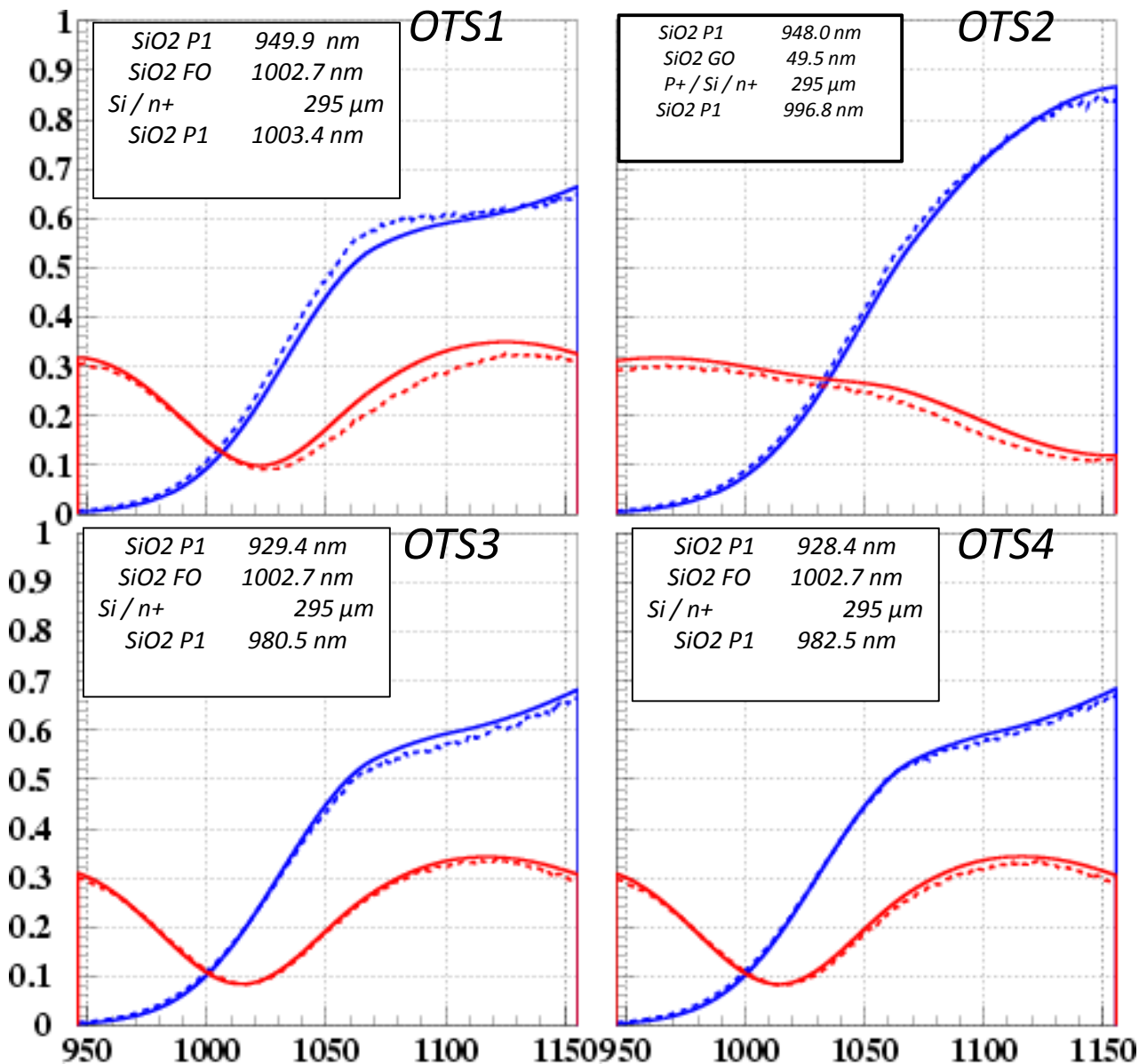
**measured**



- $T \sim 70-80\%$  test structures
- No intermediate implant  $\Delta T = +20\%$
- Metal width [3-5] μm: second order effect
  - Metal width >10 μm:  $\Delta T \leq -5\%$

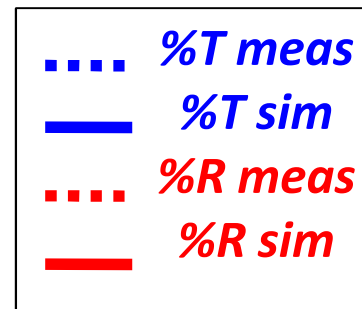


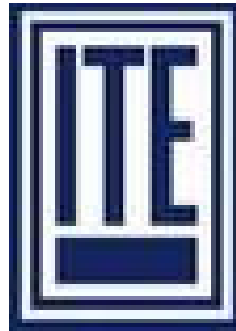
# Alignment - Measurement vs. Simulation



Optical Test structures simulated (no fit involved)

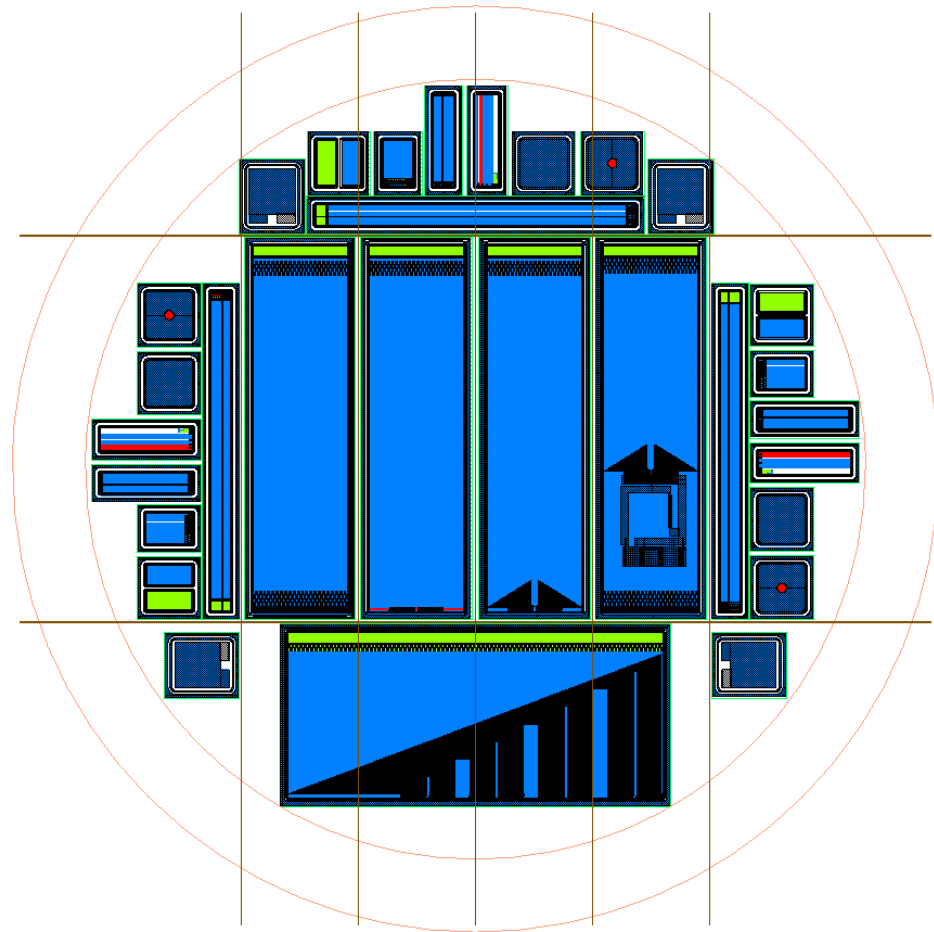
1<sup>st</sup> result:  
Transmittance of Si can be increased by ~30% with just 2 layers of 1  $\mu$ m SiO2

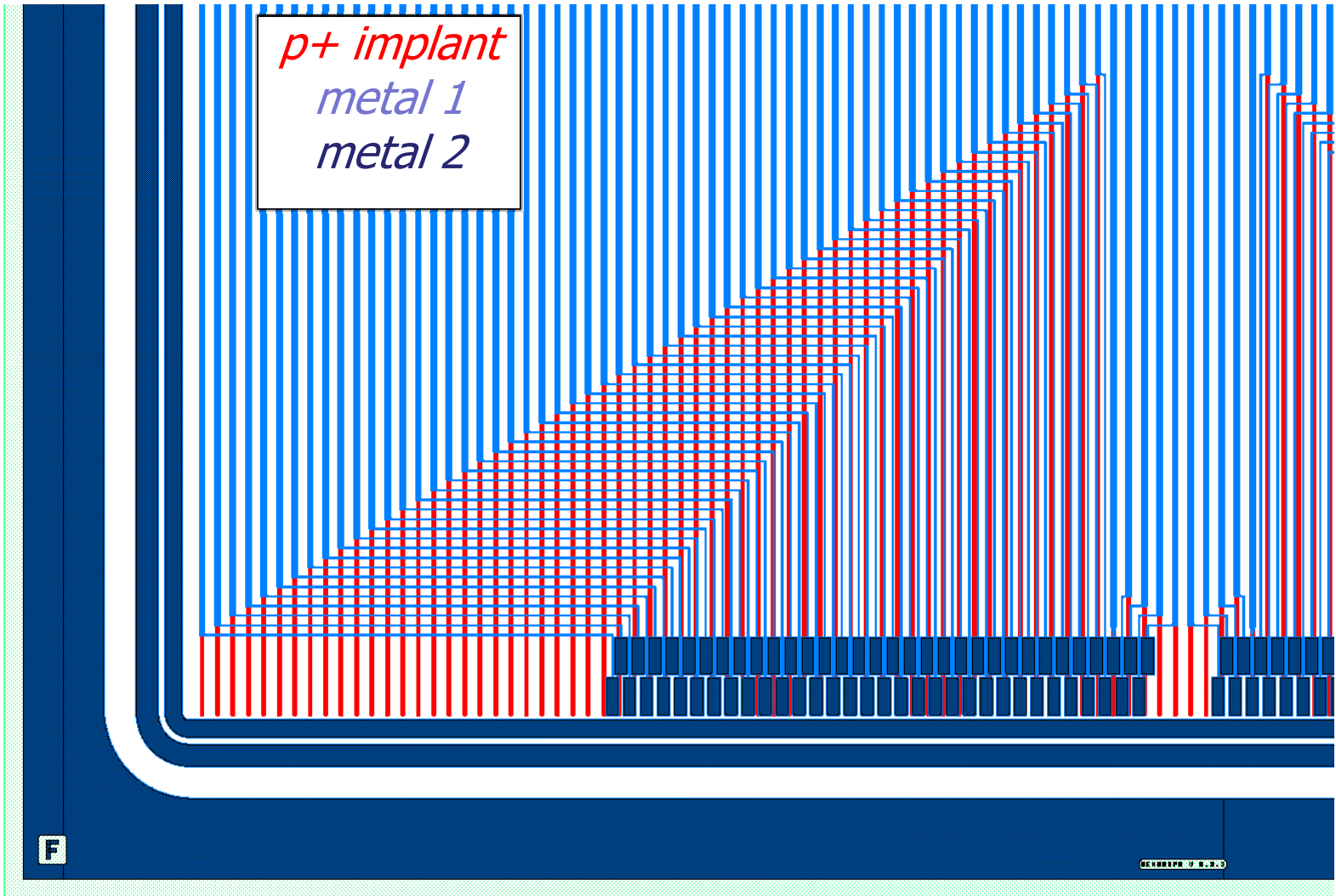


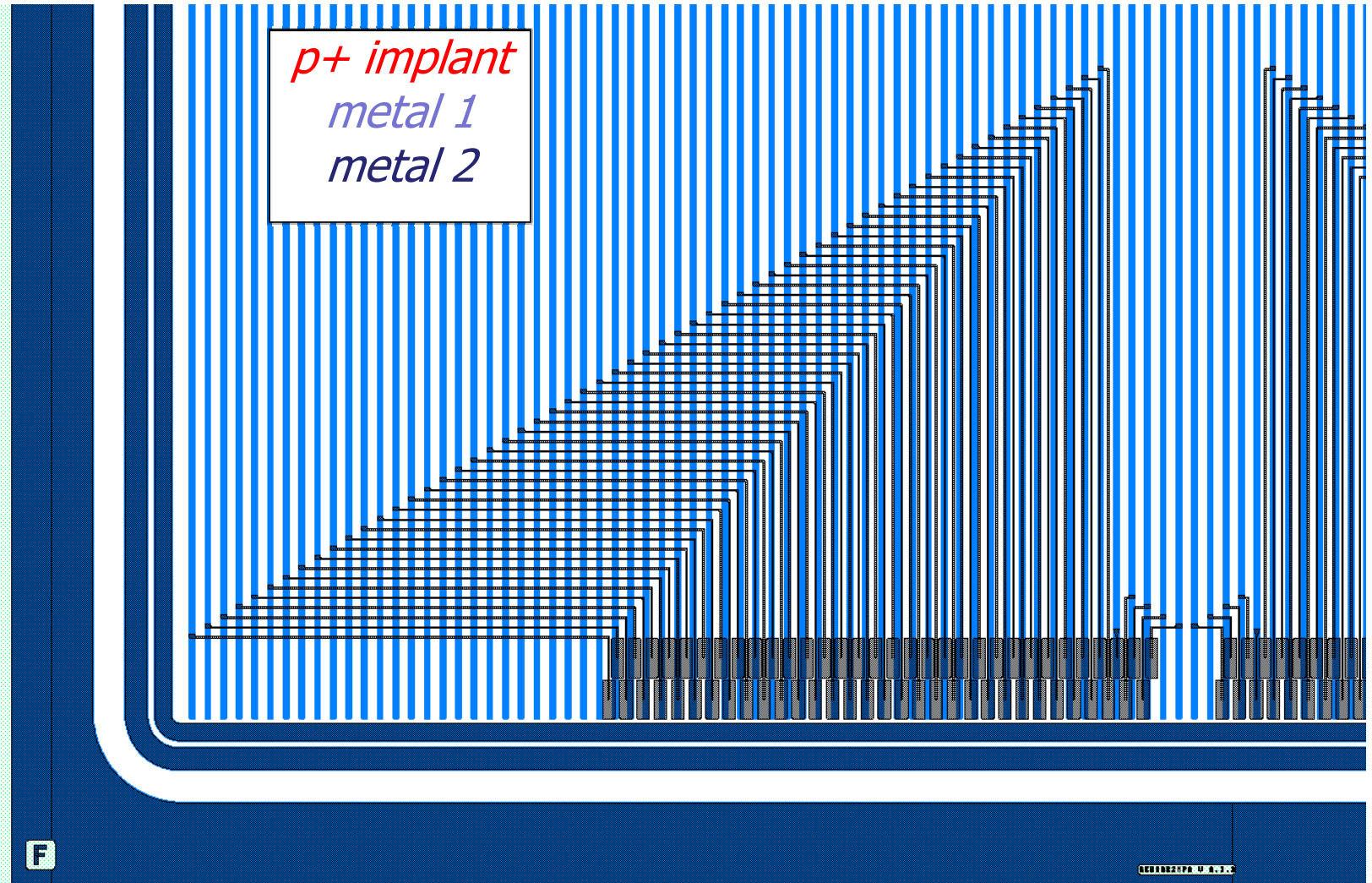


# INFRASTRUCTURE

- 3 full halfmoons with improved teststructures
  - same design as for HPK thin sensor order
- Additional teststructure (4 x TS\_DM)
  - large double metal capacitor
  - oxide thickness between metals
- 5 AC coupled sensors, 80  $\mu\text{m}$  pitch, different integrated PAs:
  - 4 x 128 strips
  - 1 x 512 strips
- Naming scheme for sensors:
  - Run Name: ITE09
  - Wafer Number: W\_
  - Structure Name: STD, PAD,...

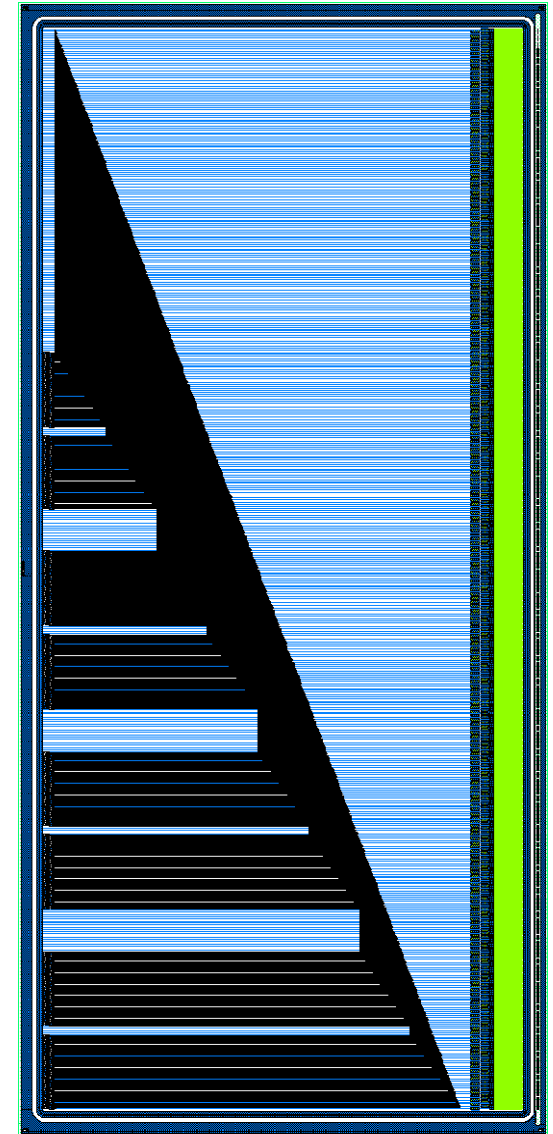




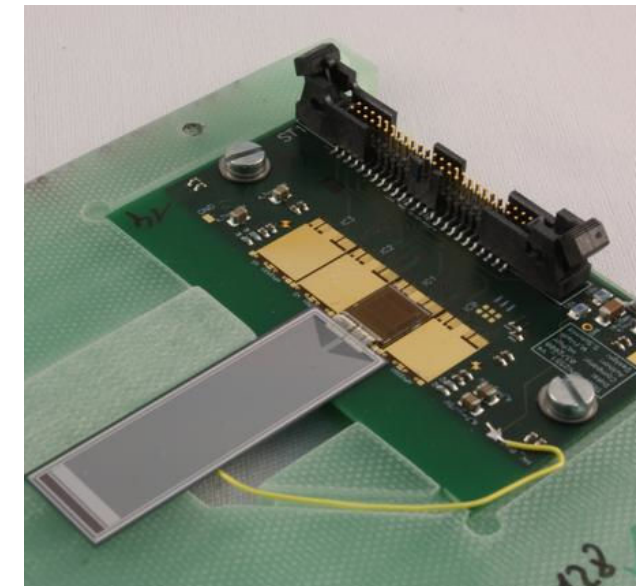


Same Strip Geometry as other Sensors but

- 512 short Strips
- Long routing lines to test influence on SNR and Crosstalk
- Routing is for a custom 4 x APV Hybrid
- Hybrid fits APVDAQ readout system



- ITE Warsaw Sensor:
  - 3 x 512
  - 2 x STD
  - 2 x PAS
  - 2 x PAD
- 2 x Alignment Modules
- 2 x Pt Module
- 2 x SiLC halfmoon for stereo measurements
- Stack of last years multigeometry sensors for calibration



## Testbeam at CERNs SPS

*(19. to 26. August 2009)*

*CERN SPS North Area: H6B*

*Low intensity 120 GeV with*

<i>Pi+</i>	<i>55.67 %</i>
<i>p</i>	<i>38.95 %</i>
<i>K+</i>	<i>5.38 %</i>

*We used the EUDET Beam Telescope to get triggers and tracks*

*Readout chain from HEPHY's Electronic 2 Group*

*Slow control/monitoring: HV, T, RH, Cooling*

*Full remote control*

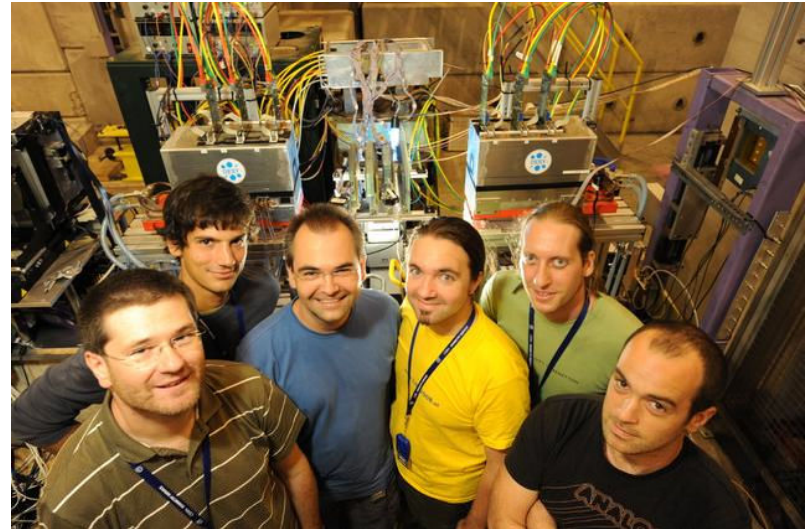
## Results

*3.2 Million events*

*1 TB of data*

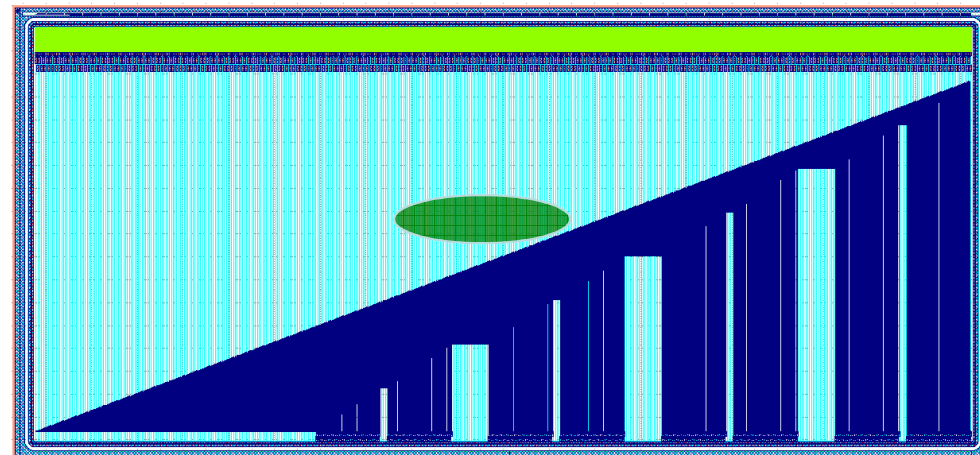
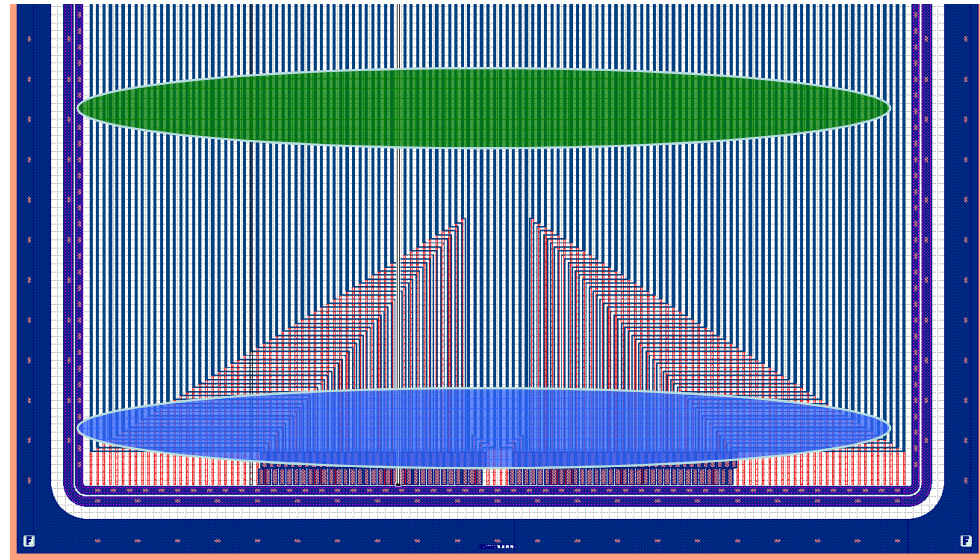
*Full Logbook at*

*<http://elog.hephy.at/testbeam-SPS09/>*





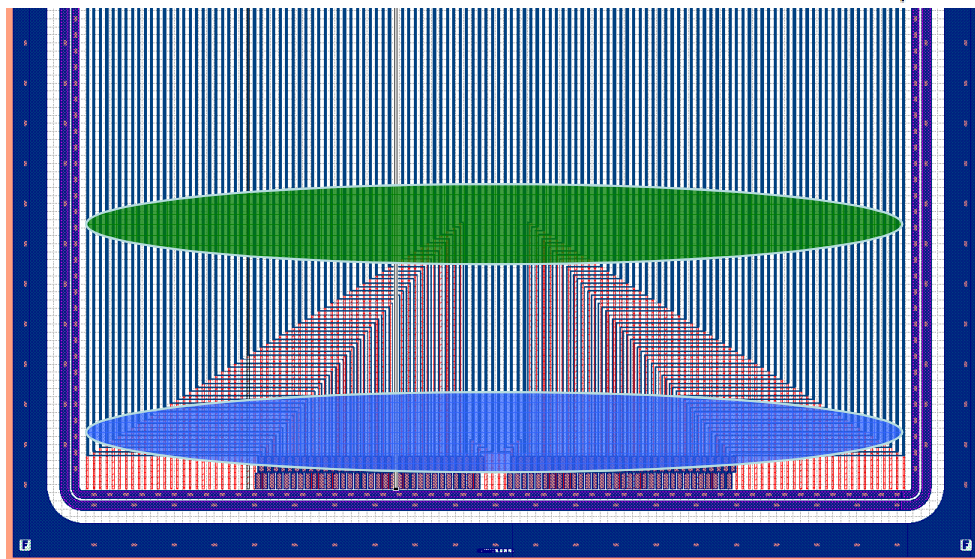
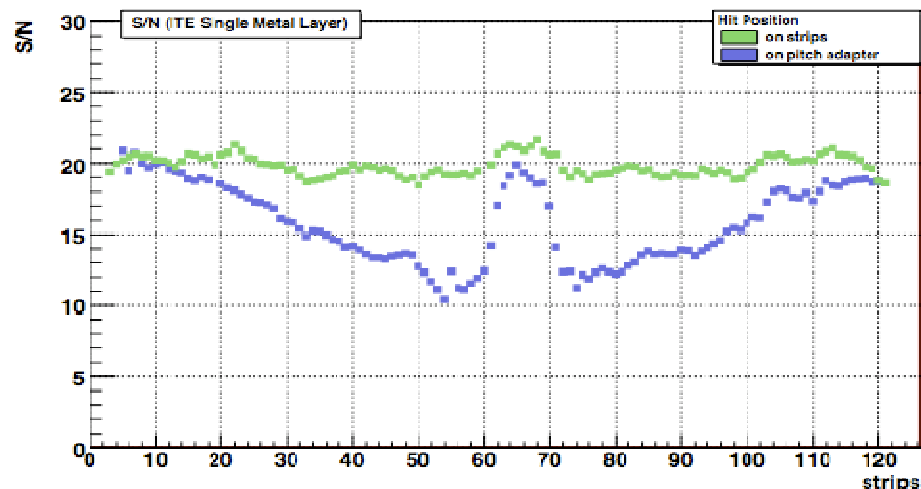
- ITE Sensors with integrated PAs
  - Beam inside PA area
  - Beam on strip area
  - Z - information from rotated SiLC sensor
  
- ITE Sensor with 512 Strips
  - Beam in center
  - Exact locations to be determined

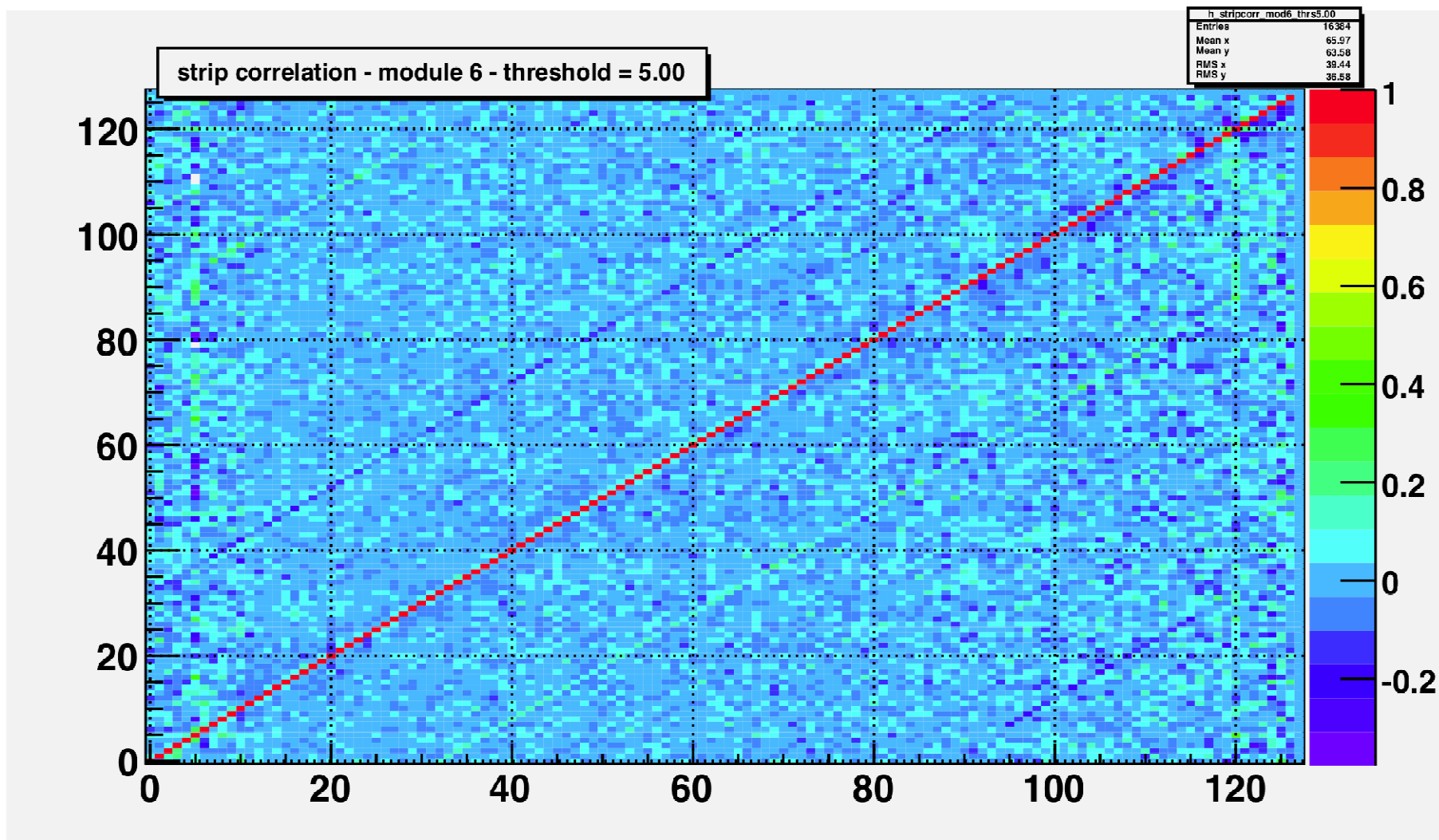


*Data is taken from two runs  
Height information from  
additional sensor rotated by  
90°*

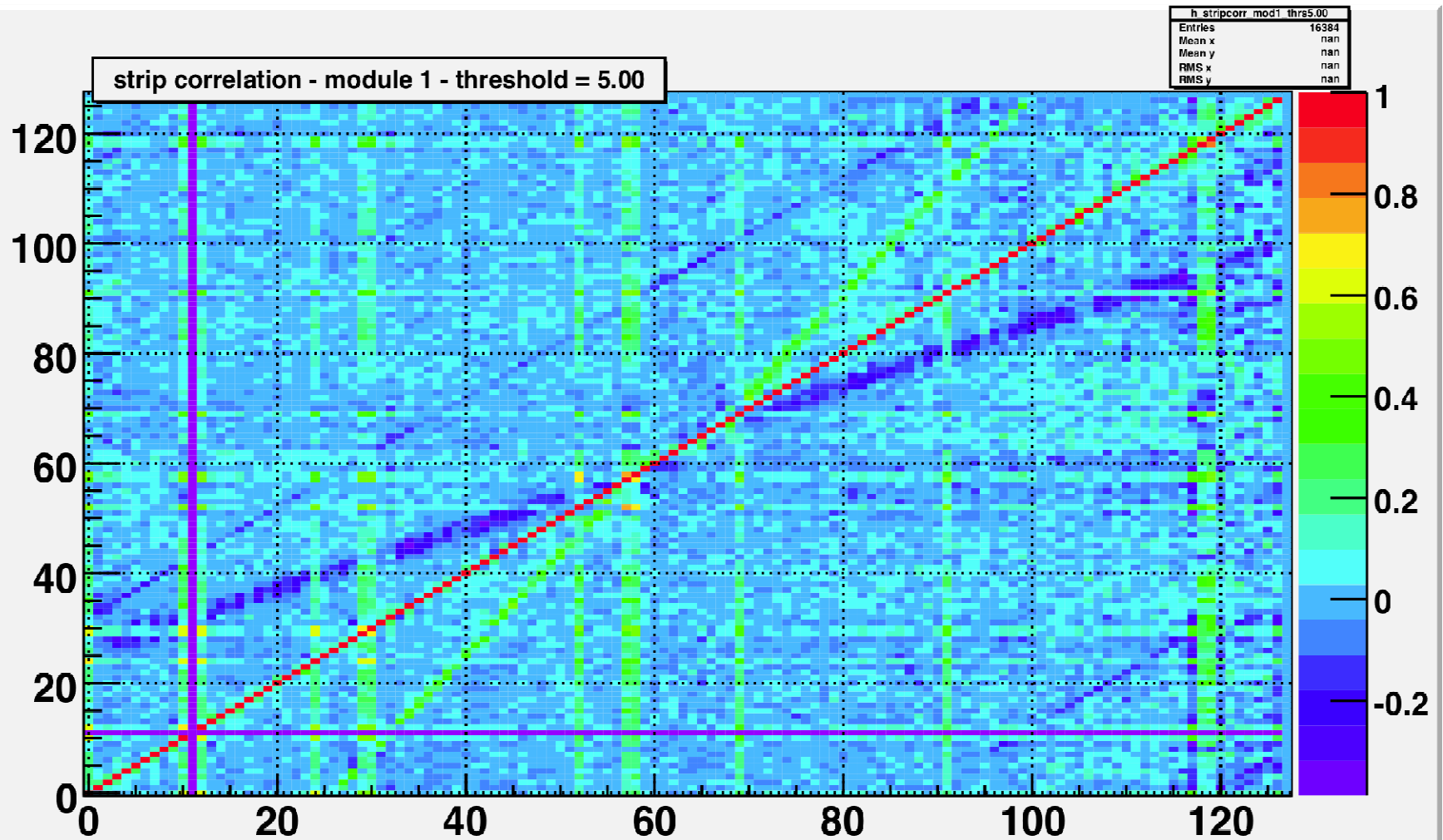
*Each hit position represents  
SNR of a cluster with hit  
location estimated at the  
respective strip*

*Closer look on signals and  
noise separately necessary  
to disentangle effects*





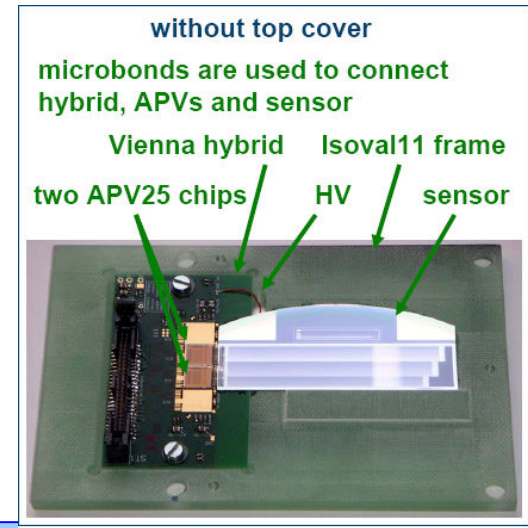
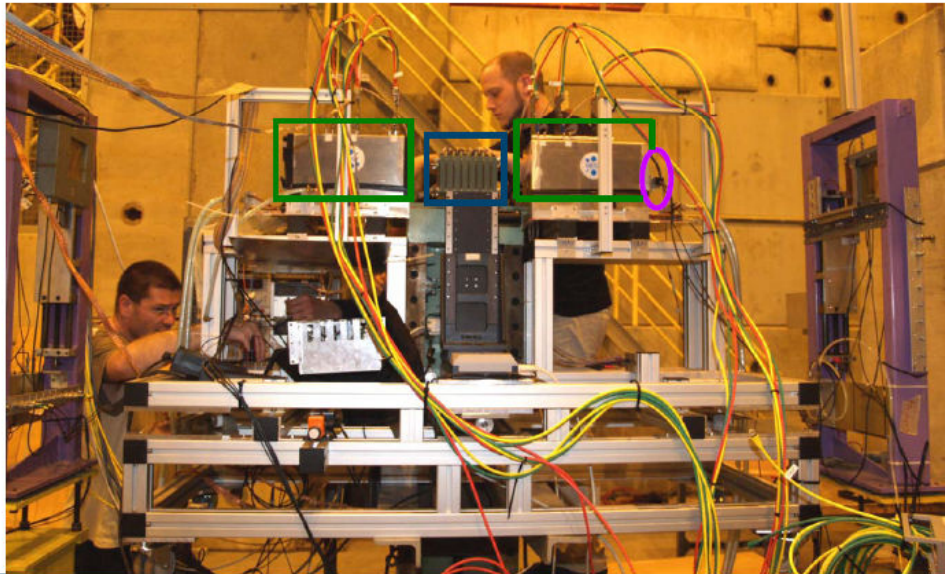
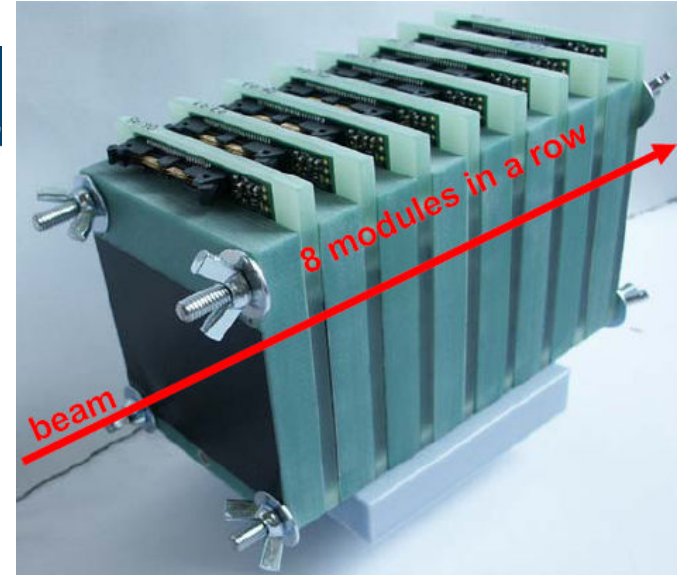
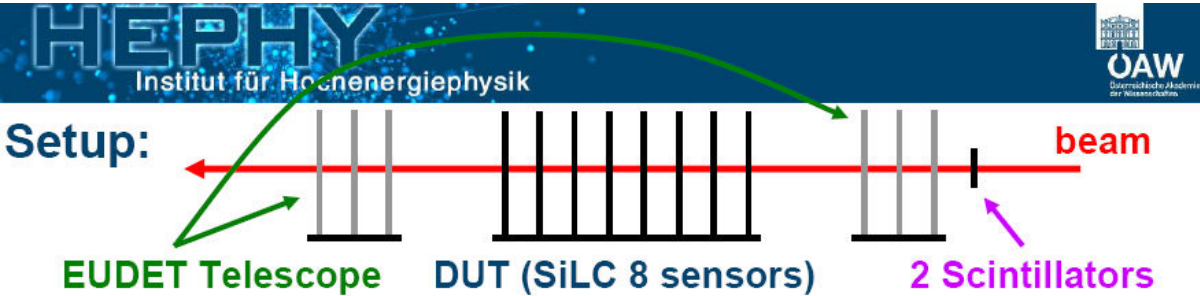
# Pitch Adapter Single Metal



# TRANSNATIONAL ACCESS

- 1 - Tests of the current alignment system with with the IR laser (Santander laser test bench) and at SPS test beam still in 2009, conducted by the ***Torino team***
- 2- Tests of new sensor technologies conducted by ***HEPHY-Vienna***  
at CERN SPS (15-30 August 2009) (see Th.Bergauer's presentation) . Will be pursued next year.
- 3 - Combined tests with calorimetry: dual readout test beam at CERN (2010), conducted by italian teams (*Pisa*)
- 4- Tests of new sensor technologies: tests of news sensors including new pixel technologies from ***IRST, VTT*** (in preparation for 2010): modules will be made at LPNHE&CERN and will be included in the present standalone test infrastructure.

# HEPHY tests infrastructure studies:

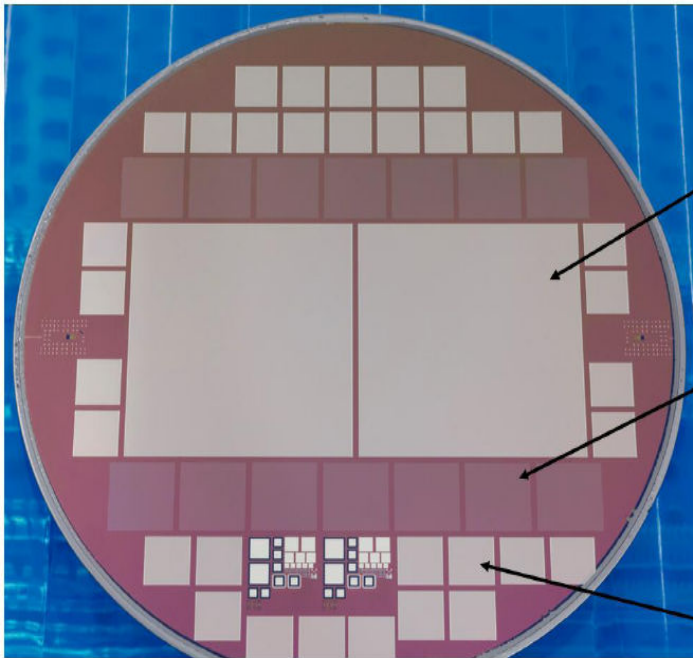


# Using standalone structure to test

VTT TECHNICAL RESEARCH CENTRE OF FINLAND



## EDGELESS DETECTORS on 6" (150 mm) WAFER



### Main edgeless strip detectors

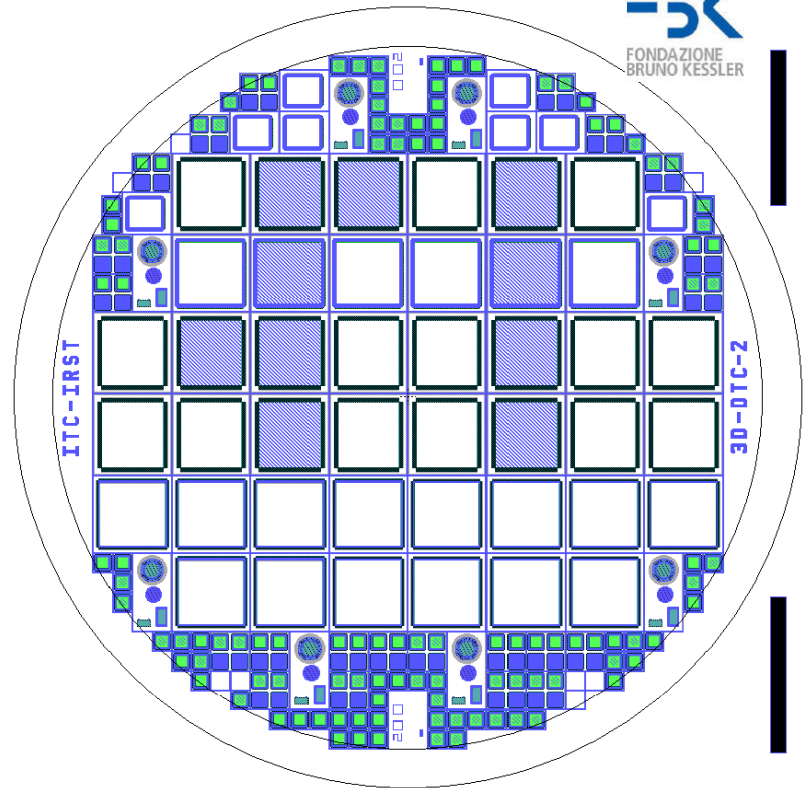
- $5 \times 5 \text{ cm}^2$
- DC & FOXFET

### Medipix 2 edgeless pixels

- $1,4 \times 1,4 \text{ cm}^2$
- 6 different designs

### Baby edgeless strip detectors

- $1 \times 1 \text{ cm}^2$
- DC, PT & FOXFET
- 24 different designs

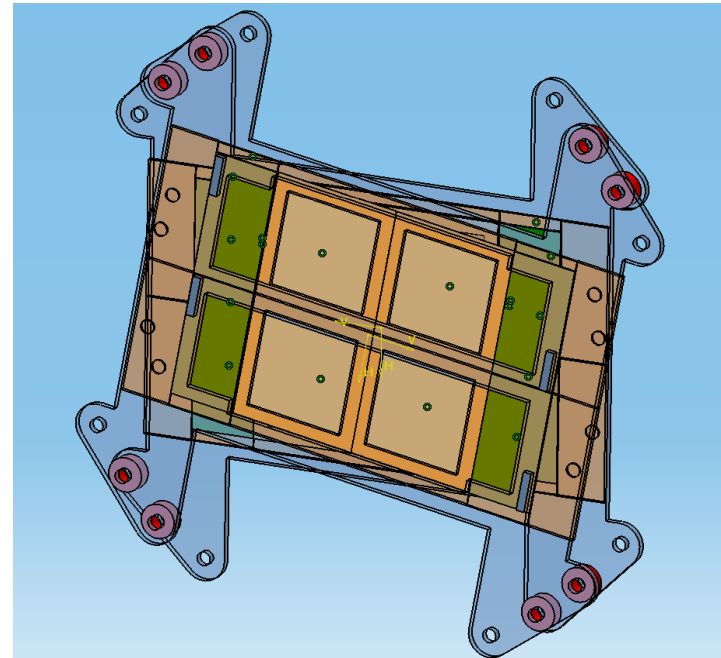
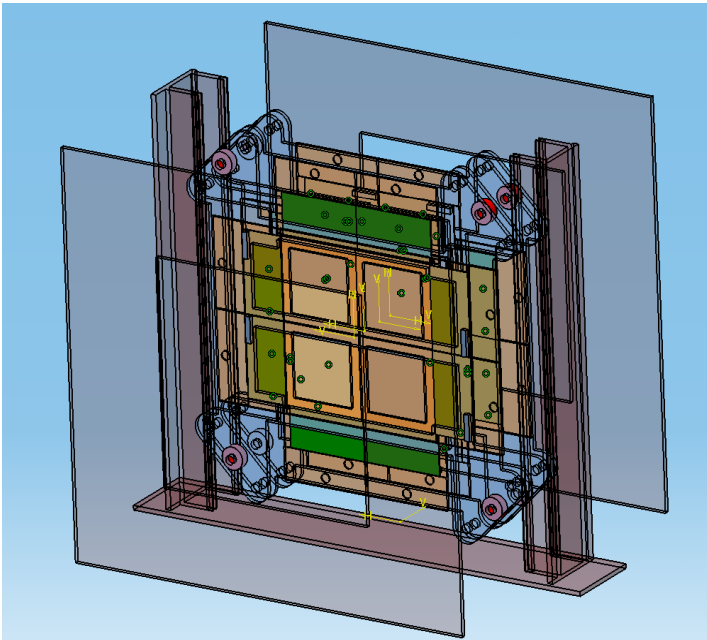


Modules are going to be designed at LPNHE to host various types of new sensor Strip prototypes: new edgeless strip sensors (left) with  $5 \times 5 \text{ cm}^2$  sensors; new short Strip sensors (right)  $1.5 \times 1.5 \text{ cm}^2$ , in 3D technology and planar edgeless strip sensors  $2.5 \times 5 \text{ cm}^2$  prototypes



# Construction of new larger modules for

*Under preparation for next year first for CALICE (can be adapted to other calorimetry tests)  
Surface to be covered: 18x18cm<sup>2</sup> in 2010 tests=> first 2 false double sided modules are built*



*Design allows to study various coupling angles between the single sided modules  
(XUV or small angle tilted modules for false double sided case)*

- SiTRA activities include: construction of prototypes, design of new FE electronics (based on ref. Chips and new chips), development of the associated DAQ (hardware & software), cooling-Faraday cage and 3D Table, plus a full alignment system based on IR laser system.
- Transnational based applications of these various infrastructures are occurring in 2009 (2) and at least 2 other before the completion of the programme in 2010.

# THANK YOU!



4th EUDET Annual Meeting, U. Geneve, 20th  
October '09, I. Vila