CALICE SiW Ecal

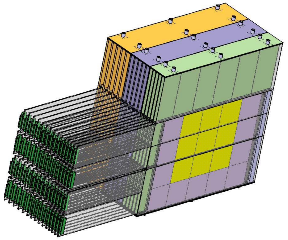
- Results and Plans -

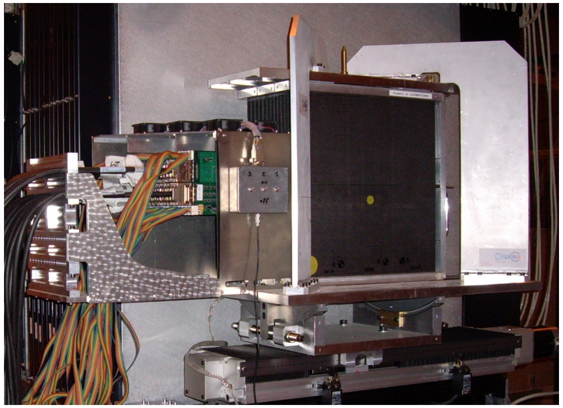
Roman Pöschl
LAL Orsay

EUDET Annual Meeting Geneva/Switzerland and CERN
October 2009

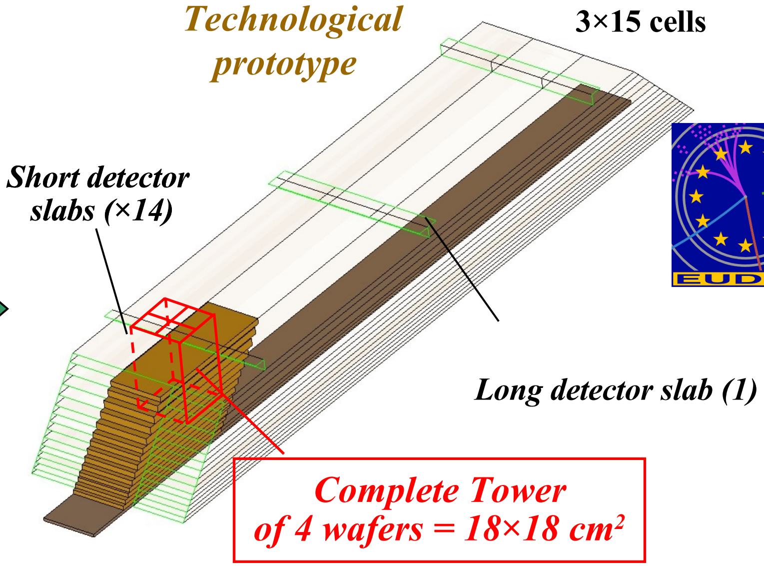
EUDET Prototype

- Logical continuation to the physical prototype study which validated the main concepts : alveolar structure , slabs, gluing of wafers, integration
- Techno. Proto : study and validation of most of technological solutions wich could be used for the final detector (moulding process, cooling system, wide size structures,…)
- Taking into account industrialization aspect of process
- First cost estimation of one module





- **3 structures : 24 X_0 (10×1,4mm + 10×2,8mm + 10×4,2mm)**
- **sizes : 380×380×200 mm3**
- **Thickness of slabs : 8.3 mm (W=1,4mm)**
- **VFE outside detector**
- **Number of channels : 9720 (10×10 mm²)**
- **Weight : ~ 200 Kg**



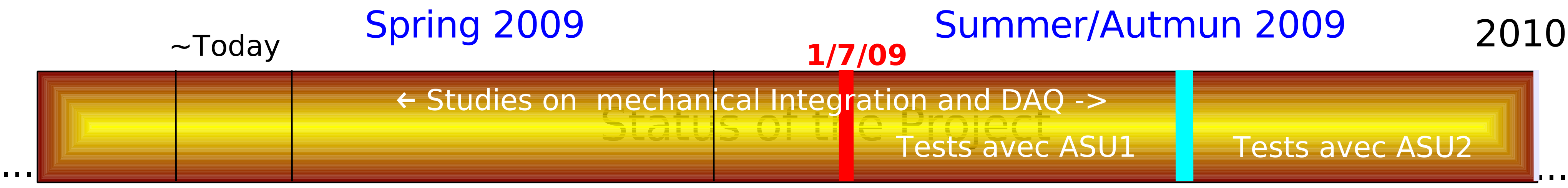
- **1 structure : ~ 23 X_0 (20×2,1mm + 9×4,2mm)**
- **sizes : 1560×545×186 mm3**
- **Thickness of slabs : 6 mm (W=2,1mm)**
- **VFE inside detector**
- **Number of channels : 45360 (5×5 mm²)**
- **Weight : ~ 700 Kg**

The groups working on the EUDET Electromagnetic Calorimeter

MANCHESTER 1824 LLR LAL Omega LPSC Grenoble UNIVERSITY OF CAMBRIDGE Royal Holloway University of London UCL FZÚ

- What we call “EUDET Module” is in fact the <u>next SiW Ecal CALICE Prototype</u>
- Financial support by EU

Time Scale of Project

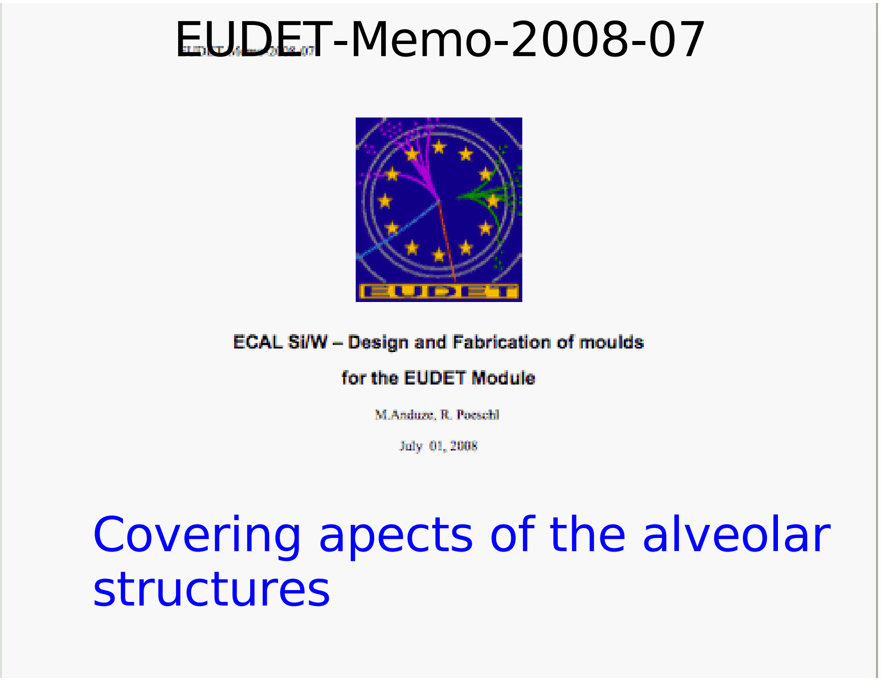


Assembly and studies with Demonstrateur

'ASU 1': SPIROC2 with FEV7_CIP

EUDET: Deadline, Alveolar Structures and ASU 1

ASU2: SPIROC2 with FEV7_COP



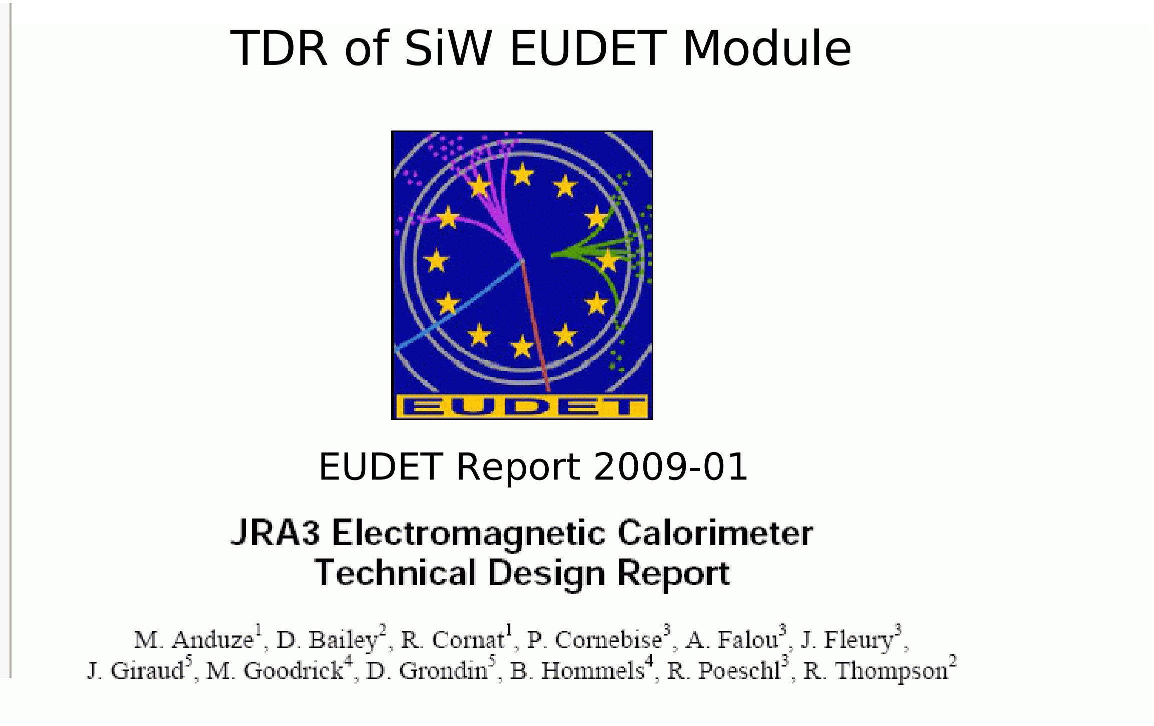
EUDET-Memo-2008-07

ECAL Si/W – Design and Fabrication of moulds
for the EUDET Module

M.Anduze, R. Poeschl

July 01, 2008

Covering apects of the alveolar structures



TDR of SiW EUDET Module

EUDET Report 2009-01

JRA3 Electromagnetic Calorimeter
Technical Design Report

M. Anduze[1], D. Bailey[2], R. Cornat[1], P. Cornebise[3], A. Falou[3], J. Fleury[3], J. Giraud[5], M. Goodrick[4], D. Grondin[5], B. Hommels[4], R. Poeschl[3], R. Thompson[2]

Detailed Technical Design of EUDET Module

Parties Involved

6 Laboratories are sharing out tasks in according to preferences and localization:

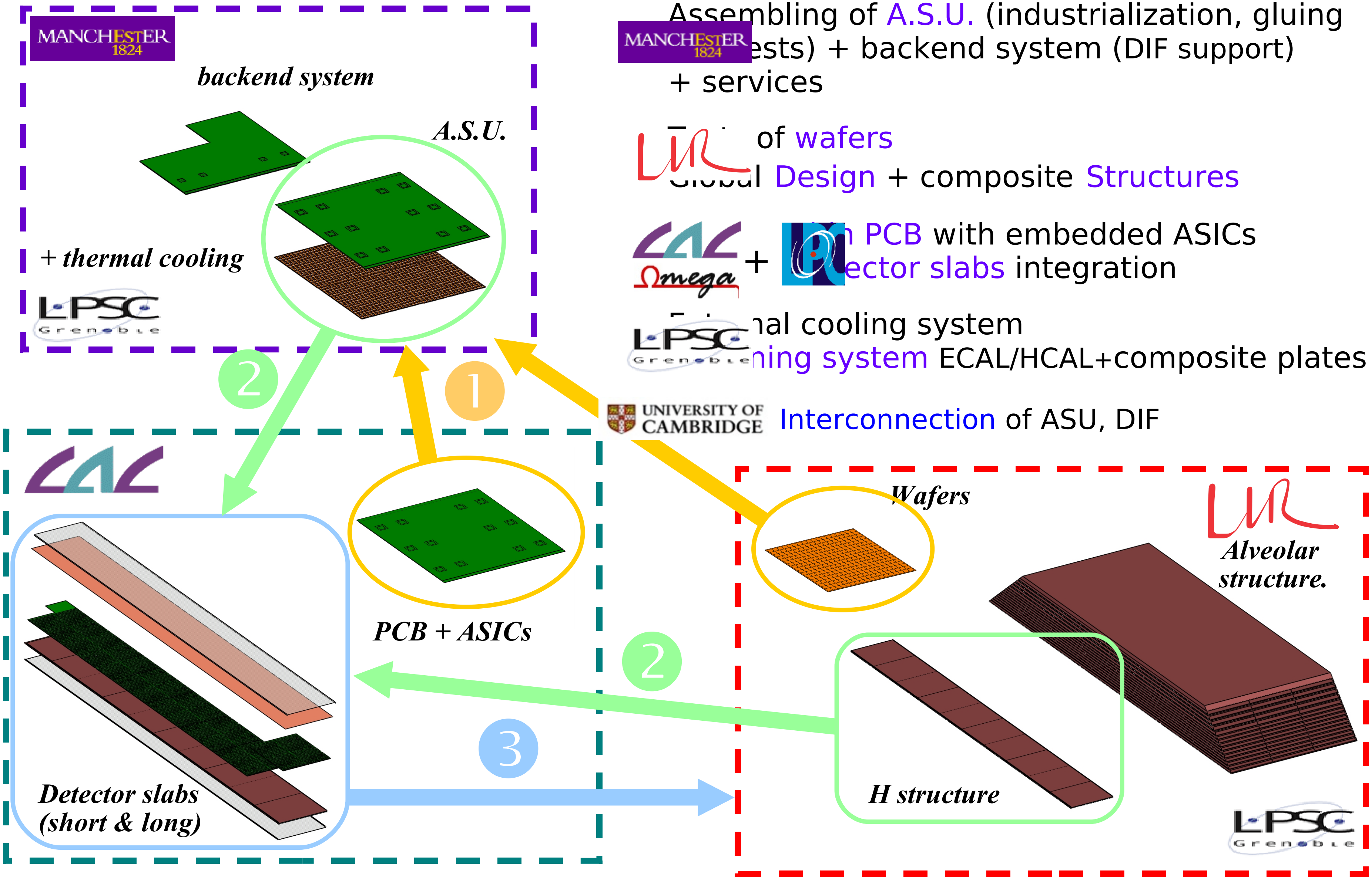
MANCHESTER 1824 Assembling of A.S.U. (industrialization, gluing ests) + backend system (DIF support) + services

of wafers
Global Design + composite Structures

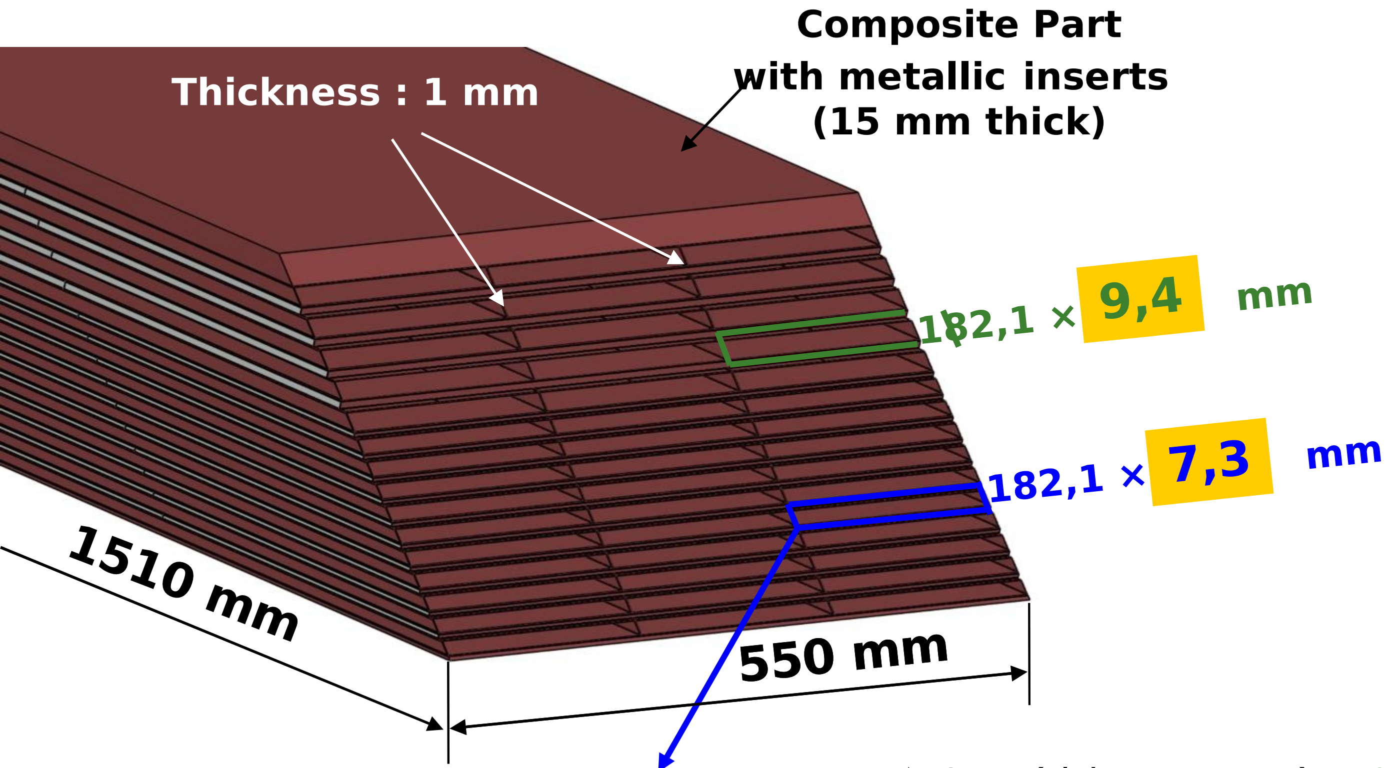
+ n PCB with embedded ASICs
ector slabs integration

nal cooling system
ning system ECAL/HCAL+composite plates

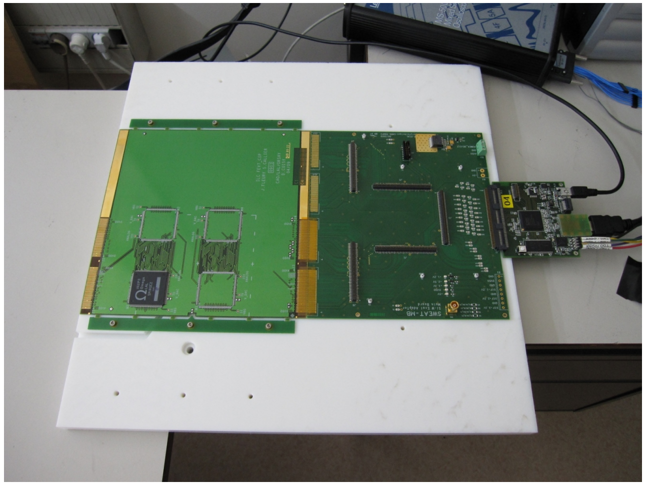
UNIVERSITY OF CAMBRIDGE Interconnection of ASU, DIF

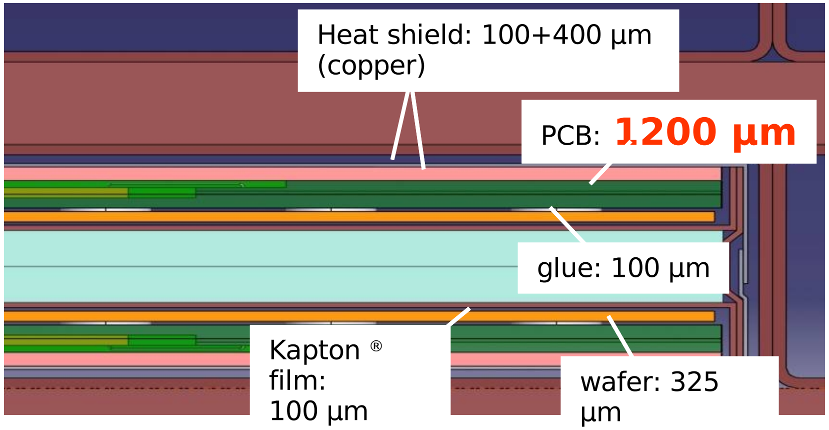


Module EUDET – Current Design (final – developped 2008)



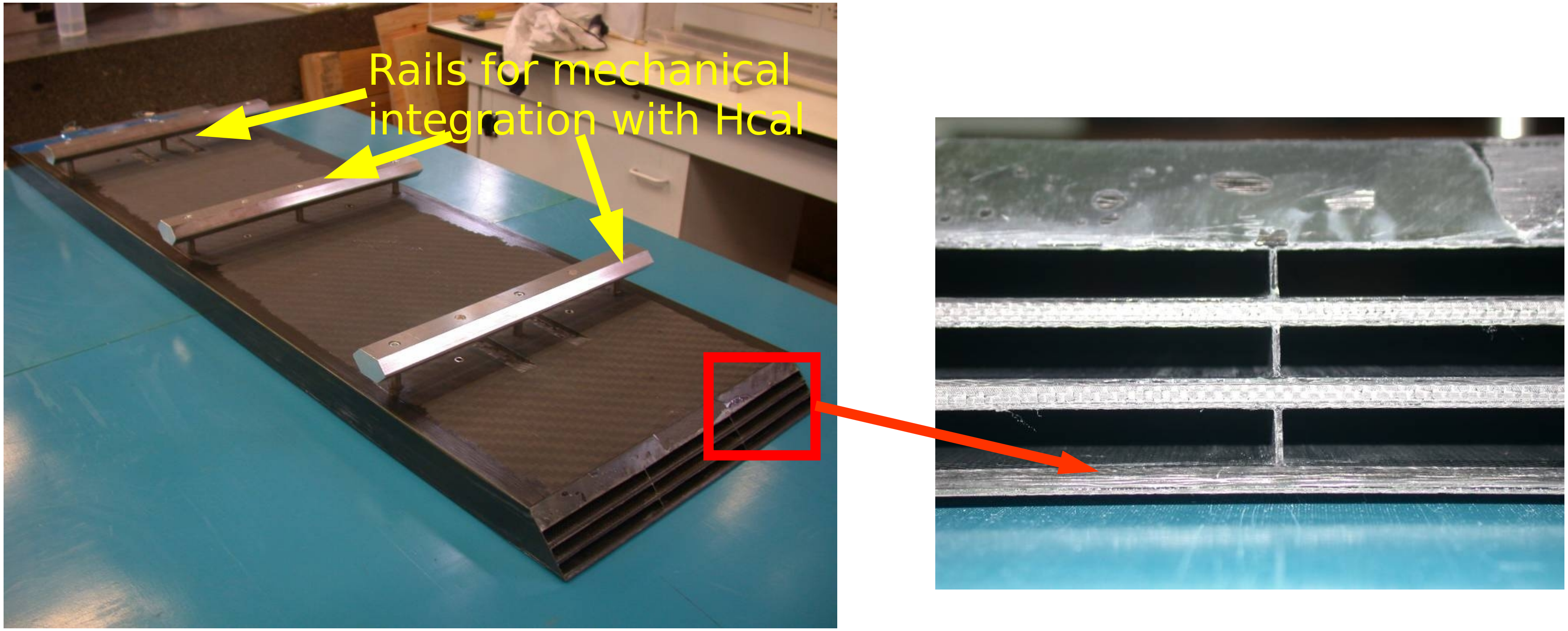
Prototype oF VFE



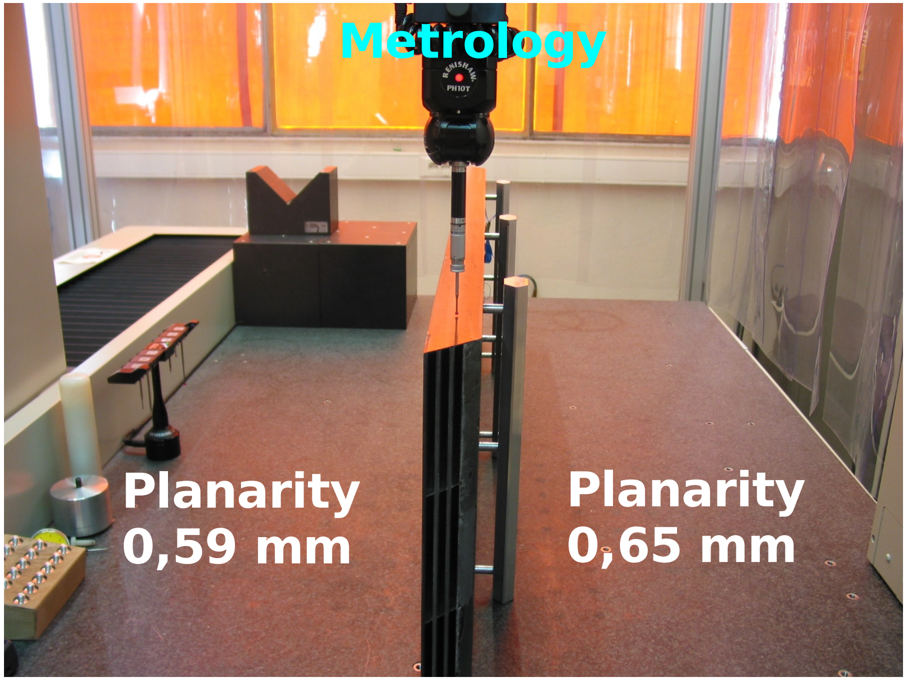


- ⇨ Gaps (slab integration) : 500 µm
- ⇨ Heat Shield: **400 µm ?** Validation with the demonstrateur
- ⇨ PCB : **~1200 µm**
- ⇨ Thickness of Glue : 100 µm
- ⇨ Thickness of SiWafer : 325 µm
- ⇨ Kapton® film HV : **100 µm ?**
- ⇨ Thickness of W : 2100/4200 µm (± 80 µm)

Alveolar Structures with (~) ILC Dimensions



Rails for mechanical integration with Hcal



Metrology

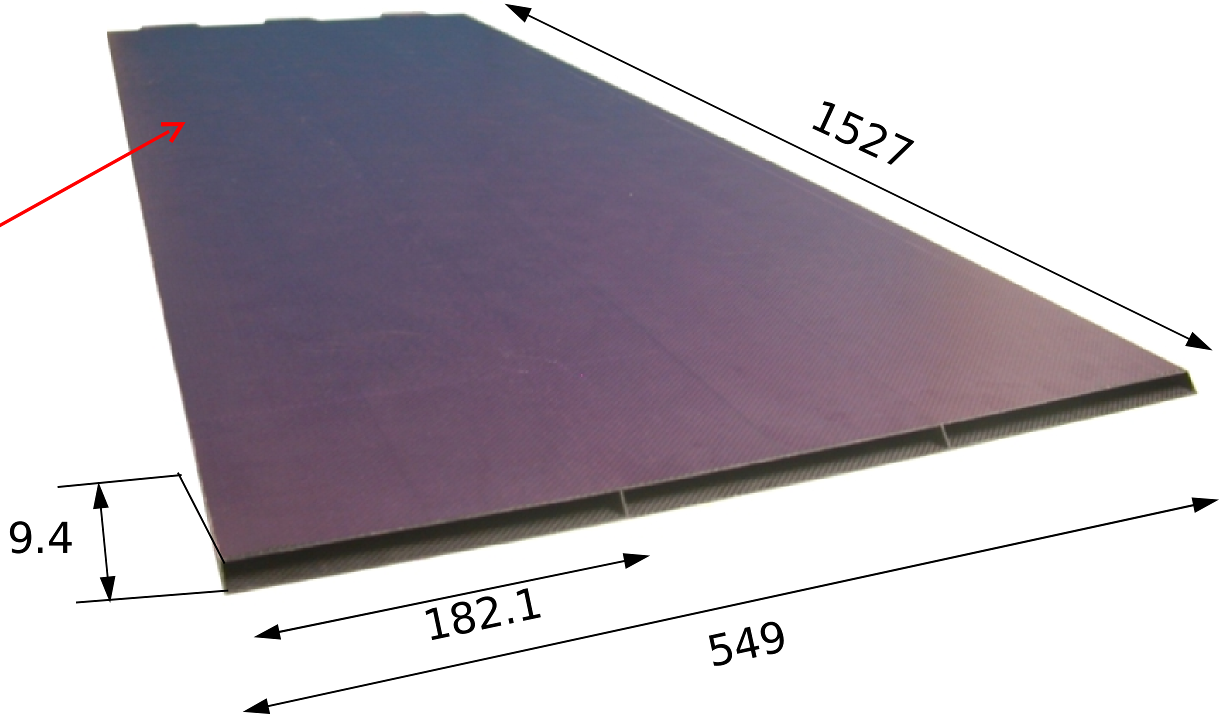
Planarity 0,59 mm

Planarity 0,65 mm

EUDET design

- **New layer built for the EUDET Module**
- Cells width is based on 182.1 mm
- Used for BEAMTESTS.

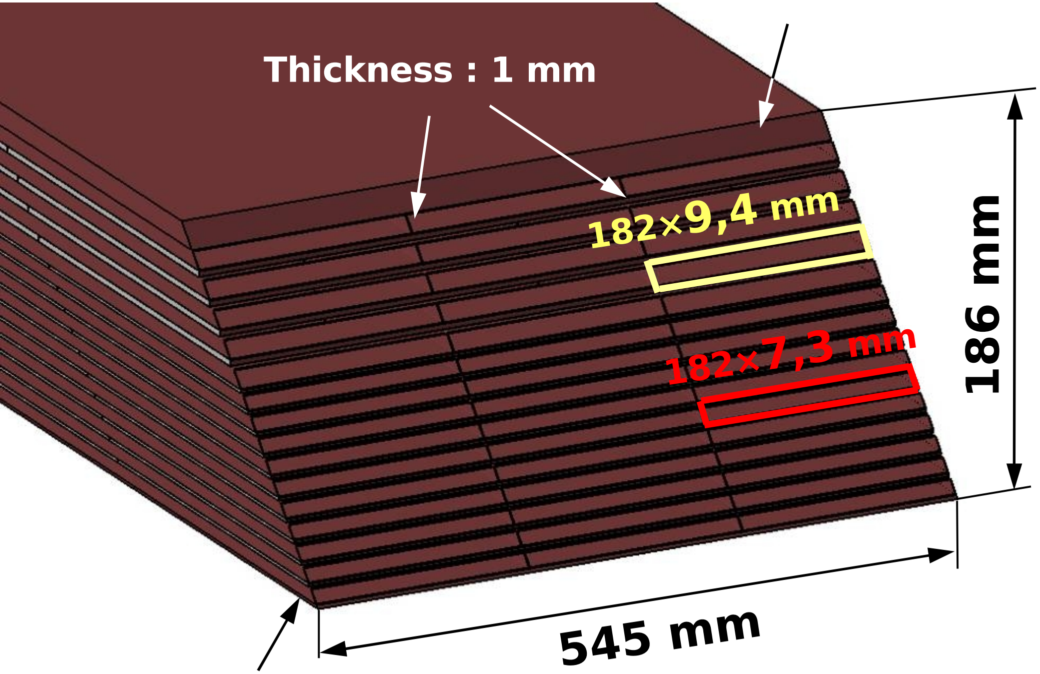
First EUDET layer alveolar structure

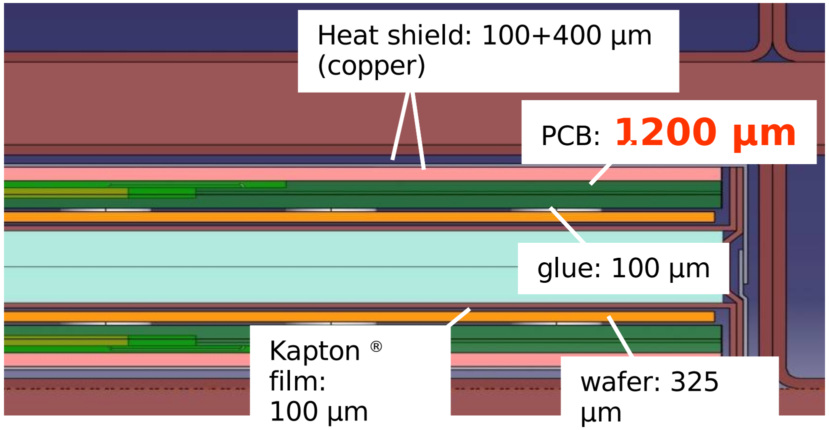


- the assembly consisted of
  - 15 alveolar layers + 14 Tungsten layers
  - 3 columns of cells : representative cells in the middle of the structure
- Width of cells : 182.1 mm
- 2 Thickness cells (7.3 mm and 9.4 mm)
- Identical global length : 1.495m
- Fastening system ECAL/HCAL
- Total weight : ~ 800 Kg

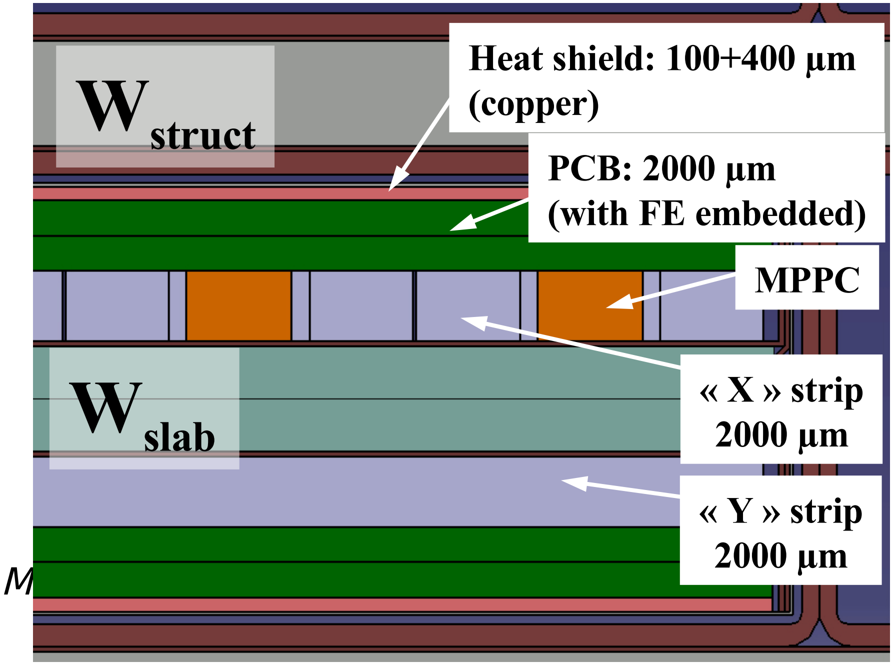
Alveolar structure (based on EUDET)

ECAL W/Si





ECAL W/Scin

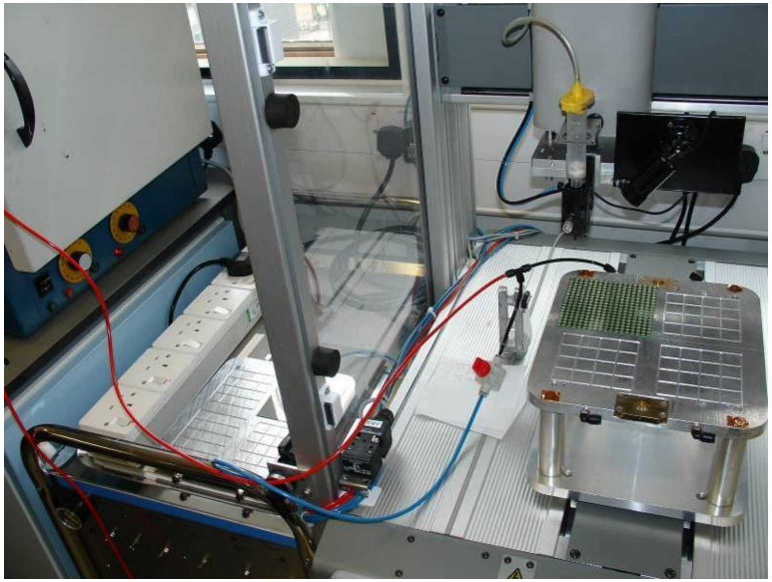


Alveolar structure applicable for alternative Ecal proposals
"TNA"

Gluing of ASUS

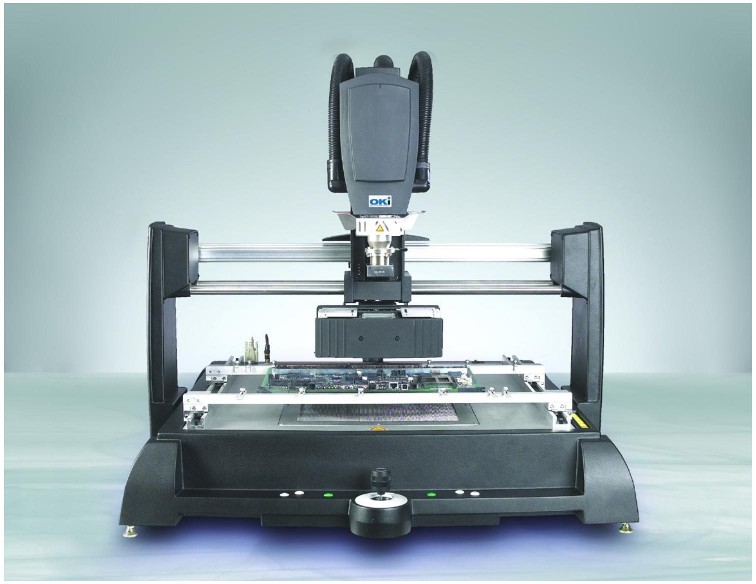
- Controlled glue dot deposition on the PCB
- The (four) Si Wafers are picked up, aligned and placed on the PCB
- Accurate thickness and planarity control via vacuum jigs
- The assembled ASU is allowed to cure

Test board with Dispenser Robot

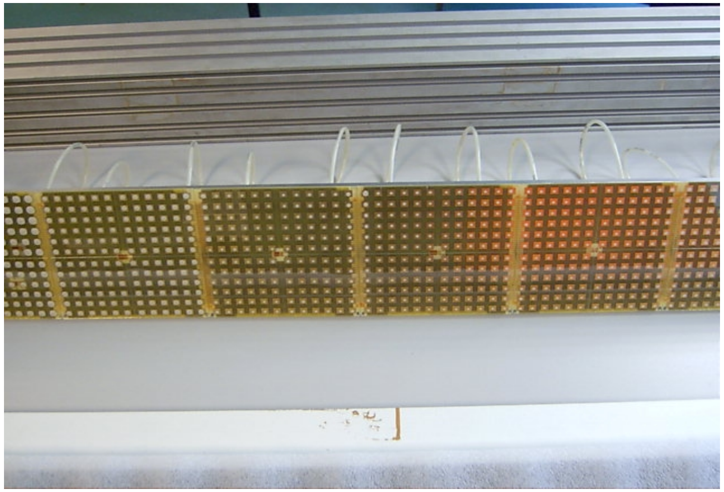


“Gluing” rate 0.4 Hz

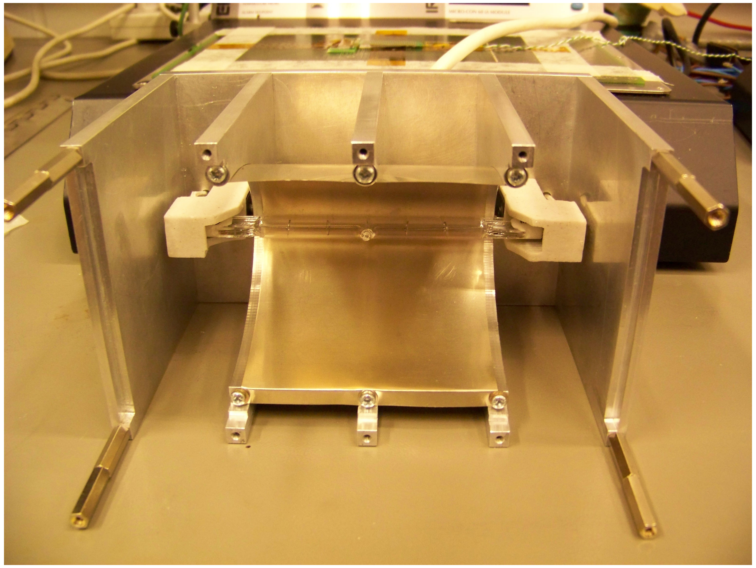
BGA Workstation for Wafer Placement

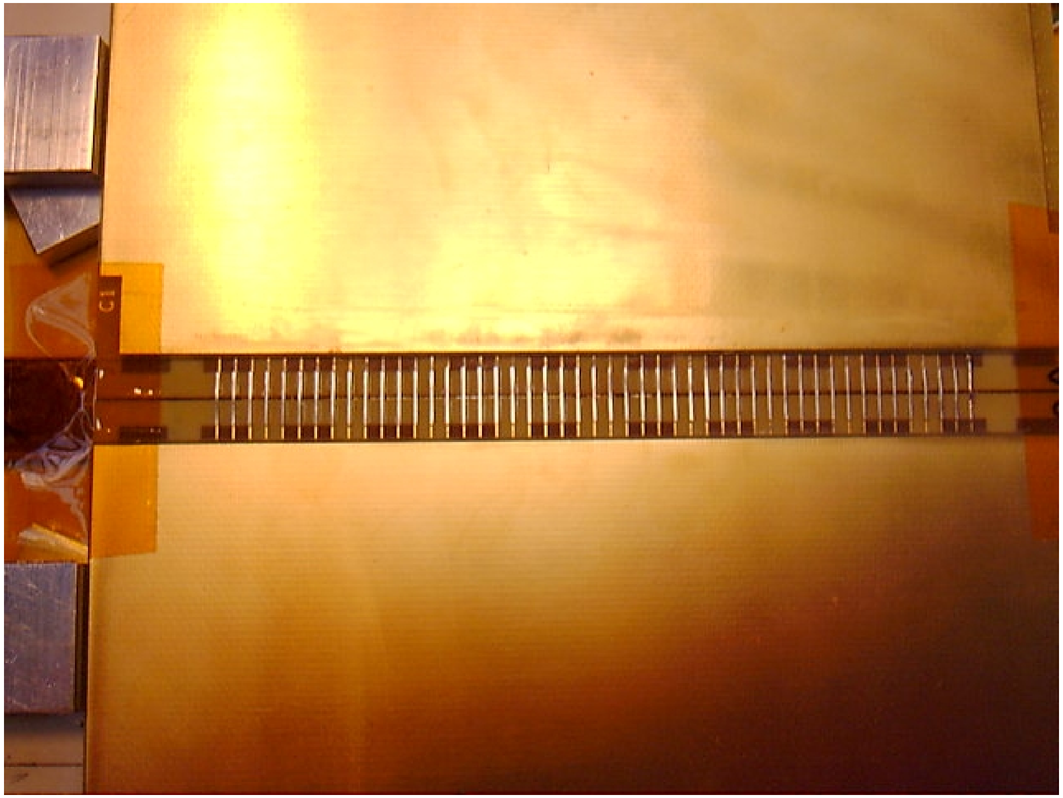


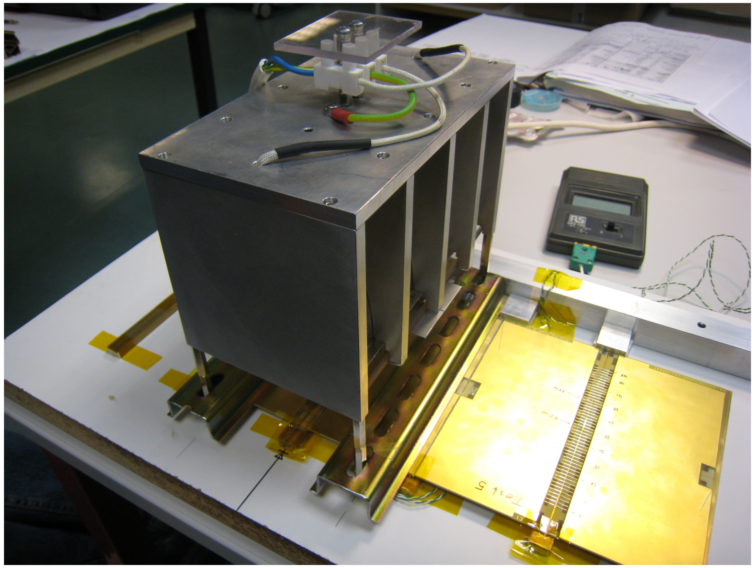
Precise Wafer Placement
by Split Field Optics



The joint between two boards





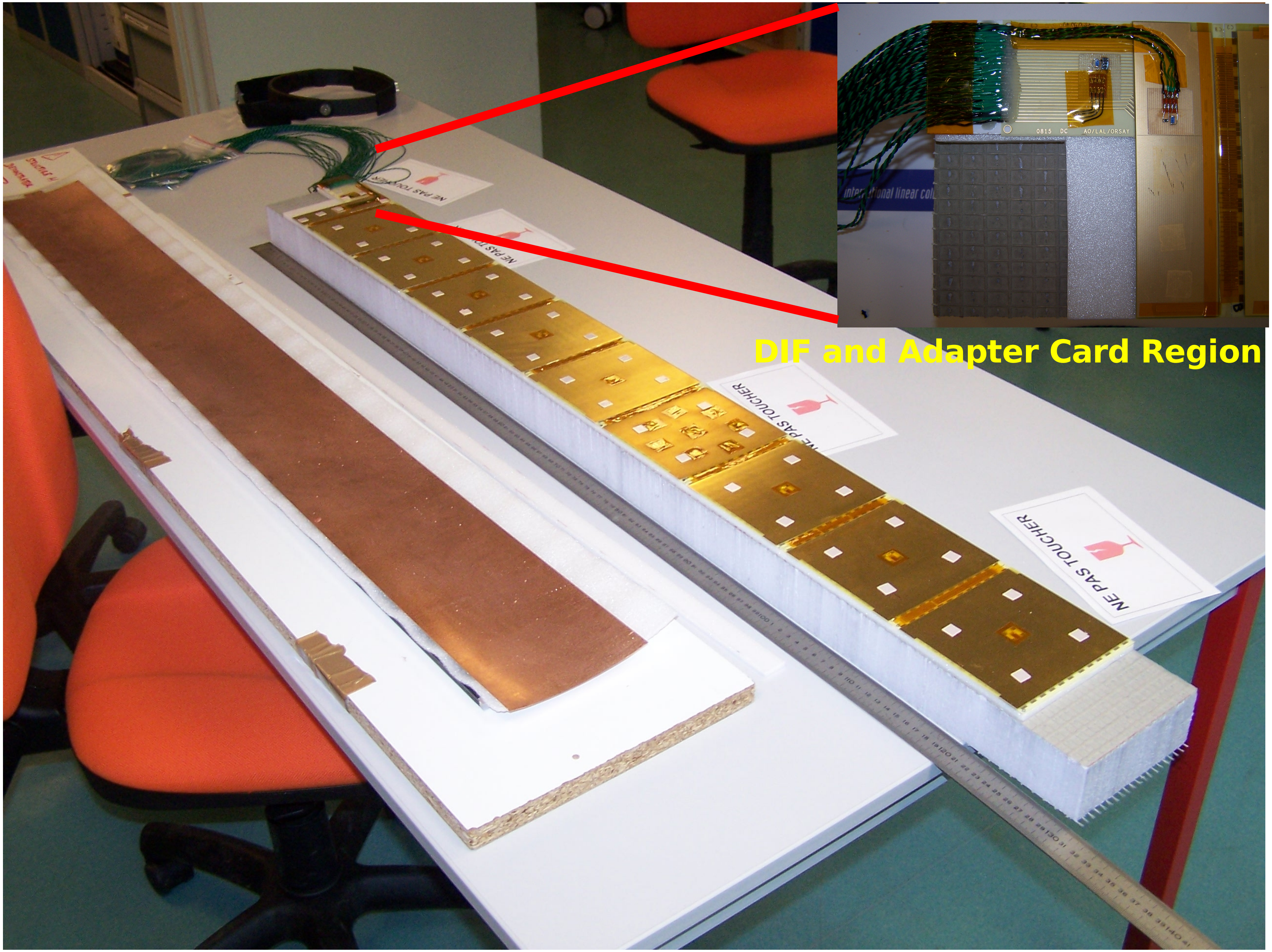


- Joint by halogen lamp heating up tin-bismuth soldering paste
  (Method developed by U. Cambridge)

- Heating Temperature ~200° C

Delicate Process for Demonstrator – Easier for EUDET Module

Thermal Layer – Developping the Techniques for Layer Construction

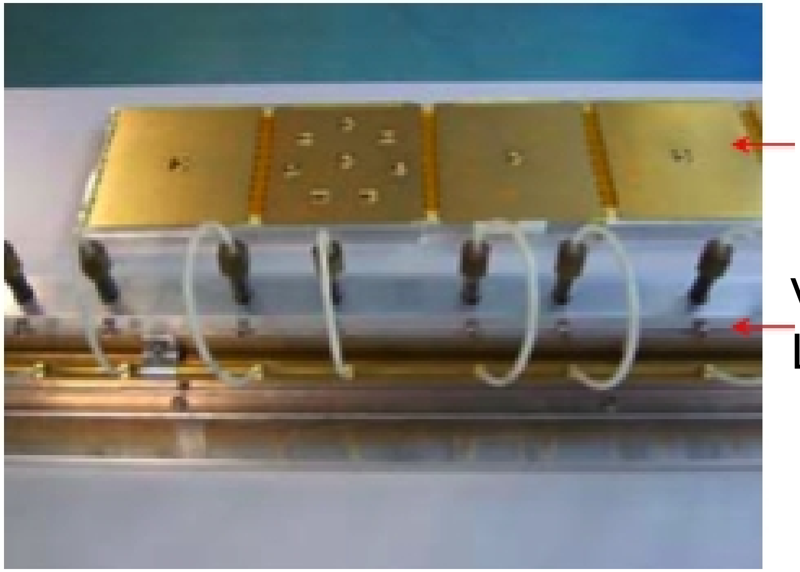


DIF and Adapter Card Region

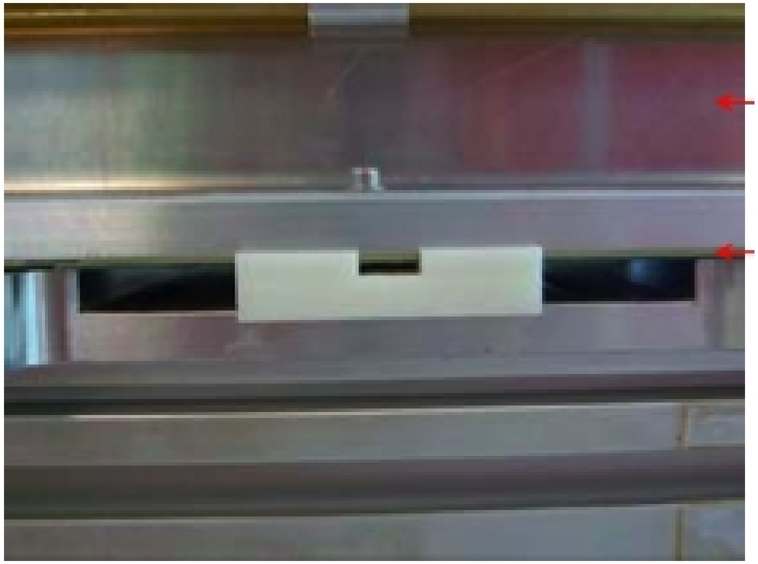
Proof-of-principle to build long layers

Assembly Tools – Handling of fragile layers

Handling by vacuum lifter



Positioning of Vacuum Lifter on ASU Line



(Careful) handling of ASU Line established

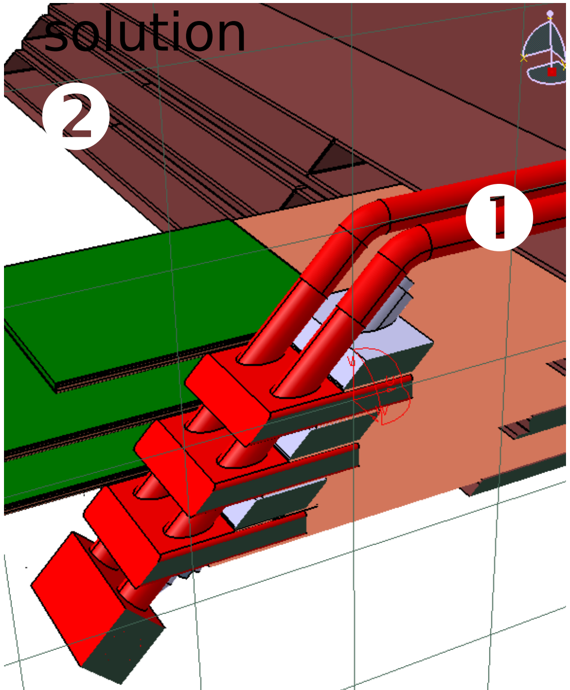
- **Detector Assembly needs more tools and an assembly hall**

EUDET COOLING

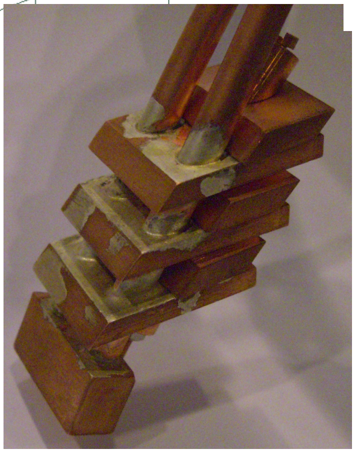
The purpose of cooling system is to maintain the electronics at an acceptable temperature (40°c maximum)

Cold plate : 3 Solutions

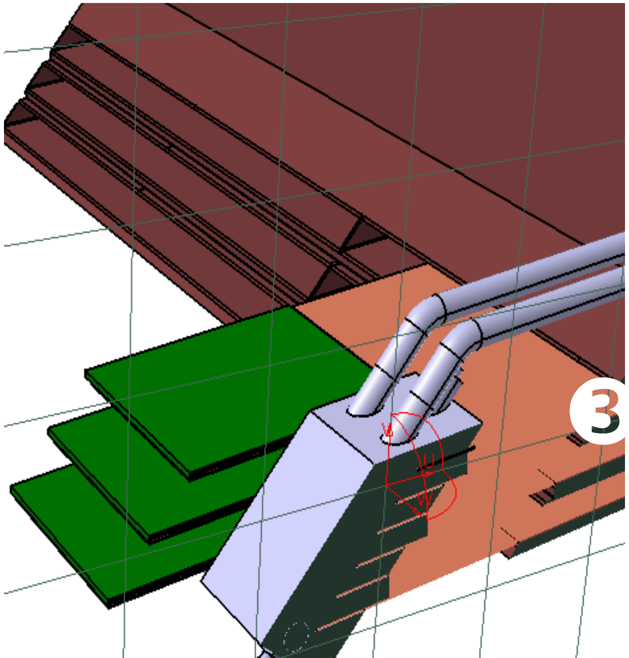
❶ Assembled solution



Water circulating into copper pipe (Internal diameter : 4 mm)



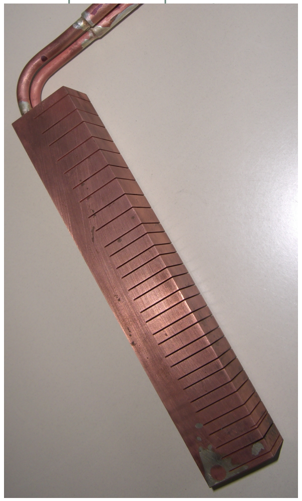
❷ Machining



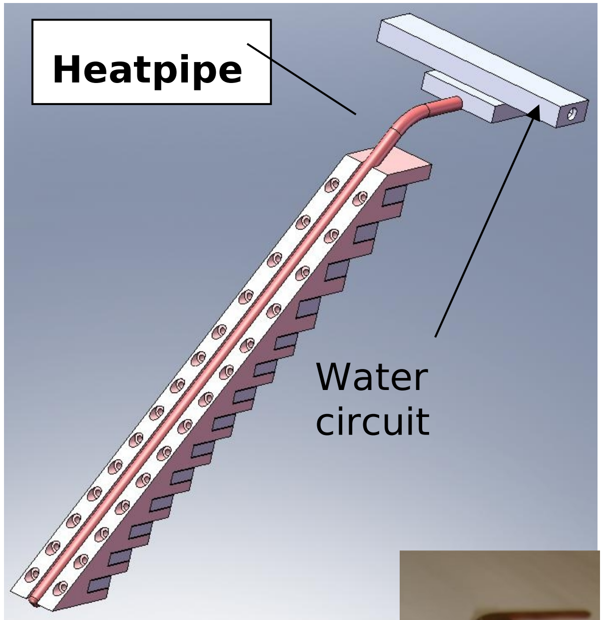
-1 block with water circulating into copper pipe

-(Internal dia.: 4 mm)

- Easier to build



❸Heatpipe



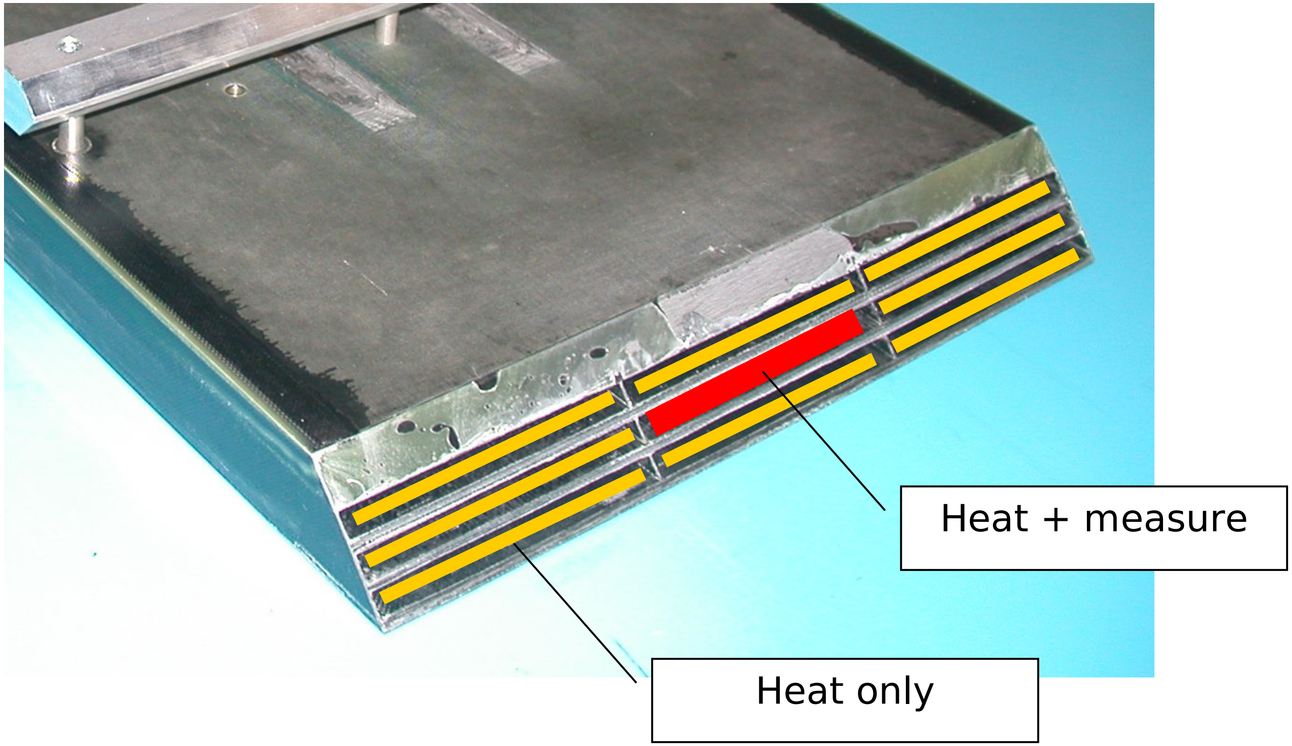
Main advantage :

Connection between Heat pipe and water circuit => contact, far from front-end.

Easy to assemble and reduces leak risk

Reminder on demonstrator – Nex step

- Insertion of wrapped thermal slab into alveolar structure
  Important step towards EUDET (and ILC!!!)

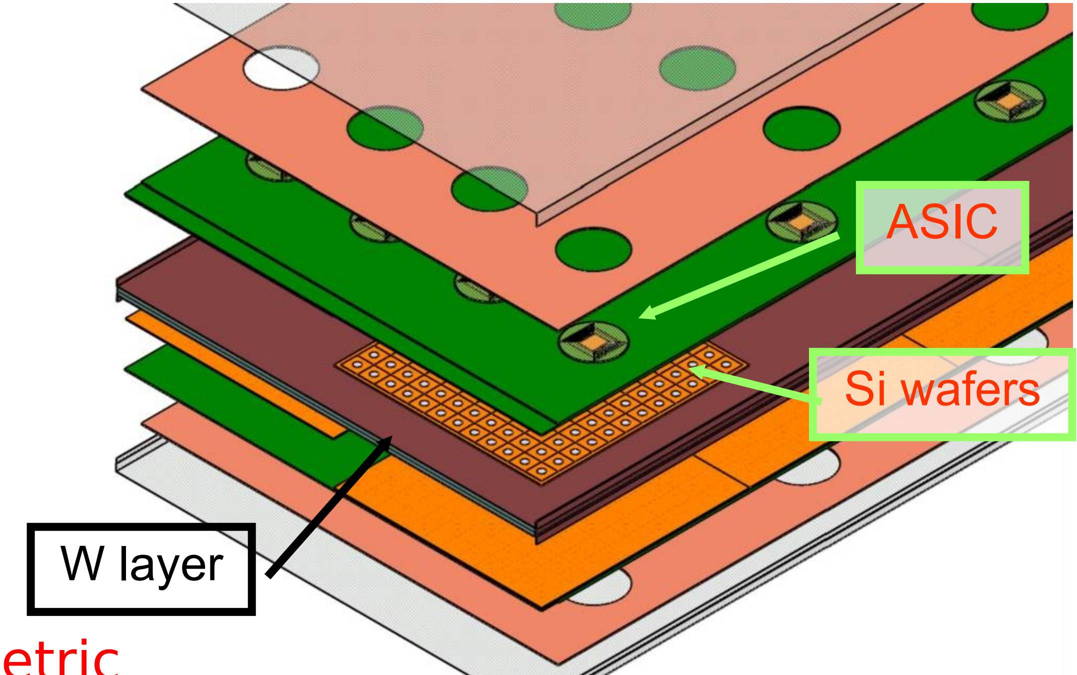


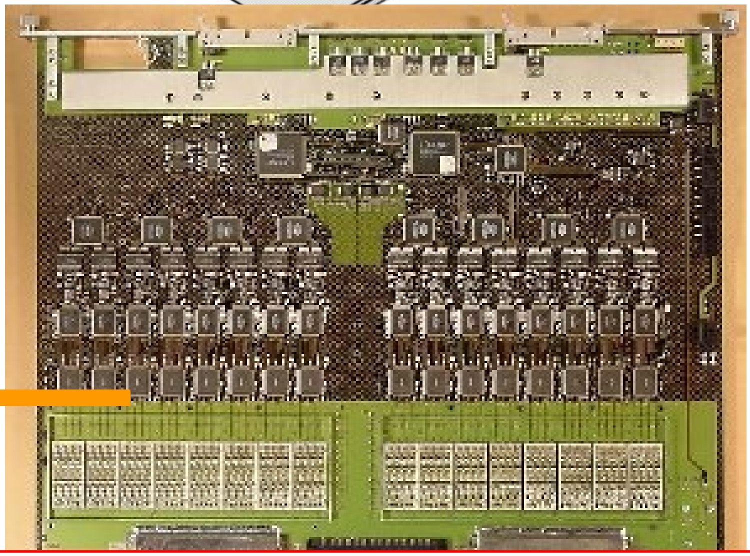
- Continuation of thermal tests with inserted thermal slab
  Construction of heating mock-ups to establish realistic conditions
  Time scale ~ September 2009

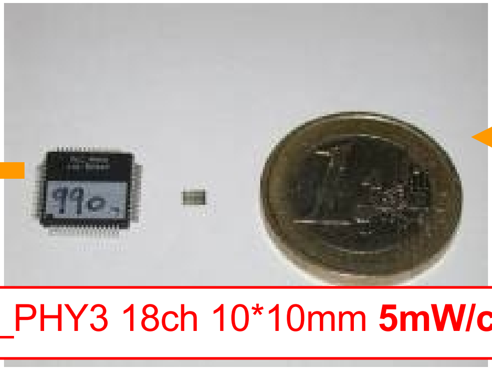
Pieces for 'read' EUDET Module will be ordered in autumn 2009
Funding assured!!!

ILC Challenges for electronics

- Requirements for electronics
  - Large dynamic range (15 bits)
  - Auto-trigger on ½ MIP
  - On chip zero suppress
  - Front-end embedded in detector
  - **Ultra-low power : («25µW/ch)**
  - 10^8 channels
  - Compactness
- « Tracker electronics with calorimetric performance »
- No chip = no detector !!







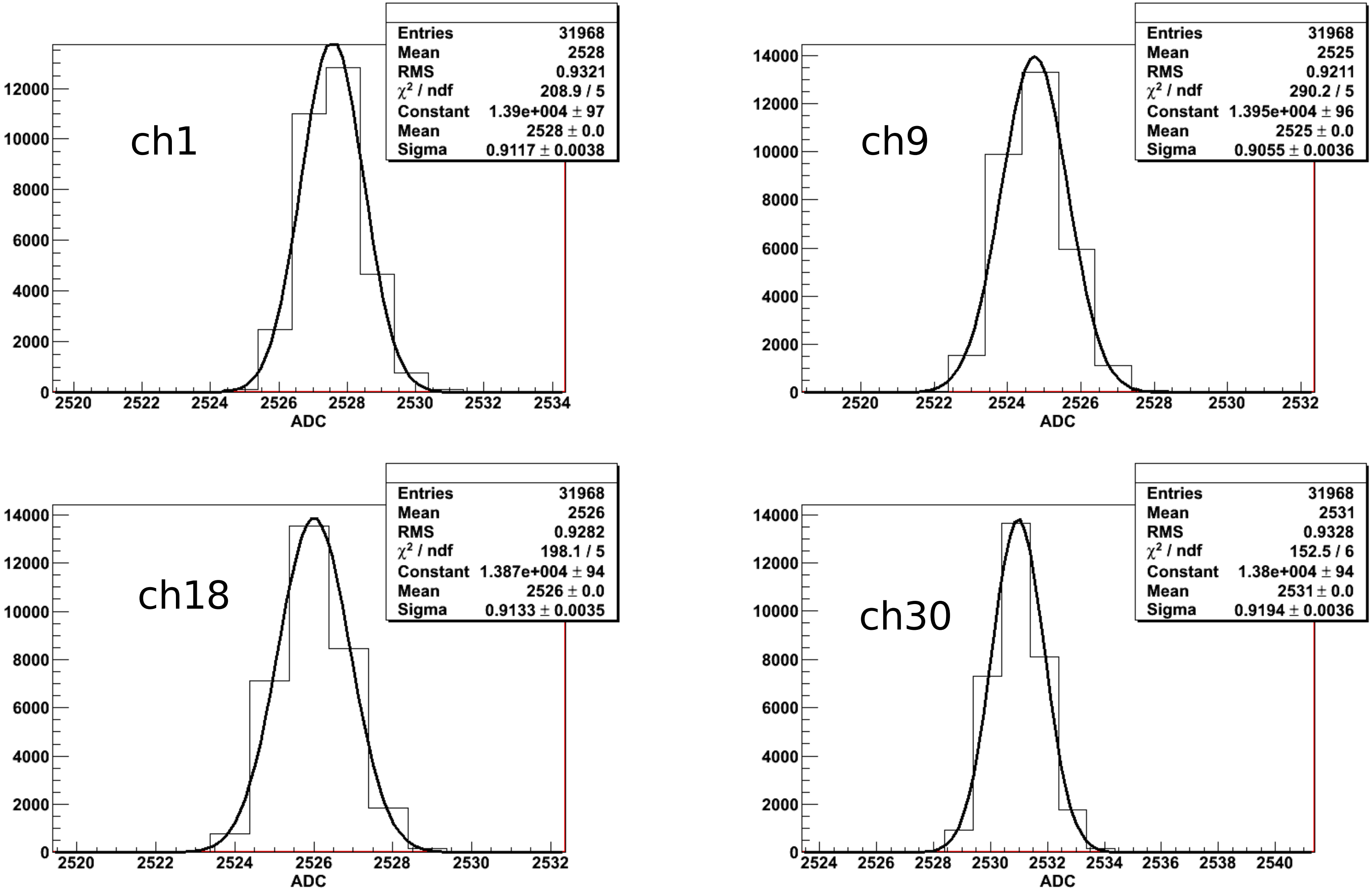
ILC : **25µW/ch**

FLC_PHY3 18ch 10*10mm **5mW/ch**

ATLAS LAr FEB 128ch 400*500mm **1 W/ch**

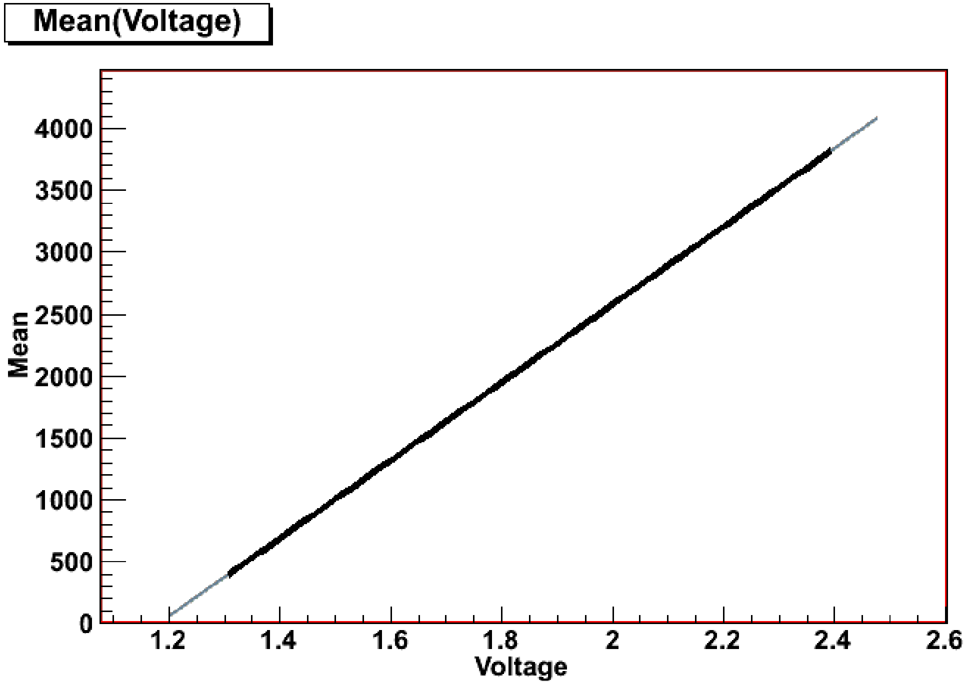
Characterisation of SPIROC2 Chip – Used for first Ecal Prototype

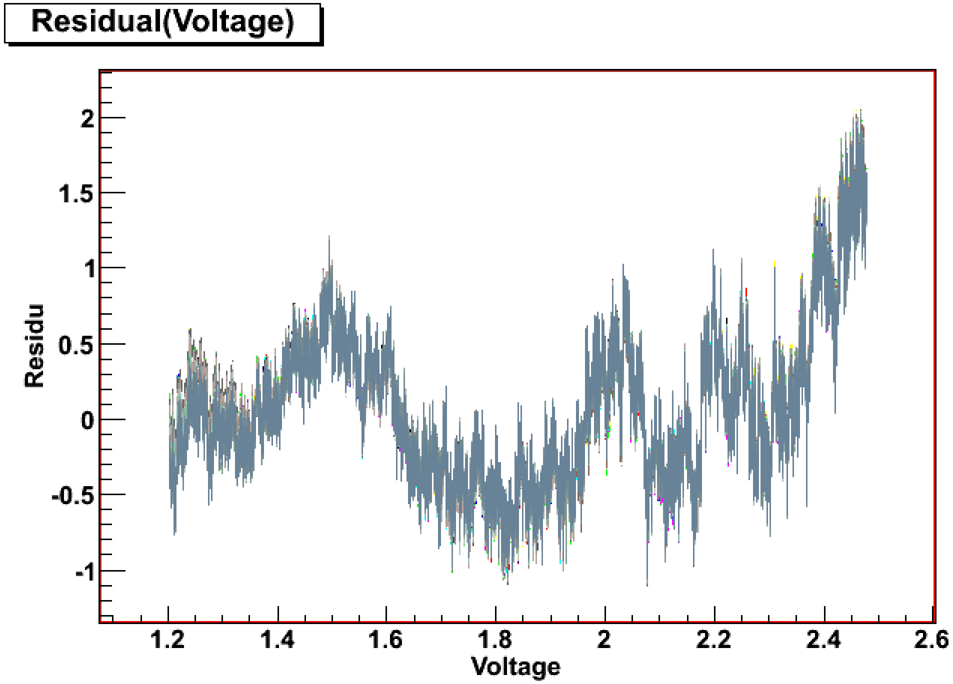
Gaussiennes – 2 Volt



Remark: SPIROC2 very similar to SKIROC2 (SiW Ecal Chip)
- 144 channels instead of 256
- Smaller dynamic range 500 MIPS instead of 2500 MIPS

Linearity of ADC - Chip n°2





- Linearity measured in 250 muV steps between 1.2V and 2.5V input Voltage
- ADC of Chips linear in dynamic range
- On going – Study of signal propagation through Chip (Pre-Amp, Shaper ...)
  Already promising results

Chip ready to be used in SiW Ecal Prototype

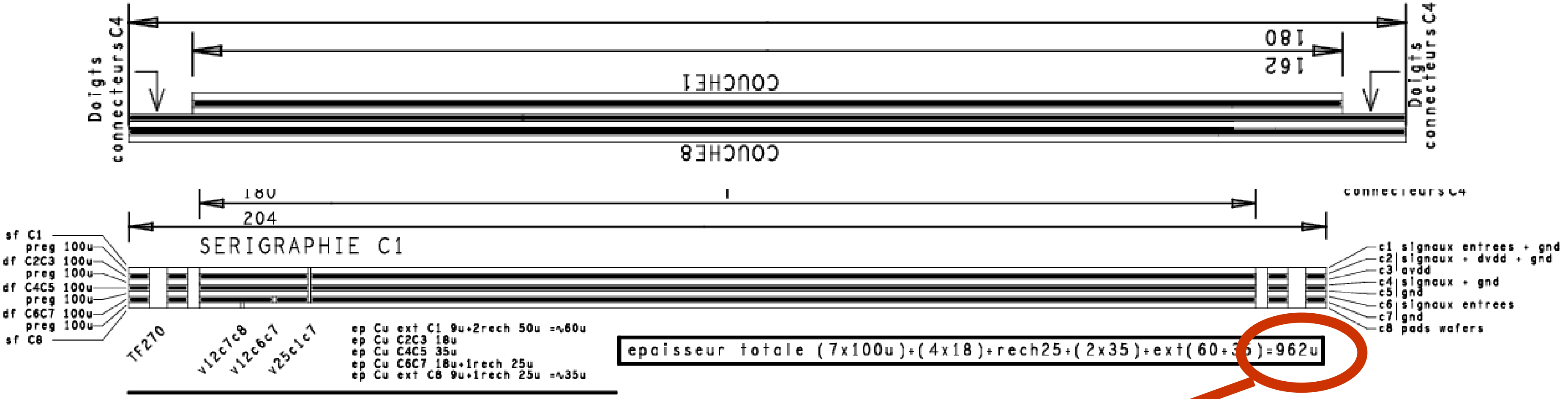
PCB for first SiW Ecal Prototype

<u>Pile-up</u>

TOP	GND + Input chip signal
C2	horizontal routing + DVDD + GND
C3	AVDD
C4	GND + vertical routing
C5	GND (pads signal shielding)
C6	pads routing
C7	GND (pads shielding)
BOT	PADS

<u>4 drilling sequences</u> :
- Laser C7-C8 120µ filled
- Laser C6-C7 120µ
- Mechanical C1-C7
- Mechanical C1-C8 (for PCB fastening)

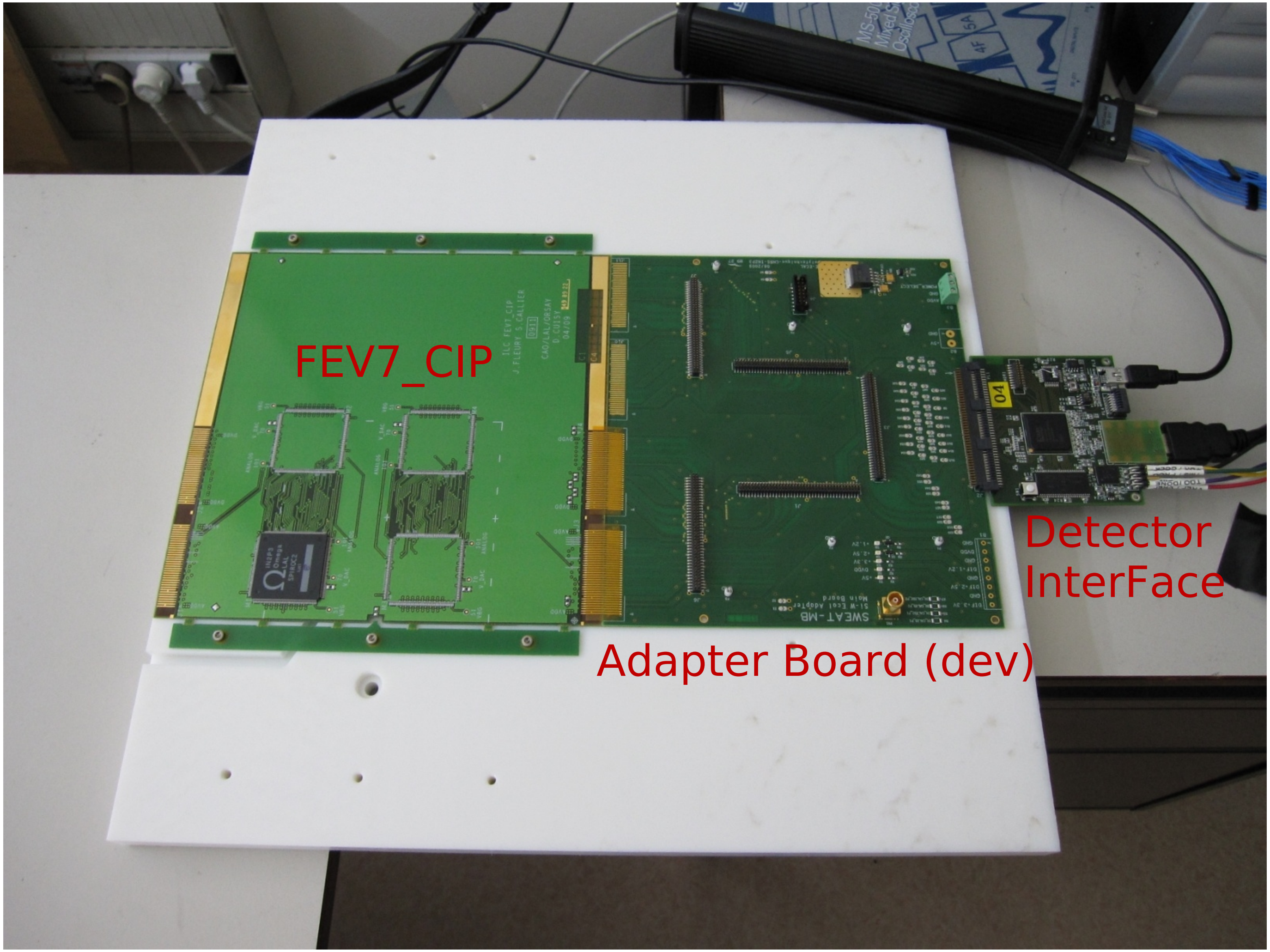
FEV 7
CIP



PCB Thickness : 962µm

FEV7_CIP (Chip in Package):Predecessor for final board with all functionalities
Next Step FEV7_COB (Chip on Board)
Final Aim FEV8

First SLAB prototype



To upstream components of **generic DAQ:**

LDA

ODR

…

Equal for all CALICE Tech. Prototypes

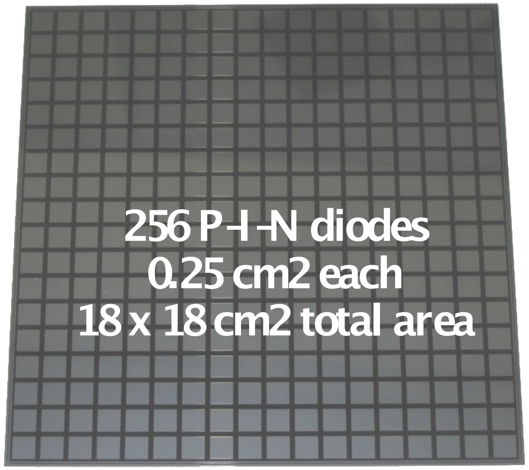
Essentially ready!!!

PIN Diodes Silicon Sensors

Designed for ILC : **Low cost, 3000 m2** Minimized number of manufacturing steps
Target is 2 EUR/cm2
Now : 15 EUR/cm2
Use of **floating guard-rings**

Known issues

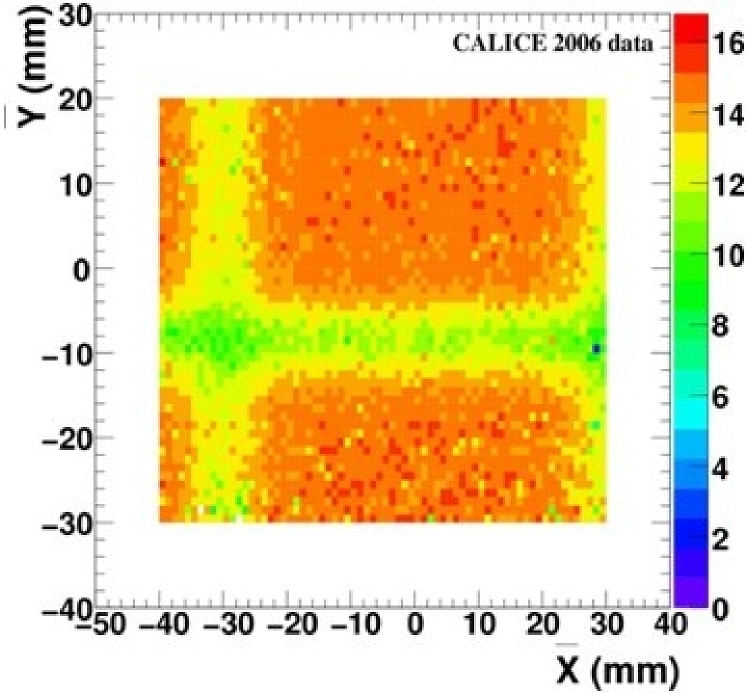
Dead space optimization
Guard-rings do not collect charges
Dead space to be reduced



256 P-I-N diodes
0.25 cm2 each
18 x 18 cm2 total area

EUDET layout

Prototype from Hamamatsu
40 Wafers at Hand
out of 180 needed!!!

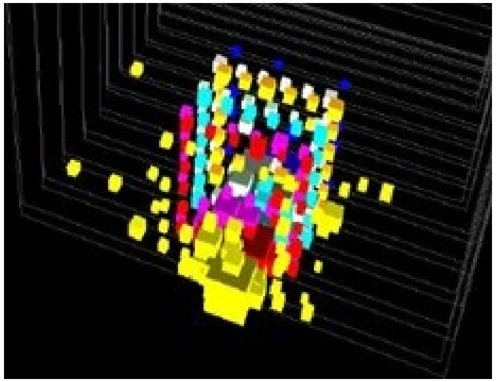


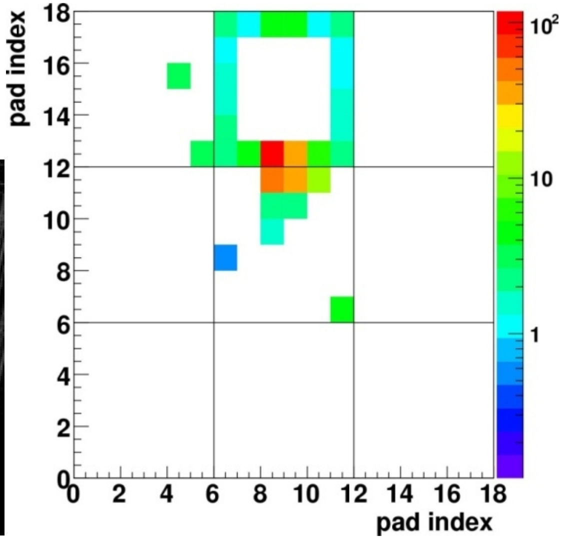
Hit map from physics prototype

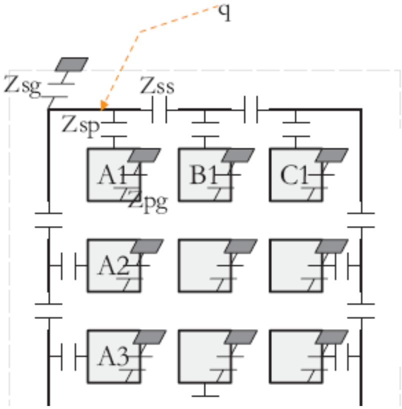
R&D on Crosstalk

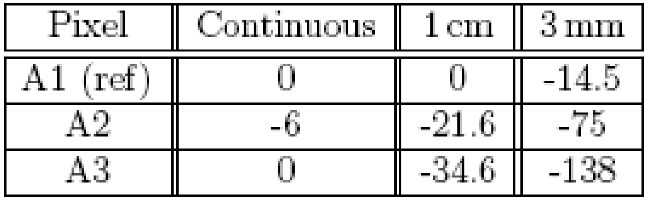
Segmented Guard Rings layout
Simulation models at Silicon or Electrical Level

Crosstalk due to floating guard-rings
Due to capacitive couplings
From metal layers at the surface







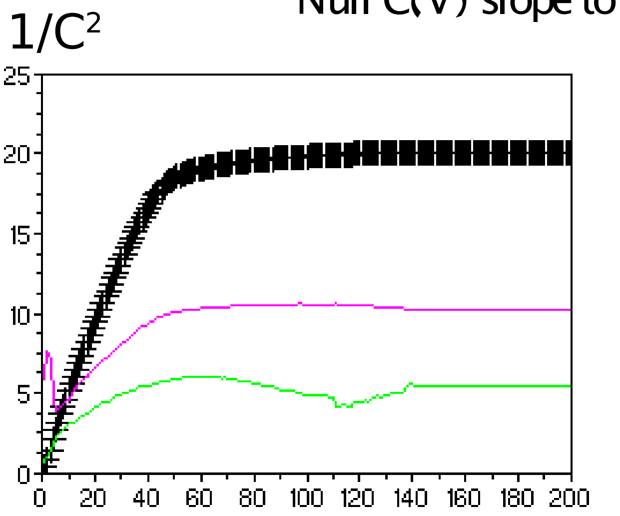


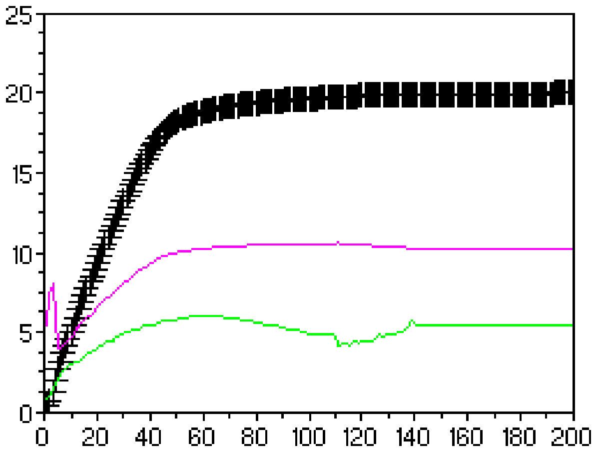
Pixel	Continuous	1 cm	3 mm
A1 (ref)	0	0	-14.5
A2	-6	-21.6	-75
A3	0	-34.6	-138

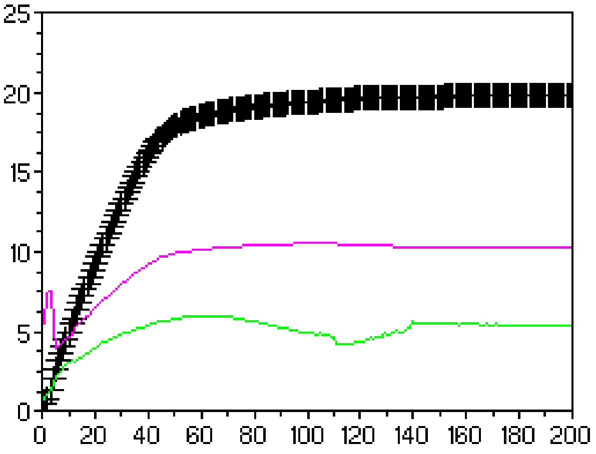
$$T = T_{elec} \times T_{pix} \times (T_{seg} \times T_{ss})^{N_{seg}} \times T_{seg} \times T_{inj}$$

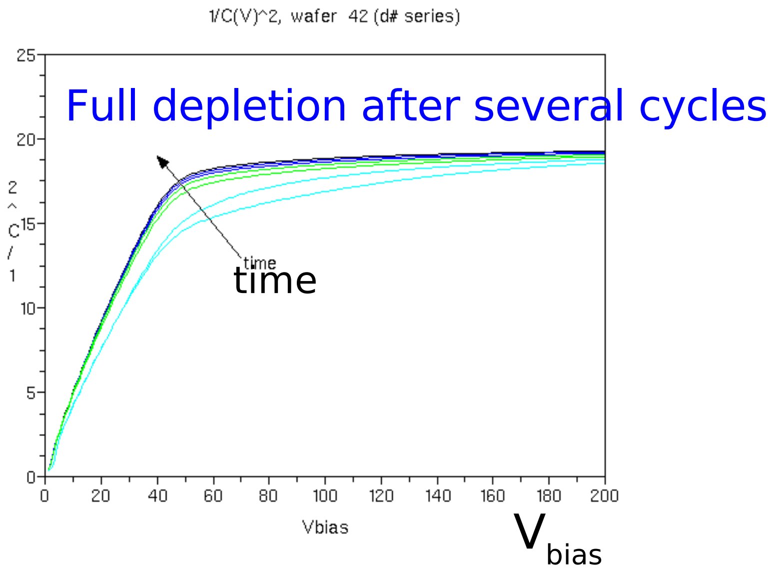
I(V) and C(V) characterization

Breakdown voltage > 500 V
Current leakage < 4 nA/pixel (chip is DC coupled)
Full depletion at 150 V
Null C(V) slope to avoid dC/dV noise









Full depletion after several cycles

Very Important Remarks

- Working set of Wafers is Milestone for EUDET √

- Finding a way to produce cost saving SiW is a very critical item for the completing the EUDET module and also for the ILC

  Will be one of the top priorities in the coming year

  Clearly, a nice opportunity for TNA
  Testing new wafers on working electronics bench

- EUDET funding exhausted by set of 'Hamamatsu SiW'

  Funding for entire module might need to be stretched over several years!!!!

Conclusion and Outlook

- Technical Design finished in Oct. 2008

Preparation of Demonstrator Tests since then

- Since February - studies with the demonstrator
  - Measurement for thermal analysis
  - Assembly of alveolar structure finished
  - Integration tools for long slab very well advanced

Demonstrator studies
cover most if not all aspects described in EUDET proposal
The collaboration is a real pleasure, thanks to everbody involved!!!

Conclusion and Outlook cont'd

- Towards the EUDET Module

- Focus of getting the VFE accomplished during 2010
  - Meeting EUDET Timeline with “intermediate” solution for VFE SPIROC in SKIROC on a FEV7 variant

- “Shipping” signals out
  Interface to the DAQ is addressed

- Results with first ASU expected during this winter
  - Electronics testbench setup – In Debugging Phase

- Construction of Alveolar Structure for 'real' EUDET Module has started
  Completion during first half of 2010

Once first cosmics on electronics testbench seen we can say

SiW Ecal protoype is ready

Funding for full blown detector is however on critical path in several fields

- Expect Assembly to start towards the beginning of 2011
  First (beam)tests with small units maybe still during 2010
  Testbeams with EUDET Module towards middle/end 2011