Readout electronics for LumiCal detector

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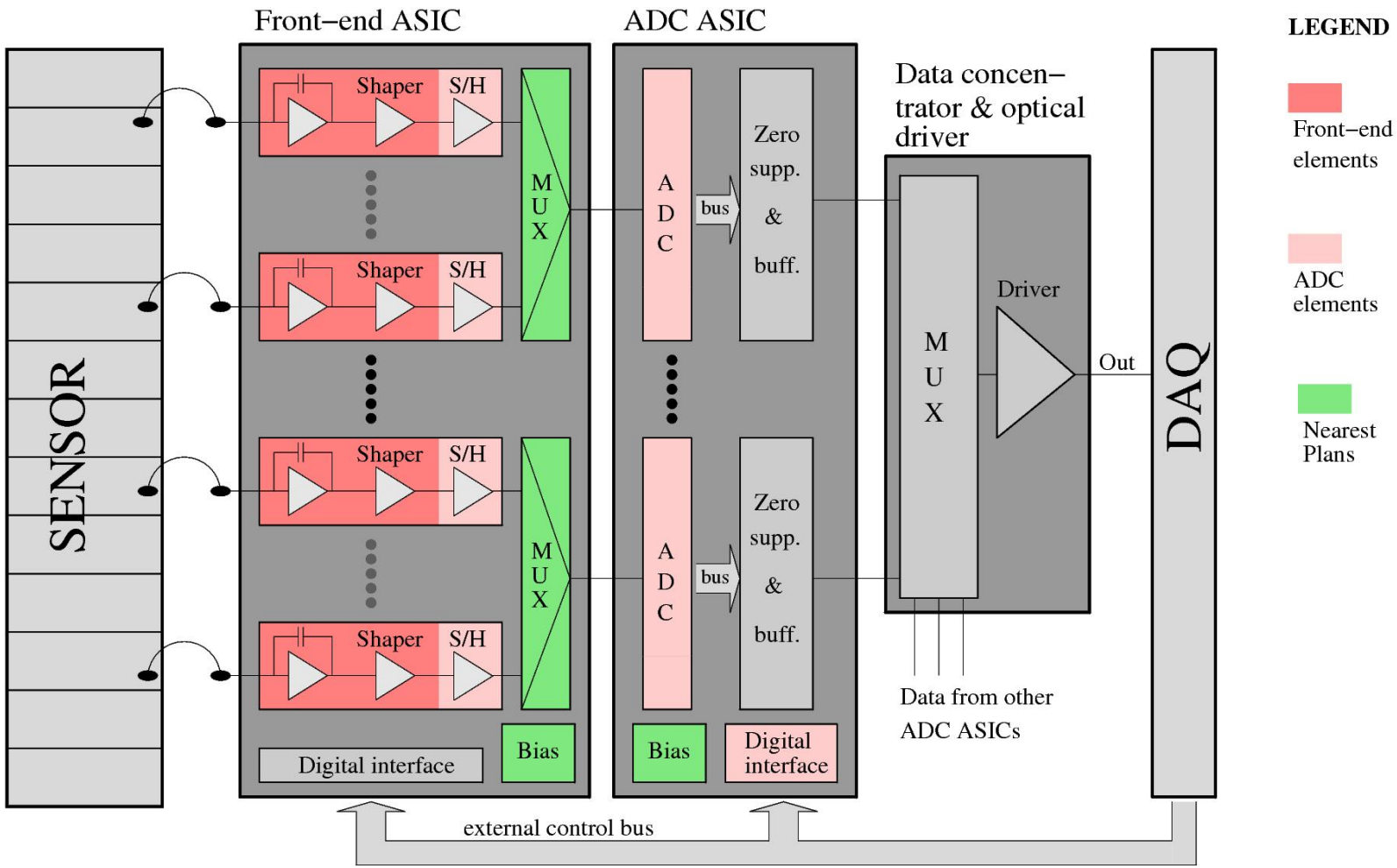
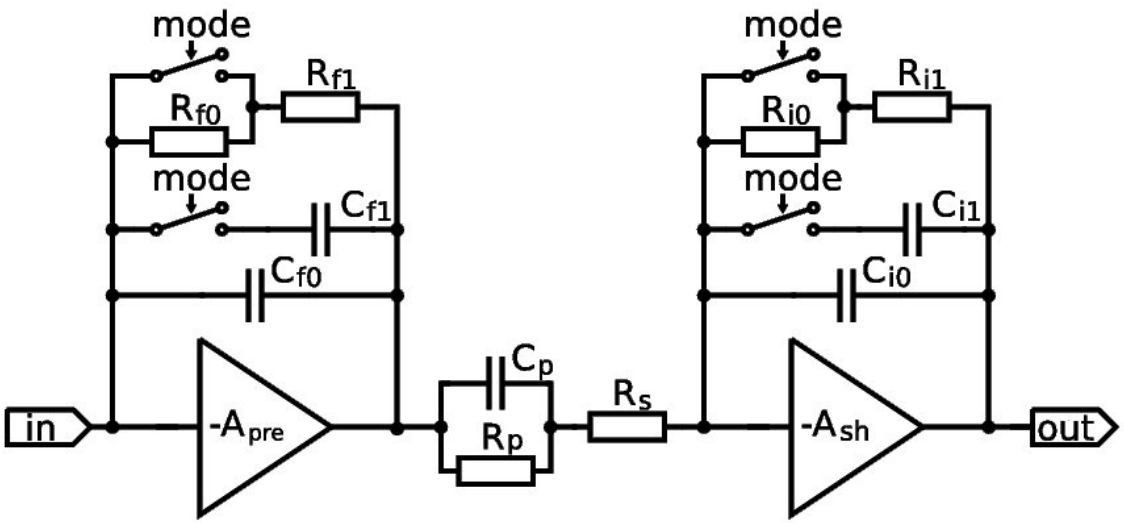
Outline

LumiCal Readout System



Present developments done in 0.35 μm CMOS technology, not necessarily final choice...

Front-end requirements (old)



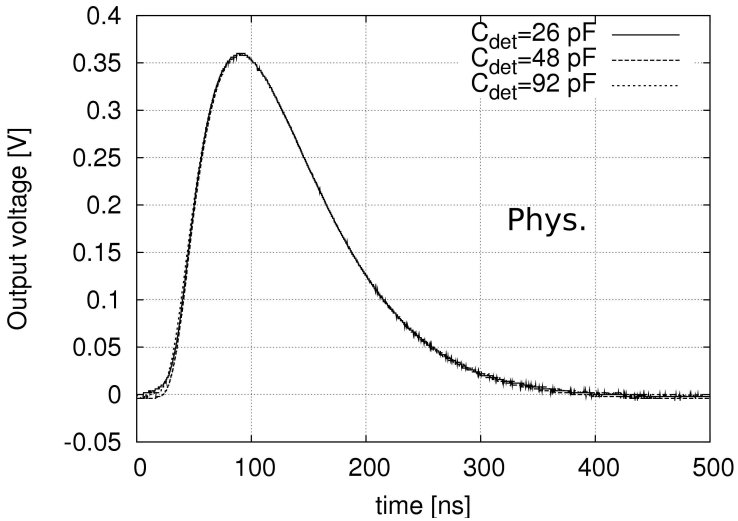
Components

- Charge amplifier
- Pole zero cancellation
- 1^{st} order shaper

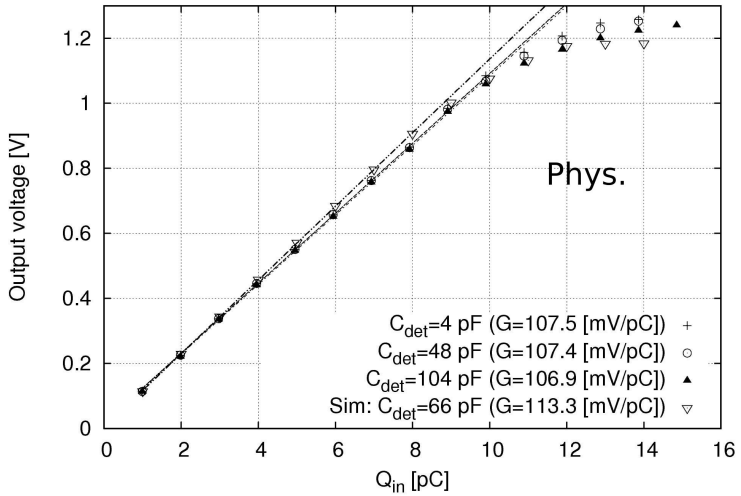
- $C_{det} = 10 \div 100$ pF $\rightarrow$ charge sensitive amplifier
- $\Delta t_{bunch} \simeq 300$ ns $\rightarrow$ $T_{peak} \simeq 60$ ns
- Two independent modes: physics and calibration (MIP) $\rightarrow$ switched gain in preamplifier and shaper
- Physics mode: $Q_{max} \approx 10$ pC $\rightarrow$ $C_f \approx 10$ pF
- Calibration mode: $S/N > 10$ for MIP requested

Front-end measurements

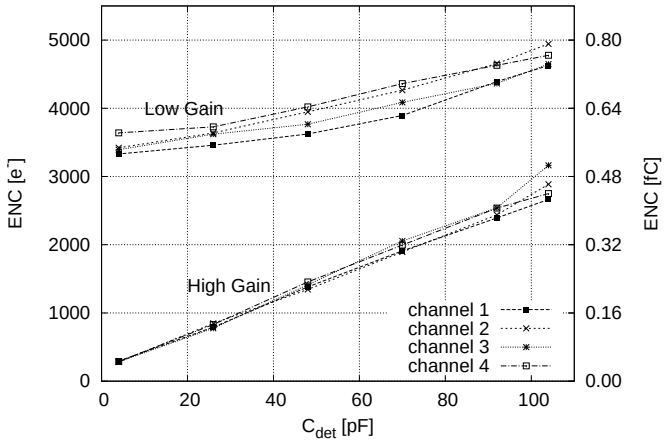
Pulse shape



Gain



Noise



- Prototype 8 channels ASIC produced
- 4 channels with resistive (R_f) and 4 with MOS feedback in preamplifier
- Both versions fully functional
- Front-end linear up to about 10 pC, works with C_{det} up to about 1000 pF

Front-end parameters summary

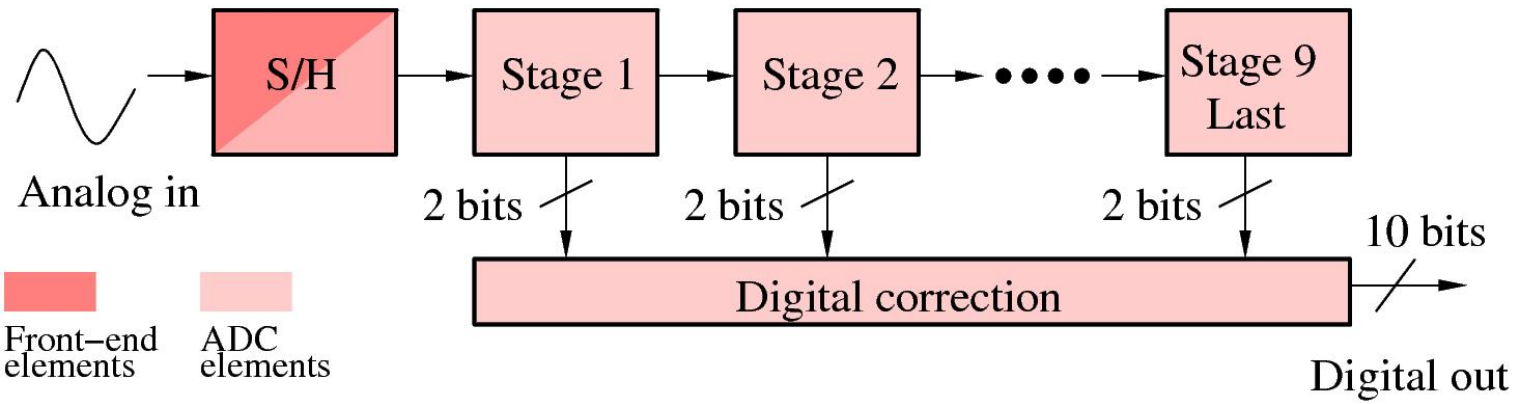
Mode	Gain [mV/fC]	Noise@50pF [fC]	Linearity [pC]	Rate [MHz]	Crosstalk [%]
Physics	0.107	0.62	10	3	≈1
Calibration	≈20	0.28	0.035	3	≈0.1

- Similar results for both R_F and *MOS* configurations (MOS slightly better)
- Crosstalk needs to be measured with sensor fanout
- Power consumption per channel is 8.9 mW
- Noise in details:
  - $\mathrm{Noise}_{\mathrm{phys}}[\mathrm{el}] = 3300 + 13 \cdot C_{in}[\mathrm{pF}]$
  - $\mathrm{Noise}_{\mathrm{cal}}[\mathrm{el}] = 170 + 26 \cdot C_{in}[\mathrm{pF}]$

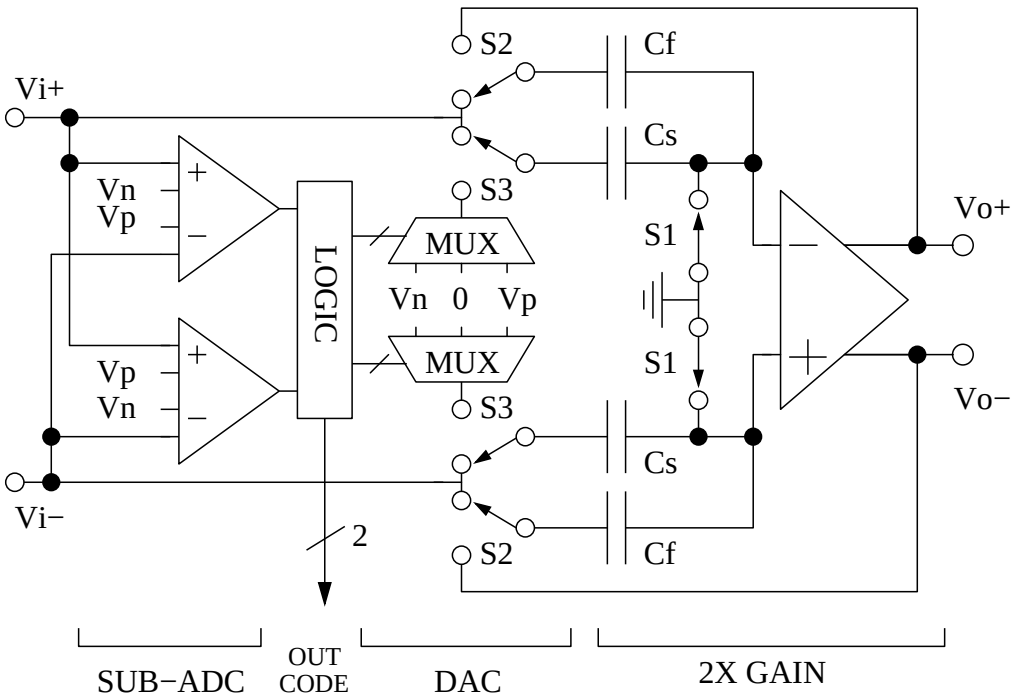
M. Idzik, Sz. Kulis, D. Przyborowski, "Development of front-end electronics for the luminoisty detector at ILC" Nucl. Instr. and Meth. A 608 (2009) pp.169-174

ADC Requirements and archirecture

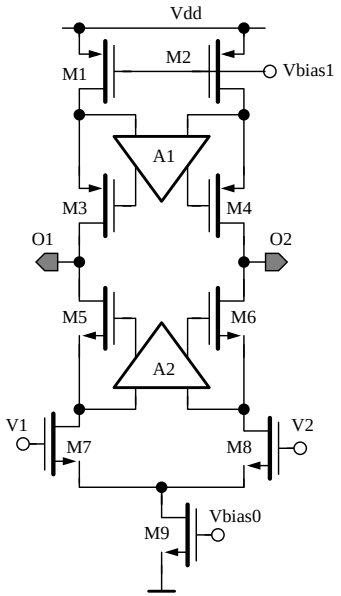
- 10 bit resolution
- Sampling frequency 3-30 MHz (depending on number of FE channels per ADC)
- With and without S/H (S/H can be a part of front-end)
- Power efficient, power and clock ON/OFF
- Fully differential pipeline architecture



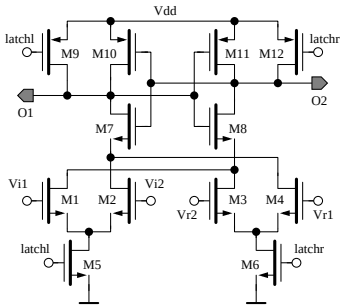
Pipeline ADC - Design



1.5 bit pipeline block

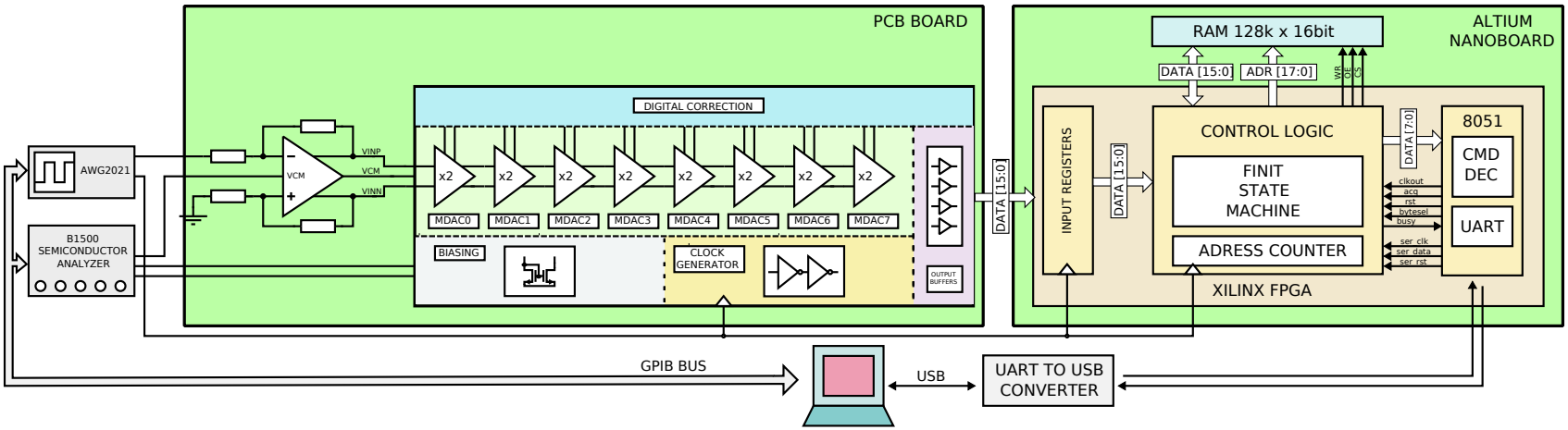


Fully differential amplifier



Dynamic latch comparator

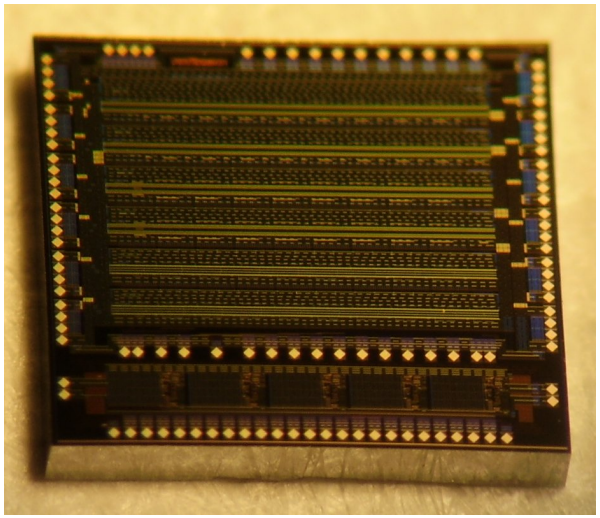
ADC Test Setup

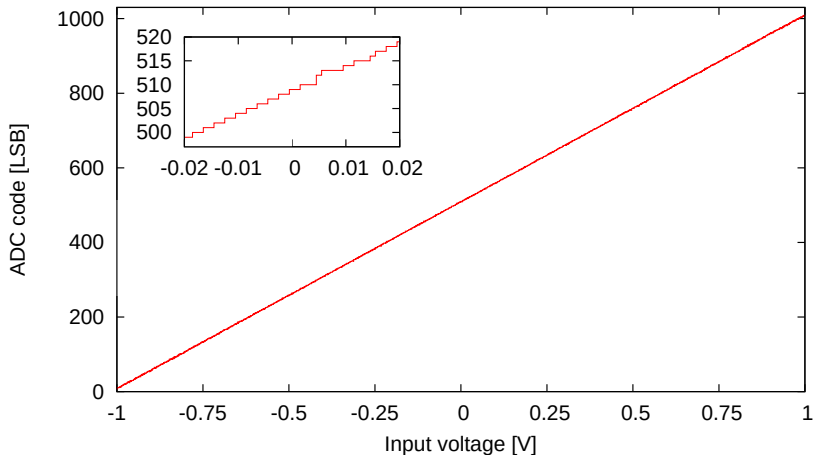


- Signal from AWG2021 generator
- External single-ended to differential converter
- FPGA based (Altium nanoboard with Xilinx Spartan2E) DAQ

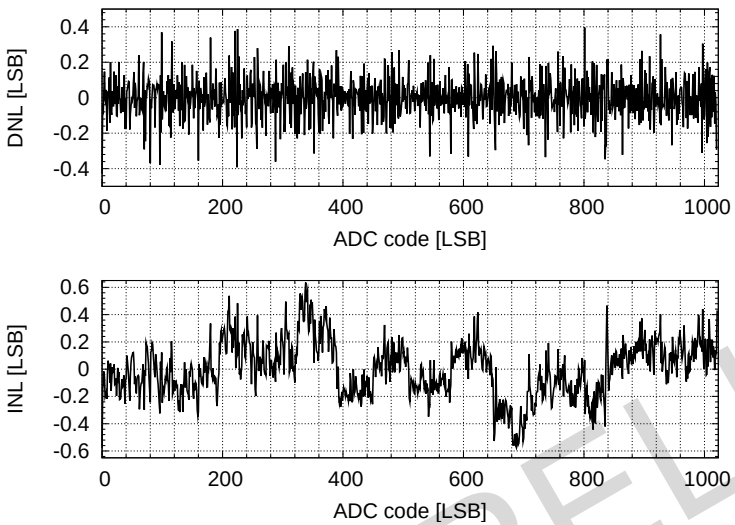
ADC - prototypes and measurements

- 1st prototype: only 8 pipeline stages
- 2nd prototype: 9 stages + S/H + digital correction + clock and power switching
- No reference voltages yet - applied externally
- Both prototypes fully functional
- Both prototypes work up to about 30 MHz

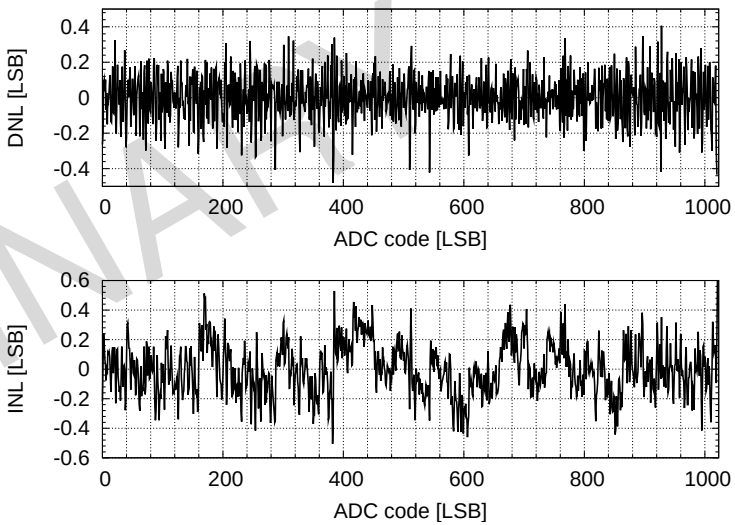




ADC - Linearity



ADC with S/H

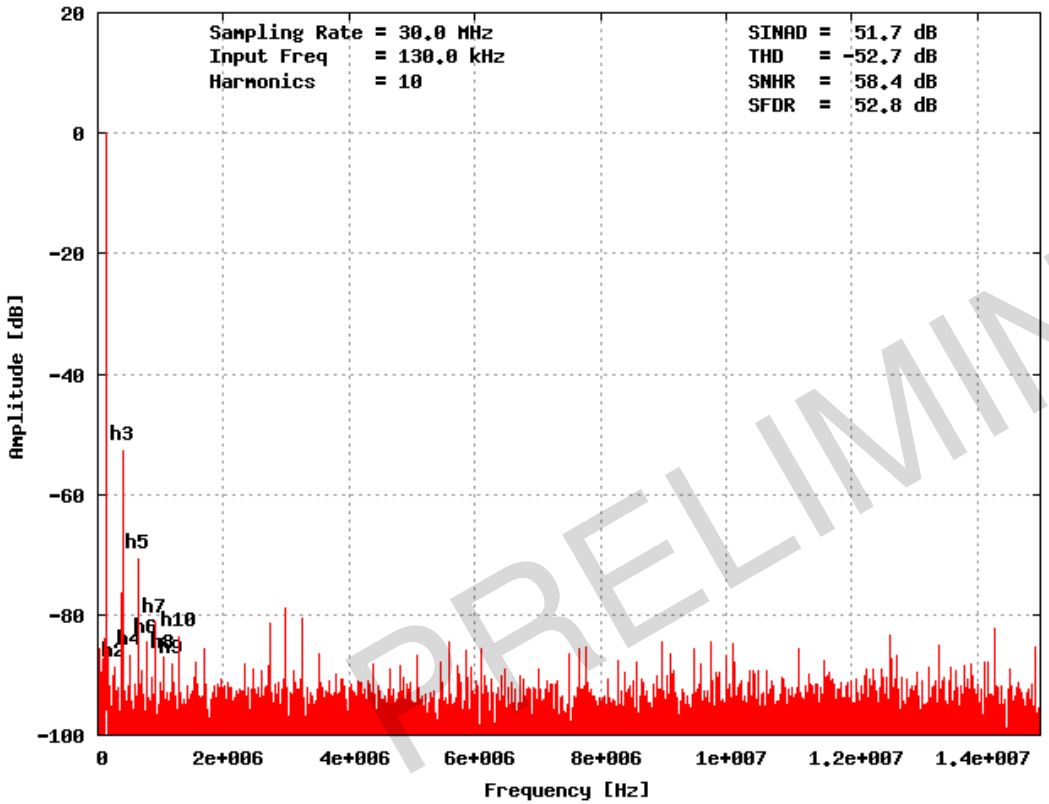


ADC without S/H

Both ADC versions show good differential (DNL<0.5 LSB) and integral linearity (INL<1 LSB)

ADC - Dynamic measurements 30 MHz

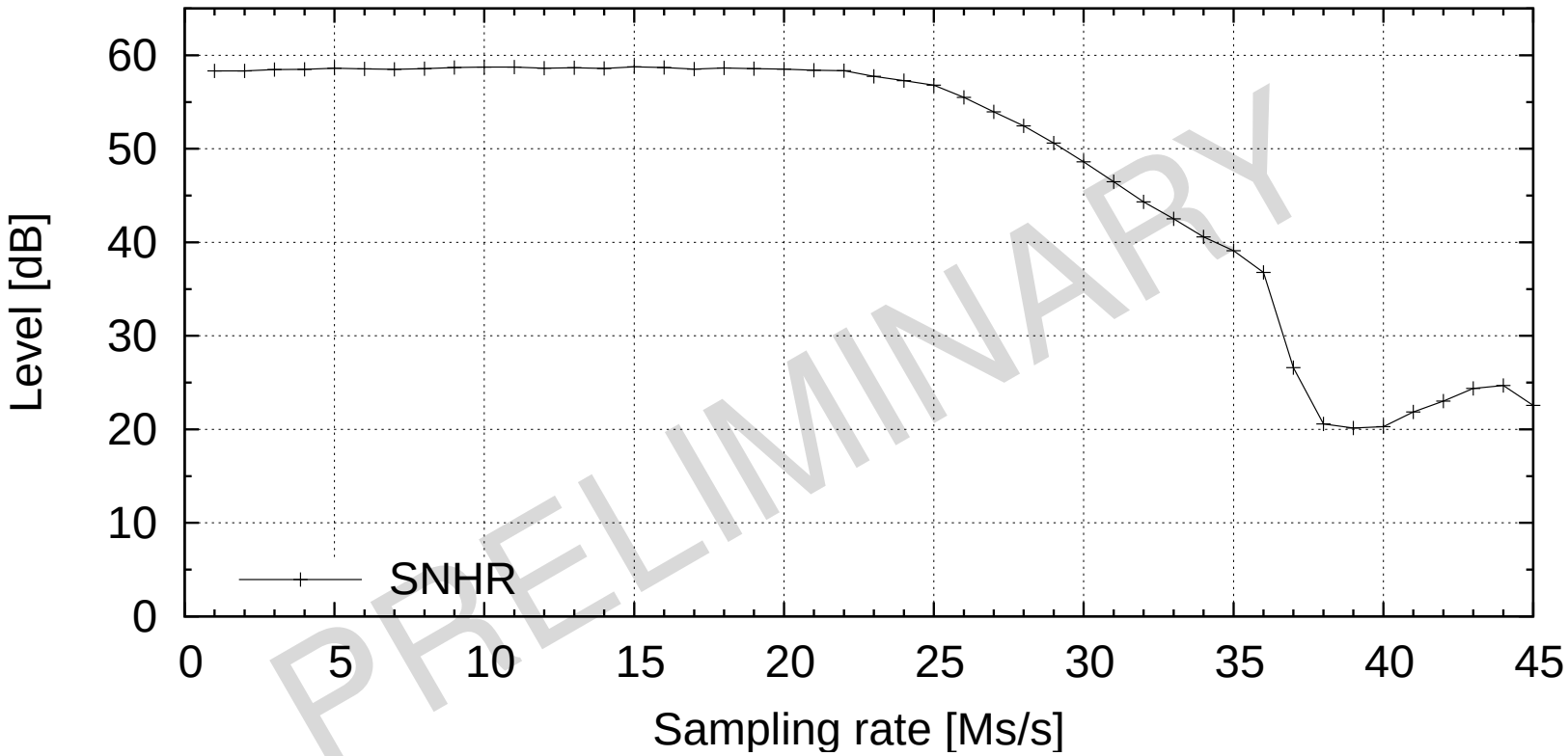
FFT spectre



- SNHR = 58.4 dB (9.4 bits)

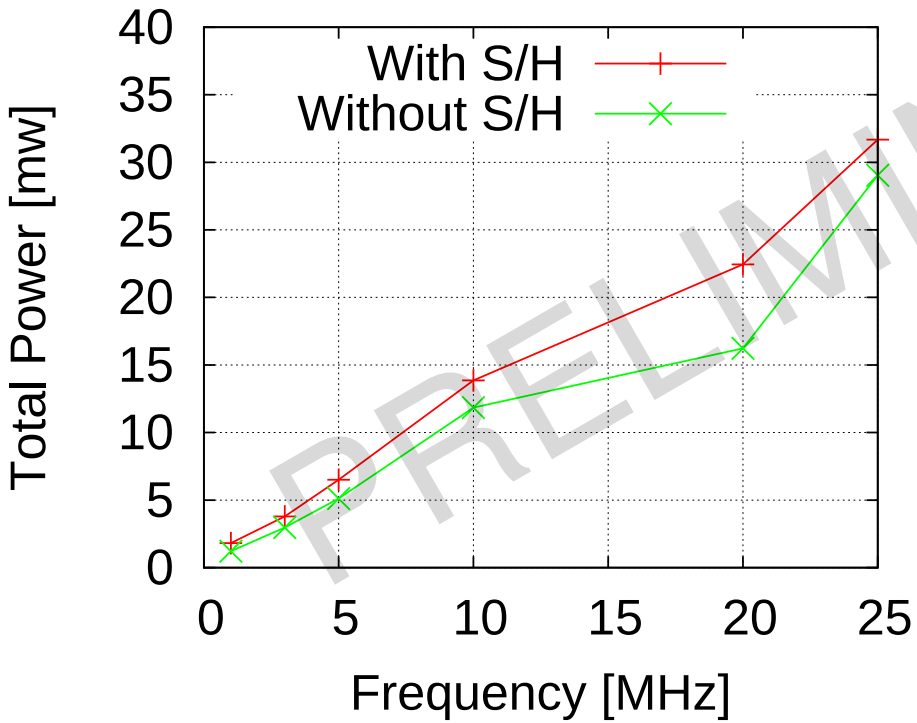
- SNHR (signal to noise) is good
- To measure harmonic distortions the setup needs to be improved (in progress)...

ADC - Dynamic measurements

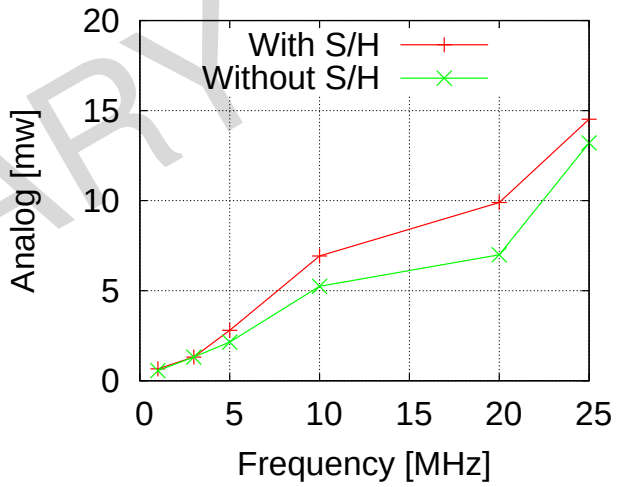


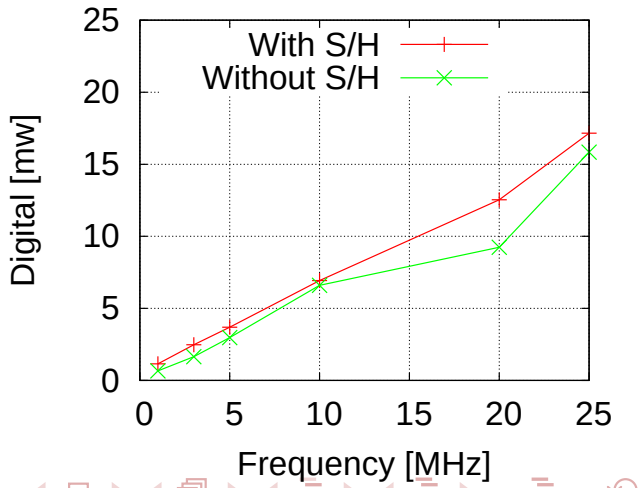
- Good SNHR up to about 25 MHz
- The scan versus input signal frequency f_{in} also needs to be done...

ADC - Power scaling



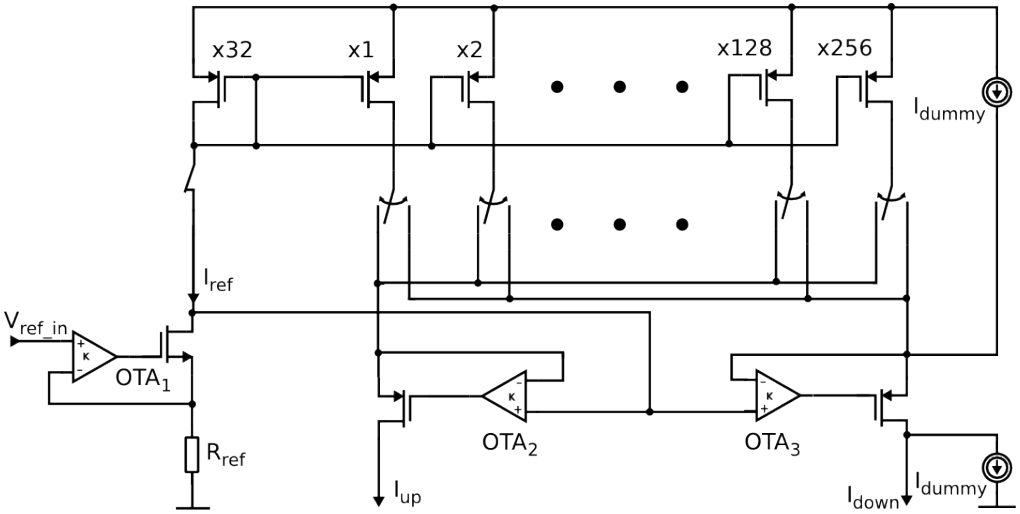
Power consumption scales linearly with sampling frequency

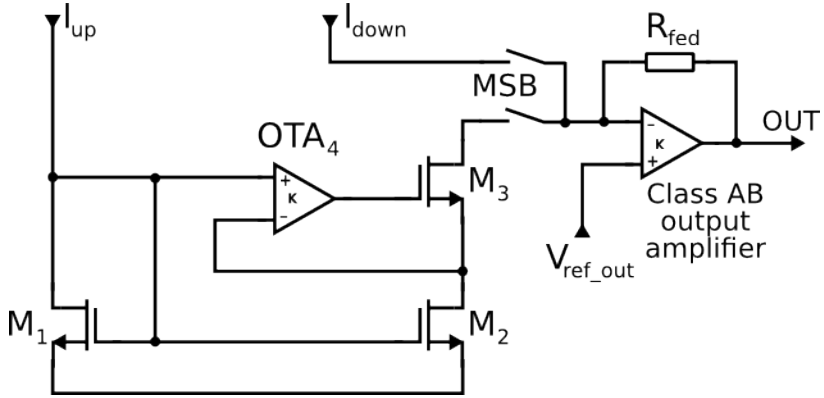




Design of low power 10 bit general purpose DAC

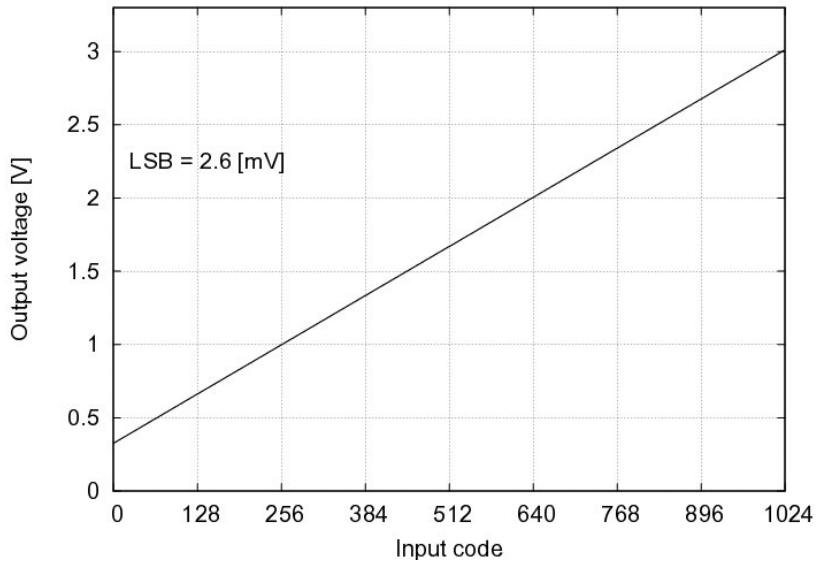
- Current steering architecture
- High-swing voltage output
- Power cons. < 0.6 mW
- Core area 0.18 mm^2

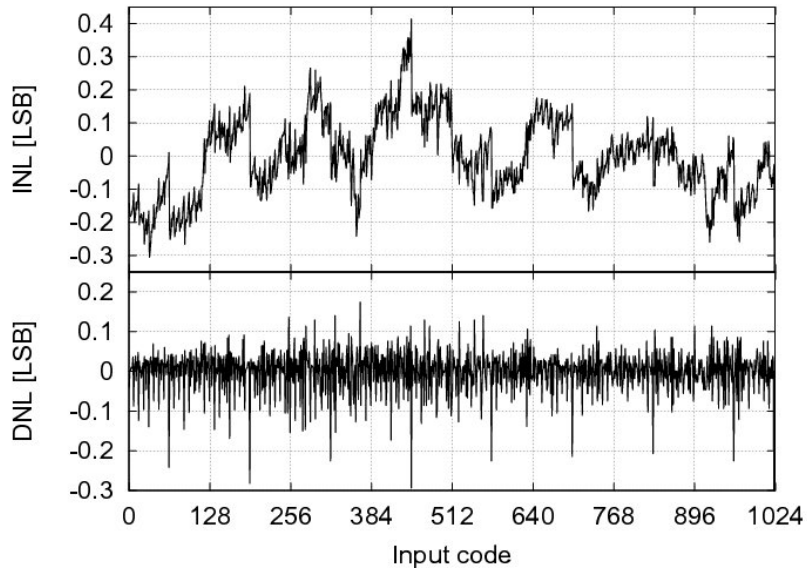




DAC measurements

- DAC fully functional
- Power cons. below 0.6 mW
- max INL < 0.42 LSB
- max DNL < 0.42 LSB
- Efective number of bits ENOB=9.85
- Update rate up to few hundred kHz





Other peripherals

- Bandgap reference voltage and temperature sensor circuit designed, fabricated and just bonded, to be tested...
- Fast (>500 MHz) LVDS transmitter and receiver designed, fabricated and just bonded, to be tested...

Summary - present status

- Front-end ASICs designed, fabricated and matching the specifications
- Front-end 8 channels prototypes ready for tests with sensors, fanout and hopefully for test beam
- New 10-bit piepline ADC prototypes fully functional and preliminary results confirm expectations
- More ADC tests needed (power switching, harmonics, power scaling)
- Very low power 10 bit DAC designed, fabricated and matching the specifications, ready to be used
- Bandgap reference designed and fabricated, to be tested
- Fast LVDS pads designed and fabricated, to be tested

Summary - future plans

- Proceed with tests (ADC, LVDS, bandgap), in progress...
- Tests of the readout chain comprising of sensor, fanout and front-end, in progress...
- Prepare the setup for test beam (as soon as the readout chain will be tested)
- Design and submission of complete multichannel (>=8) ADC, in progress, submission soon...

Digital processing & data concentrator

- Waiting for better detector specification $\rightarrow$ data flux
- Pure digital design so can be done fast in comparison to front-end and ADC
- Will first be designed and tested with FPGA
- After FPGA tests ASIC implementation should be fast (mounth or two)

Test setup (beam) preparation

- Silicon sensors from Hammamatsu ready and preliminary I-V and C-V measurements performed
- First fanout structures designed and fabricated
- Prototype front-end (8 channels) ASICs will be used
- External ADC will be used since the prototype ADC ASIC is not yet multichannel
- PCB board for test setup designed and produced