Overview of special session on Microelectronics

Michael Campbell
CERN – ESE group

EUDET Meeting, Geneva

20 October 2009

Session Agenda

09.30 Paul Aspell	The S-ALTRO Demonstrator (status report)
09.50 Xavi Llopart	News from Medipix3 measurements and impact on Timepix2
10.10 Marek Idzik	Readout electronics for the LumiCal detector
10.30 Kostas Kloukinas	Microelectronics technology support and foundry services at CERN
10.40 Christoph Brezina	Status of Gossipo3
10.55 Discussion	

Session Agenda

09.30 Paul Aspell	The S-ALTRO Demonstrator (status report)
09.50 Xavi Llopart	News from Medipix3 measurements and impact on Timepix2
10.10 Marek Idzik	Readout electronics for the LumiCal detector
10.30 Kostas Kloukinas	Microelectronics technology support and foundry services at CERN
10.40 Christoph Brezina	Status of Gossipo3
10.55 Discussion	

The S-Altro Demonstrator (status report)

An overview and status of the S-Altro Demonstrator project (at CERN).

People :

Luciano Musa … S-Altro Specifications and Architecture
Paul Aspell … Coordinator of demonstrator ASIC design.
Massimiliano De Gaspari ….. Front-end + ADC

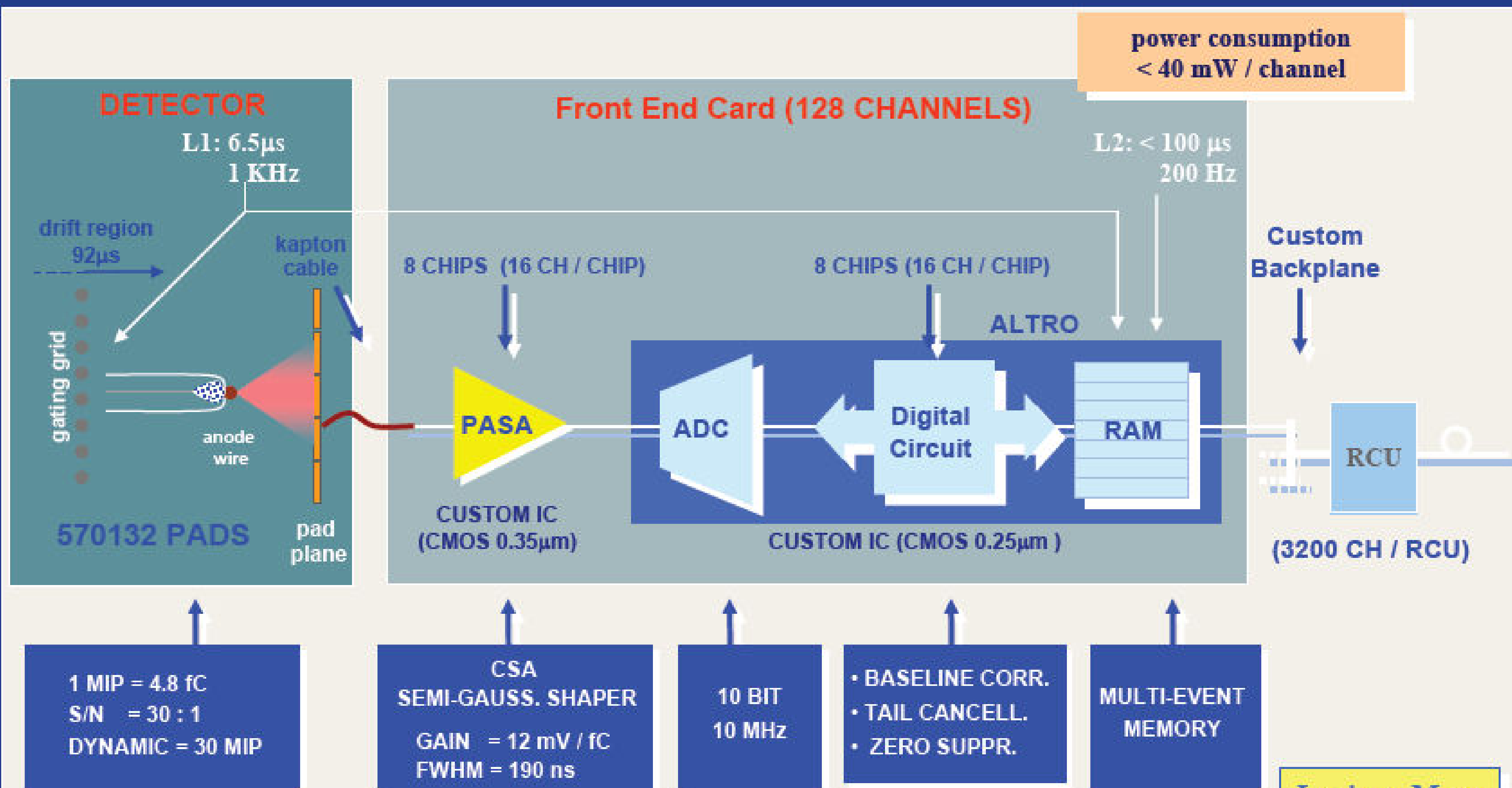
Hugo França-Santos …. ADC
Eduardo Garcia ….. Data Processing & Control

Christian Patauner …. Data compression (now moved to RCU chip)

Presented at the :
EUDET Annual Meeting 2009
Geneva University & CERN, October 19th-21st 2009

S-Altro architecture

Based on the existing PASA + Altro electronics designed for the Alice TPC



SAltro Demonstrator

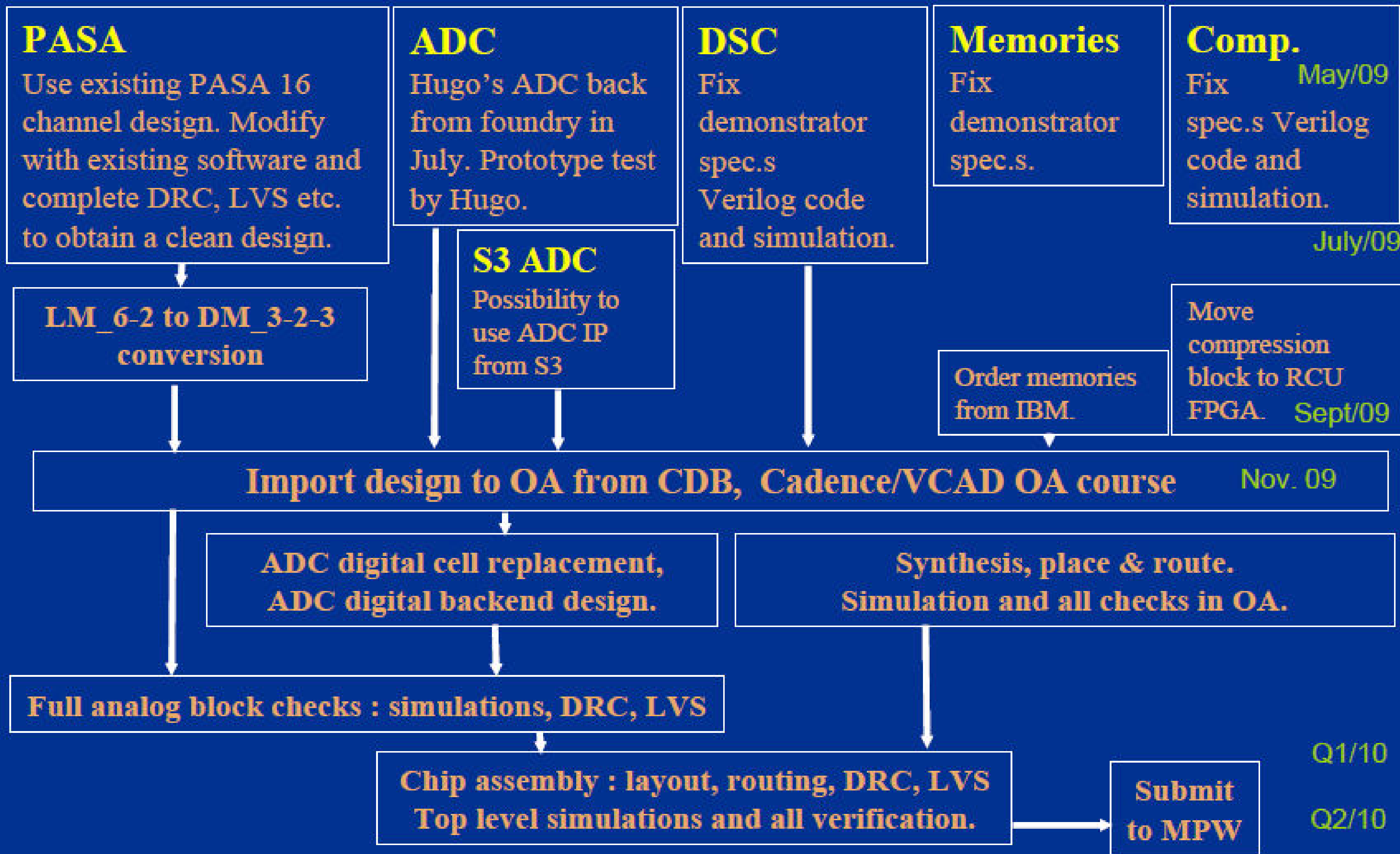
Goal :

To demonstrate integration per channel of an analog front-end, an ADC and digital signal processing in a single chip.

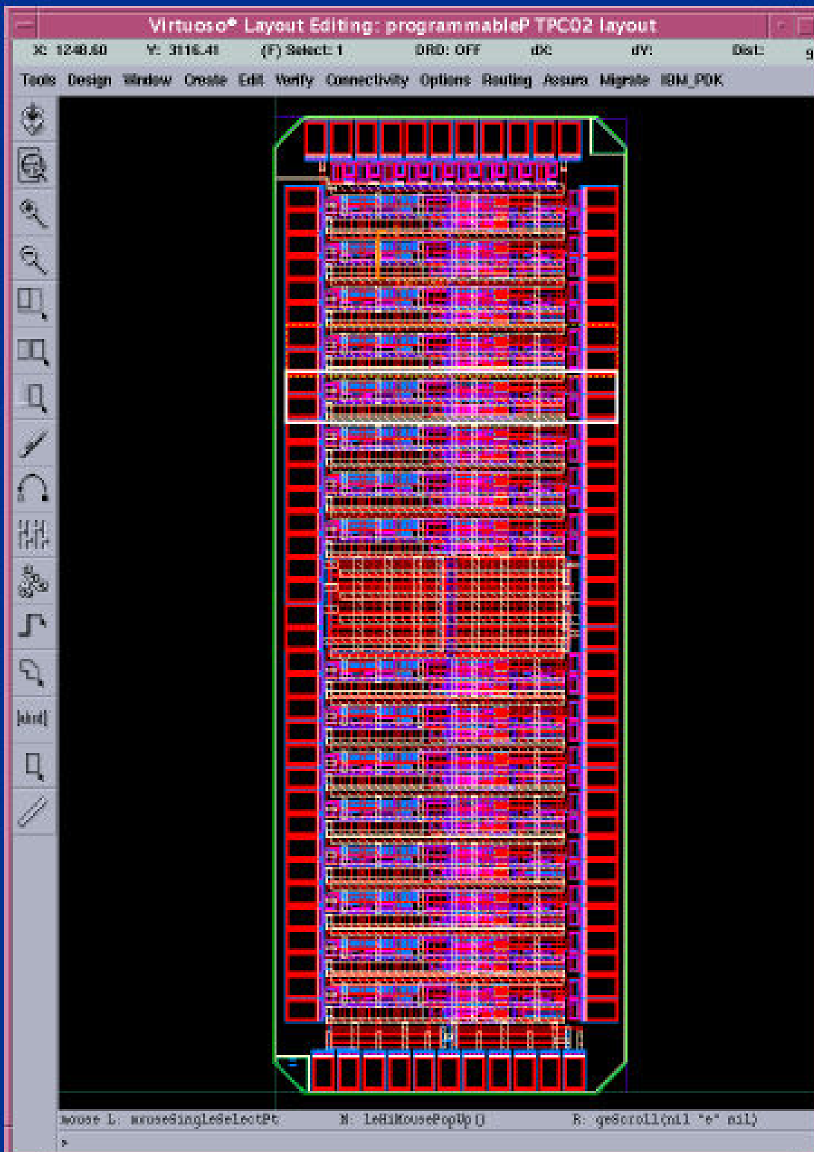
Data processing of 100us of data sampled at 10MHz.

Prepare ideas for TPC readout in the ILC & CLIC

Demonstrator work flow



PASA prototypes ; PCA 16

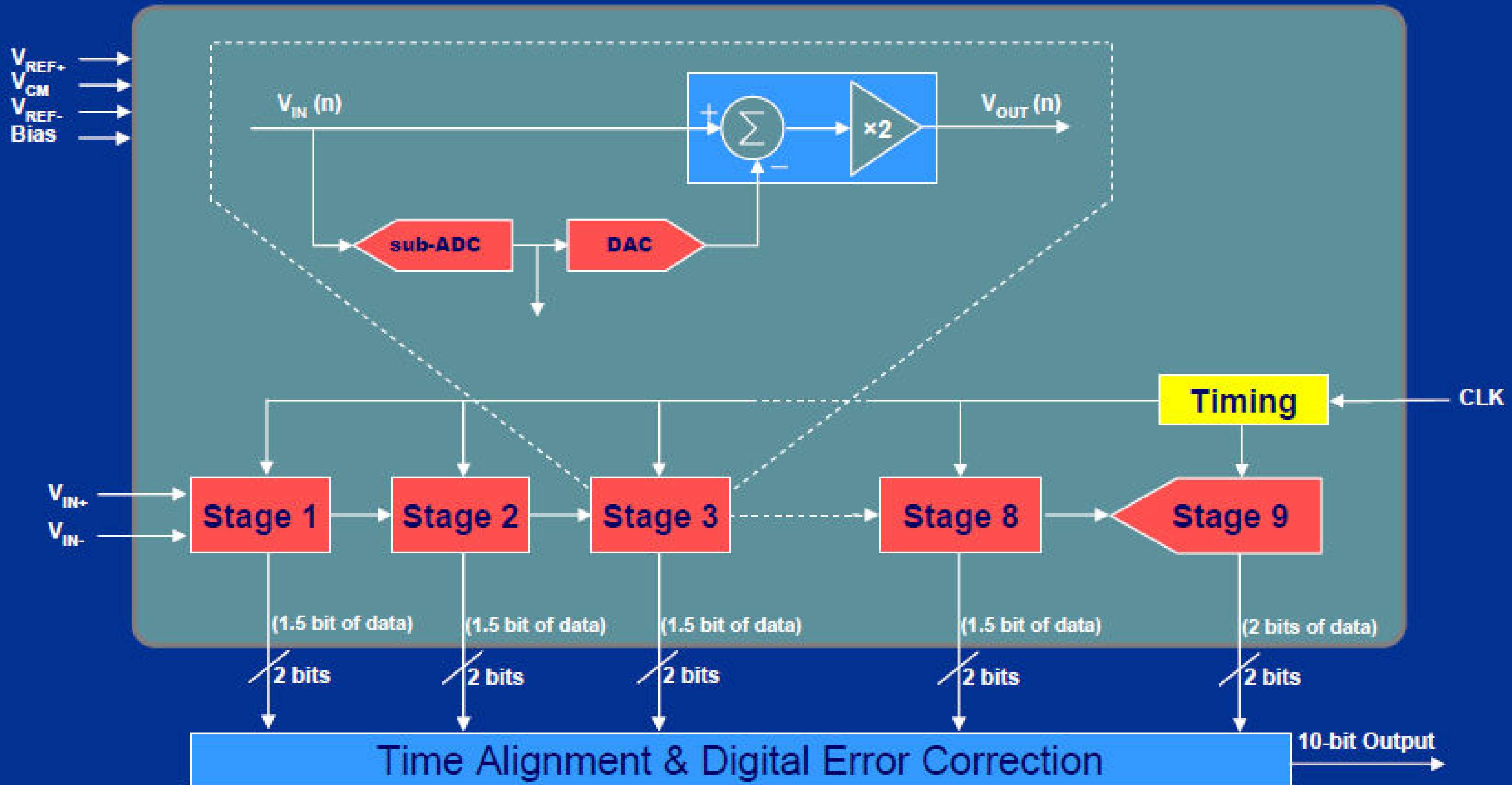


Programmable Charge Amplifier d shaper (PCA 16)

- 1.5 V Supply, power consumption , 8 mW / channel
- 16 channel charge amplifier + shaper
- Single ended preamplifier
- Fully differential output amplifier
- Both signal polarities
- Programmable peaking time (30 ns – 120 ns) – 3rd order semi Gaussian pulse shape
- Programmable gain in 4 steps (12 – 27 mV/fC)
- Pre-amp_out mode
- Tunable time constant of the preamplifier
- Pitch 190.26um, Channel length 1026um,
- Chip dimensions = 1.5mm x 4mm

Design by Gerd Trampitsch

10-bit 40MS/s Pipelined ADC



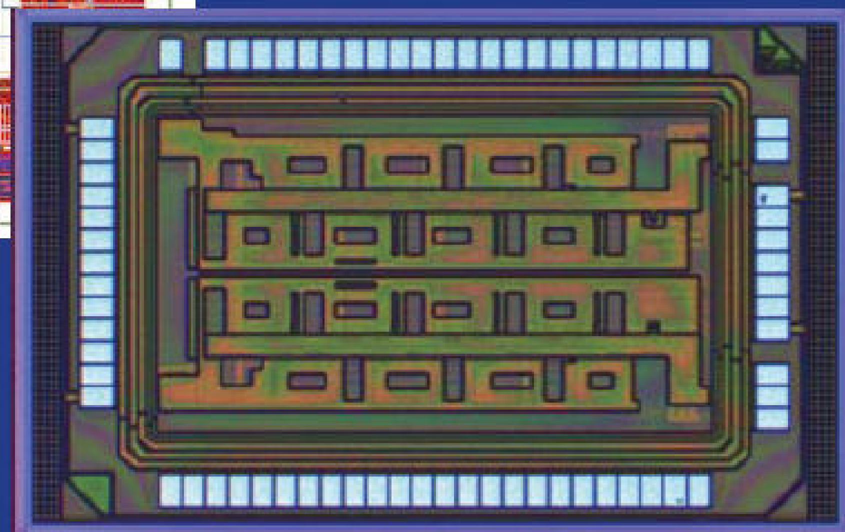
2 identical channels in the prototype.

Hugo França-Santos

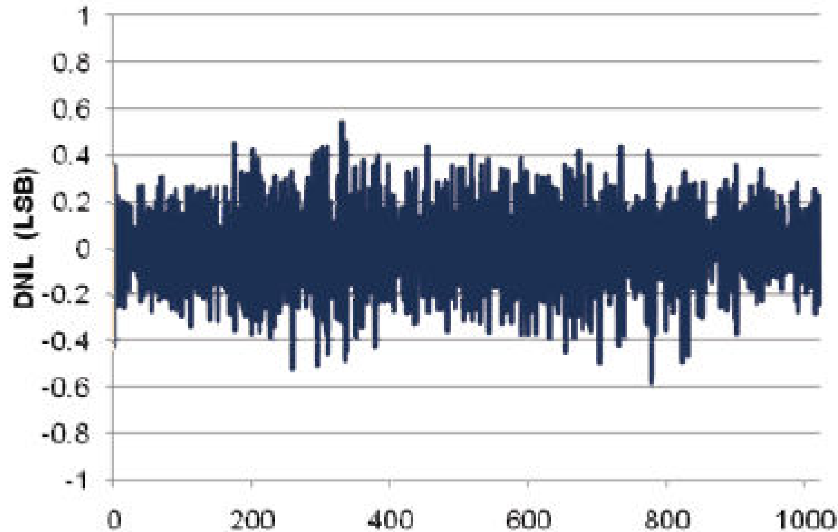
Pipelined ADC: 2-Channel Prototype Layout

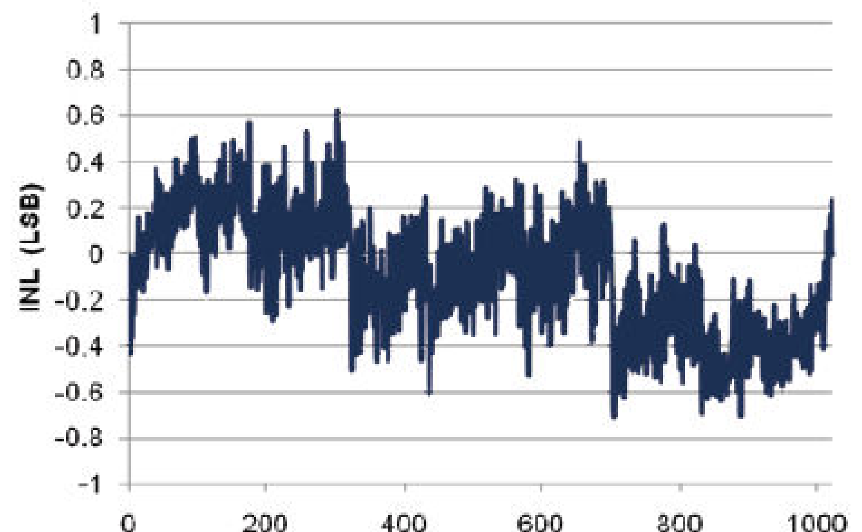
Single ADC area $1.57 \times 0.45 = 0.7\ mm^2$
Prototype area $2.35 \times 1.6 = 3.76\ mm^2$

Hugo França-Santos



ADC TEST: Static Characterization



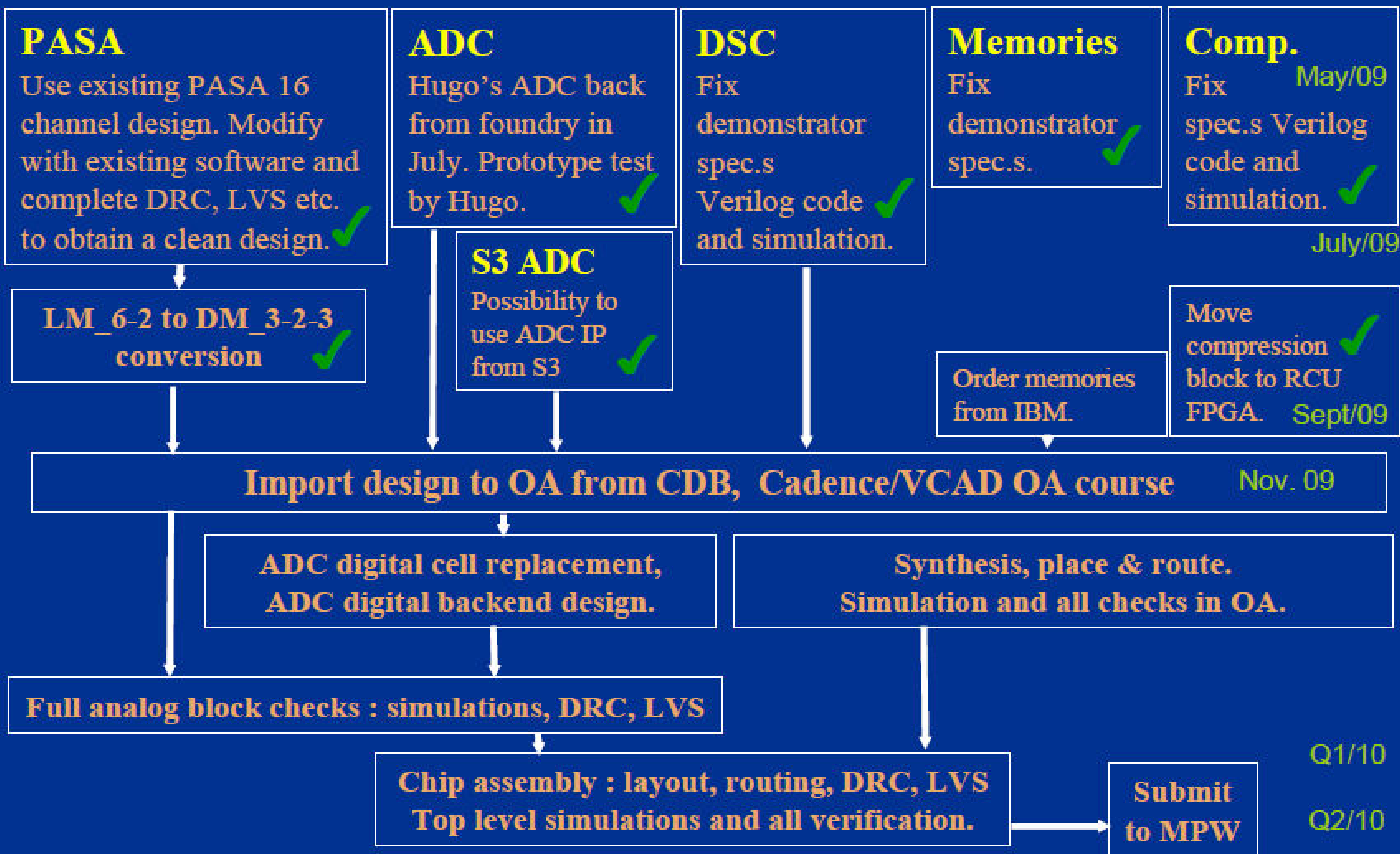


	DNL	INL
MAX	0.54	0.62
MIN	-0.58	-0.71

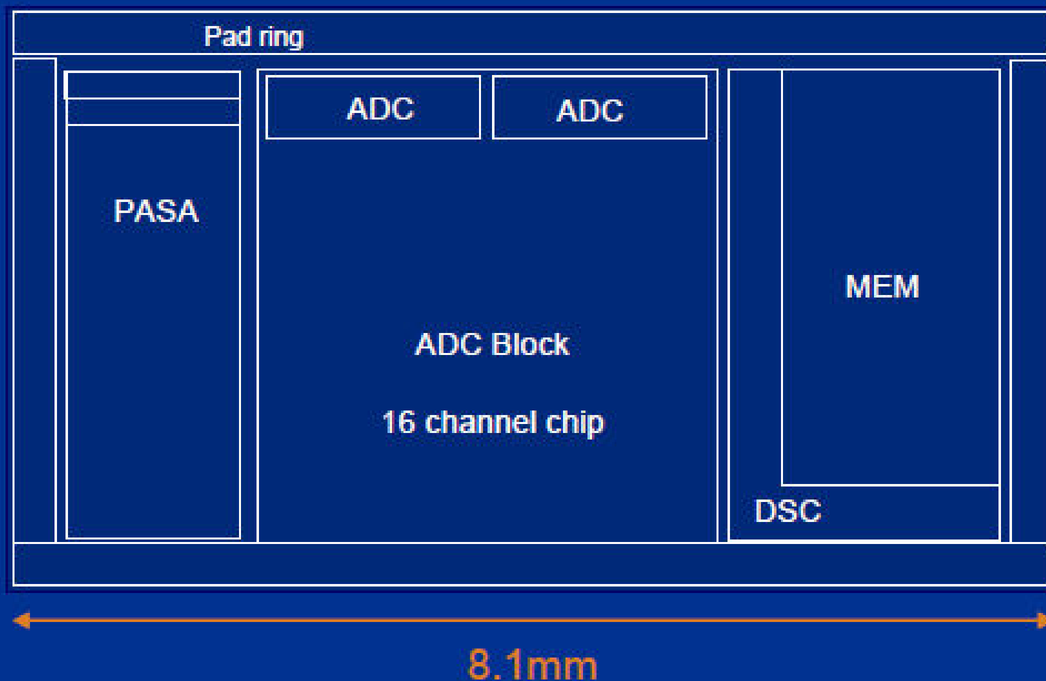
A 10-bit 40MS/s Pipelined ADC in a 0.13µm CMOS Process – TWEPP 2009

Hugo França-Santos

Demonstrator work flow



Demonstrator floor plan



DSC
16 channels = 1.8mm^2.

Control 0.06mm^2

MEM
DSC look-up tables ~ 1kByte/ch.
(10 bits wide),
MEB = 1kByte/ch. (40 bit wide)

~ 6.2mm^2 ± 20% for 16 ch.

DSC + MEM ~ 8mm^2.

PASA channel = 1.4mm x 0.2mm,
16 channels = 1.4mm x 3.6mm (3.2mm + 400um power routing)

ADC = Hugo 1.57mm x 0.45mm,

Session Agenda

09.30 Paul Aspell	The S-ALTRO Demonstrator (status report)
09.50 Xavi Llopart	News from Medipix3 measurements and impact on Timepix2
10.10 Marek Idzik	Readout electronics for the LumiCal detector
10.30 Kostas Kloukinas	Microelectronics technology support and foundry services at CERN
10.40 Christoph Brezina	Status of Gossipo3
10.55 Discussion	

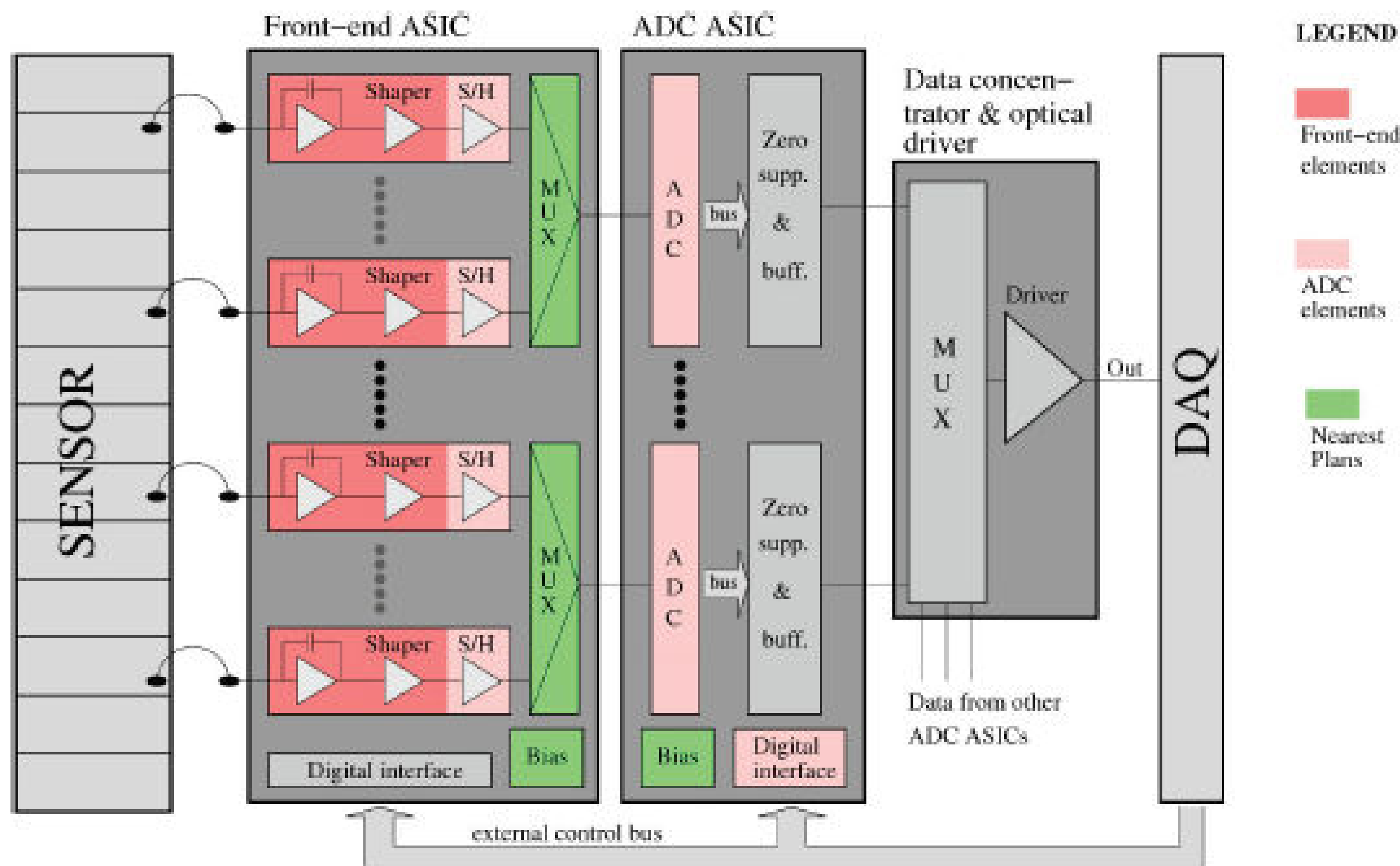
Readout electronics for LumiCal detector

M. Idzik for FCAL Collaboration

Department of Physics and Applied Computer Science
AGH University of Science and Technology, Krakow

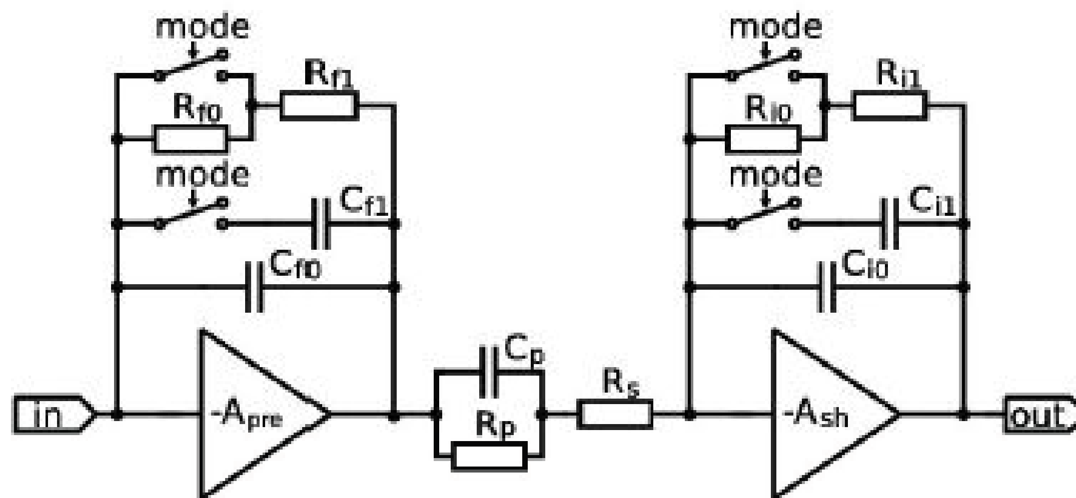
EUDET meeting 19-21 October 2009

LumiCal Readout System



Present developments done in 0.35 μm CMOS technology, not necessarily final choice...

Front-end requirements (old)



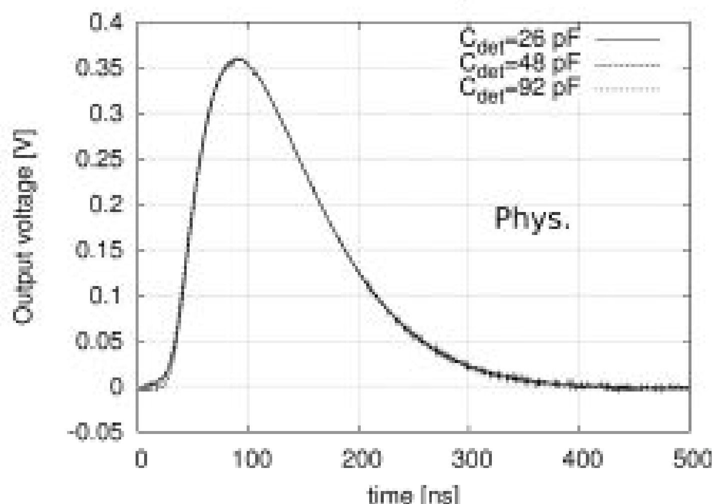
Components

- Charge amplifier
- Pole zero cancellation
- 1st order shaper

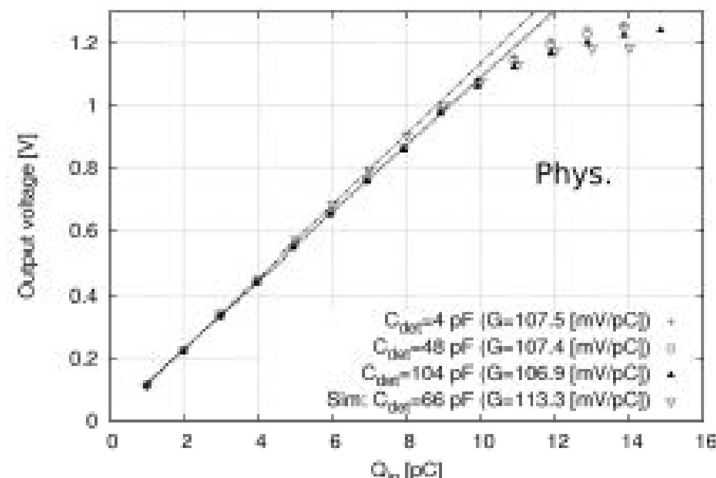
- $C_{det} = 10 \div 100$ pF $\rightarrow$ charge sensitive amplifier
- $\Delta t_{bunch} \simeq 300$ ns $\rightarrow T_{peak} \simeq 60$ ns
- Two independent modes: physics and calibration (MIP) $\rightarrow$ switched gain in preamplifier and shaper
- Physics mode: $Q_{max} \approx 10$ pC $\rightarrow C_f \approx 10$ pF
- Calibration mode: $S/N > 10$ for MIP requested

Front-end measurements

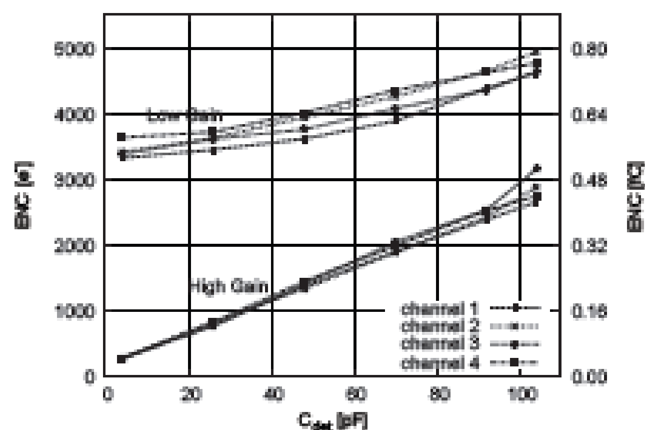
Pulse shape



Gain



Noise



- Prototype 8 channels ASIC produced
- 4 channels with resistive (R_f) and 4 with MOS feedback in preamplifier
- Both versions fully functional
- Front-end linear up to about 10 pC, works with C_{det} up to about 1000 pF

Front-end parameters summary

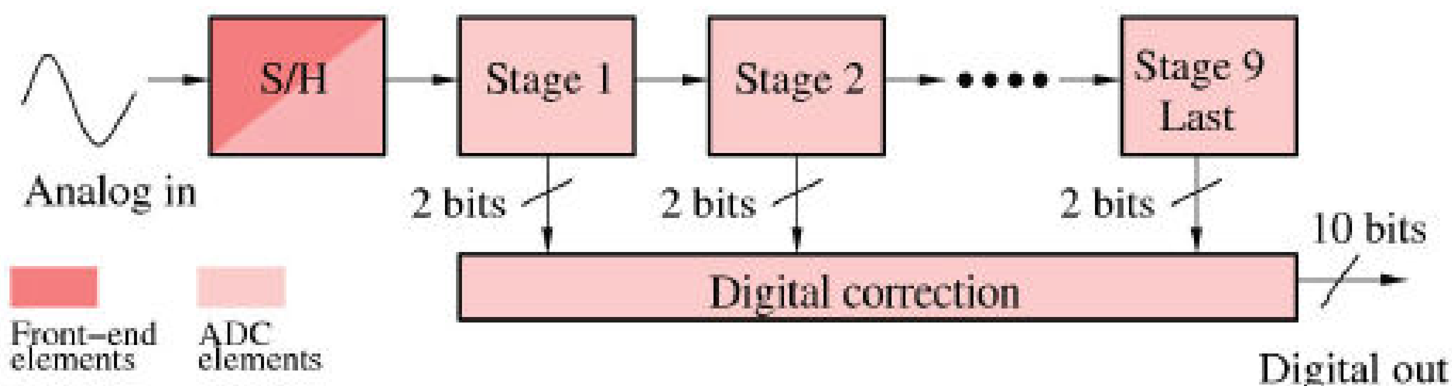
Mode	Gain [mV/fC]	Noise@50pF [fC]	Linearity [pC]	Rate [MHz]	Crosstalk [%]
Physics	0.107	0.62	10	3	≈1
Calibration	≈20	0.28	0.035	3	≈0.1

- Similar results for both R_F and *MOS* configurations (MOS slightly better)
- Crosstalk needs to be measured with sensor fanout
- Power consumption per channel is 8.9 mW
- Noise in details:
  - $\mathrm{Noise_{phys}[el]} = 3300 + 13 \cdot C_{in}\mathrm{[pF]}$
  - $\mathrm{Noise_{cal}[el]} = 170 + 26 \cdot C_{in}\mathrm{[pF]}$

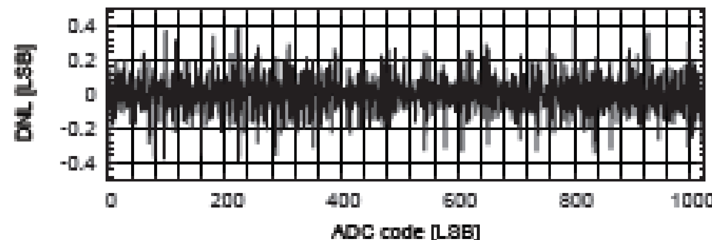
M. Idzik, Sz. Kulis, D. Przyborowski, "Development of front-end electronics for the luminoisty detector at ILC" Nucl. Instr. and Meth. A 608 (2009) pp.169-174

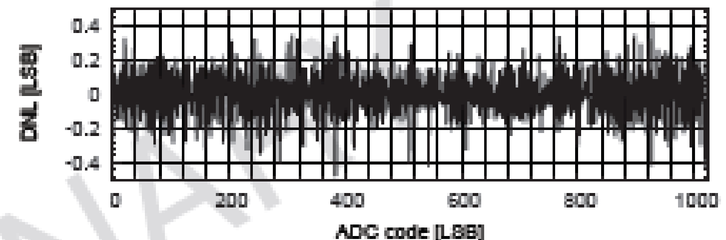
ADC Requirements and archirecture

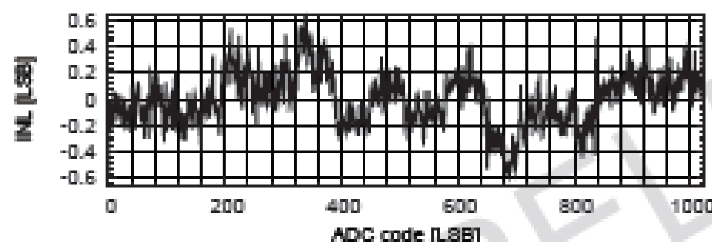
- 10 bit resolution
- Sampling frequency 3-30 MHz (depending on number of FE channels per ADC)
- With and without S/H (S/H can be a part of front-end)
- Power efficient, power and clock ON/OFF
- Fully differential pipeline architecture



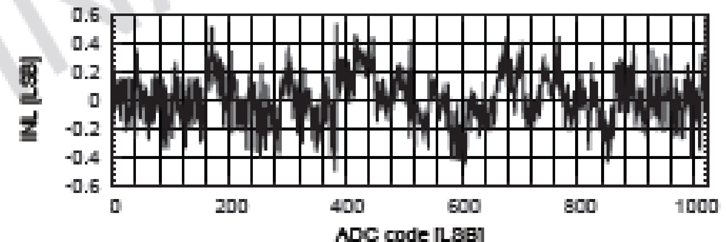
ADC - Linearity







ADC with S/H

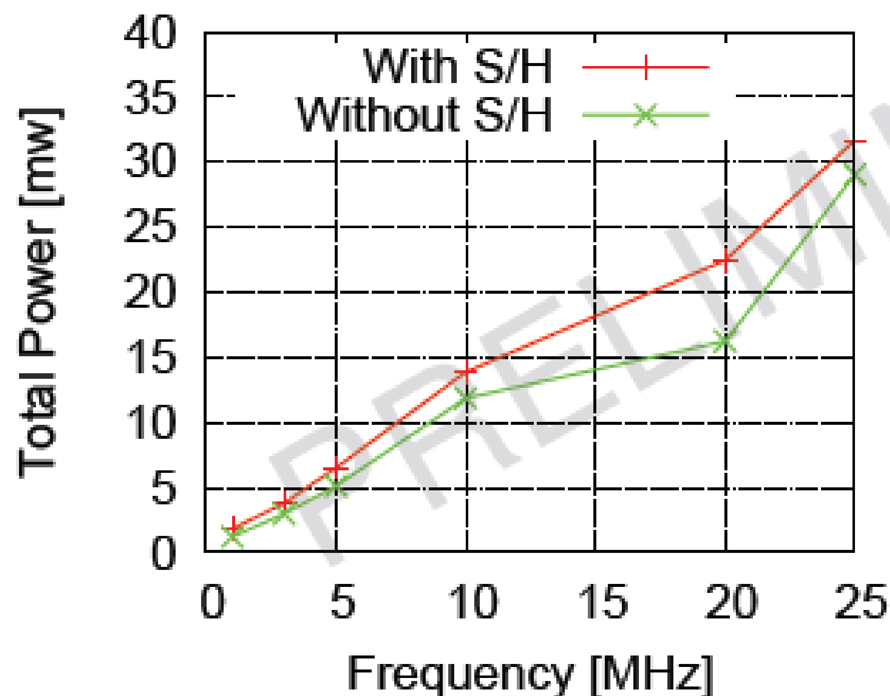


ADC without S/H

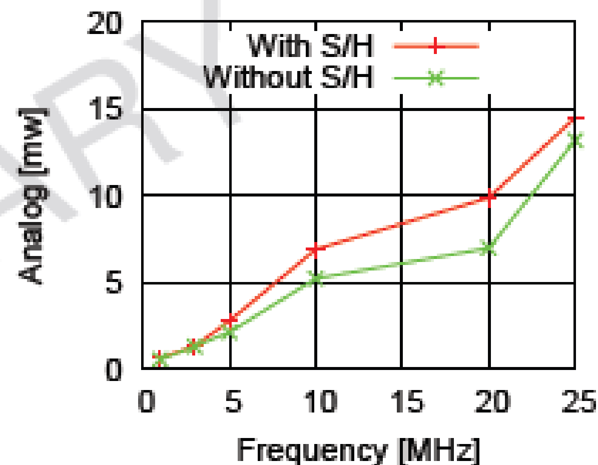
PRELIMINARY

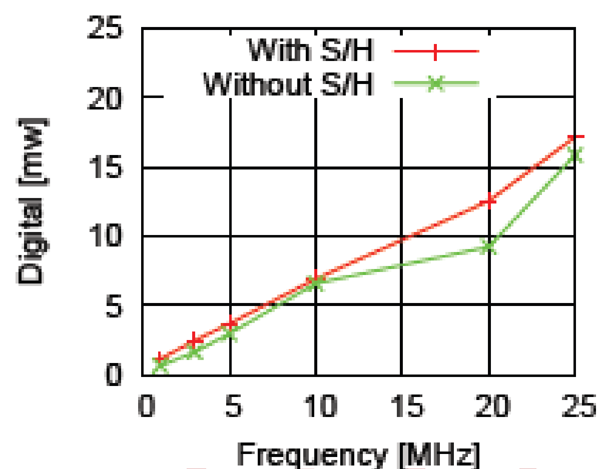
Both ADC versions show good differential (DNL<0.5 LSB) and integral linearity (INL<1 LSB)

ADC - Power scaling



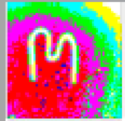
Power consumption scales linearly with sampling frequency





Session Agenda

09.30 Paul Aspell	The S-ALTRO Demonstrator (status report)
09.50 Xavi Llopart	News from Medipix3 measurements and impact on Timepix2
10.10 Marek Idzik	Readout electronics for the LumiCal detector
10.30 Kostas Kloukinas	Microelectronics technology support and foundry services at CERN
10.40 Christoph Brezina	Status of Gossipo3
10.55 Discussion	



NEWS FROM MEDIPIX3 MEASUREMENTS AND IMPACT ON TIMEPIX2

X. Llopart
CERN

Medipix3 Introduction

Medipix3 introduction
Chip description
Electrical characterization summary
Towards Medipix3 Si assemblies
Conclusions
Towards Timepix2

- Medipix3 builds on the success of Medipix2 as a single photon counting imaging chip

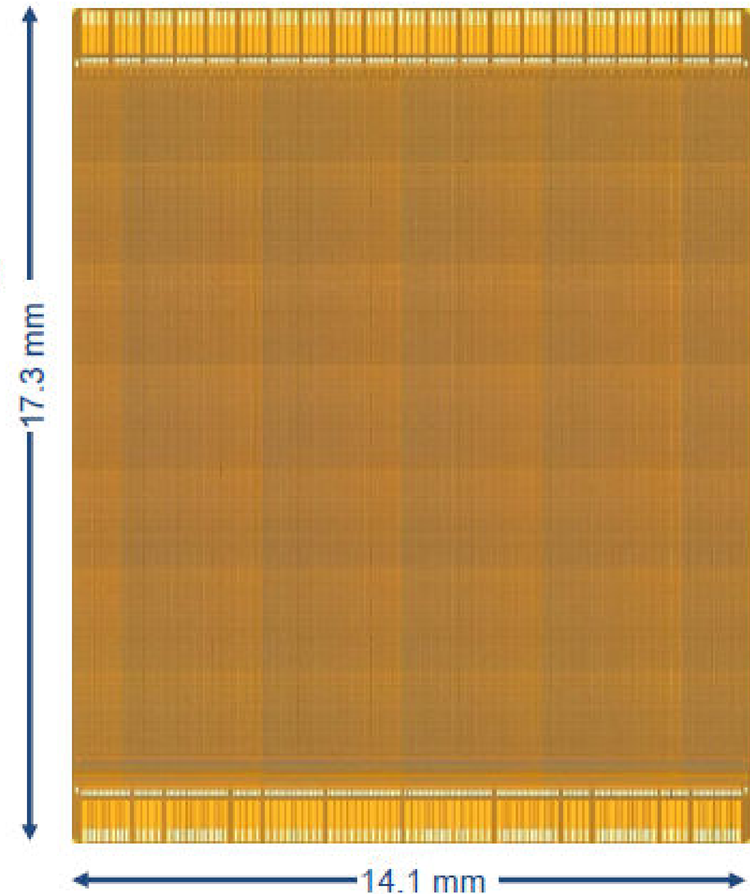
- Added Features
  - Analogue charge summing to keep all charge information
  - Spectroscopic mode with 8 threshold levels
  - Continuous Count-Read mode (no dead time)
  - 2 programmable depth binary counters (variable dynamic range)
  - Flexible readout scheme (ROI, configurable output port width)
  - Highly configurable

- Designed in a 130nm 8-metal CMOS technology

Medipix3 chip

Medipix3 introduction
Chip description
Electrical characterization summary
Towards Medipix3 Si assemblies
Conclusions
Towards Timepix2

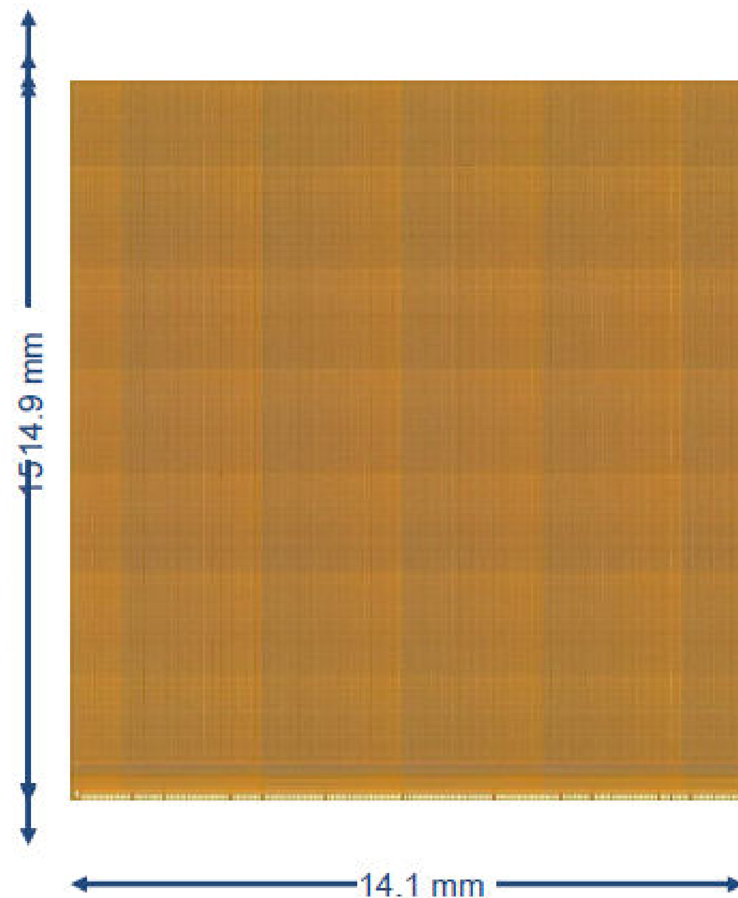
- Pixel matrix of 256 x 256 pixels
- Bottom periphery contains:
  - LVDS drivers and receivers (500 Mbps)
  - Band-Gap and 25 DACs (10 9-bit and 15 8-bit)
  - 32 e-fuse bits
  - EoC and 2 Test pulse generators per pixel column
  - Temperature sensor
  - Full IO logic and command decoder
  - Power/Ground pads
  - TSV landing pads
  - Pads extenders
- Top periphery contains:
  - Power/Ground pads
  - TSV landing pads
  - Pads extenders
- > 115 Million transistors
- Typical power consumption:
  - 600 mW in Single pixel mode
  - 900 mW in Charge summing mode



Multiple dicing options

Medipix3 introduction
Chip description
Electrical characterization summary
Towards Medipix3 Si assemblies
Conclusions
Towards Timepix2

	X [µm]	Y [µm]	Active Area
Medipix2 and Timepix	14111	16120	87.1%
Medipix3 top and bottom WB	14100	17300	81.2%
Medipix3 bottom WB	14100	15900	88.4%
Medipix3 top and bottom TVS	14100	15300	91.9%
Medipix3 bottom TVS	14100	14900	94.3%



Pixel Layout

- Design fully exploits the 130 nm CMOS technology
- ~1600 transistors per pixel

Medipix3 introduction

Chip description

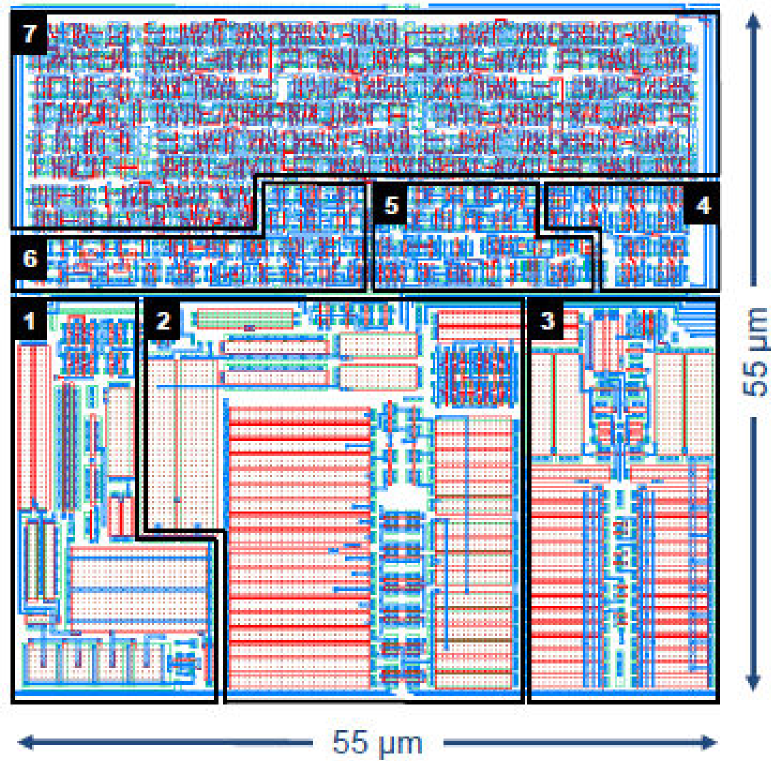
Electrical characterization summary

Towards Medipix3 Si assemblies

Conclusions

Towards Timepix2

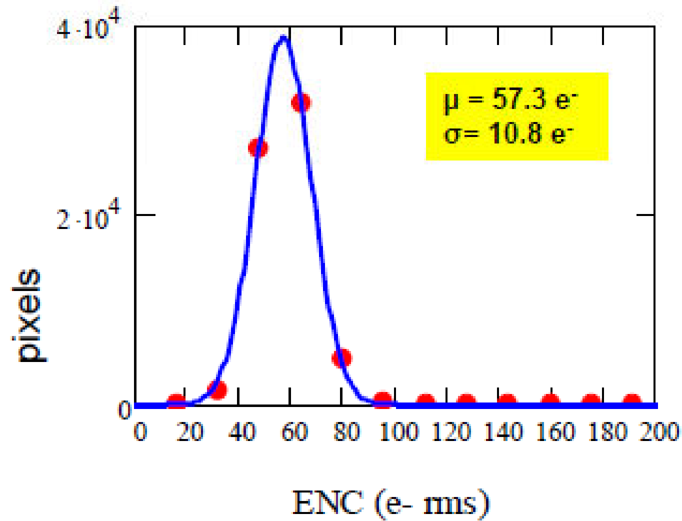
1. Preamplifier
2. Shaper
3. Two discriminators with 5-bit threshold adjustment
4. Pixel memory (13-bits)
5. Arbitration logic for charge allocation
6. Control logic
7. Configurable counter



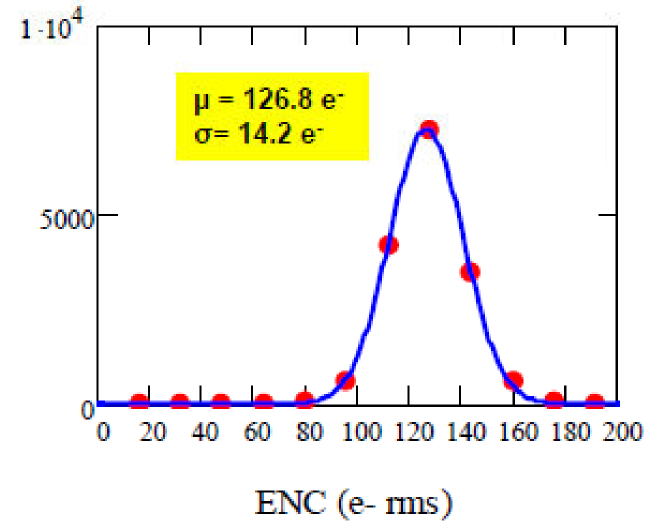
Full chip ENC distribution

Medipix3 introduction
Chip description
Electrical characterization summary
Towards Medipix3 Si assemblies
Conclusions
Towards Timepix2

Single Pixel Mode



Charge Summing Mode
(1/4th of the pixel matrix)



Measurement in charge summing

Medipix3 introduction

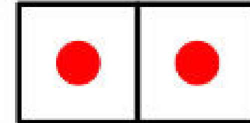
Chip description

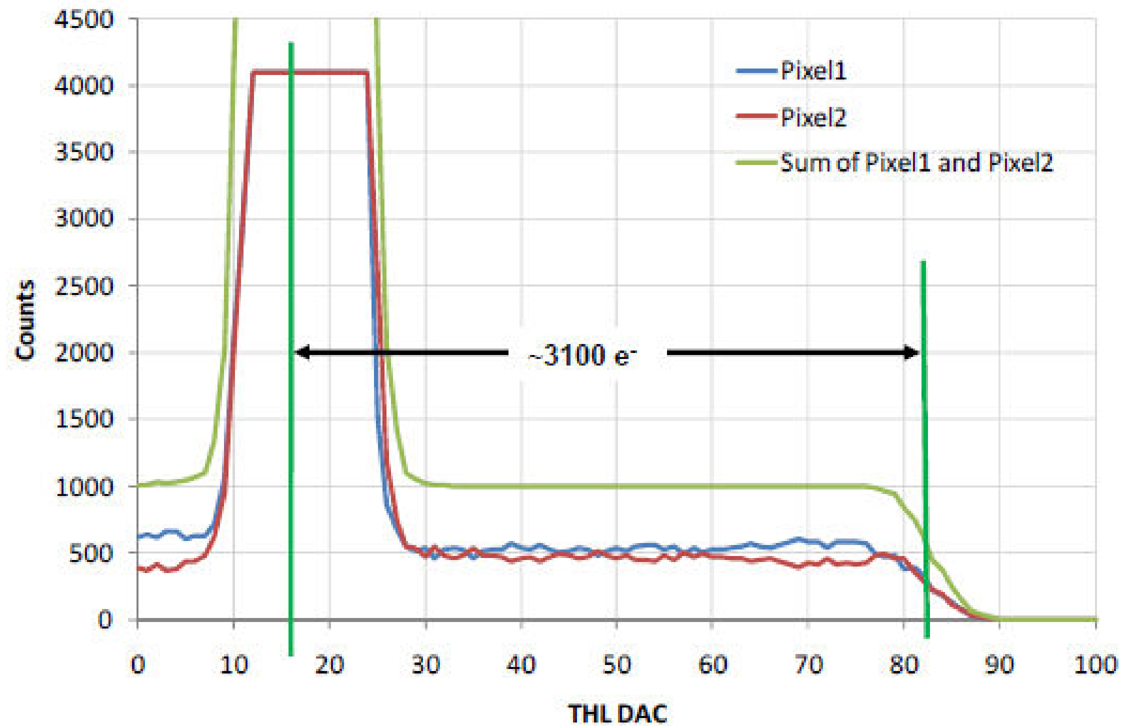
Electrical characterization summary

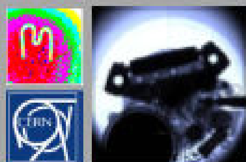
Towards Medipix3 Si assemblies

Conclusions

Towards Timepix2







Towards Timepix2 (I)

Medipix3 introduction

Chip description

Electrical characterization summary

Towards Medipix3 Si assemblies

Conclusions

Towards Timepix2

- Many building blocks used in Medipix3 can be reused for a new chip:
  - Band-Gap and DACs
  - E-fuses
  - LVDS drivers and receivers
- Our design team at CERN is currently studying some ideas for new pixel front-ends (preamplifier and discriminators)
  - improved TOT linearity
  - Temperature robustness
  - Minimize pixel to pixel gain variations
- Also a new PLL is being studied
  - Low power (<500 μW)
  - Multiple output selection up to 100 MHz

Towards Timepix2 (II)

- In the Medipix3 collaboration there is a growing interest in Timepix2
- This development will be funded by the Medipix3 Consortium
- Main specs:
  - Pixel to measure TOT and Arrival time information simultaneously
  - <2ns time resolution
  - Triggered readout
  - Sparse and very fast readout

Medipix3 introduction

Chip description

Electrical characterization summary

Towards Medipix3 Si assemblies

Conclusions

Towards Timepix2

Session Agenda

09.30 Paul Aspell	The S-ALTRO Demonstrator (status report)
09.50 Xavi Llopart	News from Medipix3 measurements and impact on Timepix2
10.10 Marek Idzik	Readout electronics for the LumiCal detector
10.30 Kostas Kloukinas	Microelectronics technology support and foundry services at CERN
10.40 Christoph Brezina	Status of Gossipo3
10.55 Discussion	

GOSSIPO 3

A front-end pixel chip prototype for read-out of MPGDs

Christoph Brezina[1], Klaus Desch[1], Harry van der Graaf[2], Vladimir Gromov[2], Ruud Kluit[2], Andre Kruth[1], Francesco Zappon[2]

[1] Institute of Physics, University of Bonn

[2] National Institute for Subatomic Physics (NIKHEF), Amsterdam

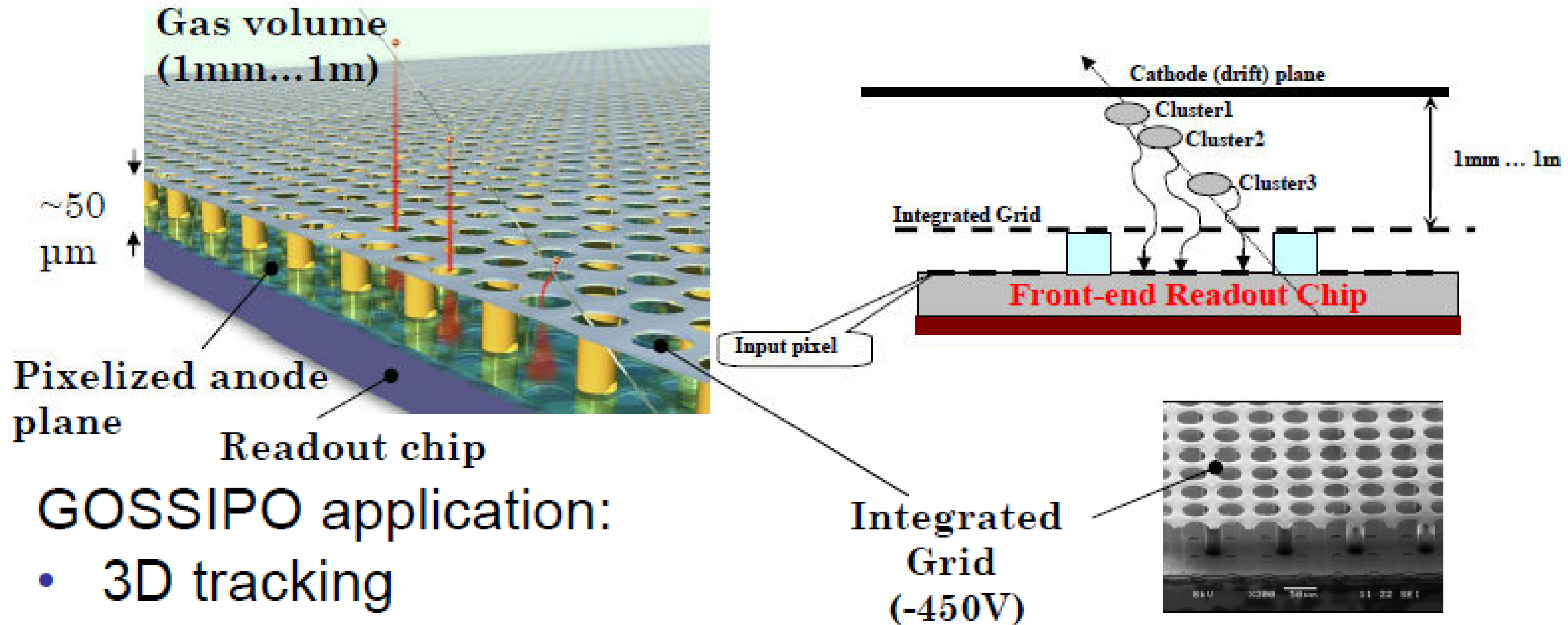
Eudet Anual – Geneva University

October 2009

NIKHEF

universitätbonn

MPGD read-out



GOSSIPO application:

- 3D tracking
- SLHC compatible
- High efficiency of detection of single primary electrons
- High resolution TDC (each pixel)
- Low power

NIKHEF

universität bonn

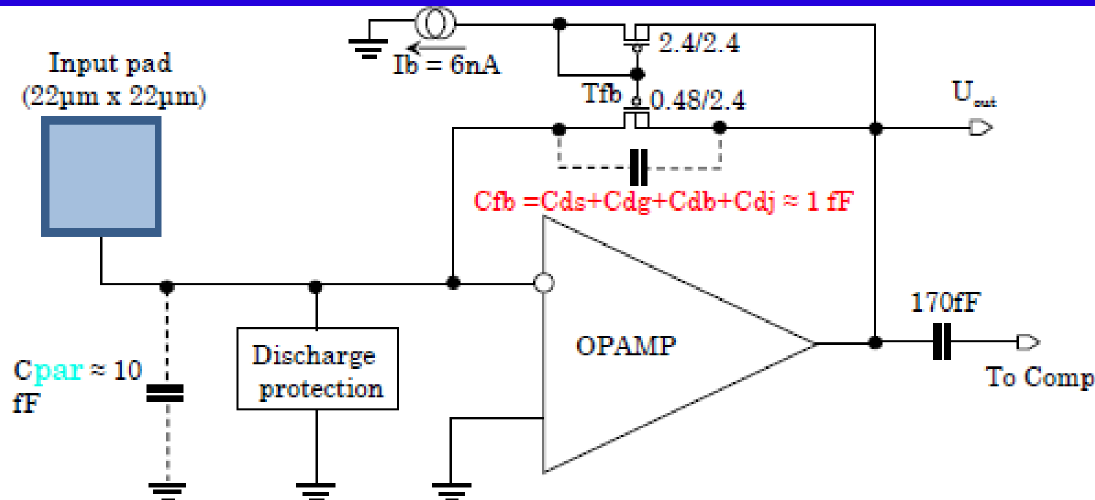
GOSSIPO3: Goals

- Prototype should lead to a chip with:
  - Pixel size ~ 60 x 60 μm^2
  - Accuracy (bin size of TDC) ~1.7ns
  - Drifttime up to 100µs
  - ToT accuracy ~ 200e^- (~ 27ns)
  - ToT up to 6.4µs (~ 28ke^-)
  - Noise ~ 70e^-
  - Rise time 20ns
  - Power consumption < 100mW/cm^2 (~ 3µW/ch)
- Features will be:
  - One of two modes: Time measurement or counting
  - Timemode allows: Hit arrival time & ToT in each pixel simultaneously
  - External trigger
  - First steps towards selftriggering (fast OR from InGrid)

NIKHEF

universitätbonn

Front-end

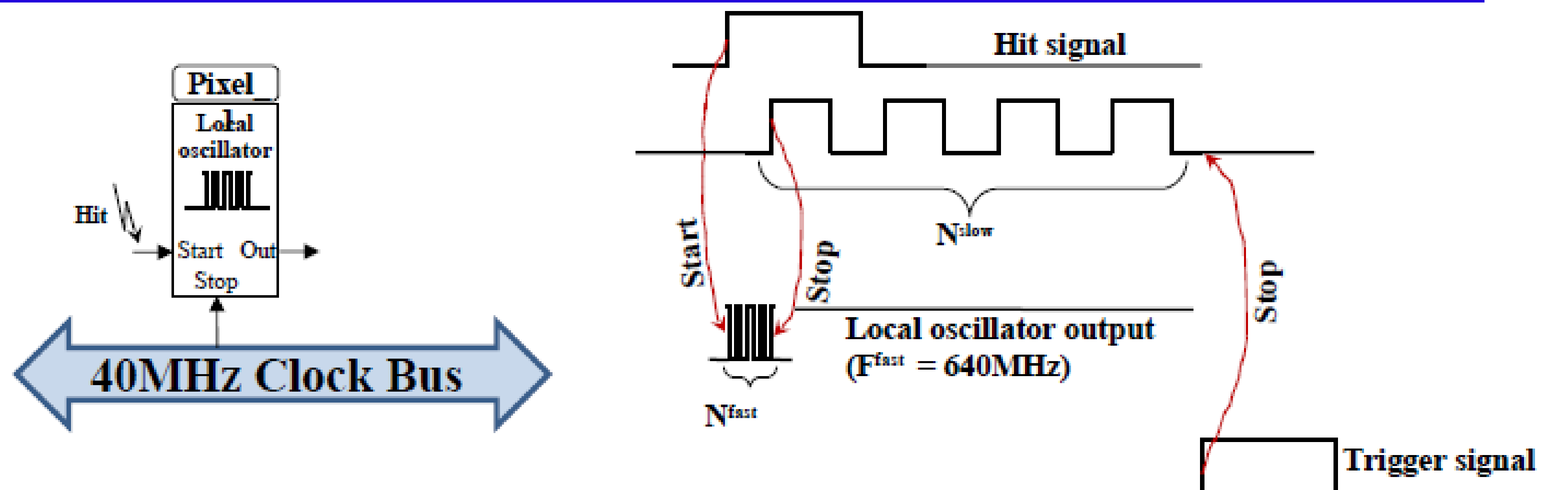


- Low parasitic capacitance (10fF)
- Very small feedback capacitor therefore high gain
- Constant current feedback (1nA)
- Low power consumption (3µW/ch)
- Low noise ($70e^-$)
- Channel to channel threshold spread ~ $70e^-$

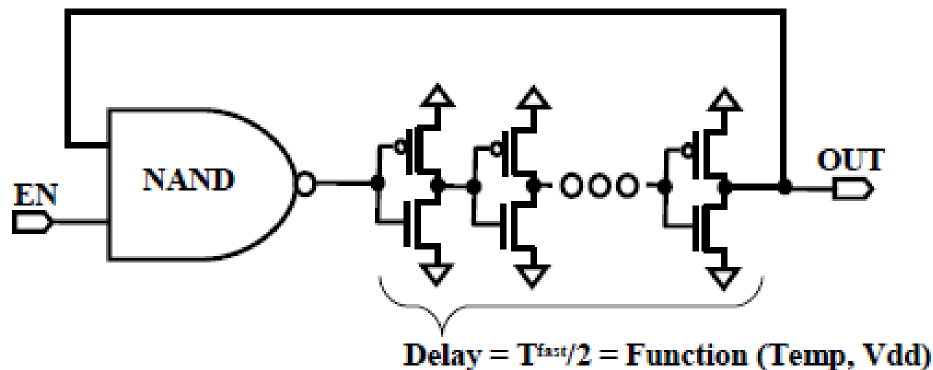
NIKHEF

universitätbonn

TDC with Local fast oscillator



- Time = $N^{slow} / F^{slow} + N^{fast} / F^{fast}$
- Eliminates need for a fast clocknet, reducing:
  - Power needs (relaxed demands to clock buffers & smaller effect of parasitcs)
  - Crosstalk

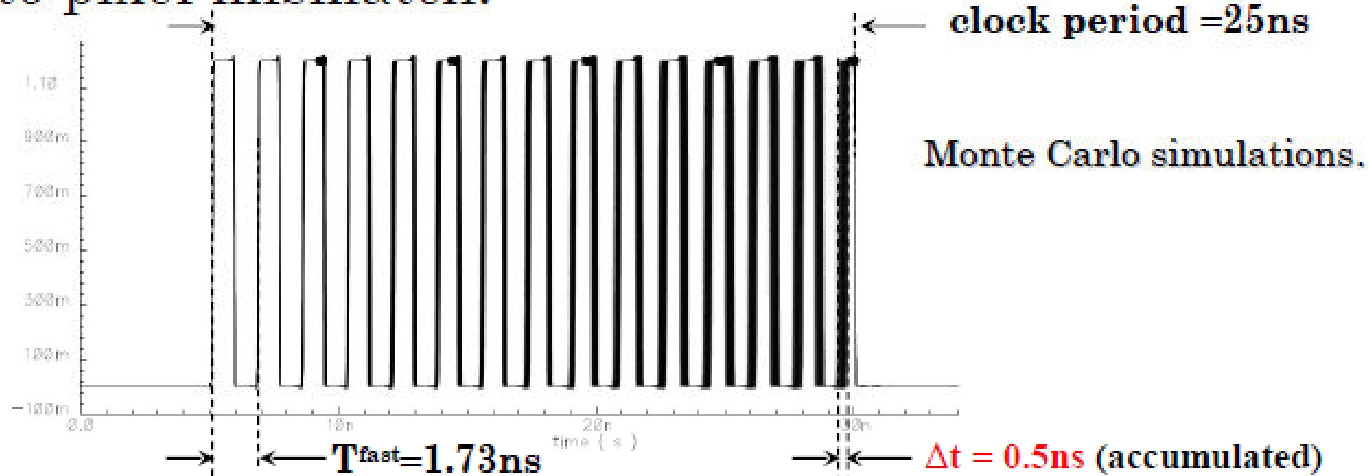


NIKHEF

universitätbonn

Matching issues

- Pixel to pixel mismatch:



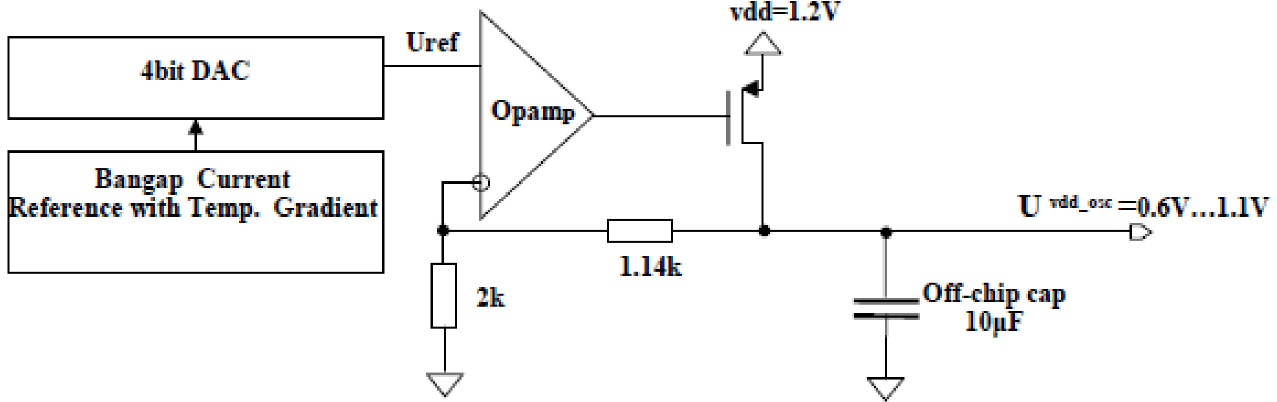
- Process variation (wafer to wafer mismatch)

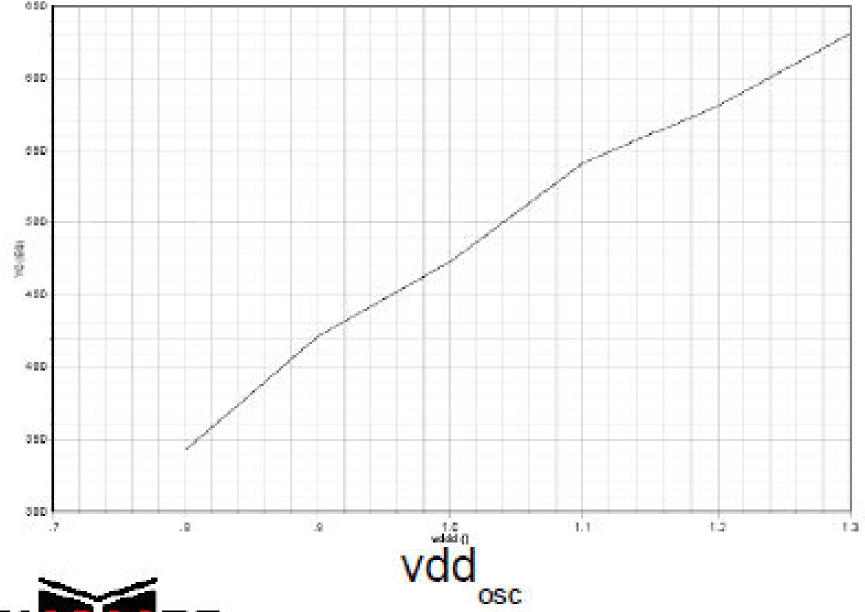
vdd_osc	nominal	lower limit	upper limit
0.61 V		1.72 ns	
0.76 V	1.73 ns	1.13 ns	2.26ns
1.1 V			1.72 ns

NIKHEF

universität bonn

Onchip LDO





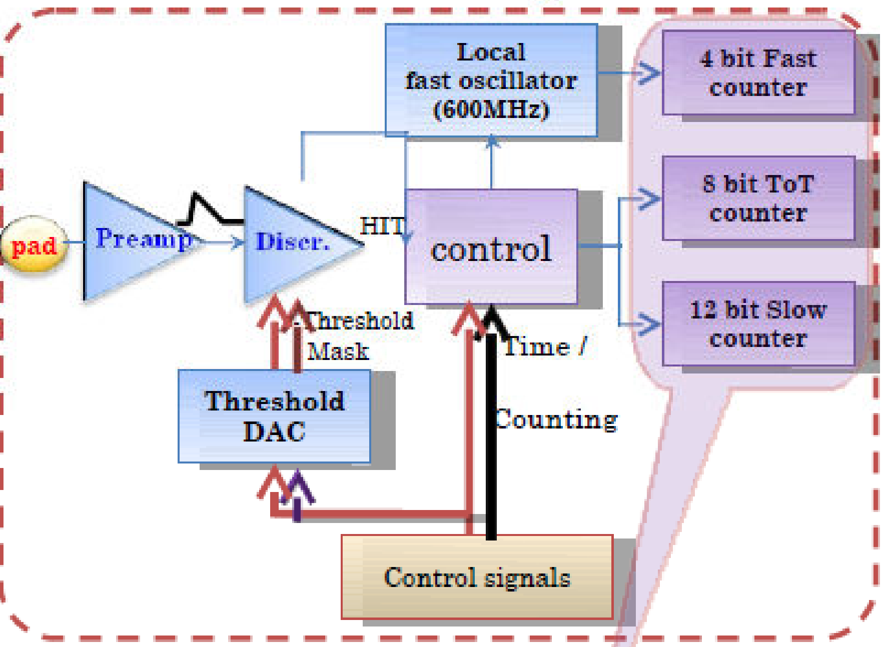
- VDD adjustment allows frequency tuning for all fast oscillators on the chip
  - This can compensate die to die frequency mismatch
  - Pixel to Pixel mismatch is negligible (no Pixel tuning needed)
  - Temperature effects may be compensated via reference voltage

NIKHEF

universitätbonn

The Pixel

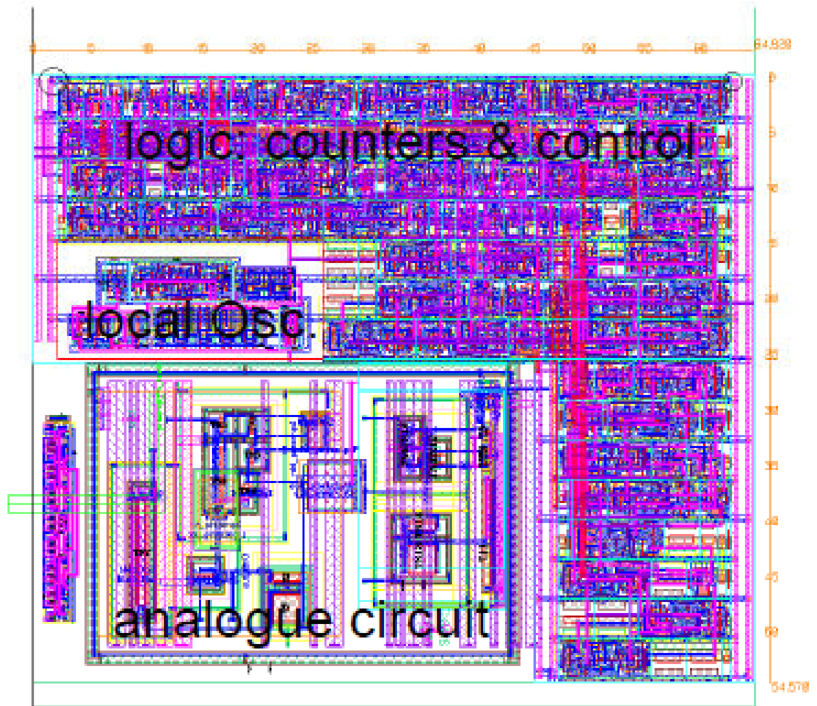
Block diagram



Control signals
- *Slow clock*
- *TRIGGER (common stop)*
- *TOKEN*
- *RESET*

LFSR = Counters (data taking)
or
LFSR = Shift registers (data read-out)

Layout



NIKHEF

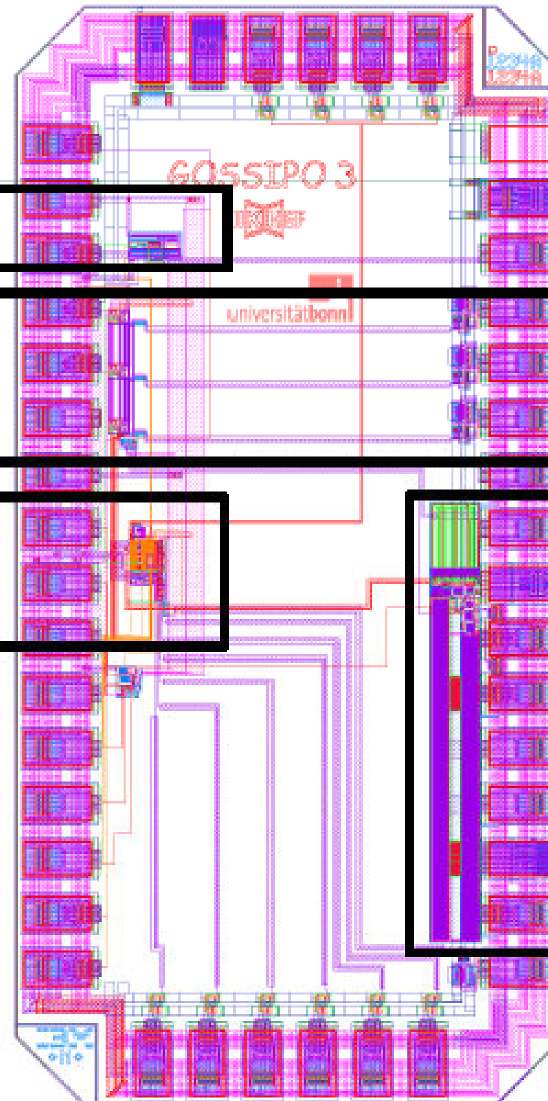
universitätbonn

MPW run on 21.09.09

InGrid preamp

Analogue signal chain
(3 preamps & comparators)

Two complete Pixels
(one without front-end)



LDO (vddd)

NIKHEF

universitätbonn

Session Agenda

09.30 Paul Aspell	The S-ALTRO Demonstrator (status report)
09.50 Xavi Llopart	News from Medipix3 measurements and impact on Timepix2
10.10 Marek Idzik	Readout electronics for the LumiCal detector
10.30 Kostas Kloukinas	Microelectronics technology support and foundry services at CERN
10.40 Christoph Brezina	Status of Gossipo3
10.55 Discussion	

Access to ASIC design tools and foundry services at CERN for SLHC

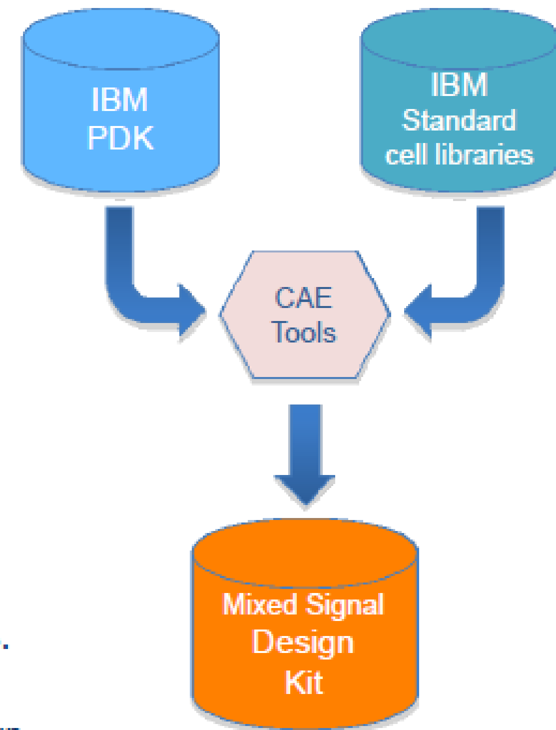
Kostas Kloukinas
CERN, PH-ESE dept.
CH1211, Geneve 23
Switzerland

Overview of Technologies

- Access to Foundry services & Technology technical support.
- 130nm (CMOS & BiCMOS) and 90nm contract available since 6/2007.
- Future technologies can be negotiated with the same manufacturer, once the necessity arise.

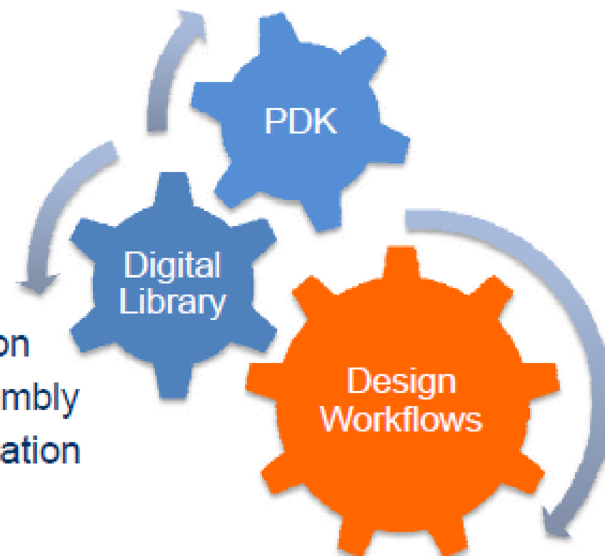
Mixed Signal design kit

- Key Features:
  - IBM PDK V1.6
  - IBM Standard cell and IO pad libraries
    - Physical Layout views available.
    - Separate substrate contacts for mixed signal low noise applications.
    - Access to standard cells libraries is legally covered by already established IBM CDAs
  - New versions of CAE Tools
    - Open Access database support for increased interoperability of Virtuoso and SOC-Encounter environments.
    - Compatible with the "Europractice" distributions.
      - Virtuoso IC 6.1.3, Analog front-end design
      - SOC Encounter 7.1 Mixed signal back-end design
      - IUS 8.1 support for simulations.
      - Calibre support for Sign-Off Physical Verification
  - Support for LINUX Platform (*qualified on RHEL4*)



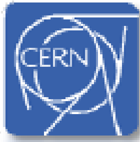
- Two independent design kits:
  - CMOS8RF-LM (6-2 BEOL)
  - CMOS8RF-DM (3-2-3 BEOL)

CMOS8RF Mixed Signal Workflows



- Analog & Mixed Signal (AMS) Workflows.
  - Standardized, validated Design Workflows
  - Top-down design Partitioning.
  - Digital Block implementation flow
    - *Presentation by Sandro Bonacini (CERN)*
  - Mixed-Signal Simulation & design Concept Validation
  - Hierarchical design Floorplaning and Physical Assembly
  - Design Performance Validation and Physical Verification

- CERN – VCAD Cadence - IBM collaboration
  - VCAD brought in their invaluable expertise on the CAE tools
    - *Presentation by Bruno Dutrey (VCAD)*
  - IBM provided the physical IP blocks and important technical assistance
  - CERN assists the development and validates the design kit functionality



Design Kit Distribution

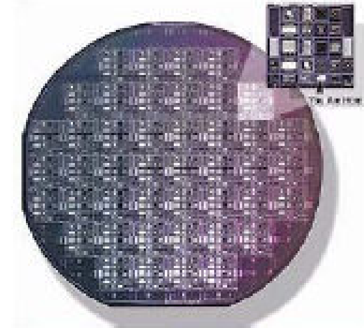
- The Design kit will be made available to collaborating institutes.
  - No access fees required.
  - Pay-per-use scheme.
    - Some small fees will be applied when prototyping the designs through CERN,
    - This should cover part of the design kit maintenance costs in the long term.
  - Planned for release in October 2009.
  - Announcement by e-mail to the “130nm user list”.

- Acquiring the CMOS8RF Mixed Signal Design Kit
  - Contact Bert.Van.Koningsveld@cern.ch
    or Kostas.Kloukinas@cern.ch
  - Establish a CDA with IBM (if not already in place).
  - Granted access to the CERN ASIC support web site.

User Support and Training

- Maintenance
  - Distribution of:
    - IBM PDK updates.
    - Design Flow updates and enhancements.
    - Updates to accommodate new releases of CAE tools.
- User Support
  - Limited to the distributed Design Kit version, running under the supported versions of the CAE design tools.
- Training sessions organized at CERN
  - Scheduled sessions:
    - 1st session: 26 to 30 October (CERN internal)
    - 2nd session: 16 to 20 November (open to external engineers)
    - 3rd session: 30 Nov to 4 December (open to external engineers)

Access to Foundry Services



- Supported Technologies:
  - IBM CMOS6SF (0.25µm), legacy designs
  - IBM CMOS8RF (130nm), mainstream process
  - IBM CMOS8WL & 8HP (SiGe 130nm)
  - IBM CMOS9SF (90nm)
- MPW services:
  - CERN offers to organize MPW runs to help in keeping low the cost of fabricating prototypes and of small-volume production by enabling multiple participants to share production overhead costs.
  - CERN has developed very good working relationships with the MPW service provider MOSIS as an alternate means to access silicon for prototyping.
- Engineering runs
  - CERN organizes submissions for design prototyping and small volume production directly with the foundry.

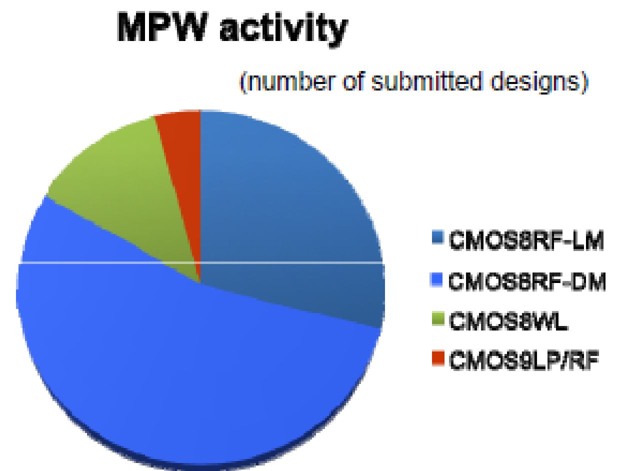
MPW runs with MOSIS

- CERN made extensive use of the MOSIS CMOS8RF MPWs last year.
  - The break-even point for the cost of a CERN MPW and a MOSIS MPW is ~150mm^2.
- Better pricing conditions for the CMOS8RF MPW services
  - MOSIS recognized the central role of CERN in research and educational activities.
  - 35% cost reduction compared to 2008 prices
  - Waived the 10mm2 minimum order limit per submission
  - CERN appreciates the excellent collaborating spirit with MOSIS
- Convenience of regularly scheduled MPW runs.
  - In 2008 there were 6 runs scheduled every 2 months.
  - In 2009 there will be 4 runs scheduled every 3 months.
- Convenience for accommodating different BEOL options:
  - DM (3 thin - 2 thick – 3 RF) metal stack.
  - LM (6thin – 2 thick) metal stack.
  - C4 pad option for bump bonding.

Prototyping activity with MOSIS

2008 - 2009

- CMOS8RF (130nm)
  - 20 designs on 5 MPW runs
    - 7 runs organized, 2 canceled by MOSIS due to insufficient number of designs
    - 2 to 8 designs per MPW run
    - Smallest design 1 mm^2, largest design 20 mm^2
    - 13 designs on 8RF-DM and 7 designs on 8RF-LM
  - 100 mm^2 total silicon area
- CMOS8WL (130nm SiGe)
  - 3 designs on 1 MPW run
  - 10 mm2 total silicon area
- CMOS9LP/RF (90nm)
  - 1 design of 4mm^2 on 1 MPW
- Re-fabrication requests: 2 designs on 8RF and 2 designs on 8WL



Prototyping activity with IBM

2008 - 2009

- CMOS8RF Engineering run **submitted** in 2008Q3.
  - "MEDIPIX-3" PIXEL matrix readout chip.
  - Size: 14 X 17 mm^2
  - 12 wafers ordered.

- CMOS8RF **scheduled** Engineering run
  - "FEI4", ATLAS PIXEL readout chip
  - 19 X 20 mm^2
  - Tape out : 2009Q4

Wrap-Up

- Technology support & foundry services.
  - Provide standardized common design kits and design flows.
  - Provide access to advanced technologies by sharing expenses.
  - Organize common Training and Information sessions.
  - Collective activities help to minimize costs and effort.

- Availability of foundry and technology services is modulated by user's demand.

- Contacts:
  - Organizational issues, contracts etc.:
    - Alessandro.Marchioro@cern.ch
  - Technology support & Foundry services:
    - Kostas.Kloukinas@cern.ch
  - Access to design kits and installation:
    - Bert.van.Koningsved@cern.ch