NEWS FROM MEDIPIX3 MEASUREMENTS AND IMPACT ON TIMEPIX2

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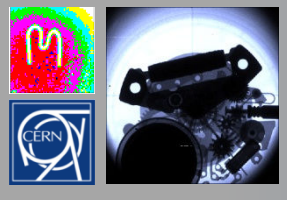
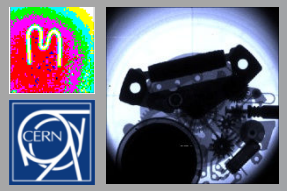
CERN



Outline

- Medipix3 introduction
- Chip description
- Electrical characterization summary
- Towards Medipix3 Si assemblies
- Conclusions
- Towards Timepix2



Medipix3 Introduction

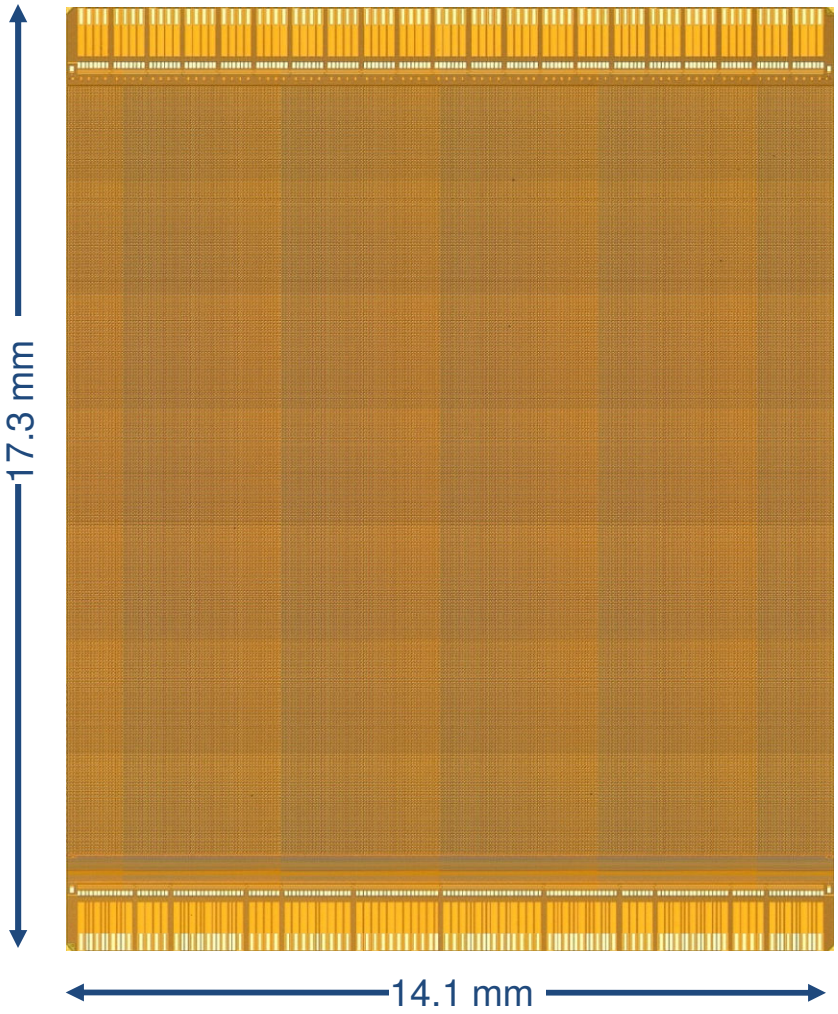
- Medipix3 builds on the success of Medipix2 as a single photon counting imaging chip

- Added Features
  - Analogue charge summing to keep all charge information
  - Spectroscopic mode with 8 threshold levels
  - Continuous Count-Read mode (no dead time)
  - 2 programmable depth binary counters (variable dynamic range)
  - Flexible readout scheme (ROI, configurable output port width)
  - Highly configurable

- Designed in a 130nm 8-metal CMOS technology

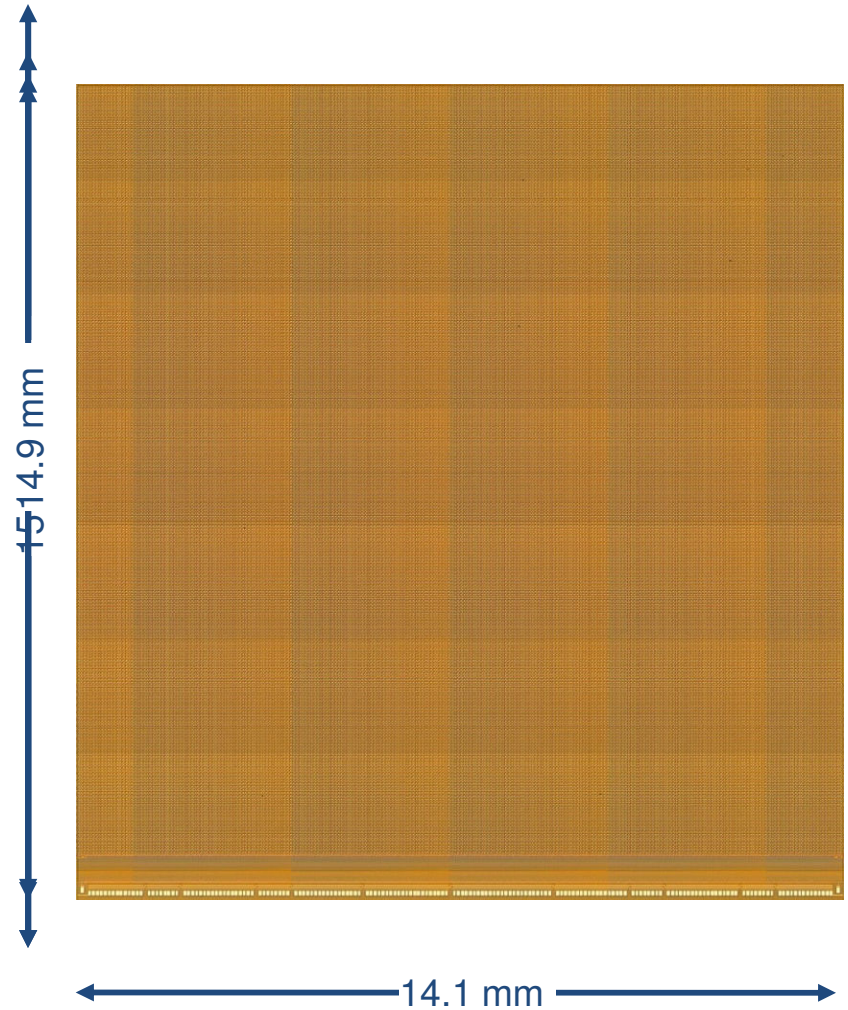
Medipix3 chip

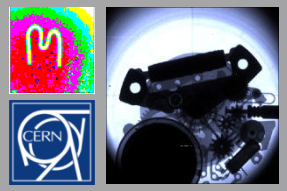
- Pixel matrix of 256 x 256 pixels
- Bottom periphery contains:
  - LVDS drivers and receivers (500 Mbps)
  - Band-Gap and 25 DACs (10 9-bit and 15 8-bit)
  - 32 e-fuse bits
  - EoC and 2 Test pulse generators per pixel column
  - Temperature sensor
  - Full IO logic and command decoder
  - Power/Ground pads
  - TSV landing pads
  - Pads extenders
- Top periphery contains:
  - Power/Ground pads
  - TSV landing pads
  - Pads extenders
- > 115 Million transistors
- Typical power consumption:
  - 600 mW in Single pixel mode
  - 900 mW in Charge summing mode



Multiple dicing options

	X [µm]	Y [µm]	Active Area
Medipix2 and Timepix	14111	16120	87.1%
Medipix3 top and bottom WB	14100	17300	81.2%
Medipix3 bottom WB	14100	15900	88.4%
Medipix3 top and bottom TVS	14100	15300	91.9%
Medipix3 bottom TVS	14100	14900	94.3%

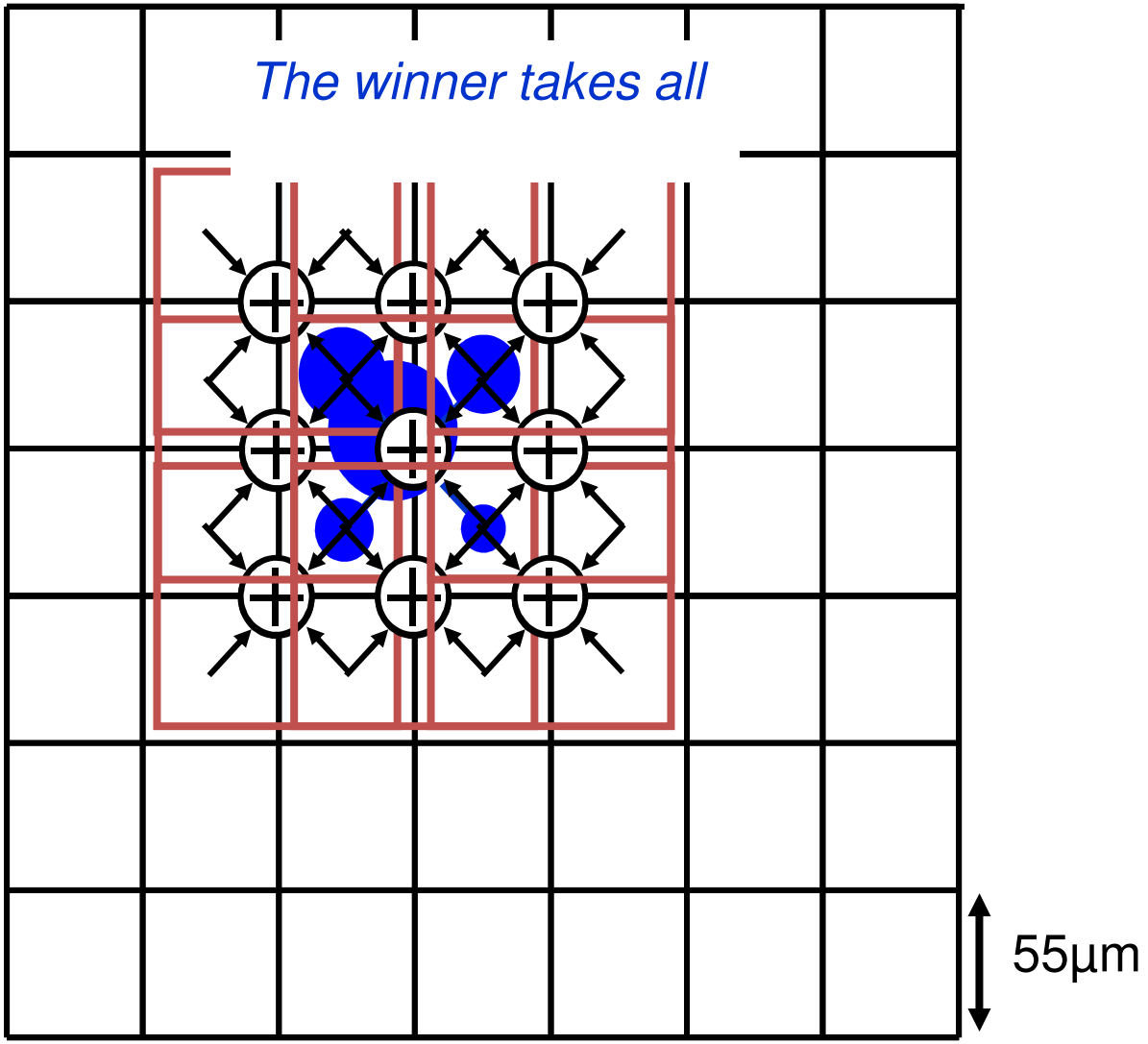




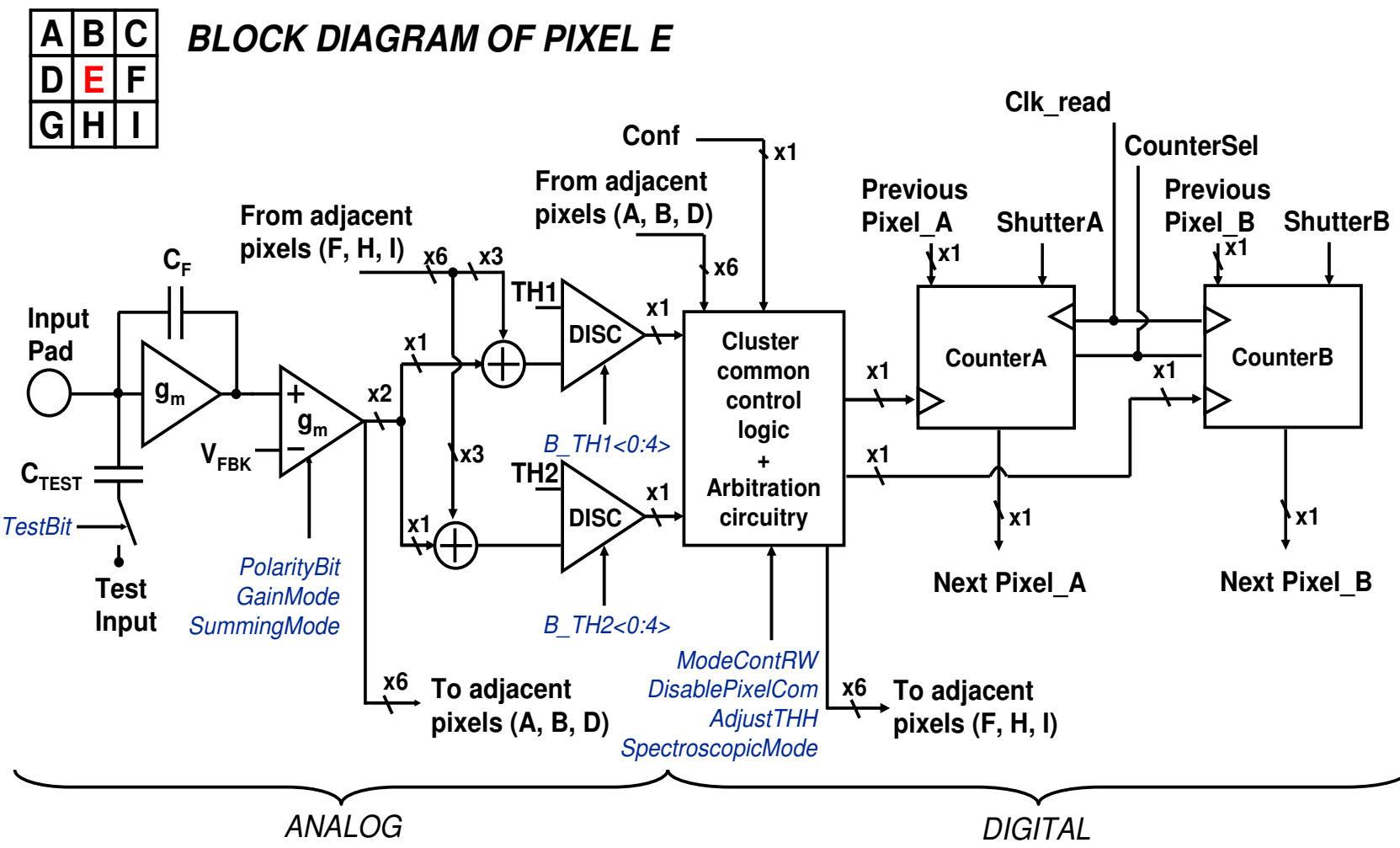
Medipix3 pixel Modes

Pixel Operation Modes	Pixel size	# Thresholds
Single Pixel	Fine Pitch Mode → 55 µm x 55 µm	2
Charge Summing		
Colour Mode	Spectroscopic Mode → 110 µm x 110 µm	8
Colour Mode with charge Summing		
Pixel Gain Modes	**Linearity**	**# Thresholds**
High Gain Mode	~10 ke^-	2
Low Gain Mode	~20 ke^-	
Pixel Counter Modes	**Dynamic range**	**# Counters**
1-bit	1	2
4-bit	15	2
12-bit	4095	2
24-bit	16777215	1
Pixel Readout Modes	**# Active Counters**	**Dead Time**
Sequential Count-Read (SCR)	2	Yes
Continuous Count-Read (CCR)	1	No

Charge summing and allocation concept



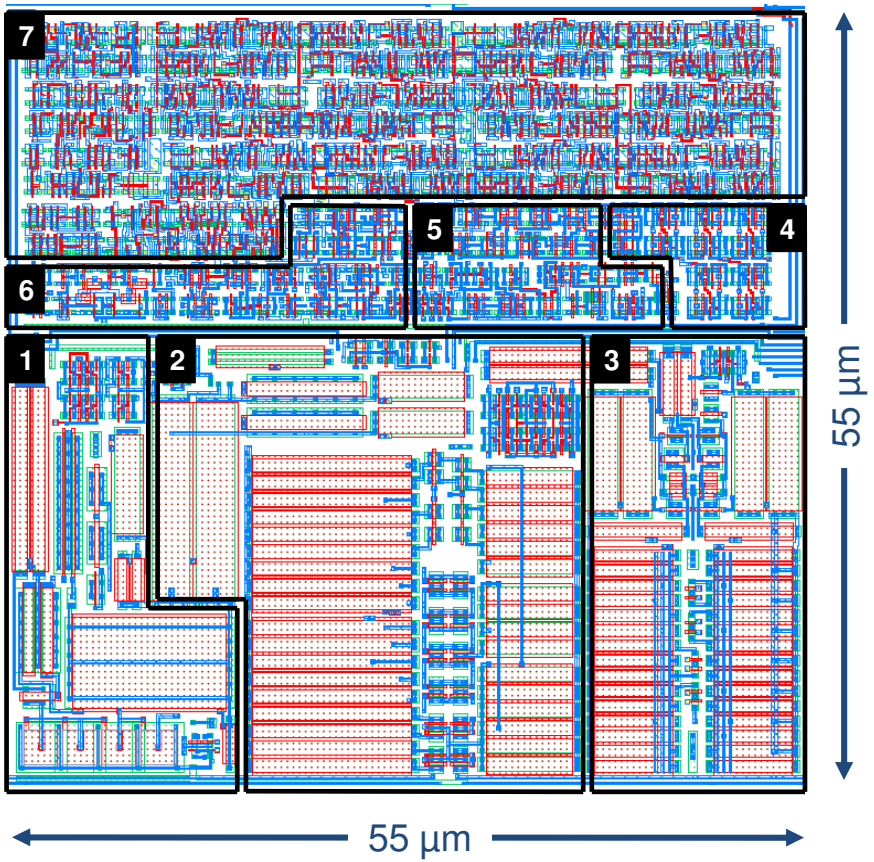
Medipix3 Cell Schematic



Pixel Layout

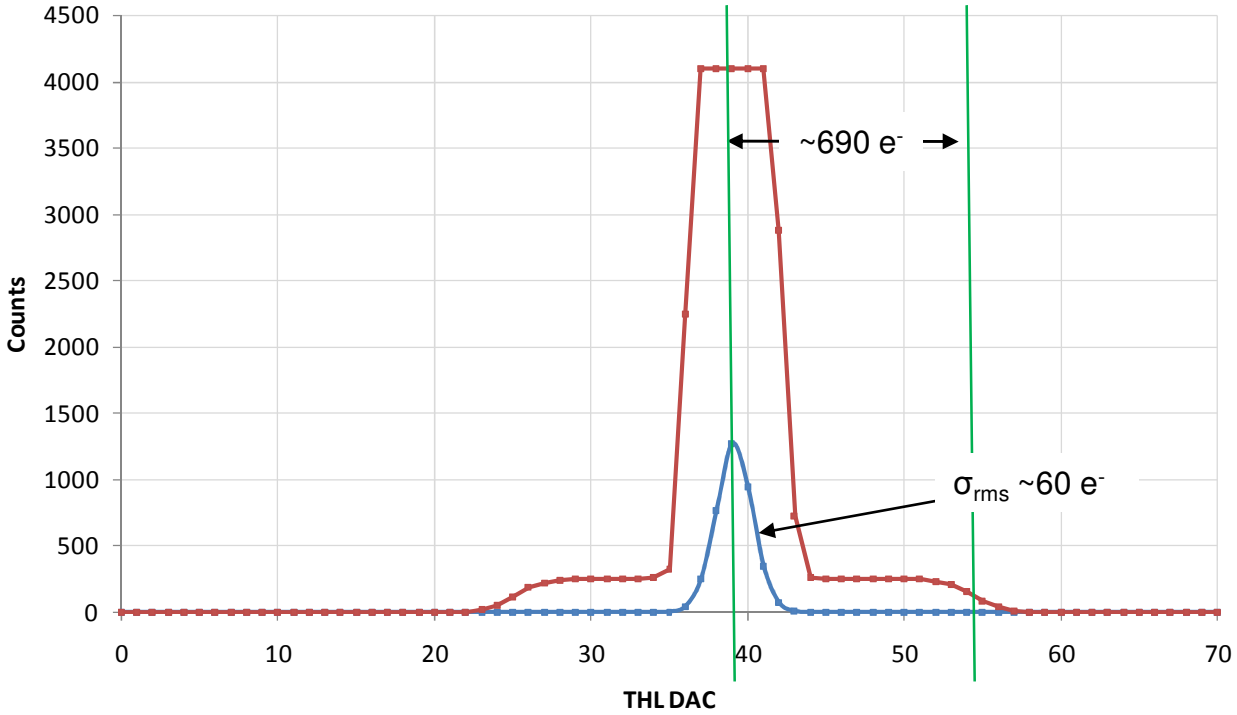
- Design fully exploits the 130 nm CMOS technology
- ~1600 transistors per pixel

1. Preamplifier
2. Shaper
3. Two discriminators with 5-bit threshold adjustment
4. Pixel memory (13-bits)
5. Arbitration logic for charge allocation
6. Control logic
7. Configurable counter



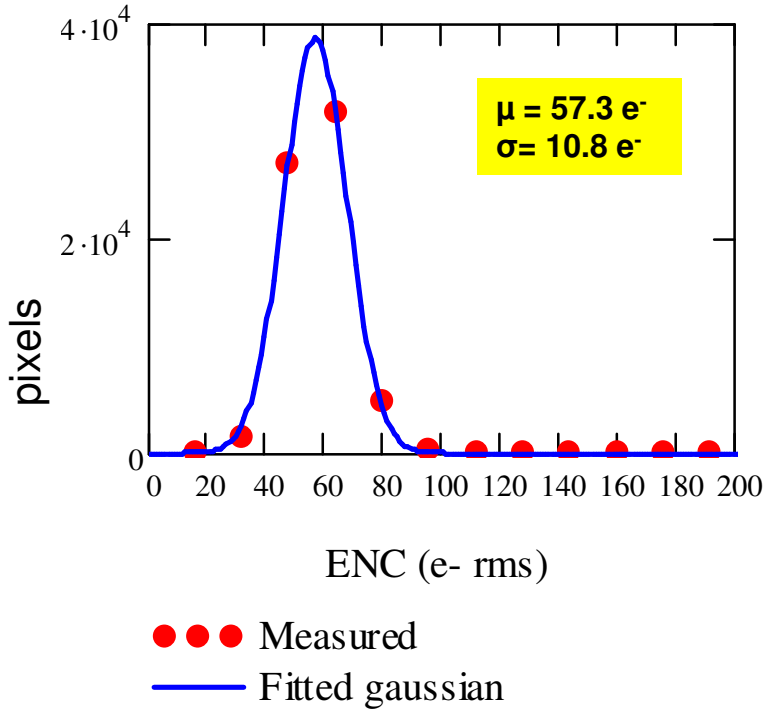
Electrical characterization

- Using the S-curve method the ENC, gain and threshold can be extracted

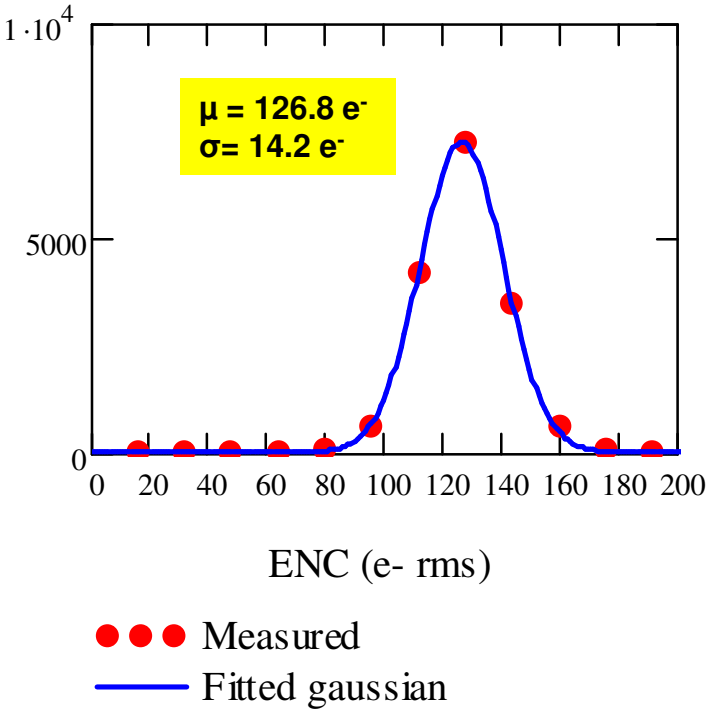


Full chip ENC distribution

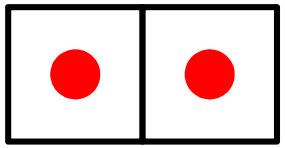
Single Pixel Mode

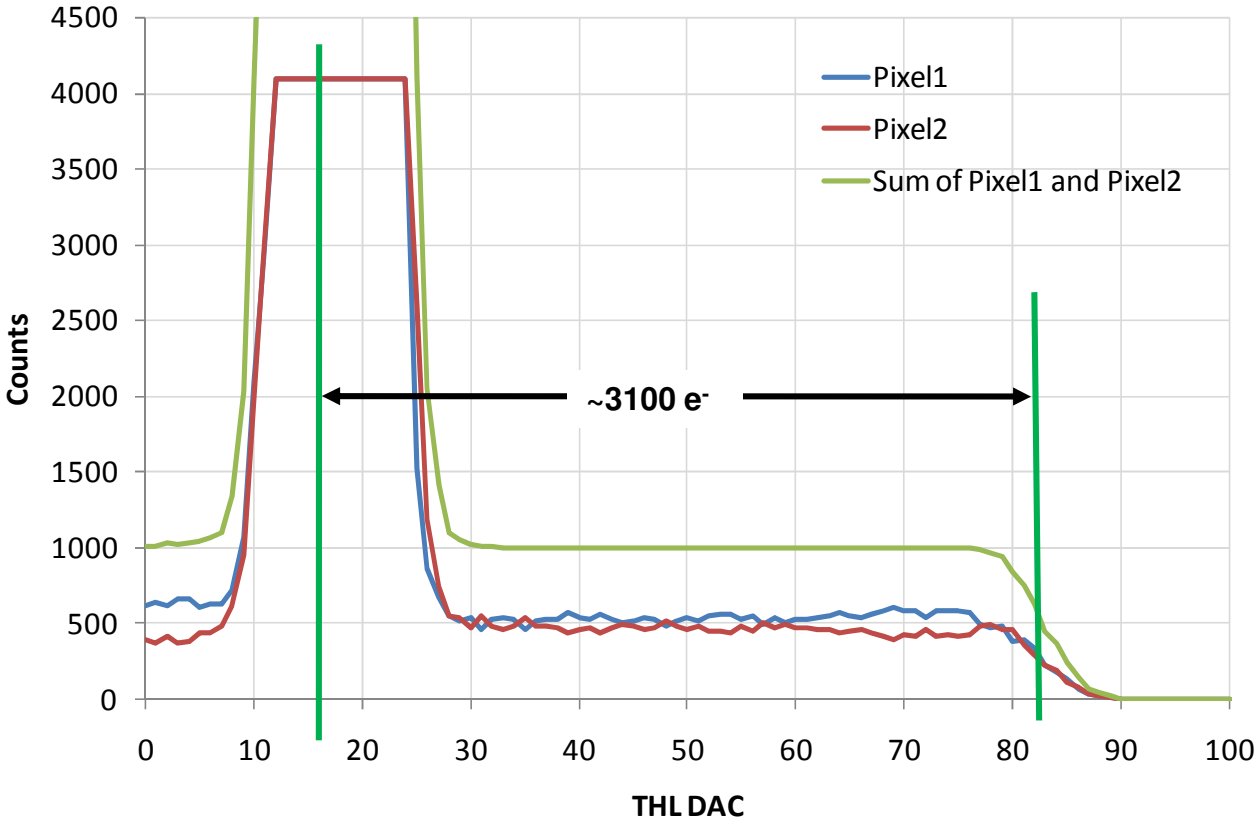


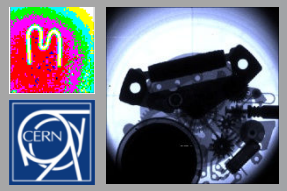
Charge Summing Mode
(1/4th of the pixel matrix)



Measurement in charge summing



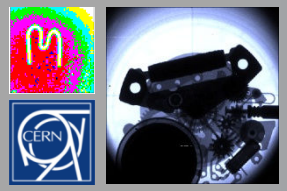




Electrical pixel measurements summary

		Single Pixel Mode	Charge Summing Mode
CSA Gain		11.4 mV/ke$^-$	
CSA-Shapper Gain	High Gain	34 nA/ke$^-$	
	Low Gain	20 nA/ke$^-$	
Non-Linearity	High Gain	<5% up to 10 ke$^-$	
	Low Gain	<5% up to 20 ke$^-$	
Peaking time	HG / LG	~110 ns	
Return to baseline	High Gain	<1.5 µs for 12 ke$^-$	
	Low Gain	<2.5 µs for 25 ke$^-$	
Electronic noise (unbonded)	High Gain	~60 e^-_{rms}	~130 e^-_{rms}
	Low Gain	~85 e^-_{rms}	~180 e^-_{rms}
Unadjusted Threshold spread	High Gain	~1000 e^-_{rms}	~1800 e^-_{rms}
	Low Gain	~1900 e^-_{rms}	~3200 e^-_{rms}
Expected Minimum threshold*	High Gain	~450 e$^-$	~900 e$^-$
	High Gain	~650 e$^-$	~1300 e$^-$
Pixel power consumption	HG / LG	8 µW	15 µW

- These electrical measurements have to be validated once the first Medipix3 assemblies will be available



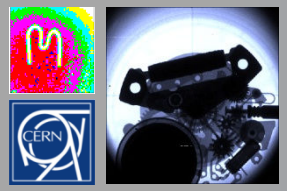
3 design flaws found

1) The incomplete modeling of the analog multiplexers leakage current at full chip scale:
   - 2 DACs show shorter dynamic range output as expected
   - Temperature variations an increase induced radiation modifies the front-end bias operation point

2) The pixel input protection diode was not designed radiation hard:
   - The increase in leakage current degrades the analog performance of the pixel

- A new bias operation point of the pixel front-end has been found which allows more margin for bias voltages shifts

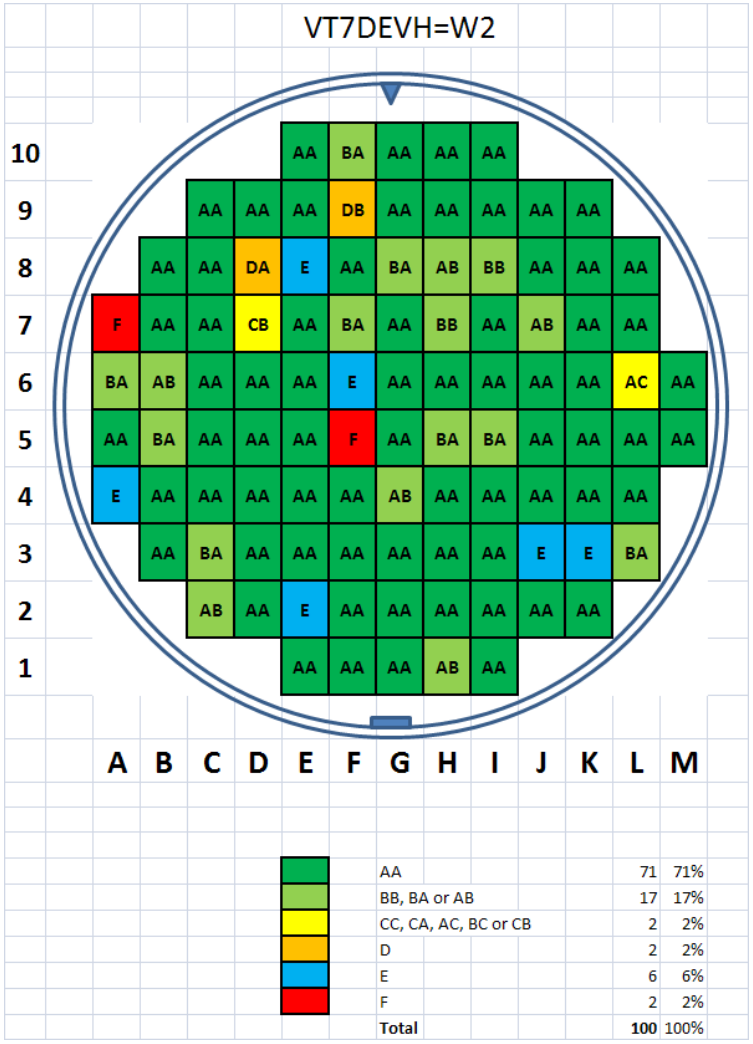
3) Incomplete mixed-signal modeling of a full custom logic block in the pixel counters:
   - Prevents the Continuous Count-Read mode to perform as designed.

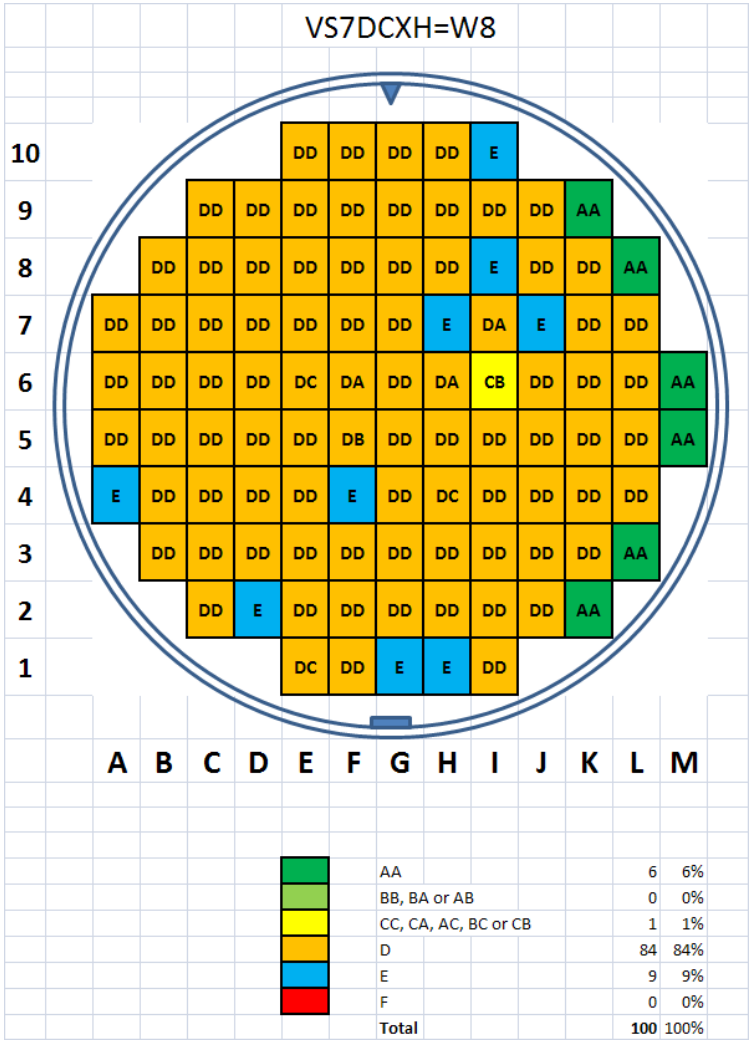


Wafer Probing Summary

Name	#	AA	Bs	Cs	Ds	E	F	# Chips	Where
VK7DG2H	0							100	CERN/diced
VT7DCWH	1	27	10	11	45	3	4	100	CERN
VT7DEVH	2	71	17	2	2	6	2	100	Bump bonding
VV7DFAH	3	33	18	6	32	7	4	100	CERN
VN7DE0H	4	57	18	2	15	8	0	100	Bump bonding
VU7DCVH	5	18	5	1	63	10	3	100	CERN
VW7DF9H	6	36	18	4	30	6	6	100	CERN
VQ7DCZH	7	61	18	2	8	6	5	100	Bump bonding
VS7DCXH	8	6	0	1	84	9	0	100	CERN
VU7DDCH	9	47	21	2	16	12	2	100	CERN
VL7DFJH	10	33	19	7	36	5	0	100	CERN
VW7DDAH	11	48	22	5	15	9	1	100	CERN
		437	**166**	**43**	**346**	**81**	**27**	**1100**	
		39.7%	15.1%	3.9%	31.5%	7.4%	2.5%	100.0%	

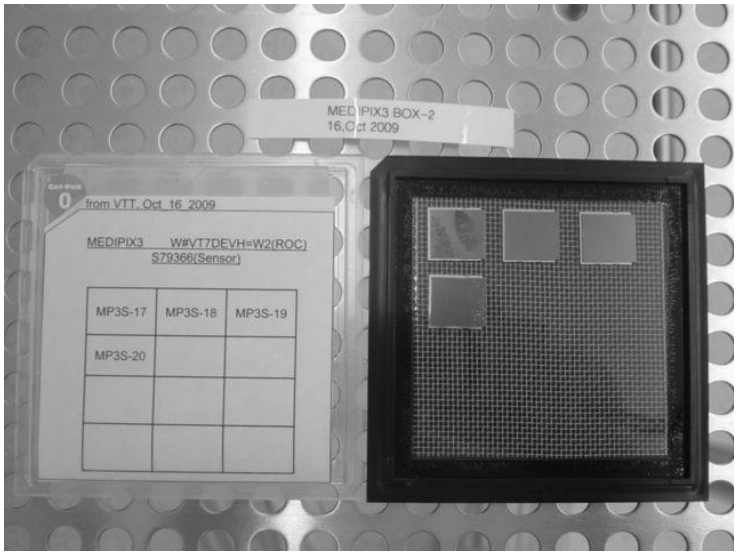
Best and worst wafer



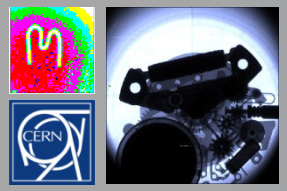


First Medipix3 Assemblies @ CERN

- First 20 300 µm Si detectors bonded to single Medipix3 readout chips arrived at CERN this week end
- First assemblies will be mounted soon (today) and tested this week.
- First results to be presented next week in NSS-MIC09 (Orlando, USA)

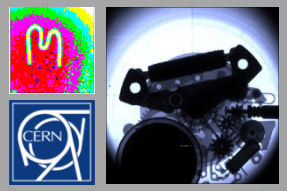


Images from Gädda Akiko (VTT, Finland)



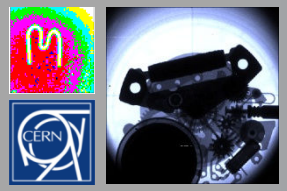
Conclusions on Medipix3

- The Medipix3 chip is the first last scale mixed mode chip built in 130nm CMOS technology in the High Energy Physics community
- The chip is highly configurable and it is prepared for 4-side butting with an active area of ~95%
- The inter-pixel architecture aimed to minimize the impact of charge sharing on energy resolution works
- Electrical characterization is completed and measurements show good agreement with the designed values.
- Yield results are reasonable given the chip size
- First Si assemblies will be available this week and will be used to confirm electrical measurements



Towards Timepix2 (I)

- Many building blocks used in Medipix3 can be reused for a new chip:
  - Band-Gap and DACs
  - E-fuses
  - LVDS drivers and receivers
- Our design team at CERN is currently studying some ideas for new pixel front-ends (preamplifier and discriminators)
  - improved TOT linearity
  - Temperature robustness
  - Minimize pixel to pixel gain variations
- Also a new PLL is being studied
  - Low power (<500 μW)
  - Multiple output selection up to 100 MHz



Towards Timepix2 (II)

- In the Medipix3 collaboration there is a growing interest in Timepix2
- This development will be funded by the Medipix3 Consortium
- Main specs:
  - Pixel to measure TOT and Arrival time information simultaneously
  - <2ns time resolution
  - Triggered readout
  - Sparse and very fast readout