The S-Altro Demonstrator (status report)

An overview and status of the S-Altro Demonstrator project (at CERN).

People :

Luciano Musa … S-Altro Specifications and Architecture
Paul Aspell … Coordinator of demonstrator ASIC design.
Massimiliano De Gaspari ….. Front-end + ADC

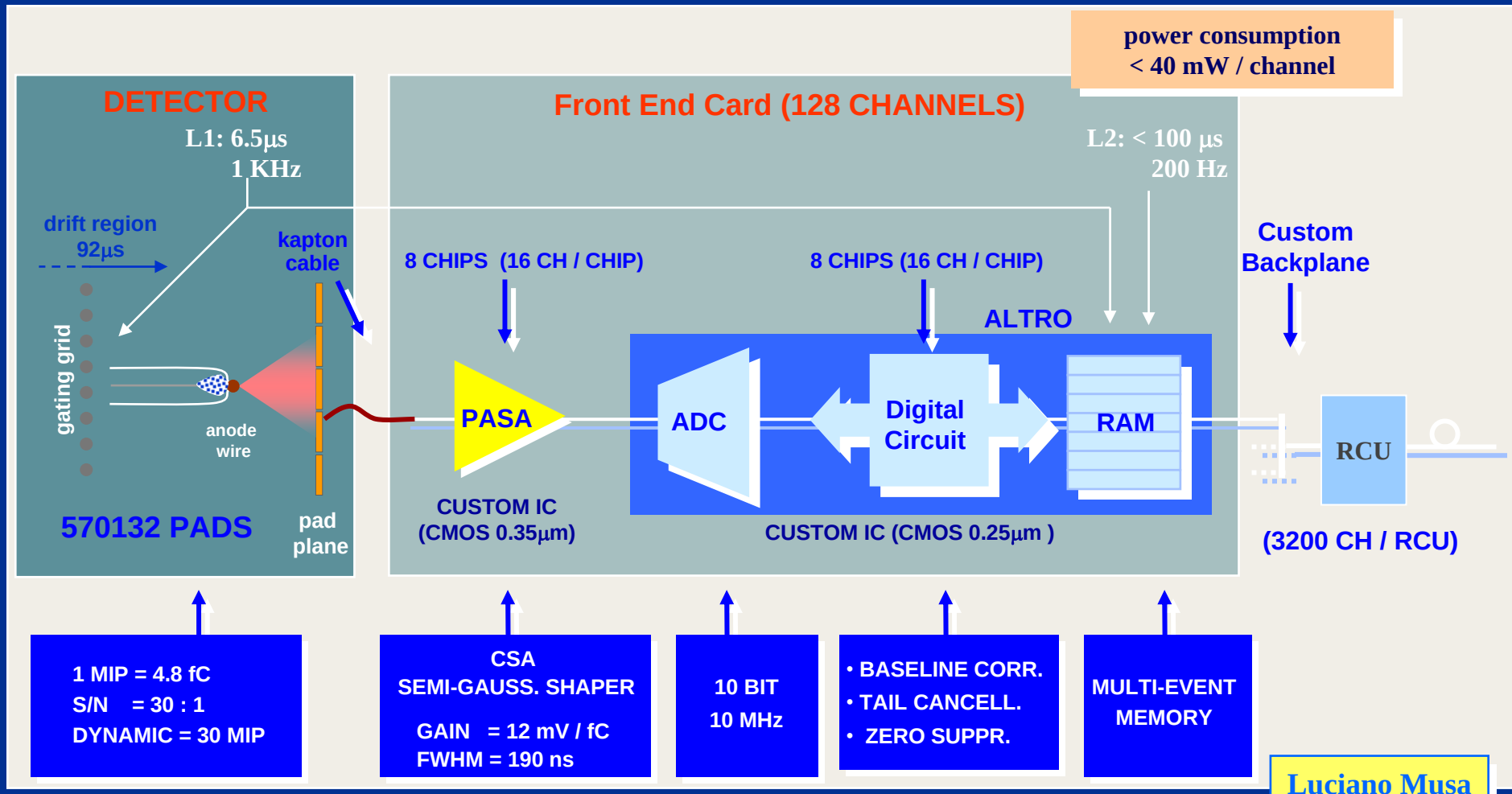
Hugo França-Santos …. ADC
Eduardo Garcia ….. Data Processing & Control

Christian Patauner …. Data compression (now moved to RCU chip)

Presented at the :
EUDET Annual Meeting 2009
Geneva University & CERN, October 19th-21st 2009

S-Altro architecture

Based on the existing PASA + Altro electronics designed for the Alice TPC



Luciano Musa

SAltro Demonstrator

Goal :

To demonstrate integration per channel of an analog front-end, an ADC and digital signal processing in a single chip.

Data processing of 100us of data sampled at 10MHz.

Prepare ideas for TPC readout in the ILC & CLIC

Technology

Process	**IBM 130nm CMOS 8RFDM** **Metal stack 3-2-3** *Implications : The PASA design existed in LM with a different metal stack. Hence layout conversion from the existing design to DM3-2-3 necessary.*
MPW	**MPW through CERN and MOSIS** **Cost \$3K/mm^2** **Includes 40 samples** **Turn around time 70 days** **Submissions every 2 months;**
Standard cells	**Should do new designs using IBM standard cells.**

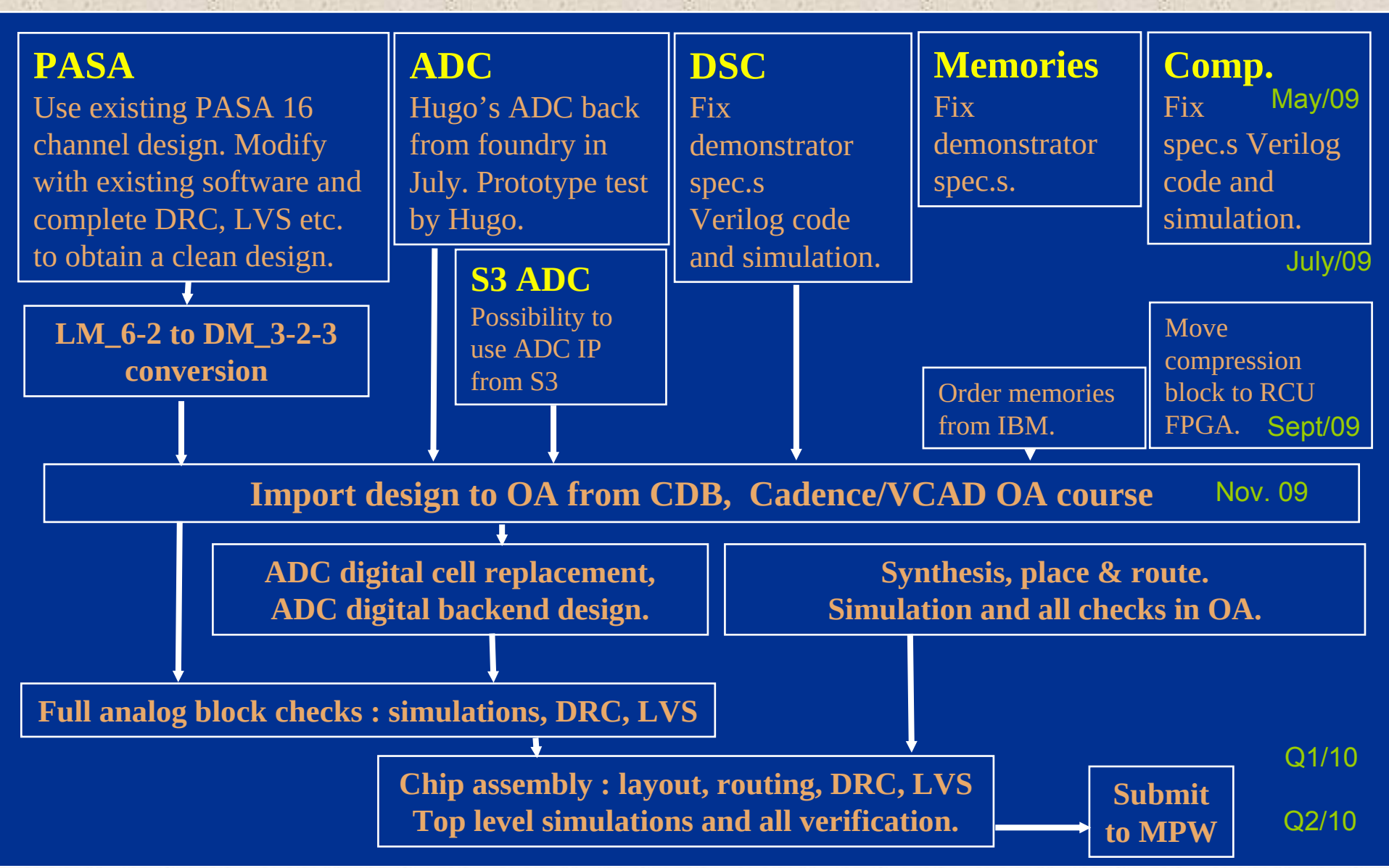
Design software

Software — **Cadence / VCAD Open Access (OA) environment and design flow**
All microelectronics design will move to the new OA framework.

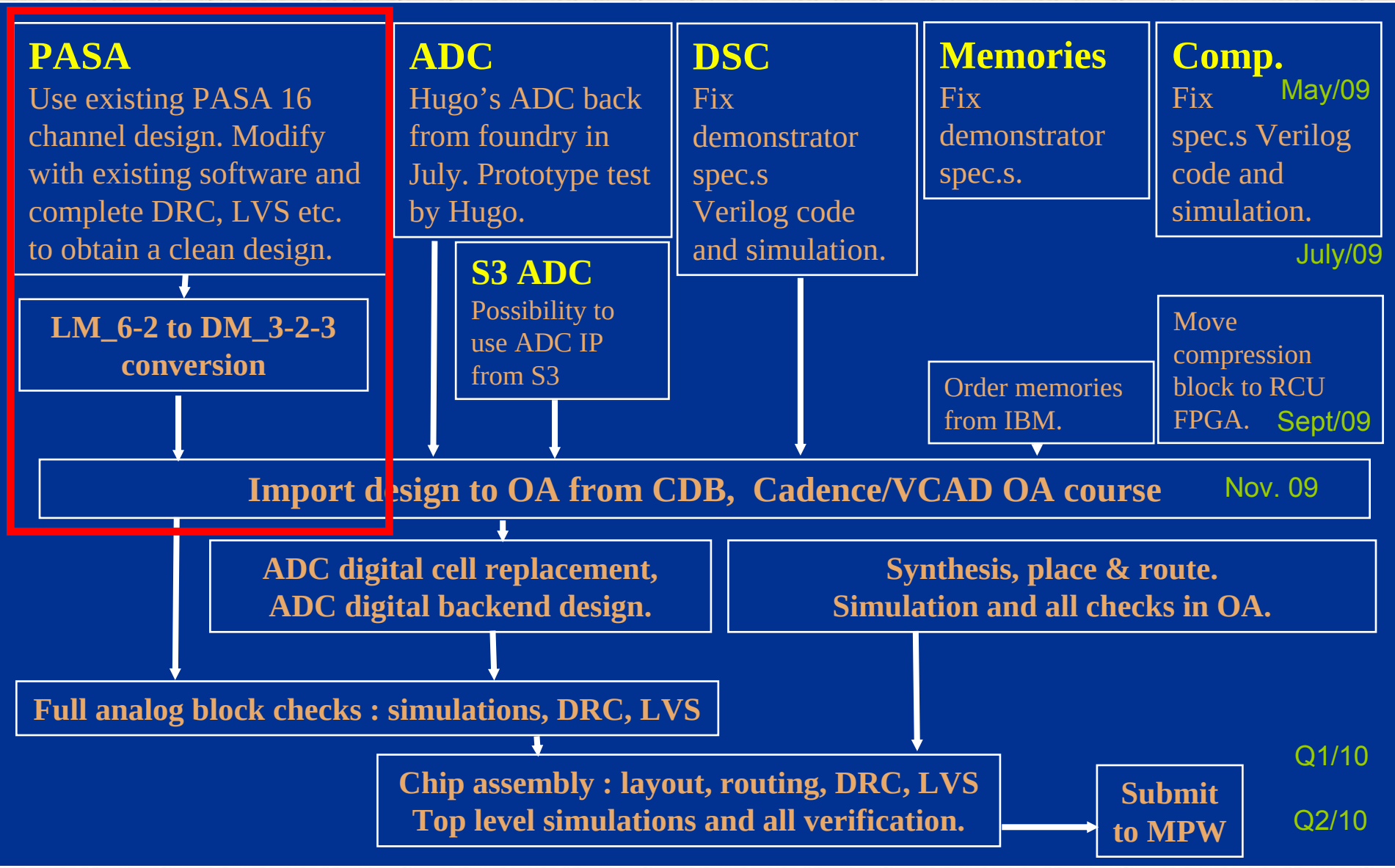
Courses — **Training will be provided by Cadence / VCAD at CERN**
First classes in Autumn.

Implications : Old designs need to be imported and checked for translation errors.

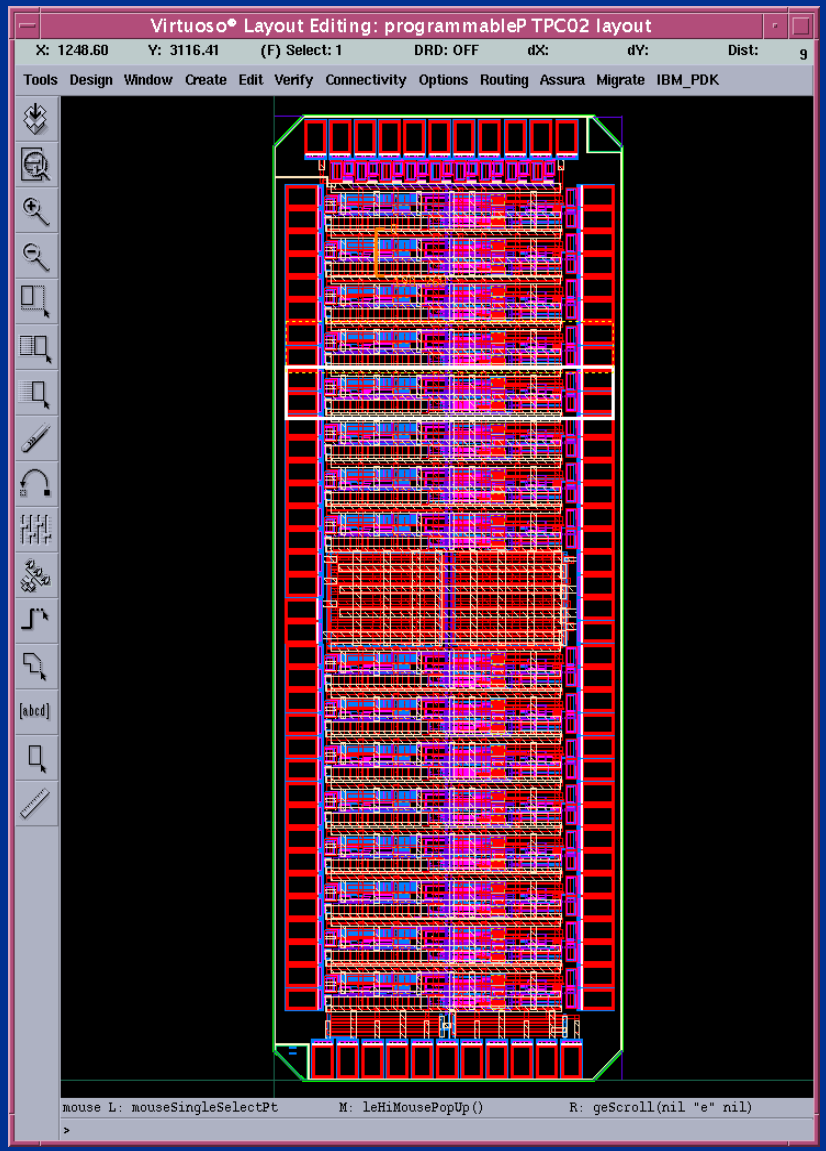
Demonstrator work flow



Demonstrator work flow



PASA prototypes ; PCA 16



Programmable Charge Amplifier d shaper (PCA 16)

- 1.5 V Supply, power consumption , 8 mW / channel
- 16 channel charge amplifier + shaper
- Single ended preamplifier
- Fully differential output amplifier
- Both signal polarities
- Programmable peaking time (30 ns – 120 ns) – 3rd order semi Gaussian pulse shape
- Programmable gain in 4 steps (12 – 27 mV/fC)
- Pre-amp_out mode
- Tunable time constant of the preamplifier
- Pitch 190.26um, Channel length 1026um,
- Chip dimensions = 1.5mm x 4mm

Design by Gerd Trampitsch

IBM CMOS8SF 130nm technology
Migration LM --> DM options

	LM	DM	Sheet resistance	Min width
"old" VNCAPs	M1-3	M1-3		
	M4		64mΩ/□	200nm
	MQ	MQ	38mΩ/□	400nm
	LM		38mΩ/□	400nm
		MG	38mΩ/□	400nm
"new" MIMCAPs		LY	89mΩ/□	600nm
		E1	6mΩ/□	1.5um
		MA	7mΩ/□	4um

Metal layers used for the existing PASA (LM) and layers available for the next submission (DM)

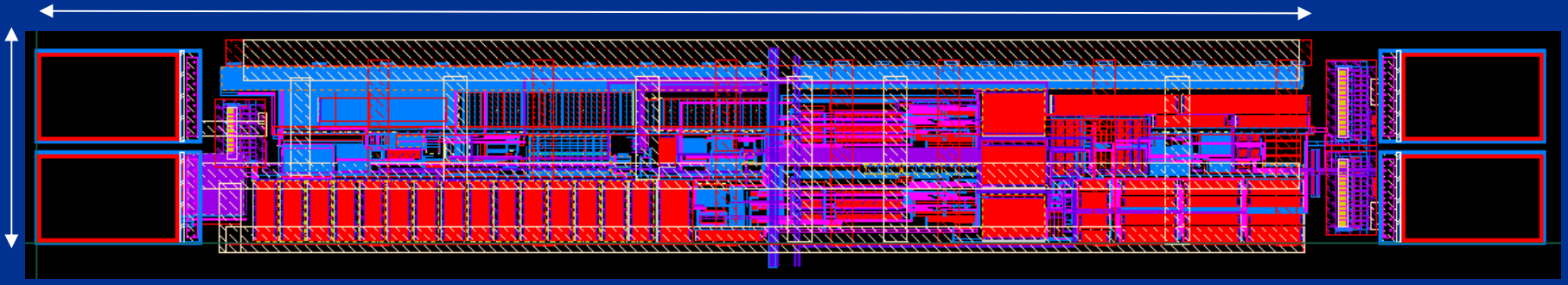
	Cap / "active" area	Total area for 190fF	Total area for 1.79pF
LM vncap	~0.8fF/μm^2 (M1-4)	282μm^2	2411μm^2
DM vncap	~0.6fF/μm^2 (M1-3)	426μm^2	3413μm^2
DM mimcap	2.05fF/μm^2	374μm^2	1502μm^2
DM dualmimcap	4.1fF/μm^2	min 680fF	1190μm^2

Area comparison between LM VNCAP and its available alternatives

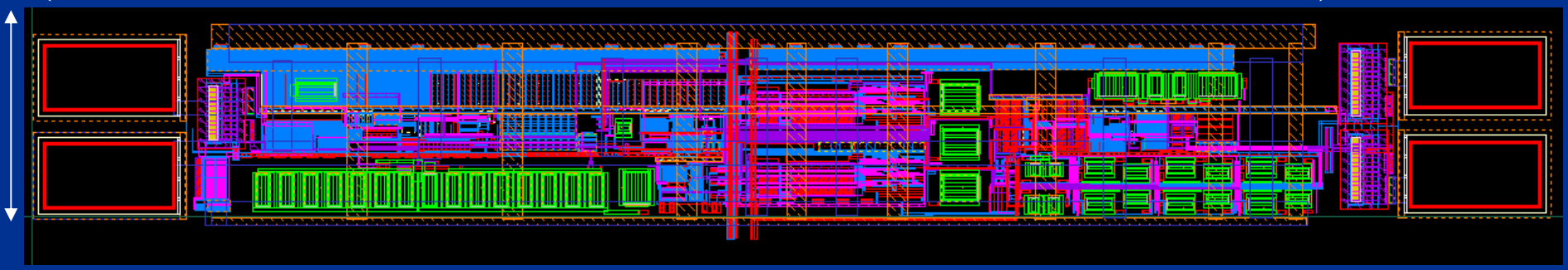
Massimiliano De Gaspari

Original and modified channel layout

1200um X 200um Original Layout



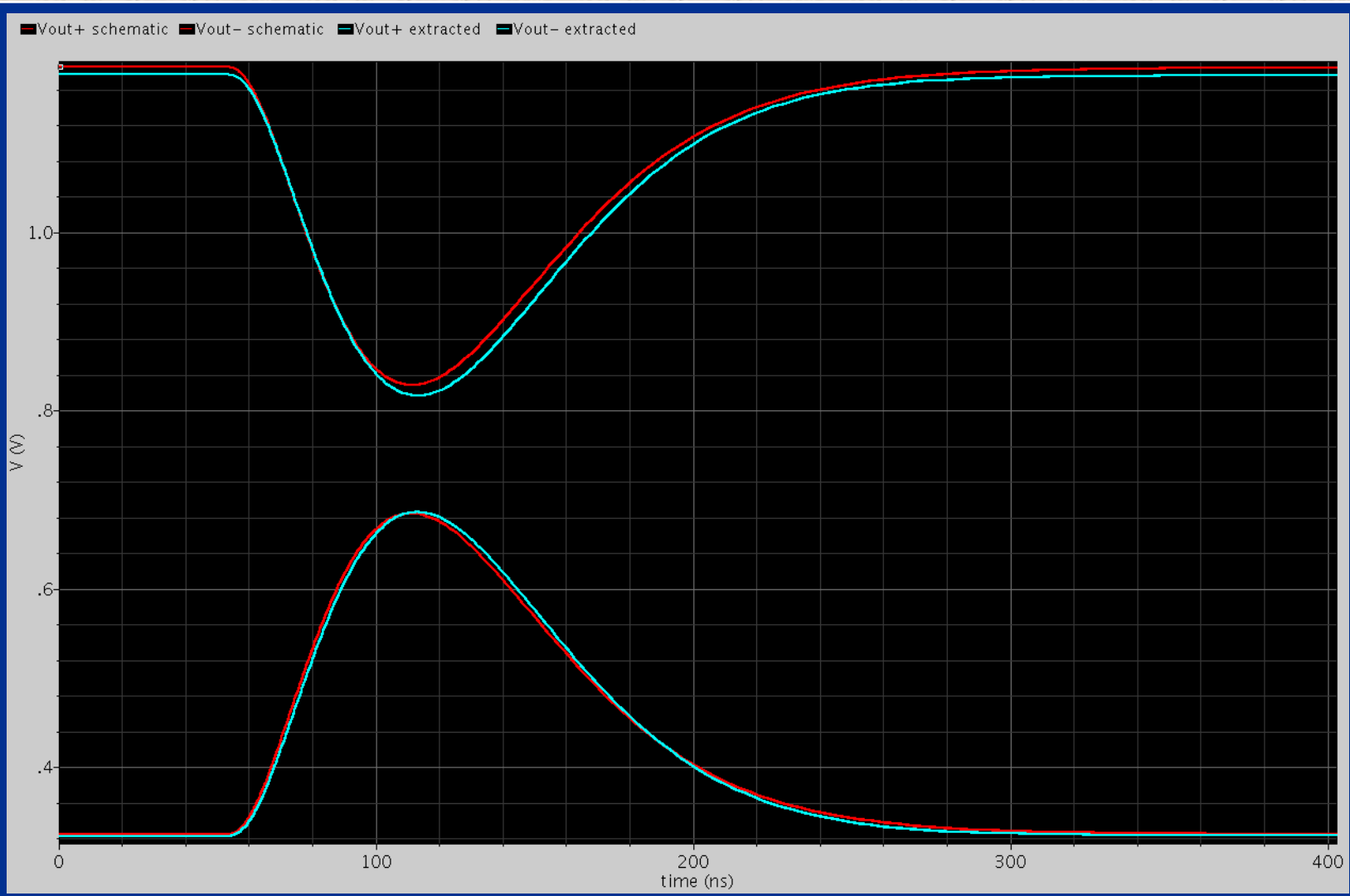
1270um X 200um Modified Layout



MIMCAPs are smaller than LM-VNCAP for cap>500fF (30 larger, 12 smaller) ➔ 6% area increase

Massimiliano De Gaspari

Simulation: schematic vs layout-extracted, typical input pulse

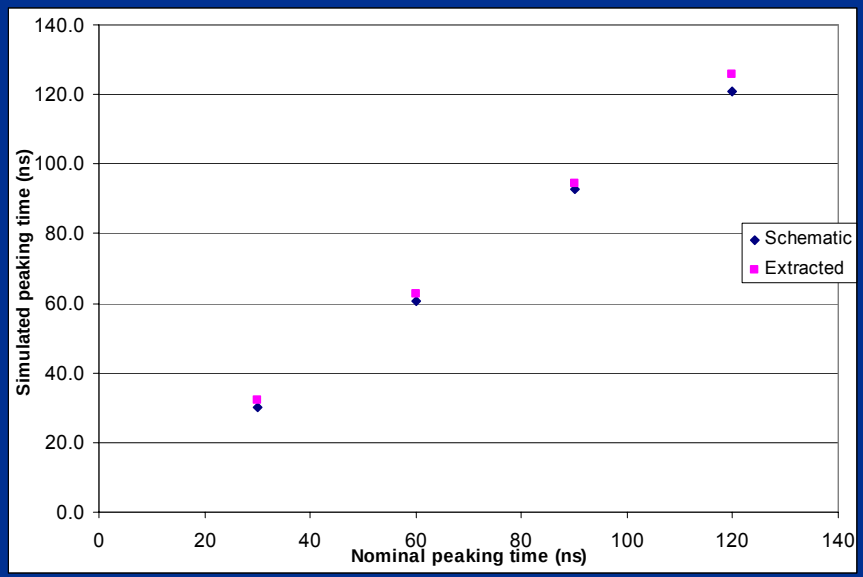


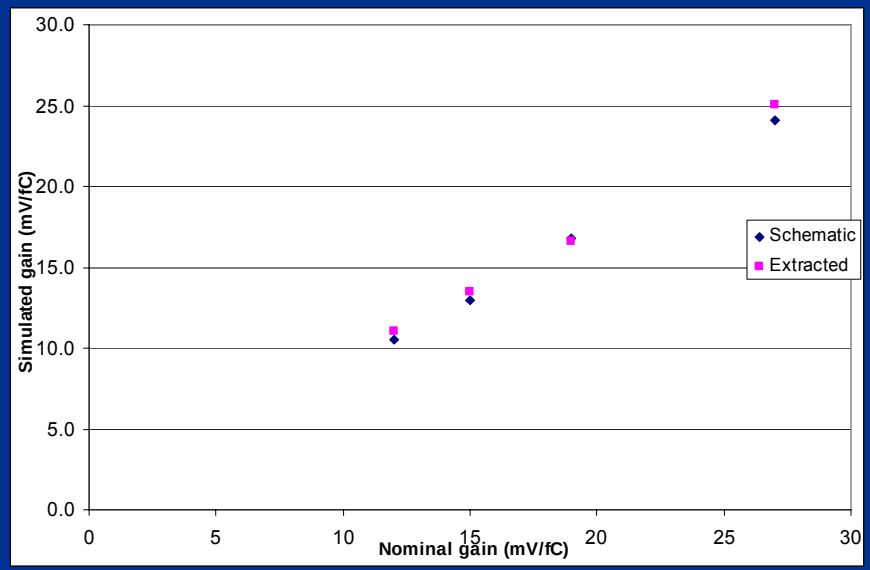
Massimiliano De Gaspari

Shaper mode: peaking time, gain

Peaking time (ns), 50fC input		
Nominal	Schematic	Extracted
30	30.1	32.2
60	60.8	62.8
90	92.6	94.6
120	120.8	125.8

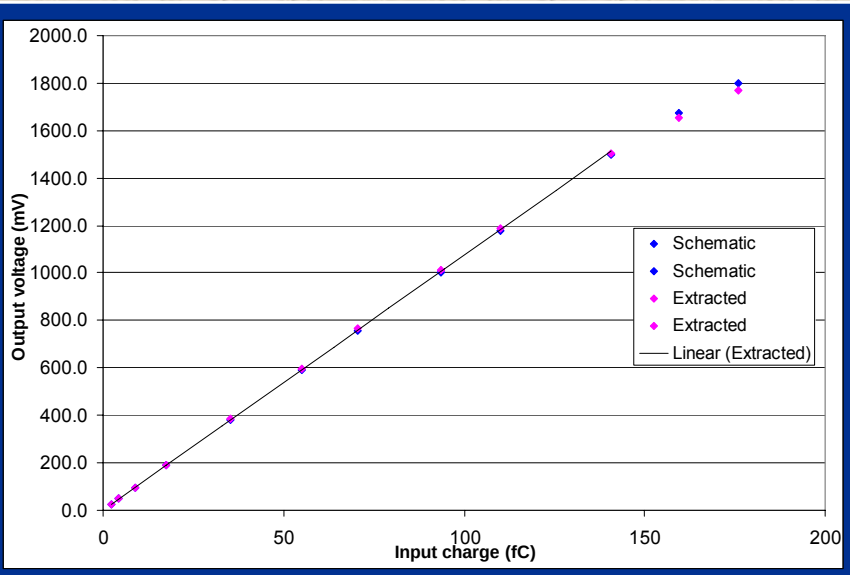
Gain (mV/fC), 50fC input		
Nominal	Schematic	Extracted
12	10.6	11.0
15	12.9	13.5
19	16.8	16.7
27	24.1	25.0

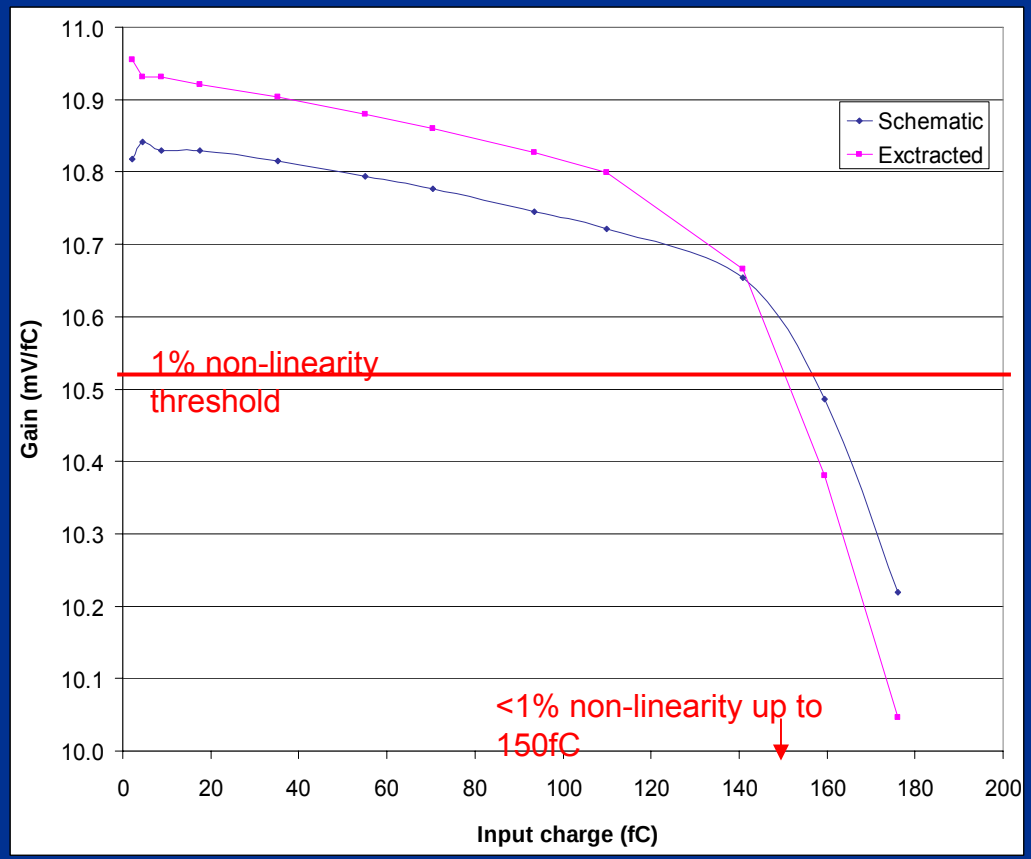




Massimiliano De Gaspari

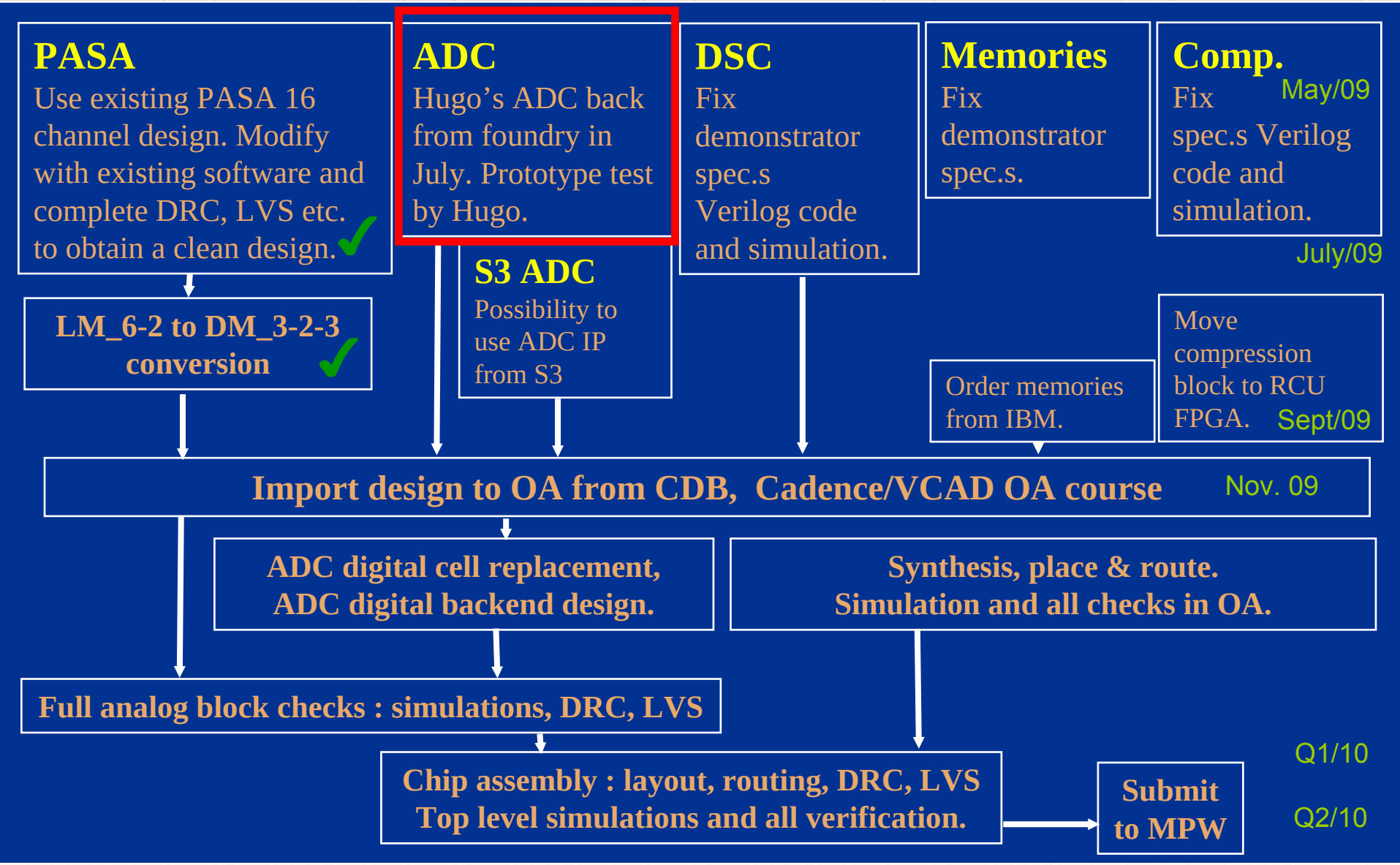
Shaper mode: linearity



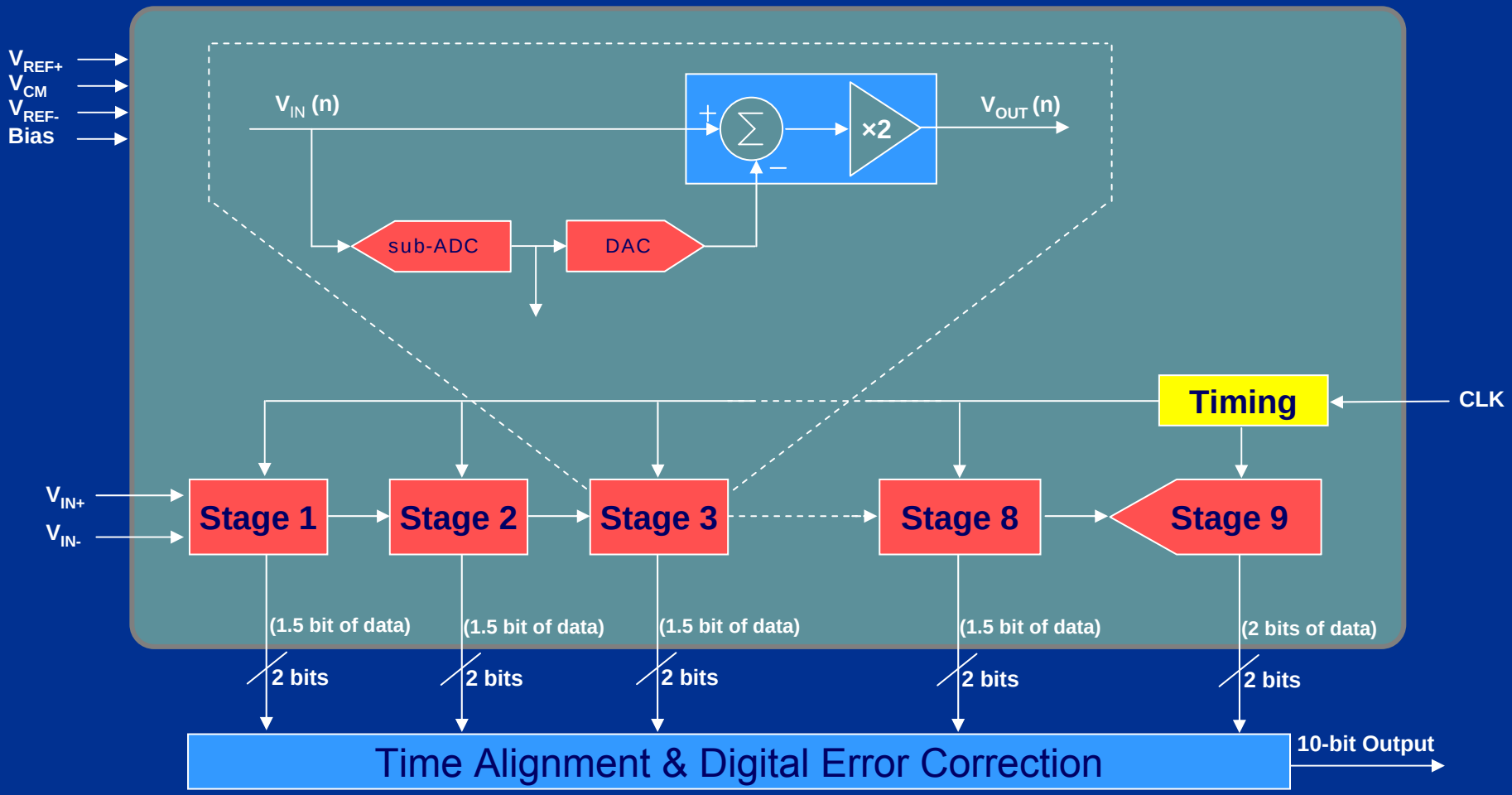


Massimiliano De Gaspari

Demonstrator work flow



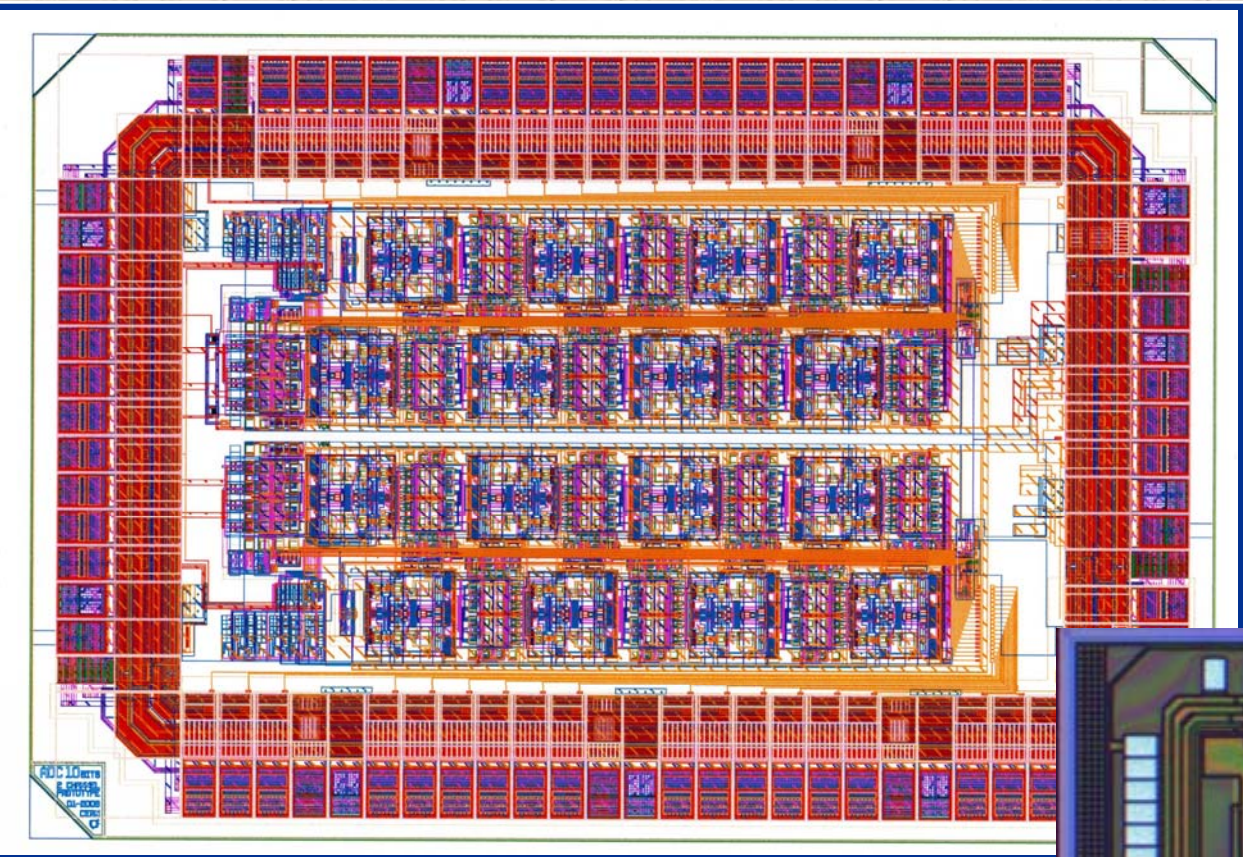
10-bit 40MS/s Pipelined ADC

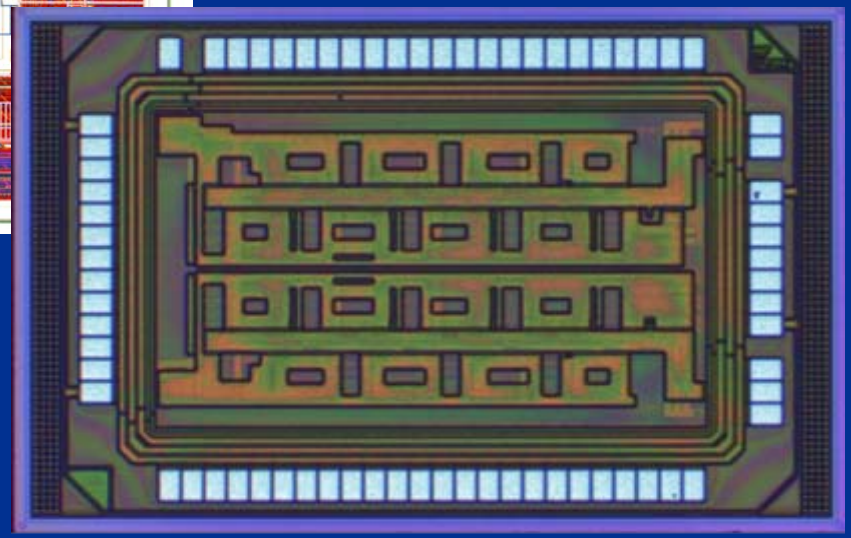


2 identical channels in the prototype.

Hugo França-Santos

Pipelined ADC: 2-Channel Prototype Layout

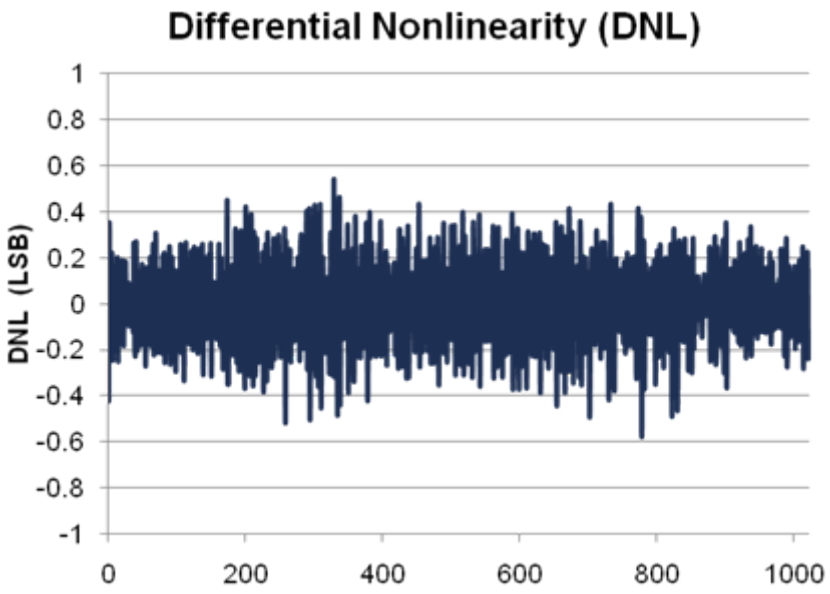


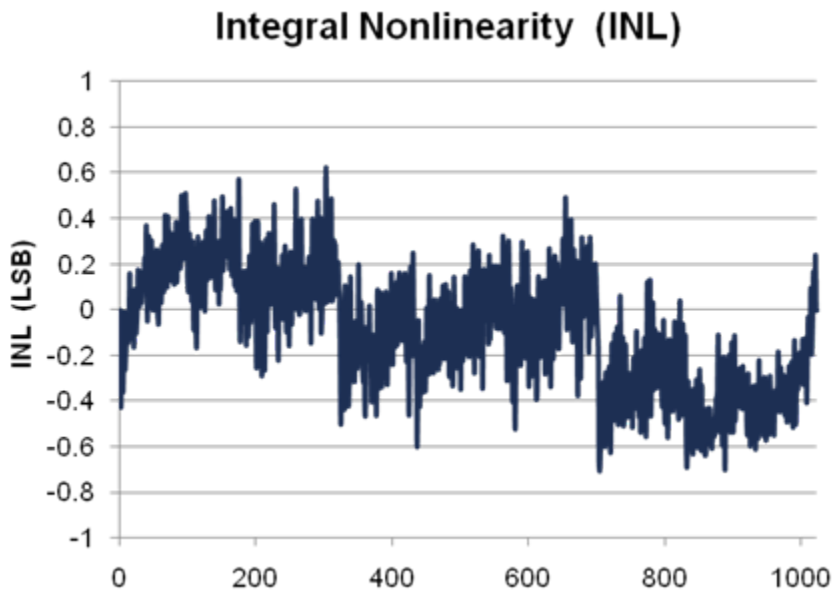


Single ADC area 1.57 X 0.45 = 0.7 mm^2
Prototype area 2.35 X 1.6 = 3.76 mm^2

Hugo França-Santos

ADC TEST: Static Characterization





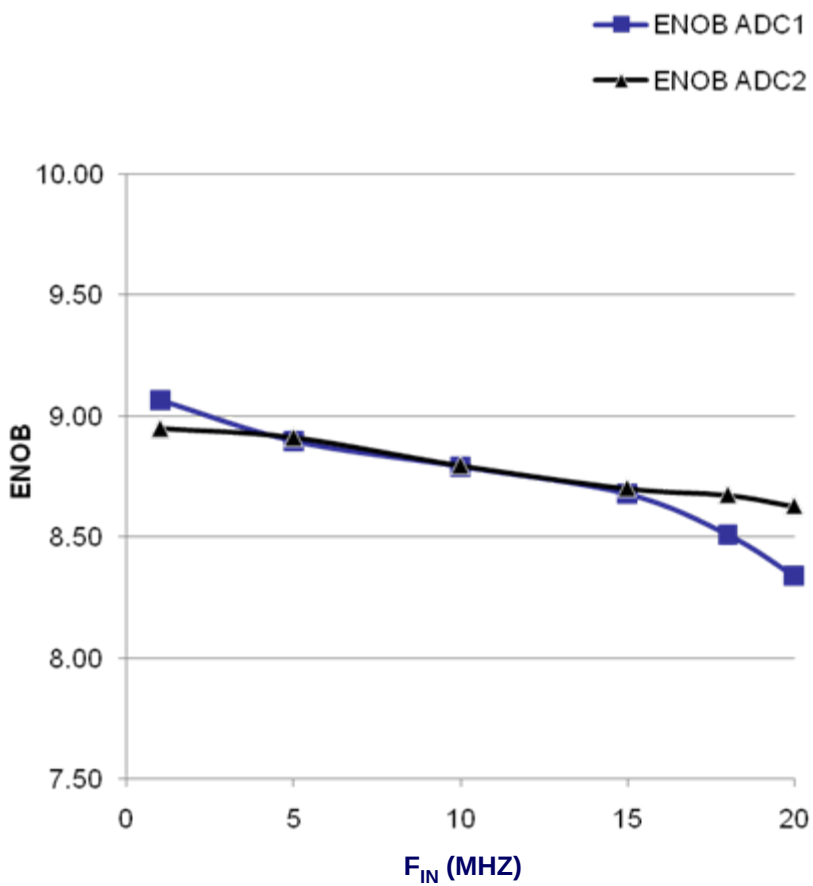
	DNL	INL
MAX	0.54	0.62
MIN	-0.58	-0.71

A 10-bit 40MS/s Pipelined ADC in a 0.13µm CMOS Process – TWEPP 2009

Hugo França-Santos

ADC TEST: Dynamic Characterization at 40MS/s

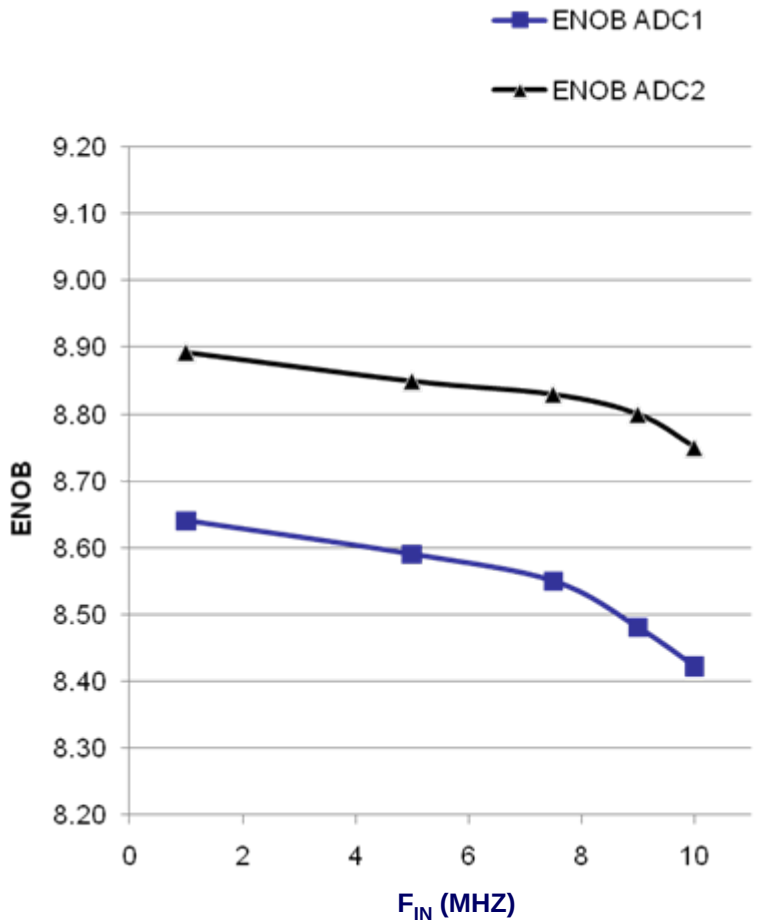
Dynamic Performance at 40MS/s		ENOB		
PARAMETER	INPUT FREQUENCY	ADC1	ADC2	UNIT
Effective Number of Bits (ENOB)	1.0071MHz	9.07	8.95	Bits
	4.9988MHz	8.90	8.91	
	9.9915MHz	8.79	8.80	
	14.9841MHz	8.68	8.70	
	17.9993MHz	8.51	8.67	
	19.9890MHz	8.34	8.63	
Signal to noise and distortion ratio (SINAD)	1.0071MHz	56.33	55.63	dB
	4.9988MHz	55.32	55.41	
	9.9915MHz	54.68	54.71	
	14.9841MHz	54.00	54.14	
	17.9993MHz	52.98	53.97	
	19.9890MHz	51.96	53.70	
Spurious free dynamic range (SFDR)	1.0071MHz	-75.03	-74.08	dB
	4.9988MHz	-71.12	-69.94	
	9.9915MHz	-64.78	-68.74	
	14.9841MHz	-61.13	-72.25	
	17.9993MHz	-58.89	-66.34	
	19.9890MHz	-56.89	-68.06	
Total Harmonic Distortion (THD)	1.0071MHz	-69.66	-70.73	dB
	4.9988MHz	-63.12	-66.90	
	9.9915MHz	-64.44	-65.65	
	14.9841MHz	-67.57	-69.26	
	17.9993MHz	-62.01	-64.66	
	19.9890MHz	-60.87	-65.69	



Power Consumption: 34 mW

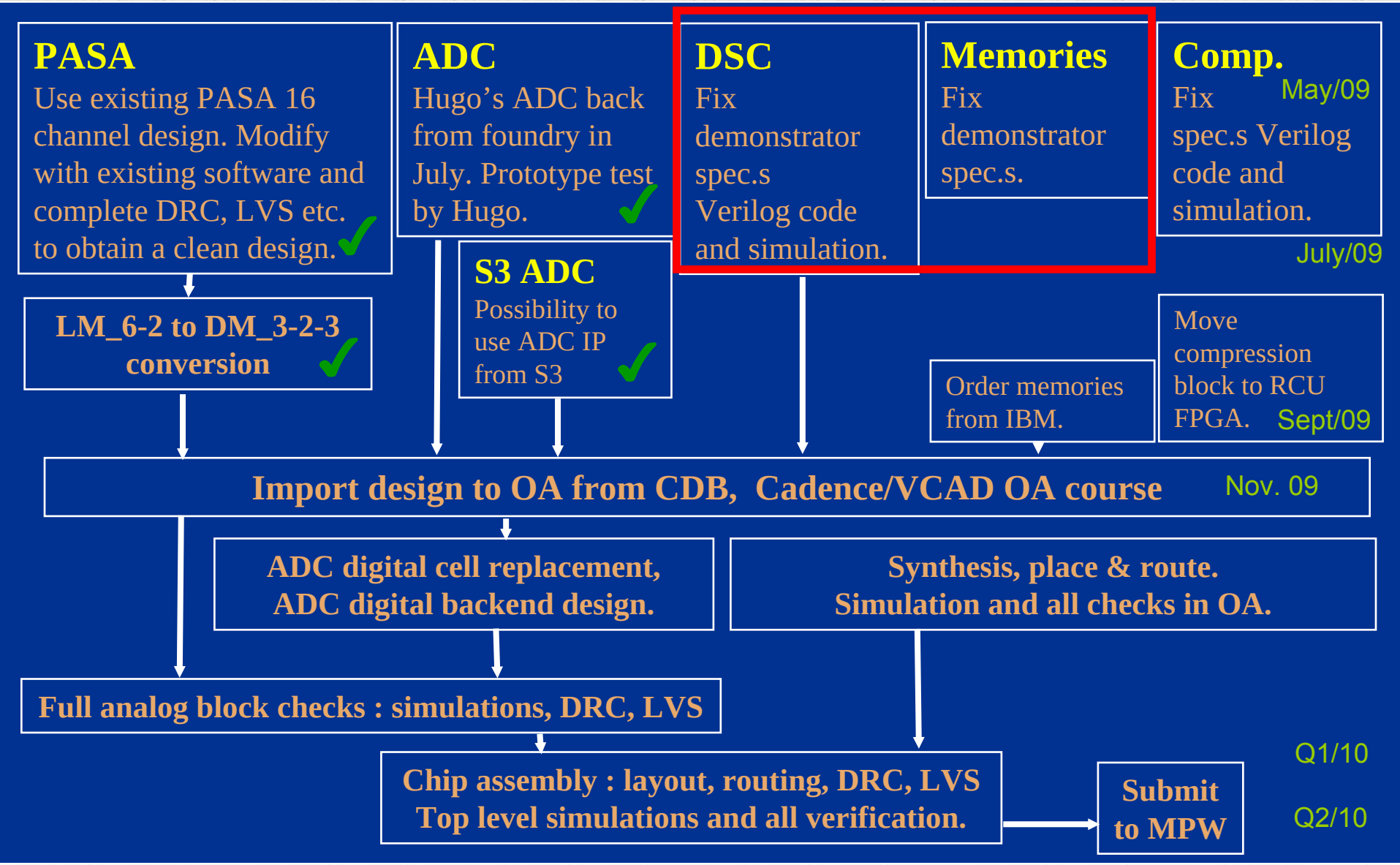
ADC TEST: Dynamic Characterization at 20MS/s

Dynamic Performance at 20MS/s		ENOB		
PARAMETER	INPUT FREQUENCY	ADC1	ADC2	UNIT
Effective Number of Bits (ENOB)	0.9949MHz	8.64	8.89	Bits
	4.9988MHz	8.59	8.85	
	7.5012MHz	8.55	8.83	
	9.0027MHz	8.48	8.80	
	10.0037MHz	8.42	8.75	
Signal to noise and distortion ratio (SINAD)	0.9949MHz	53.77	55.30	dB
	4.9988MHz	53.25	54.98	
	7.5012MHz	53.49	54.82	
	9.0027MHz	52.81	54.93	
	10.0037MHz	52.46	54.13	
Spurious free dynamic range (SFDR)	0.9949MHz	-66.83	-73.46	dB
	4.9988MHz	-59.80	-66.07	
	7.5012MHz	-63.50	-67.50	
	9.0027MHz	-58.96	-68.15	
	10.0037MHz	-58.87	-63.88	
Total Harmonic Distortion (THD)	0.9949MHz	-62.08	-65.22	dB
	4.9988MHz	-59.72	-63.52	
	7.5012MHz	-63.28	-65.42	
	9.0027MHz	-58.88	-64.87	
	10.0037MHz	-58.83	-61.68	

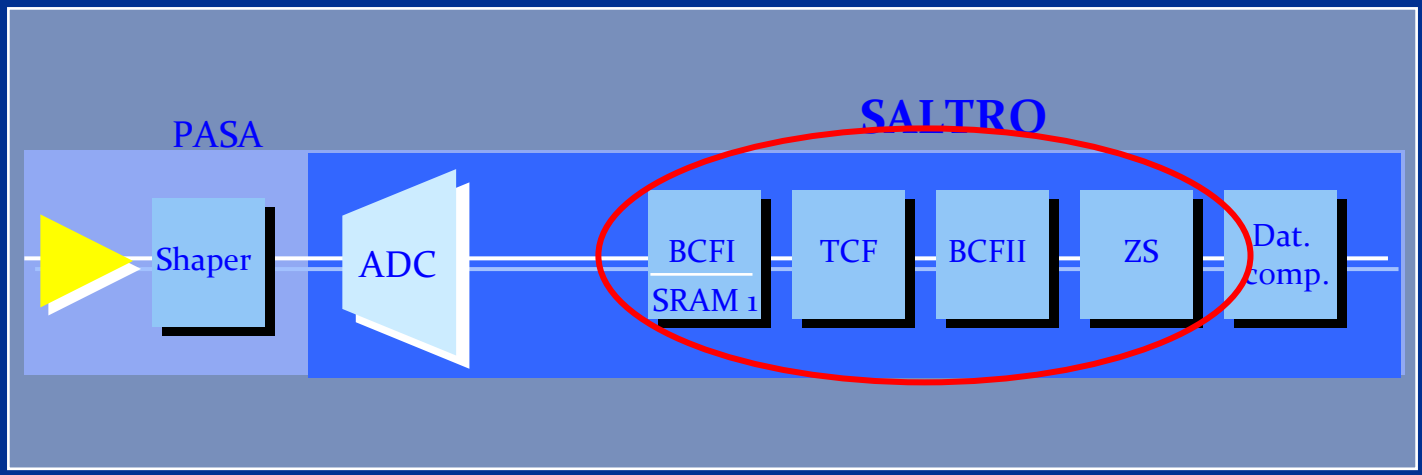


Power Consumption: 26 mW

Demonstrator work flow



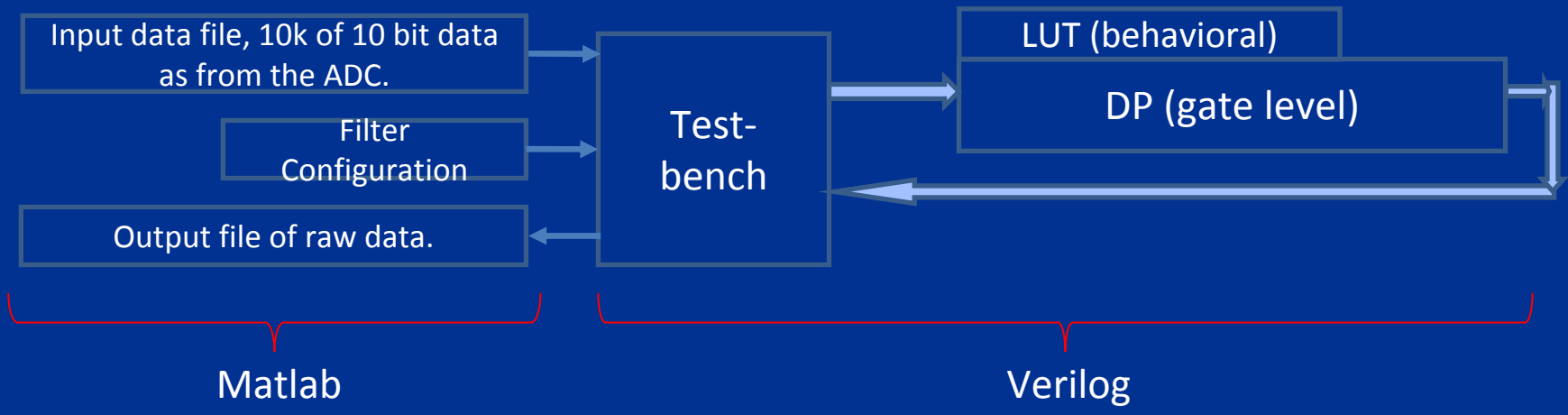
DP functions



Baseline correction 1	Removes systematic offsets that may have been introduced due to clock noise pickup etc. SRAM 1 is used for storage of baseline constants which can then be used a look-up table and subtracted from the signal.
Tail cancellation	Compensates the distortion of the signal shape due to very long ion tails.
Baseline correction 2	Reduces low frequency baseline movements based on a moving average filter.
Zero suppression	Removes samples that fall below a programmable threshold.

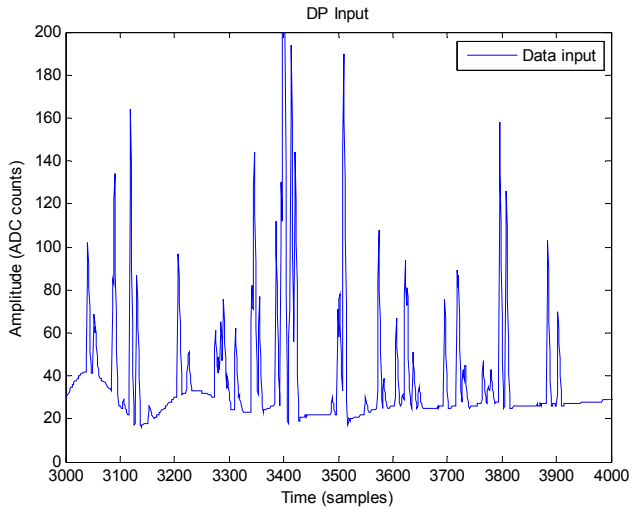
Eduardo Garcia

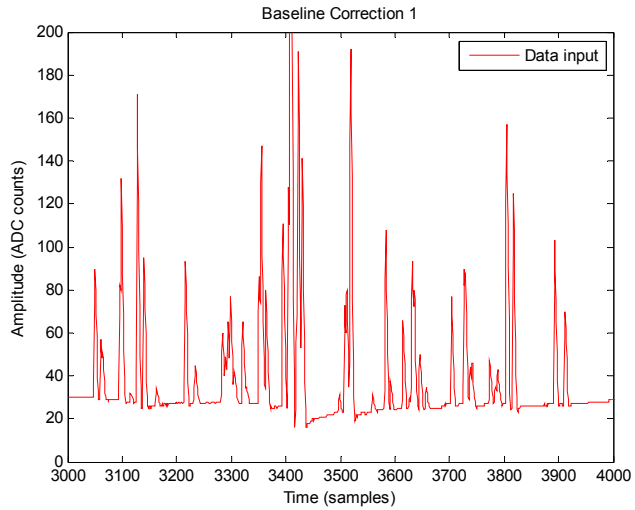
DP Simulation status



Eduardo Garcia

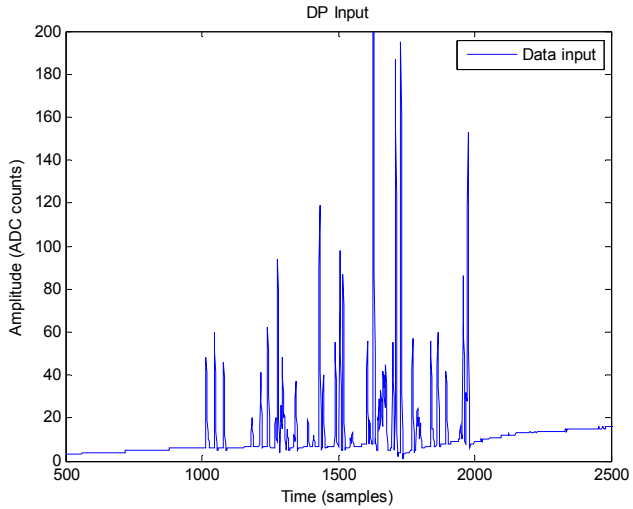
DP simulation results

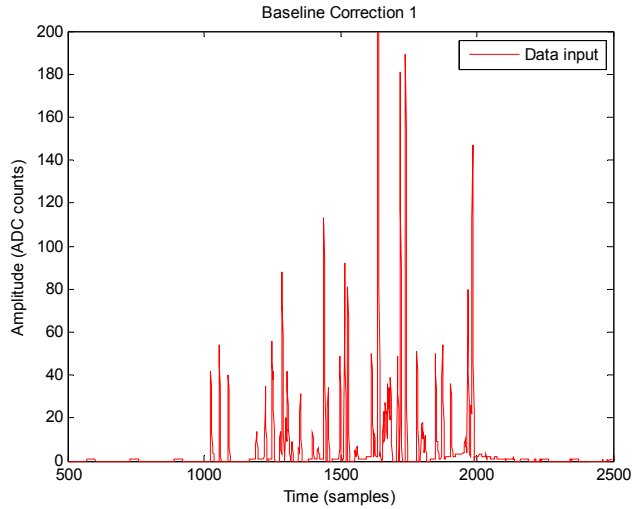




BC1 example test: rest of the filters are disabled.

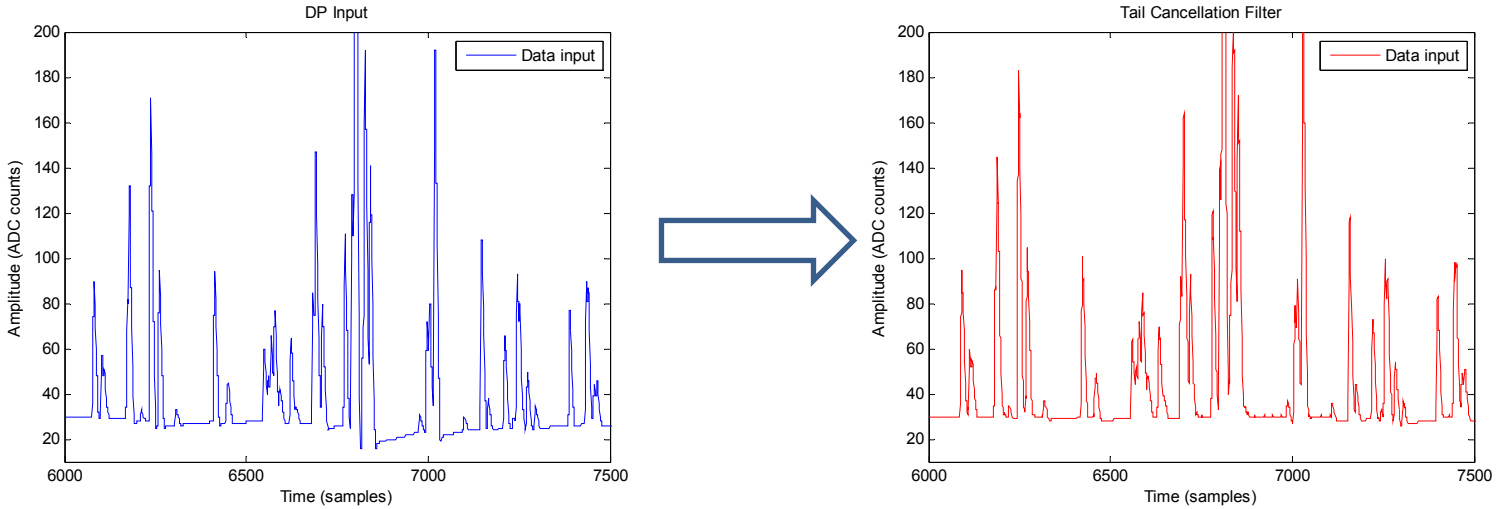
Eduardo Garcia





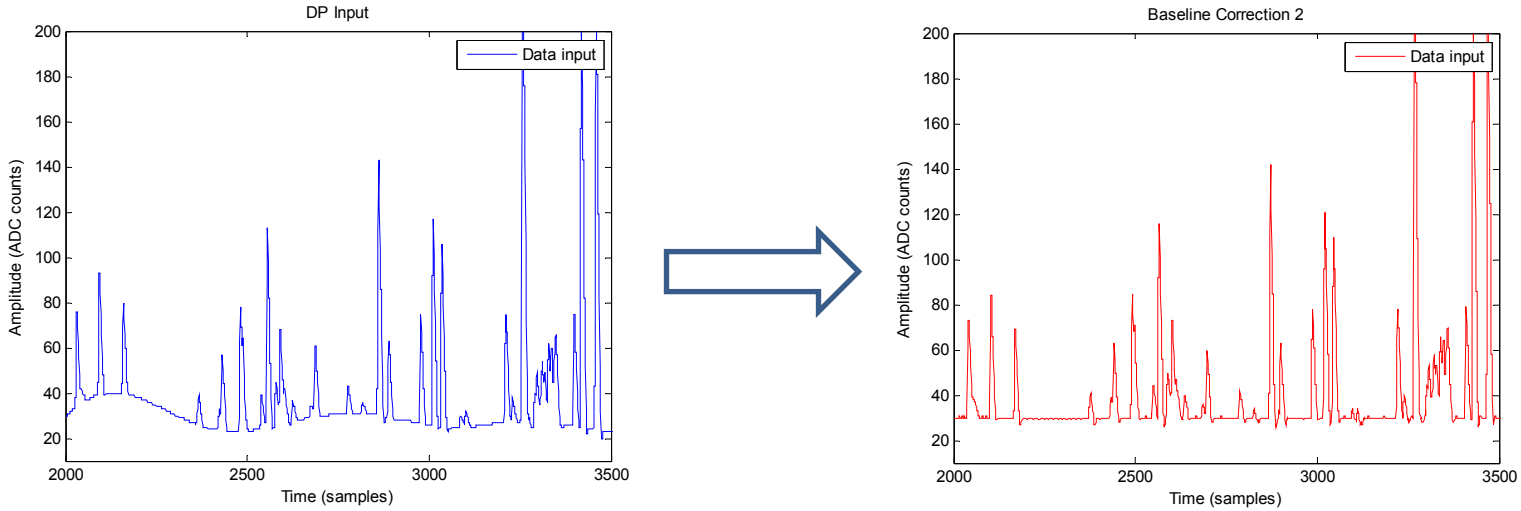
DP simulation results

- TCF example test: rest of the filters are disabled.

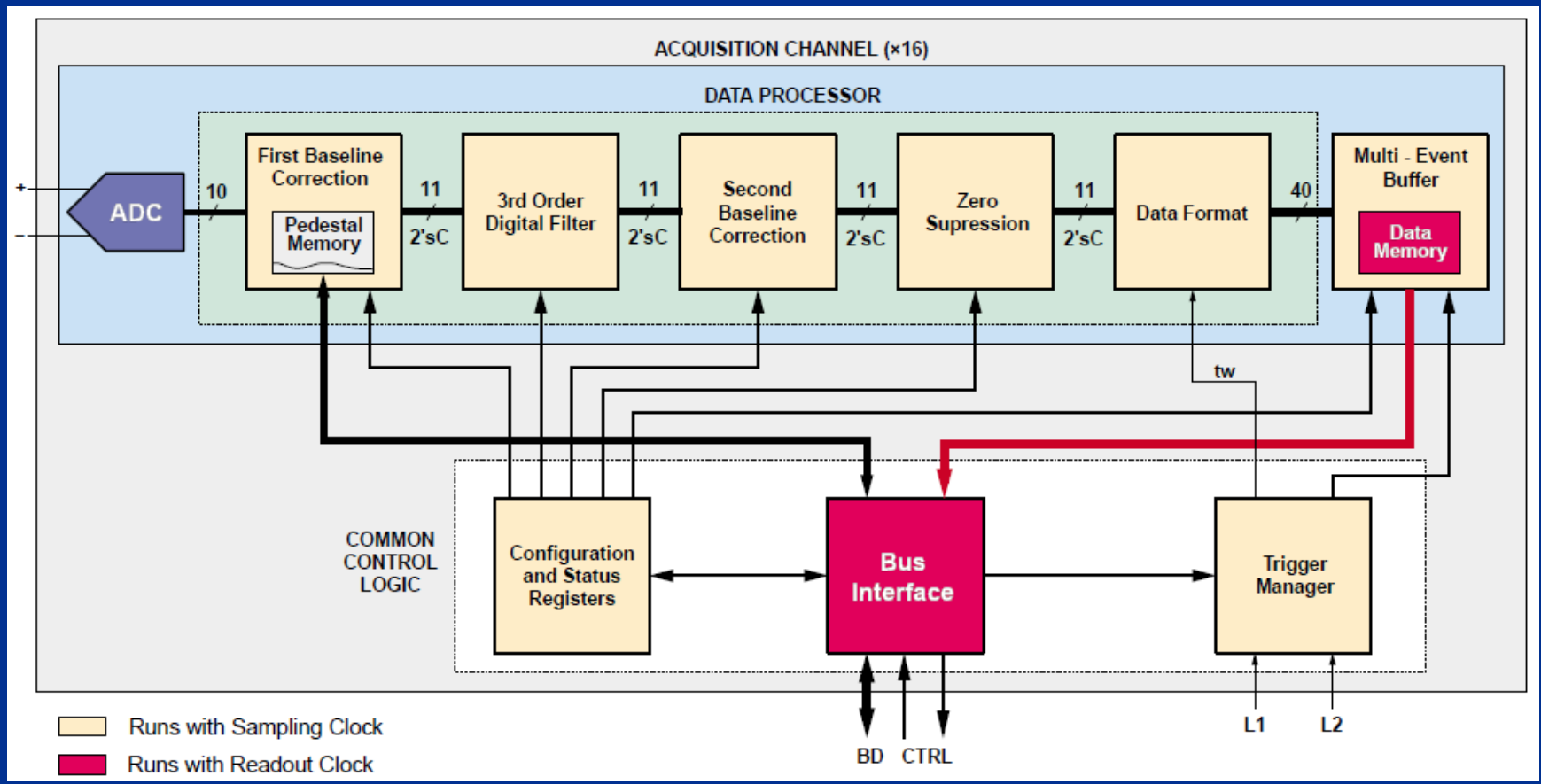


- BC2 example test: rest of the filters are disabled.

Eduardo Garcia



S-ALTRO DP plus Altro control and interface

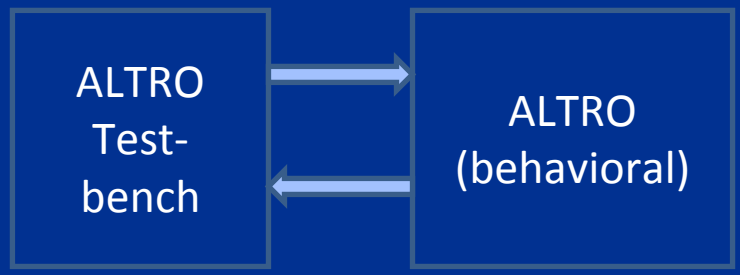


L1: Starts the data acquisition.
L2: Validates data from previous L1.
BD : 40 bit bidirectional bus; 20 bits address + 20 bit data. 80 Mbps readout.
CTRL : 6 bits including
Global Reset, Sampling and Readout clocks.

Eduardo Garcia

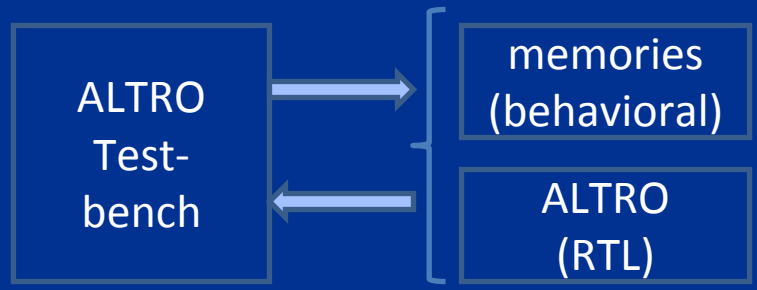
Interface, control and memories simulated in 3 stages.

1st step

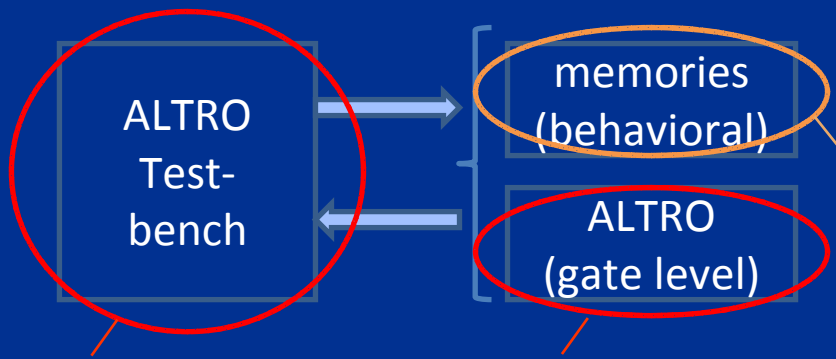


Verilog code validated with the current ALTRO design

2nd step



3rd step



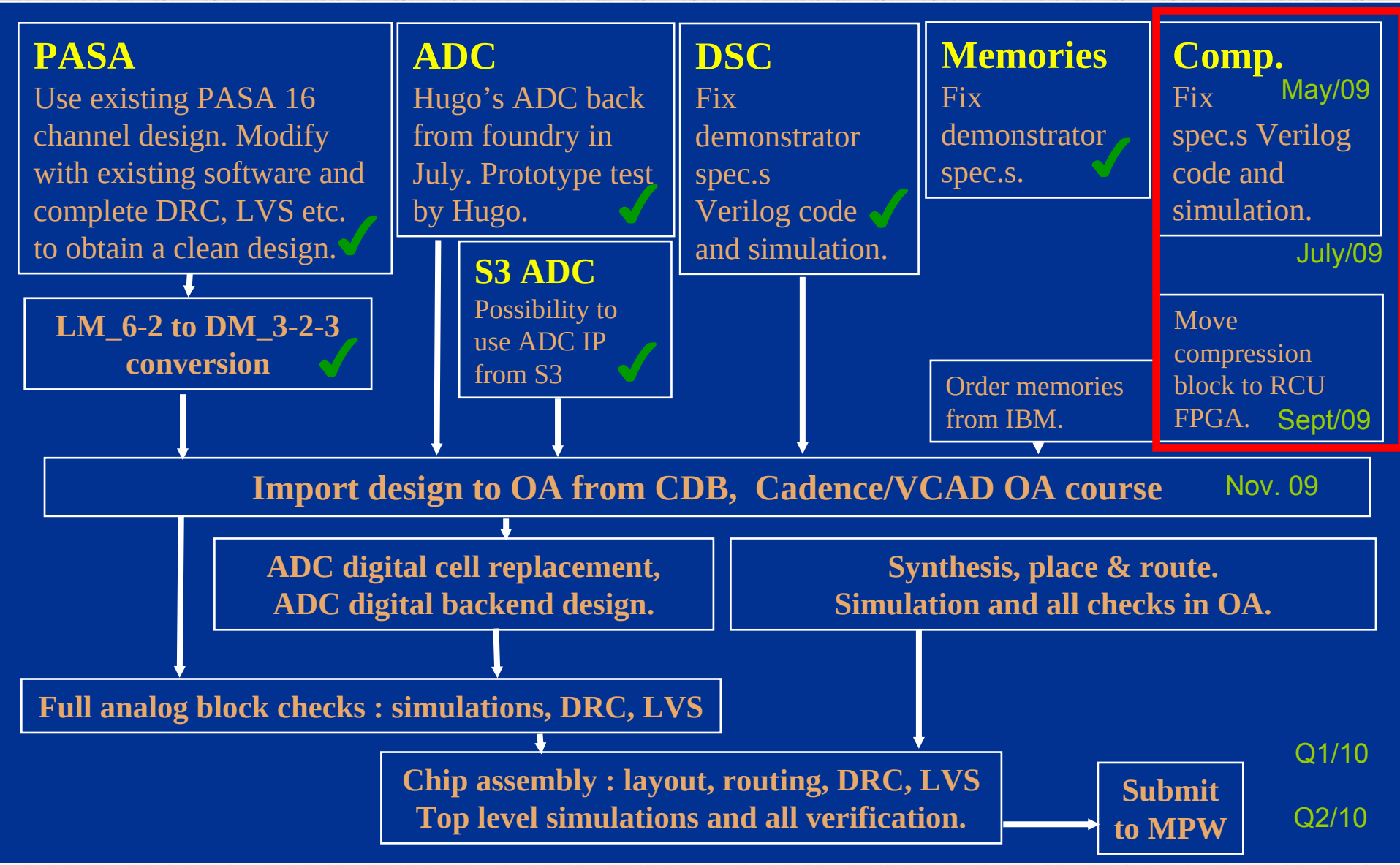
Eduardo Garcia

To do :

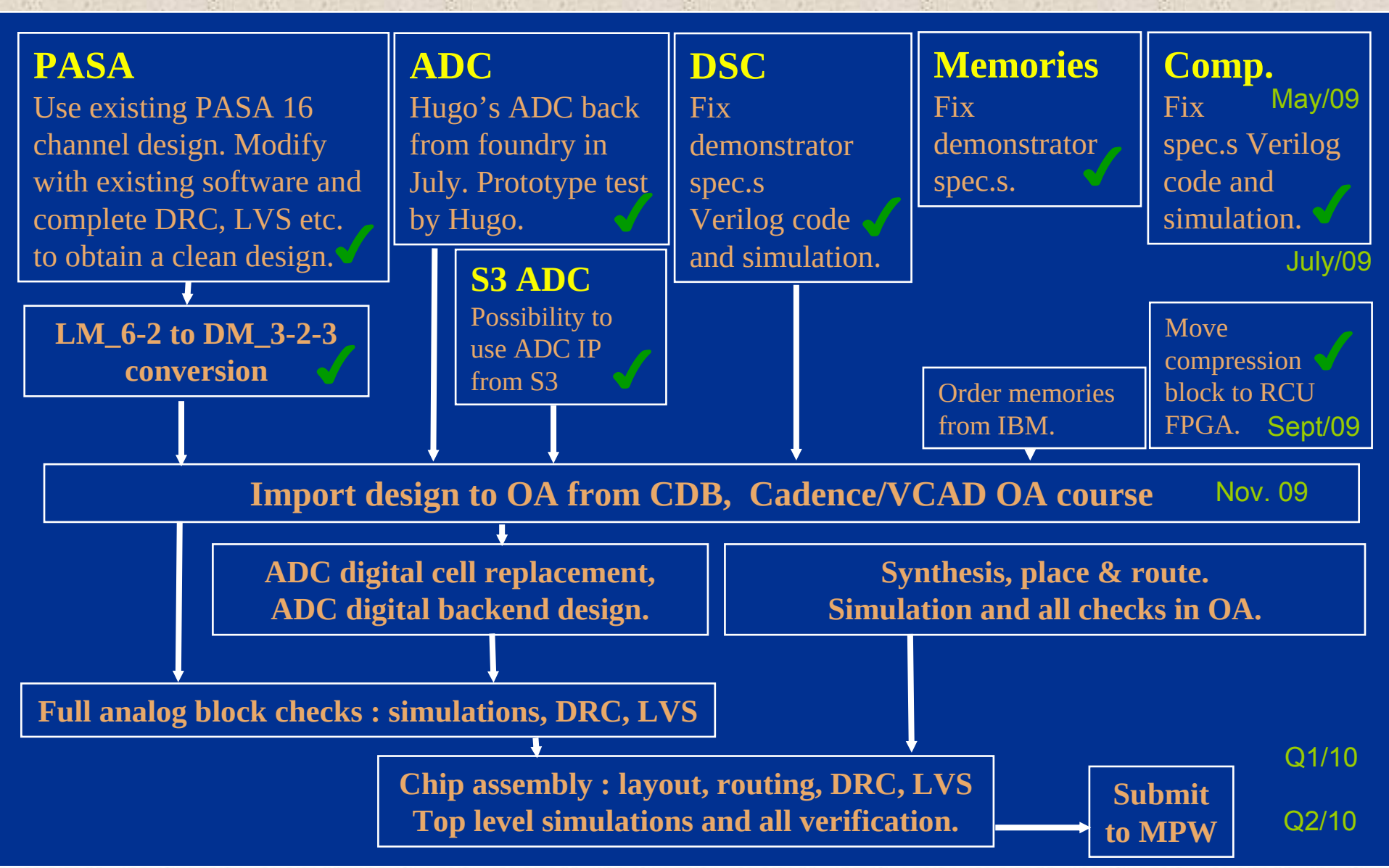
Add additional DP options intended for the demonstrator.

Include the IBM memories

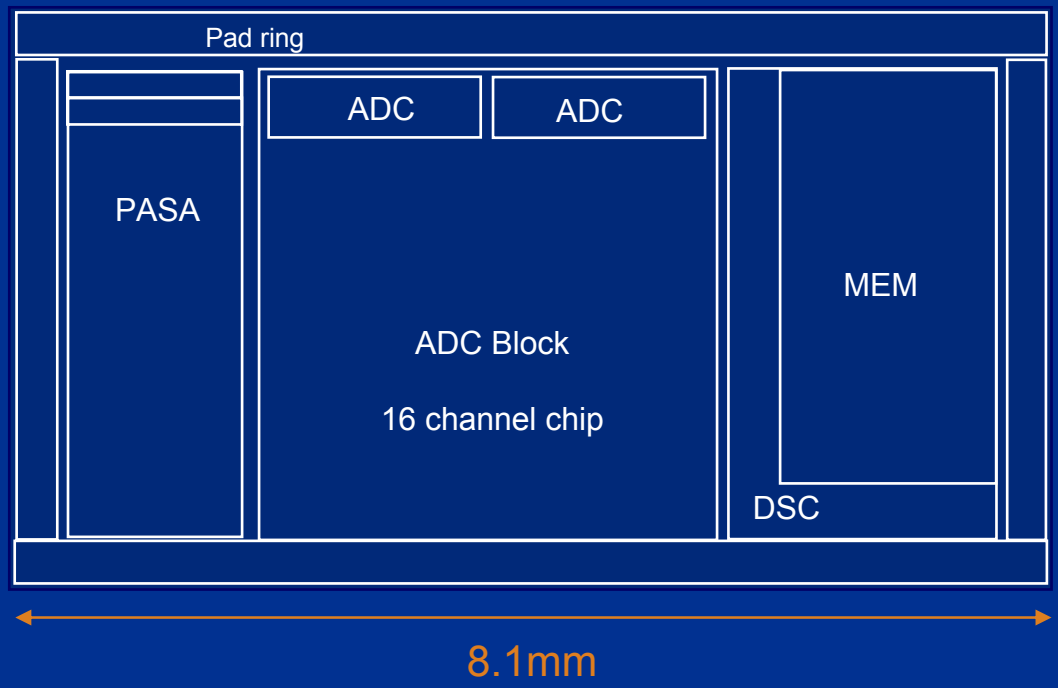
Demonstrator work flow



Demonstrator work flow



Demonstrator floor plan



DSC
16 channels = 1.8mm^2.

Control 0.06mm^2

MEM
DSC look-up tables ~ 1kByte/ch. (10 bits wide),
MEB = 1kByte/ch. (40 bit wide)

~ 6.2mm^2 ± 20% for 16 ch.

DSC + MEM ~ 8mm^2.

PASA channel = 1.4mm x 0.2mm,
16 channels = 1.4mm x 3.6mm (3.2mm + 400um power routing)

ADC = Hugo 1.57mm x 0.45mm,