Access to ASIC design tools and foundry services at CERN for SLHC

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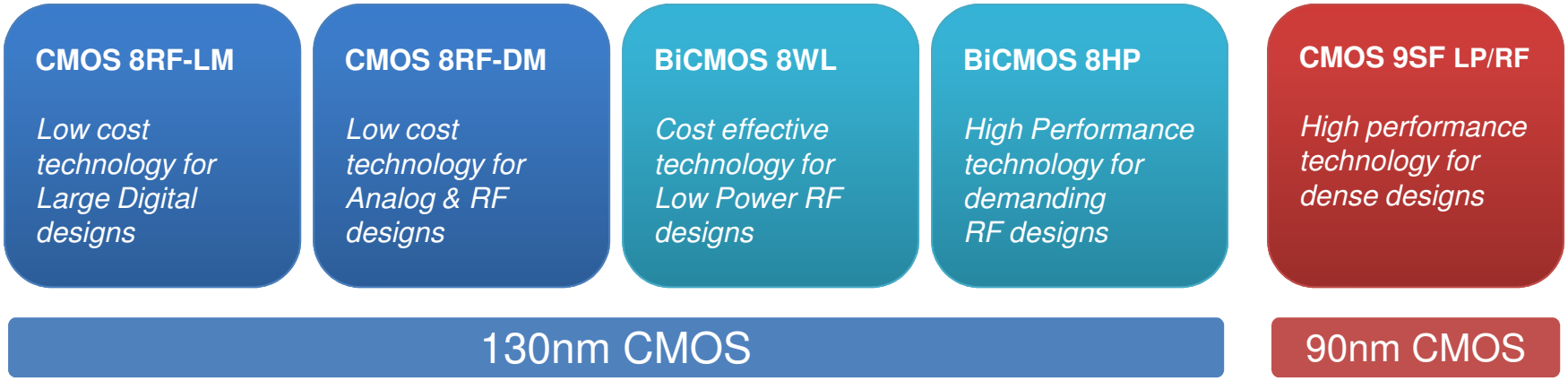
ASIC Technology Support

Overview of Technologies



- Access to Foundry services & Technology technical support.
- 130nm (CMOS & BiCMOS) and 90nm contract available since 6/2007.
- Future technologies can be negotiated with the same manufacturer, once the necessity arise.

Challenges

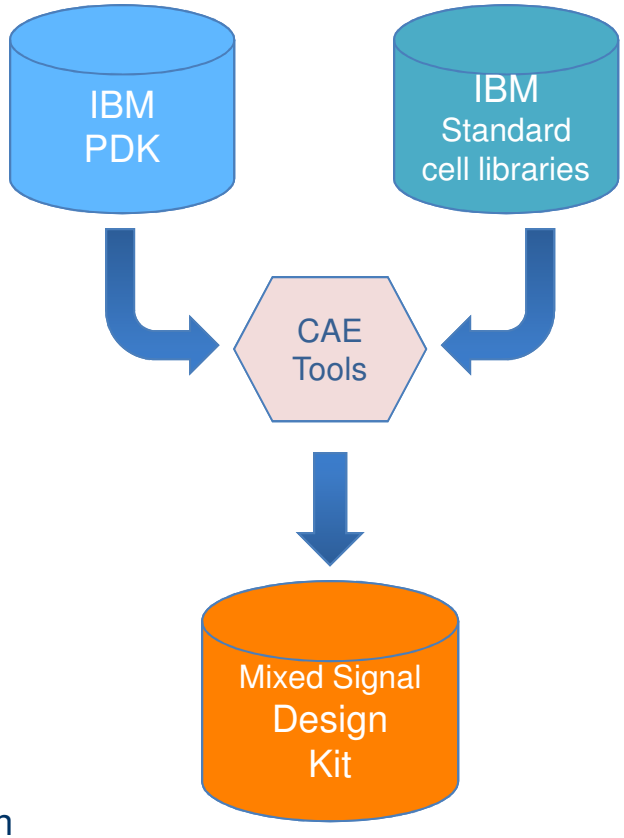
- Technology
  - Complex physical design rules and Manufacturability constrains.
  - Multiple corners for design simulations.
  - Tough Signal Integrity issues, and difficult final Timing Closure.
  - Expensive prototyping.
- CAE Tools
  - Multiplicity of tools and complicated - non linear - design flows.
  - Numerous data formats used when interfacing tools from different tool vendors.
- Designs
  - Demanding Power analysis and power management.
  - Chip level integration and assembly.
  - Large chips require to extend design efforts to multiple teams across geographically distributed institutes.

Objectives

- Development of:
  - “Mixed Signal Design Kit”
  - “Analog & Mixed Signal Methodologies (Workflows)”
- Provide:
  - Maintenance
  - Training
  - Support

Mixed Signal design kit

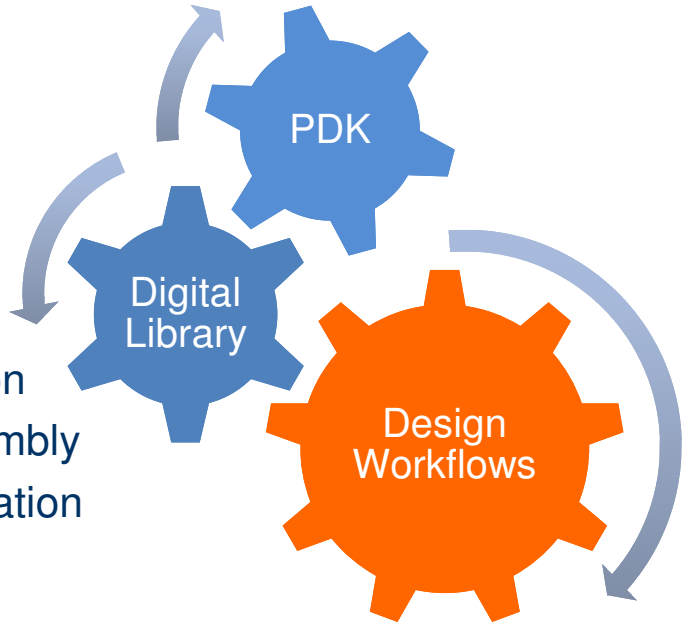
- Key Features:
  - IBM PDK V1.6
  - IBM Standard cell and IO pad libraries
    - Physical Layout views available.
    - Separate substrate contacts for mixed signal low noise applications.
    - Access to standard cells libraries is legally covered by already established IBM CDAs
  - New versions of CAE Tools
    - Open Access database support for increased interoperability of Virtuoso and SOC-Encounter environments.
    - Compatible with the “Europractice” distributions.
      - Virtuoso IC 6.1.3, Analog front-end design
      - SOC Encounter 7.1 Mixed signal back-end design
      - IUS 8.1 support for simulations.
      - Calibre support for Sign-Off Physical Verification
  - Support for LINUX Platform (*qualified on RHEL4*)



- Two independent design kits:
  - CMOS8RF-LM (6-2 BEOL)
  - CMOS8RF-DM (3-2-3 BEOL)

CMOS8RF Mixed Signal Workflows

- Analog & Mixed Signal (AMS) Workflows.
  - Standardized, validated Design Workflows
  - Top-down design Partitioning.
  - Digital Block implementation flow
    - *Presentation by Sandro Bonacini (CERN)*
  - Mixed-Signal Simulation & design Concept Validation
  - Hierarchical design Floorplaning and Physical Assembly
  - Design Performance Validation and Physical Verification



- CERN – VCAD Cadence - IBM collaboration
  - VCAD brought in their invaluable expertise on the CAE tools
    - *Presentation by Bruno Dutrey (VCAD)*
  - IBM provided the physical IP blocks and important technical assistance
  - CERN assists the development and validates the design kit functionality

Design Kit Distribution

- The Design kit will be made available to collaborating institutes.
  - No access fees required.
  - Pay-per-use scheme.
    - Some small fees will be applied when prototyping the designs through CERN,
    - This should cover part of the design kit maintenance costs in the long term.
  - Planned for release in October 2009.
  - Announcement by e-mail to the “130nm user list”.

- Acquiring the CMOS8RF Mixed Signal Design Kit
  - Contact Bert.Van.Koningsveld@cern.ch
    or Kostas.Kloukinas@cern.ch
  - Establish a CDA with IBM (if not already in place).
  - Granted access to the CERN ASIC support web site.

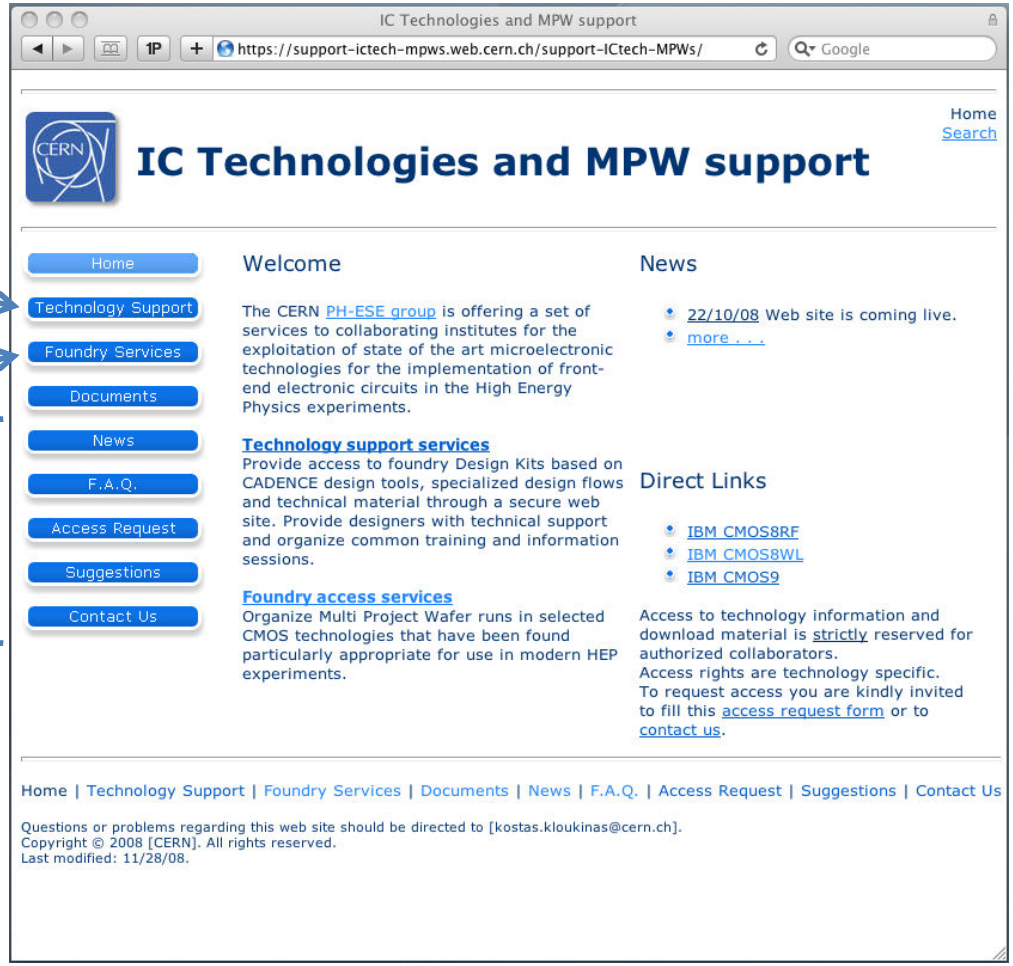
The CERN ASIC support website

http://cern.ch/asic-support

Download Design Kits and access technical documents (**restricted access**)

Information about MPW runs and foundry access services.

Communicate news and User support feedback forms and access request forms.



This website replaces our ‘afs’ based download facility.

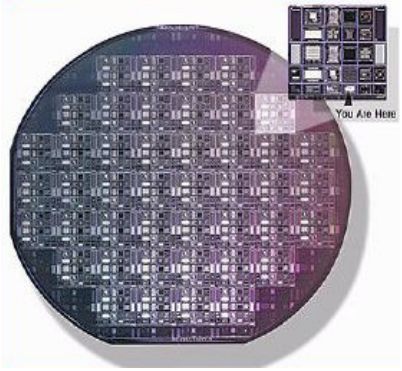
User Support and Training

- Maintenance
  - Distribution of:
    - IBM PDK updates.
    - Design Flow updates and enhancements.
    - Updates to accommodate new releases of CAE tools.
- User Support
  - Limited to the distributed Design Kit version, running under the supported versions of the CAE design tools.
- Training sessions organized at CERN
  - Scheduled sessions:
    - 1st session: 26 to 30 October (CERN internal)
    - 2nd session: 16 to 20 November (open to external engineers)
    - 3rd session: 30 Nov to 4 December (open to external engineers)

Foundry Access Services

Access to Foundry Services

- Supported Technologies:
  - IBM CMOS6SF (0.25μm), legacy designs
  - IBM CMOS8RF (130nm), mainstream process
  - IBM CMOS8WL & 8HP (SiGe 130nm)
  - IBM CMOS9SF (90nm)



- MPW services:
  - CERN offers to organize MPW runs to help in keeping low the cost of fabricating prototypes and of small-volume production by enabling multiple participants to share production overhead costs.
  - CERN has developed very good working relationships with the MPW service provider MOSIS as an alternate means to access silicon for prototyping.
- Engineering runs
  - CERN organizes submissions for design prototyping and small volume production directly with the foundry.

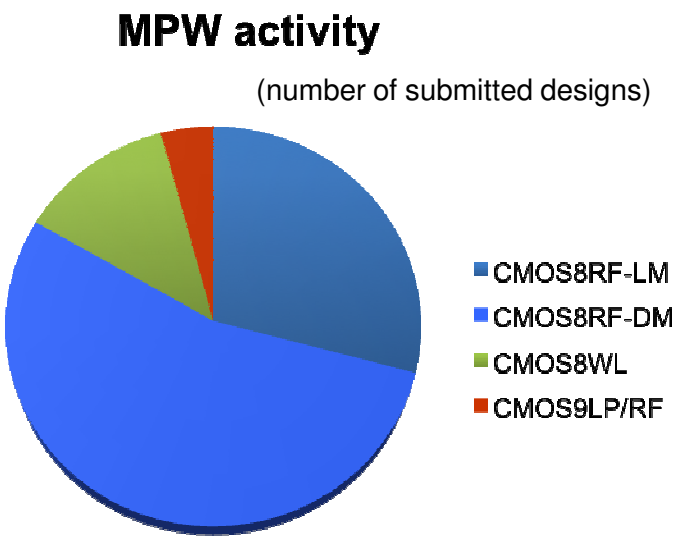
MPW runs with MOSIS

- CERN made extensive use of the MOSIS CMOS8RF MPWs last year.
  - The break-even point for the cost of a CERN MPW and a MOSIS MPW is ~150mm^2.
- Better pricing conditions for the CMOS8RF MPW services
  - MOSIS recognized the central role of CERN in research and educational activities.
  - 35% cost reduction compared to 2008 prices
  - Waived the 10mm2 minimum order limit per submission
  - CERN appreciates the excellent collaborating spirit with MOSIS
- Convenience of regularly scheduled MPW runs.
  - In 2008 there were 6 runs scheduled every 2 months.
  - In 2009 there will be 4 runs scheduled every 3 months.
- Convenience for accommodating different BEOL options:
  - DM (3 thin - 2 thick – 3 RF) metal stack.
  - LM (6thin – 2 thick) metal stack.
  - C4 pad option for bump bonding.

Prototyping activity with MOSIS

2008 - 2009

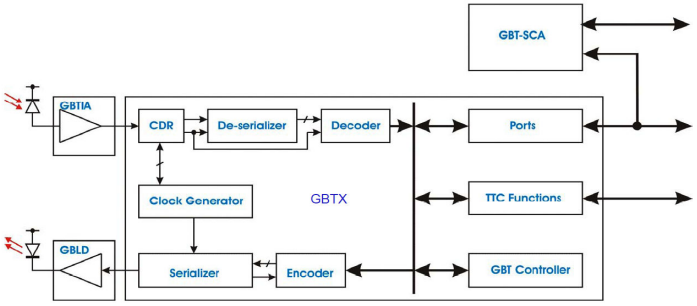
- CMOS8RF (130nm)
  - 20 designs on 5 MPW runs
    - 7 runs organized, 2 canceled by MOSIS due to insufficient number of designs
    - 2 to 8 designs per MPW run
    - Smallest design 1 mm^2, largest design 20 mm^2
    - 13 designs on 8RF-DM and 7 designs on 8RF-LM
  - 100 mm^2 total silicon area
- CMOS8WL (130nm SiGe)
  - 3 designs on 1 MPW run
  - 10 mm2 total silicon area
- CMOS9LP/RF (90nm)
  - 1 design of 4mm^2 on 1 MPW
- Re-fabrication requests: 2 designs on 8RF and 2 designs on 8WL



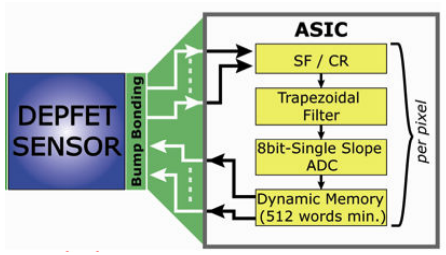
Major Projects

not a comprehensive list

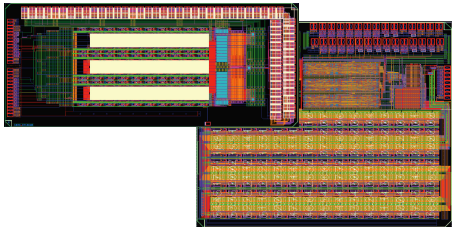
- Gigabit Transceiver Project (GBT)
  - "GBLD" Gigabit Laser Driver chip
  - "GBT-TIA"Tranimpedance Amplifier chip
  - "e-link" test chip
  - "GBTX", first prototype transceiver chip (2009Q4 MPW)



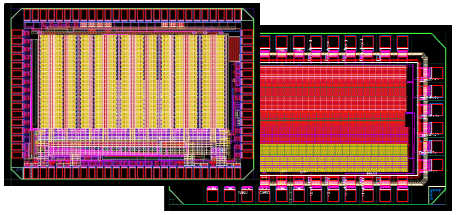
- DSSC Project for the XFEL Synchrotron Radiation Source
  - DRAM test chip, SRAM, test chip, some digital blocks
  - Front-End with source follower readout for DEPFET
  - Front-End with drain follower readout for DEPFET
  - Current-mode trapezoidal filter
  - First proto with all elements in the pixel, bump test chip (2010 MPW)



- NA62 Pixel Gigatracker detector
  - Readout test chip with ON pixel TDC cell
  - Readout test chip with End-Of-Column TDC cell



- ATLAS PIXEL 'b-layer upgrade'
  - Discriminator test chip
  - SEU evaluation test chip
  - FEI4 first full scale prototype chip (2009Q4 engineering run)



Prototyping activity with IBM

2008 - 2009

- CMOS8RF Engineering run **submitted** in 2008Q3.
  - "MEDIPIX-3" PIXEL matrix readout chip.
  - Size: 14 X 17 mm^2
  - 12 wafers ordered.

- CMOS8RF **scheduled** Engineering run
  - "FEI4", ATLAS PIXEL readout chip
  - 19 X 20 mm^2
  - Tape out : 2009Q4

Wrap-Up

- Technology support & foundry services.
  - Provide standardized common design kits and design flows.
  - Provide access to advanced technologies by sharing expenses.
  - Organize common Training and Information sessions.
  - Collective activities help to minimize costs and effort.

- Availability of foundry and technology services is modulated by user's demand.

- Contacts:
  - Organizational issues, contracts etc.:
    - Alessandro.Marchioro@cern.ch
  - Technology support & Foundry services:
    - Kostas.Kloukinas@cern.ch
  - Access to design kits and installation:
    - Bert.van.Koningsved@cern.ch

THANK YOU

Mixed Signal Design kit

- Objectives
  - Development of a “Design Kit” for Mixed Signal environments.
    - With integrated standard cell libraries.
    - Establish well defined Analog & Mixed Signal design workflows.
    - Targeted to **big “A”** (analog), **small “D”** (digital) **ASICs**.
    - Implemented on modern versions of CAE Tools.
  - Replace our previous Design Kit distribution.
    - Based on the ARM/ARTISAN cells and an automated *digital only* design flow.
    - Making use of old versions of CAE tools.
    - Two years in service.
    - Already distributed to 25 institutes
    - Users can continue using the old design kit and the ARM libraries since they have signed NDAs directly with ARM. Maintenance and technical support will be provided by ARM.

MR Design kit