Chronopixe status

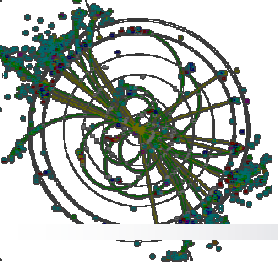
J. E. Brau, N. B. Sinev, D. M. Strom
University of Oregon, Eugene

C. Baltay, H. Neal, D. Rabinowitz
Yale University, New Haven

EE work is contracted to Sarnoff Corporation

Outline of the talk

- Brief remainder how it works
- Milestones
- Test stand at SLAC
- Test results
  - Problem with power distribution found
  - Performance parameters
  - Noise level
  - Comparators offsets spread
  - Fe55 source test
  - Leakage currents.
- Conclusions
- Next steps



How Chronopixel works

- When signal generated by particle crossing sensitive layer exceeds threshold, snapshot of the time stamp, provided by 14 bits bus is recorded into pixel memory, and memory pointer is advanced.
- If another particle hits the same pixel during the same bunch train, second memory cell is used for this event time stamp.
- During readout, which happens between bunch trains, pixels which do not have any time stamp records, generate EMPTY signal, which advances IO-MUX circuit to next pixel without wasting any time. This speeds up readout by factor of about 100.
- Comparator offsets of individual pixels are determined in the calibration cycle, and reference voltage, which sets the comparator threshold, is shifted to adjust thresholds in all pixels to the same signal level.
- To achieve required noise level (about 25 e r.m.s.) special reset circuit (soft reset with feedback) was developed by Sarnoff designers. They claim it reduces reset noise by factor of 2.

Sensor design

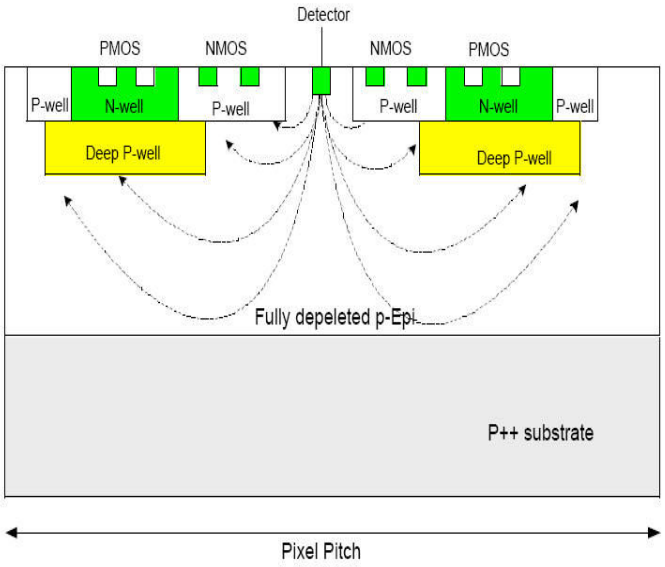


Figure 11.1 Proposed pixel architecture employing the deep p-well layer

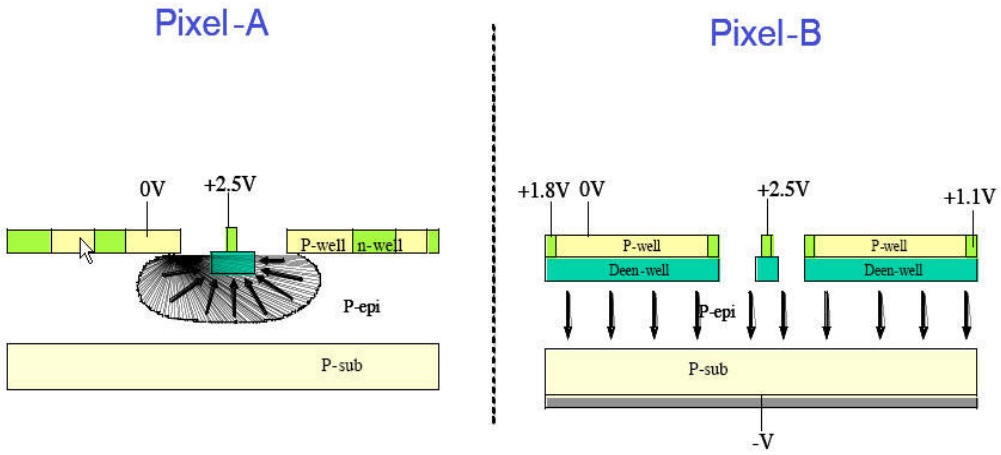


Figure 6.3 Comparison of the vertical cross section views of two pixels

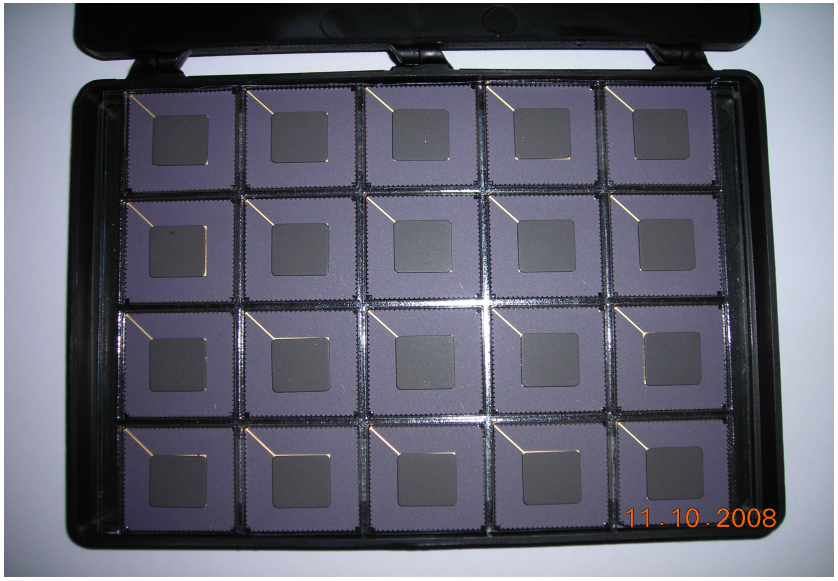
Ultimate design, as envisioned

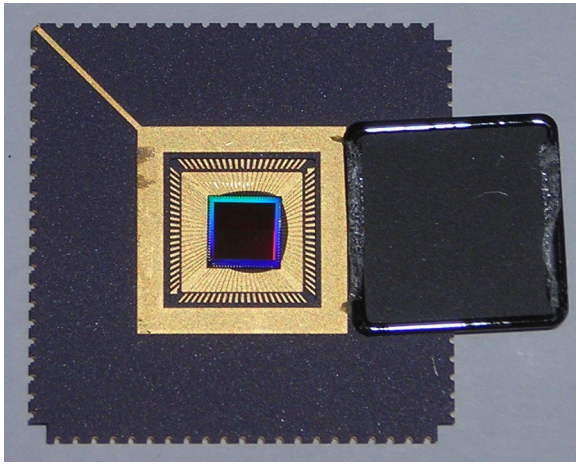
Two sensor options in the fabricated chips

- **TSMC process does not allow for creation of deep P-wells. Moreover, the test chronopixel devices were fabricated using low resistivity (~ 10 ohm*cm) epi layer. To be able to achieve comfortable depletion depth, Pixel-B employs deep n-well, encapsulating all p-wells in the NMOS gates. This allow application of negative (up to -10 V) bias on substrate.**

Milestones

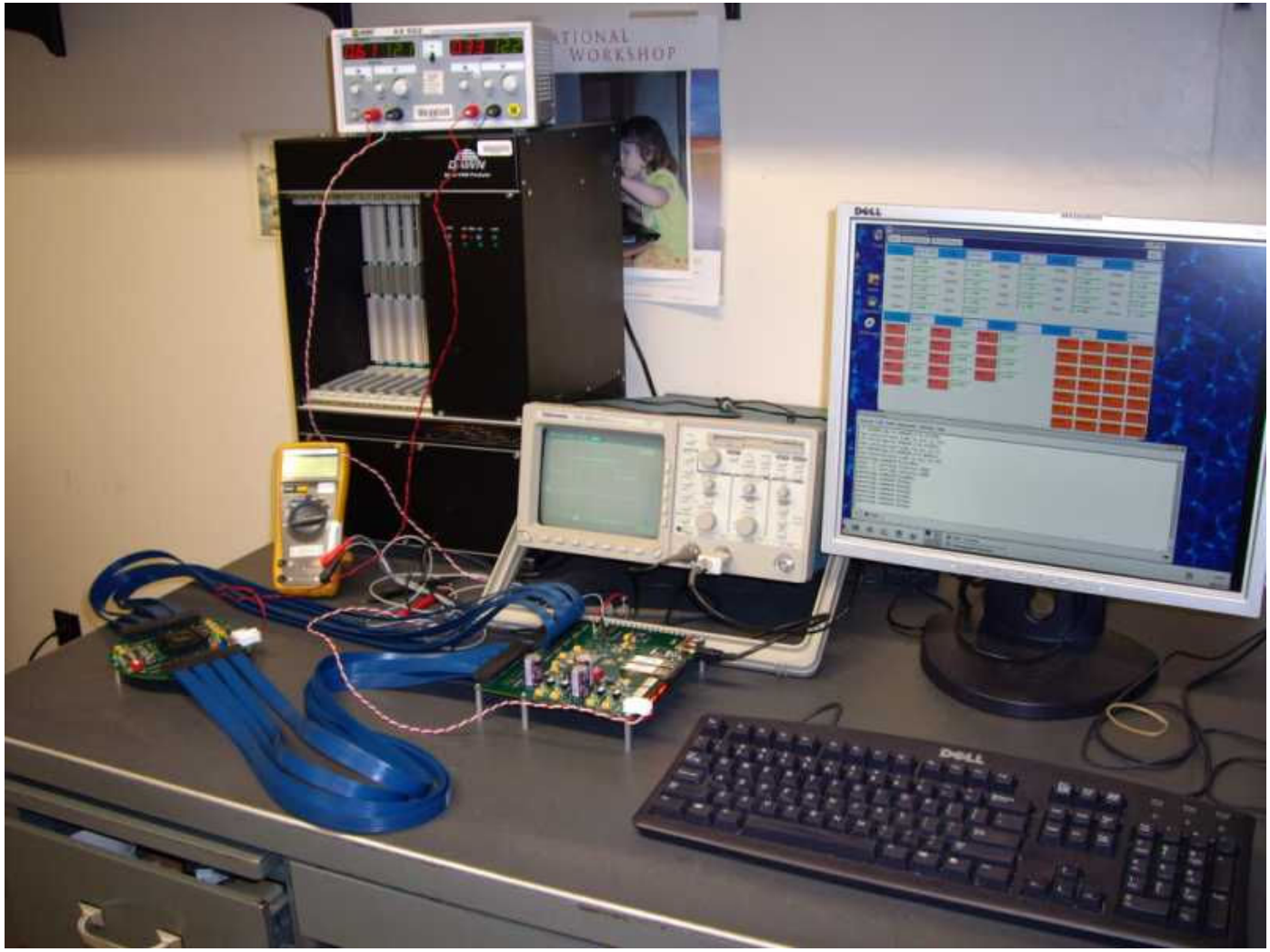
- January, 2007
  - Completed design – Chronopixel
    - **2 buffers, with calibration**
- May 2008
  - Fabricated 80 5x5 mm chips, containing 80x80 50 μm Chronopixels array (+ 2 single pixels) each
  - TSMC 0.18 μm ⇒ ~50 μm pixel
    - Epi-layer only 7 μm
    - Low resistivity (~10 ohm*cm) silicon
    - Talking to JAZZ (15 μm epi-layer)
- October 2008
  - Design of test boards started at SLAC
- June 2009
  - Test boards fabrication. FPGA code development started.
- August 2009
  - Debugging and calibration of test boards
- September 2009
  - Chronopixel chip tests started
- February 2010
  - Chronopixel chip tests completed





Test Stand at SLAC - GUI

Test stand is working !

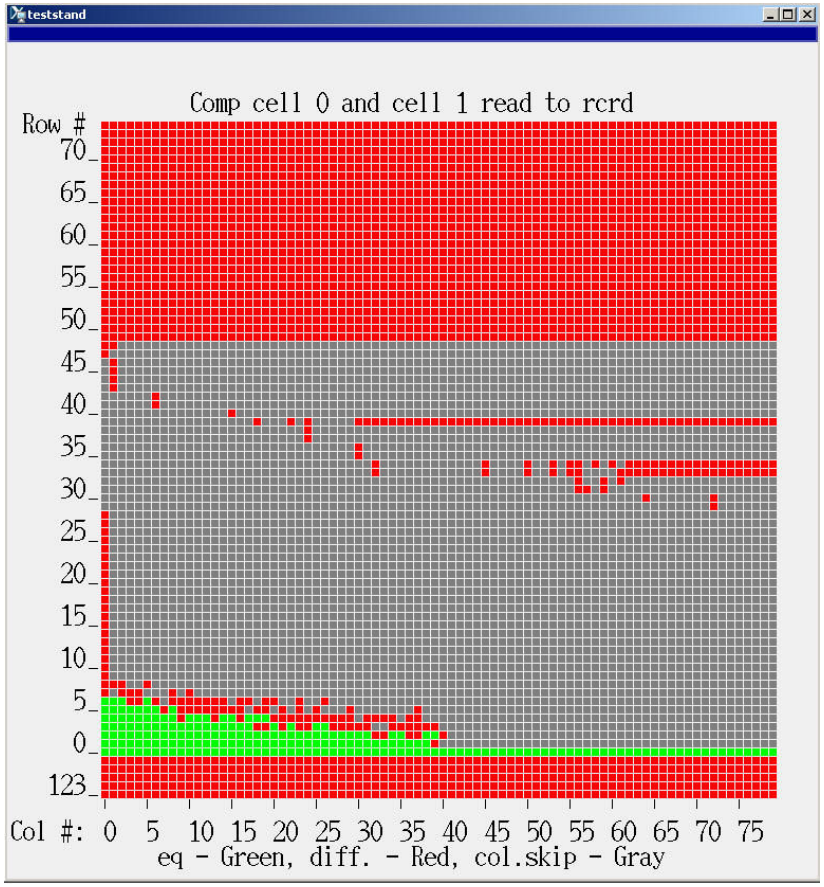


Test results for test pixels

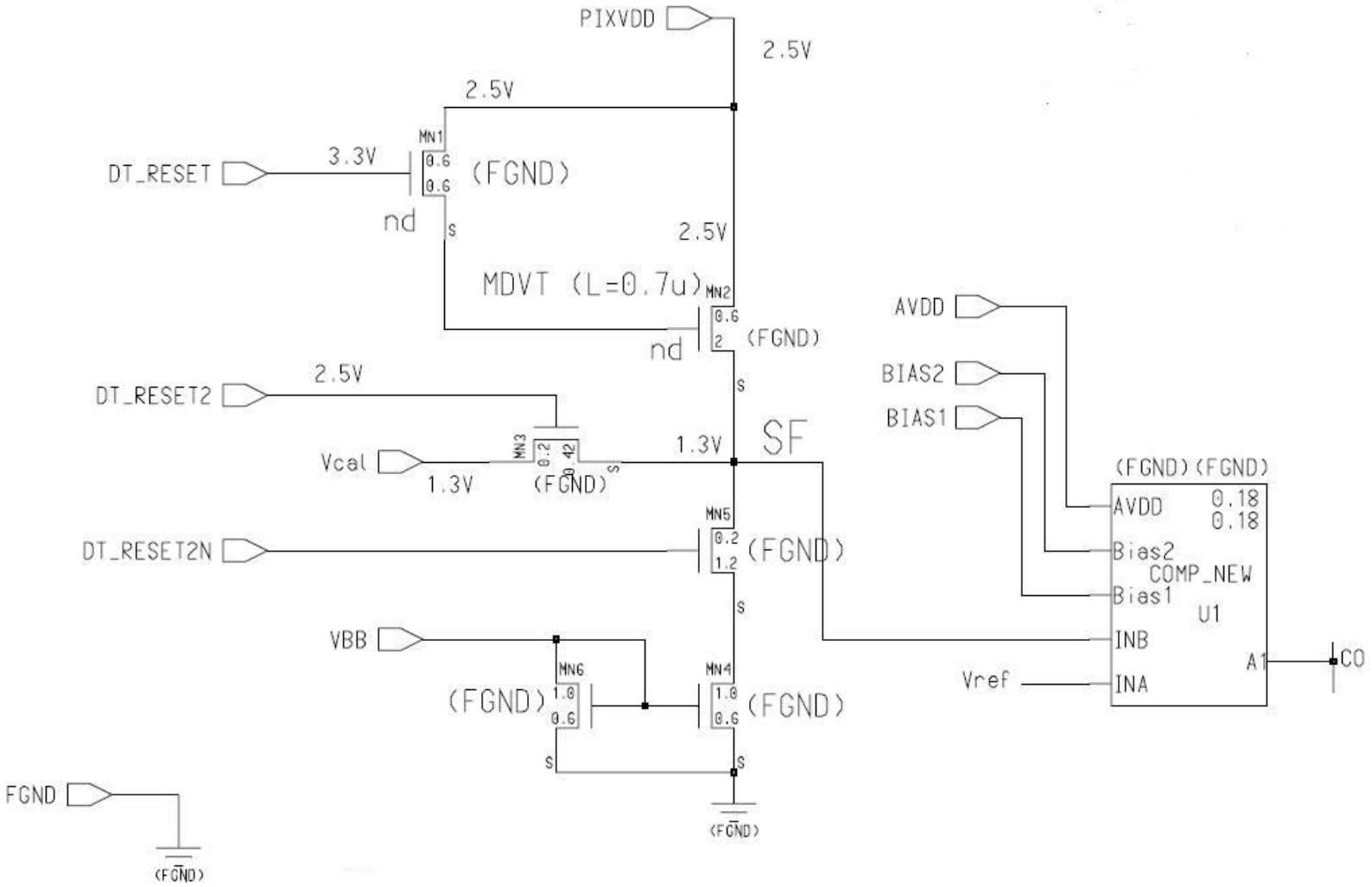
- As was mentioned earlier, in addition of array of 6400 pixels, each chip contains 2 test pixels, which could be accessed without involving addressing logics. This pixels were tested first, and it was found:
  - Memory operations are working as designed. Maximum timestamp recording speed – 7.27 MHz (we need at least 3 MHz).
  - Calibration circuit operates properly.
  - Noise level looks like higher than expected. However, because it is difficult to make test with Fe55 source with single pixel (too small area), we can't express noise in the units of charge. From the estimation of sensor capacitance (~ 7.5 fF) we expect reset noise at the level of 800 μV, measured value ~ 1.3 mV. From Fe55 signal in pixel array, sensor capacitance is rather 4.5 fF, so measured noise is 36.4 e. Specification is 25 e. But for single pixel we can't implement "soft reset", which, by designers claim should reduce noise by factor of 2. So final noise figures will be discussed in pixel array test results.

Pixel array: Problems with power distribution

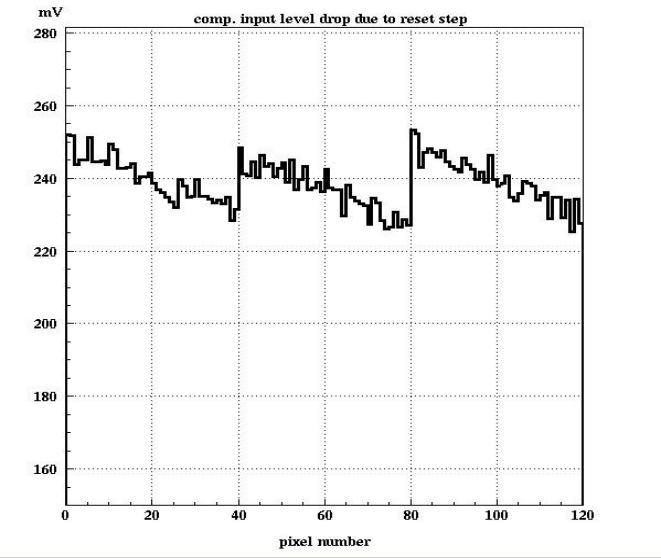
- Correct memory operation for array of 6400 pixels is shown with green color. Readout starts from non-existing row 123 to make sure correct operation of row 0 is not correlated with it to be first in readout sequence.
- As we can see, only 3 first rows of pixels A (columns 0-40) and 1 row of pixels B shows correct memory operations.
- Gray color corresponds to pixels, claiming they are "empty", do not have anything recorded.
- Red color corresponds to pixels, which have different read back value from the written to memory value.

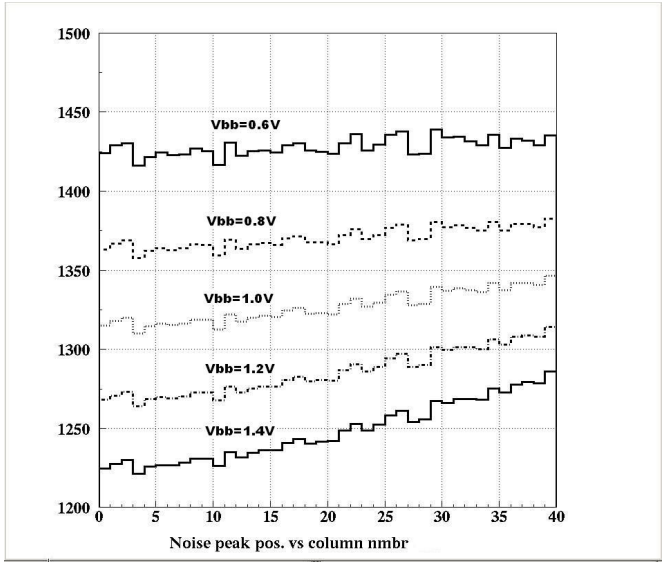


Around sensor schematics



Power distribution problem





- On the left you can see the value of crosstalk in individual pixels for 3 rows of pixels A from pixel reset signal. This signal is formed in each pixel and has amplitude equal to 3.3V supply. We can see, that signal is larger at the start of the row. This tells us, that 3.3V drops as it reaches farther along row.
- Same can be seen from right plot. It shows source follower output level for different pixels depending on the Vbb bias. This bias control current through source follower, and higher bias value leads to lower output level. So, Vbb also drops along row.

Power distribution problem (why?)

- The resistivity of most metal layers in TSMC 0.18 process is 80 mohm/□. So, with trace width 0.23 μm 1 cm trace would have resistivity of 3.5 Kohm. Middle of the row is 2 mm from the edge, so current 0.6 mA will create 0.3 V voltage drop.
- And result of it is, that in the fabricated prototypes only few first rows are working (in fact, only one first row for pixels B, and 3 rows for A) . It was found, that most critical is the drop of 1.8 V supply (may be just because it is highest current circuit). And we can slightly increase number of operating rows by boosting 1.8 V supply to 2.1 V.

Noise measurements

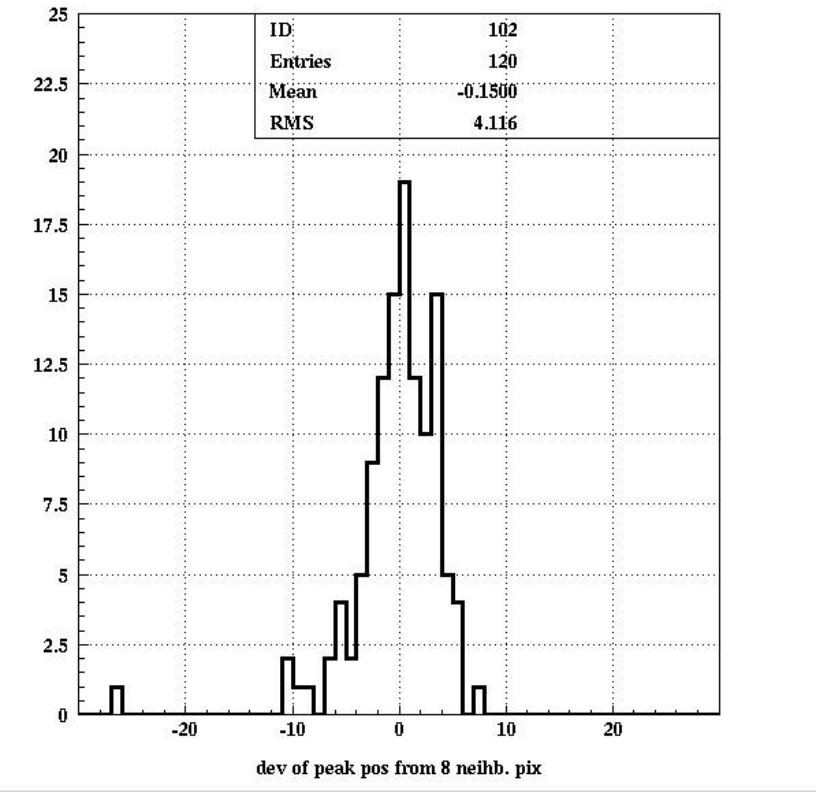
- It is expected, that major noise contributor is so-called "reset noise" or "kTC" noise – the thermal noise on the RC circuit. It does not depend on R, but if R is low, the bandwidth of the comparator may be not enough to see high frequency components. We can adjust the reset gate resistance by changing 3.3V supply and see that noise reaches reset noise values. This is most clean method, as it does not involve pulse on reset gate, which can lead to additional noise from cross talks. From calculations, noise level is ~ 2000 µV/sqrt(C(fF)). For pixels A observed noise is 1.13 mV, which corresponds to C=3.1 fF. Another method – measurement after reset gives 1.2 mV.
- If we try to estimate sensor capacitance from sensor area and depletion depth for 10 ohm·cm silicon, we should expect C ~7.5 fF.
- So, may be resistivity of our silicon is a bit higher. Also, chip is certainly hotter, than room temperature. Anyway, estimation of the sensor capacitance, made from Fe55 signal indicates sensor capacitance value of about 4.5 fF - almost consistent with noise figure.

Soft reset works ?

- Varying reset pulse parameters, I was able to achieve noise distribution with σ=0.86 mV. This is better than noise measured with high resistivity of reset transistor (1.13 mV). So, may be special forming of reset pulse really helps. I did not have enough time to investigate this in details. And for pixels B I could not find such parameters that would noticeably improve noise compare to high resistivity measurements. Pixels B in general have much worse performance, but I don't know if it is because of deep n-well employed here, or just because they are farther on the power bus.

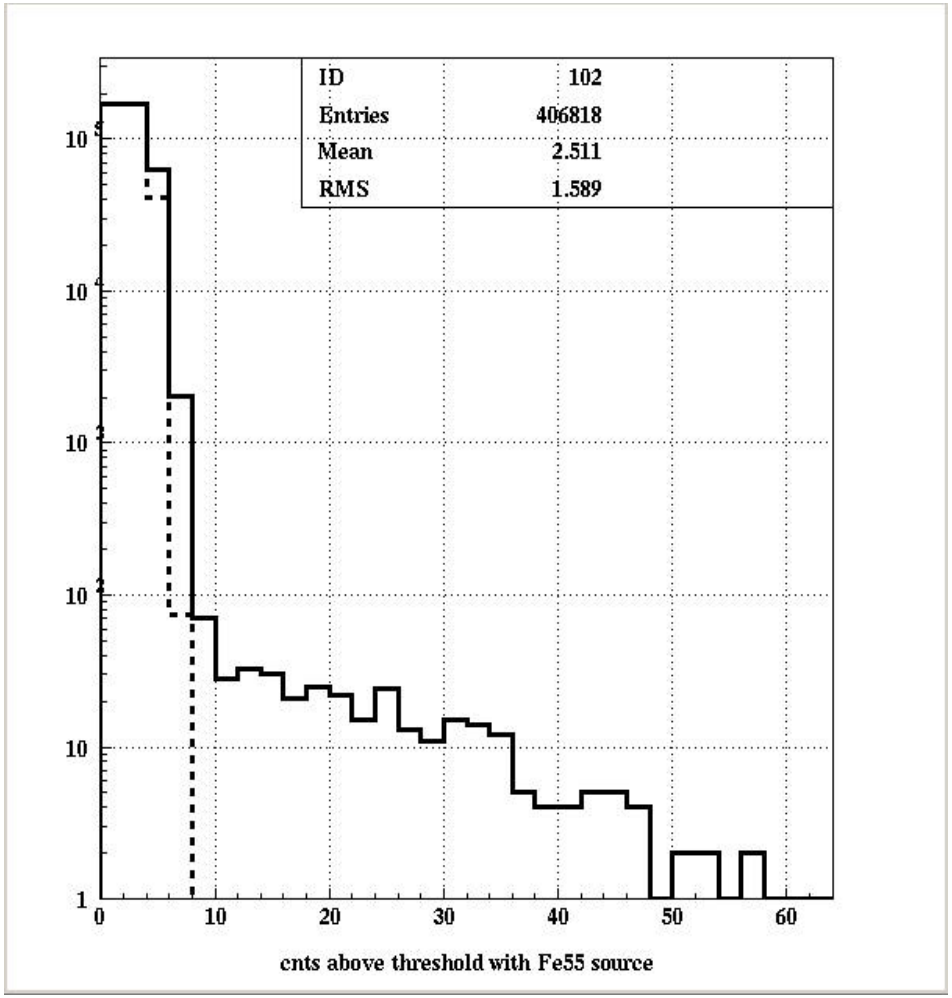
Comparator thresholds spread

- We need the ability to set thresholds in all pixels at the level of about 5 σ of noise with accuracy of about 1 σ. With specified sensors sensitivity of 10 μV/e and specified noise of 25 e, that means that after calibration threshold accuracy should be 250 μV, and from the fact that calibrator has 10 steps, total spread of comparator offsets before calibration should not be larger than 2.5 mV. From plot at right (after correction for systematic shift due to power problems) spread σ=4.1 mV, and full spread is 6 σ, 24.6 mV – 10 times we want. However, situation is a little better if we take into account that our real sensitivity is about 3.5 times higher than specified (see Fe55 test results).



Test with Fe55 source

- Distributions of number of hits above threshold with and without Fe55 source placed above chronopixel device are shown at right (without source – dashed line). Maximum signal seen is about 50 mV, and it corresponds to ~1400 e generated by Fe55 X-rays of 5.9 KeV. So, sensor sensitivity is ~35.7 µV/e , exceeding specified 10 µV/e.
- This sensitivity tells us, that sensor capacitance is ~4.48 fF (compare to estimation of 3.3 fF from noise measurement and 7.5 fF from sensor area and calculated depletion depth).



Leakage currents measurement.

- Moving sampling point relative to reset pulse, I was able to measure voltage drift of about **0.1 mV/μs** both for pixels A and B. Applying measured value of sensor capacitance 4.48 fF, we will get the value of leakage current of $4.48 \cdot 10^{-13}$ A per pixel, or $1.8 \cdot 10^{-8}$ A/cm^2 . This is comfortable value.

Conclusions

- Tests of the first chronopixel prototypes are completed.
- Tests show that general concept is working.
- Mistake was made in the power distribution net on the chip, which led to only small portion of it is operational.
- Calibration circuit works as expected in test pixels, but for unknown reason does not work in pixels array.
- Noise figure with "soft reset" is within specifications (0.86 mV/35.7μV/e = 24 e, specification is 25 e).
- Comparator offsets spread 25 mV is about 10 times larger than specified, but expressed in input charge (700 e) is only 2.8 times larger required (250 e). Reduction of sensor capacitance (increasing sensitivity) may help in bringing it within specs.
- Sensors leakage currents ($1.8 \cdot 10^{-8} A/cm^2$) is not a problem.
- Sensors timestamp maximum recording speed (7.27 MHz) is adequate.

Next steps

- We plan to meet SARNOFF engineers in the beginning of April to discuss design of the next prototype. In addition to fixing found problems, we hope to move to deep p-well process, which will allow us to have high efficiency of hit registration.
- Simultaneously with production of next prototype, test stand will be modified.
- We hope to get next prototypes by the end of the year 2010, and will start testing immediately.