BeamCal Instrumentation: ASIC Overview and Preliminary Tests Results

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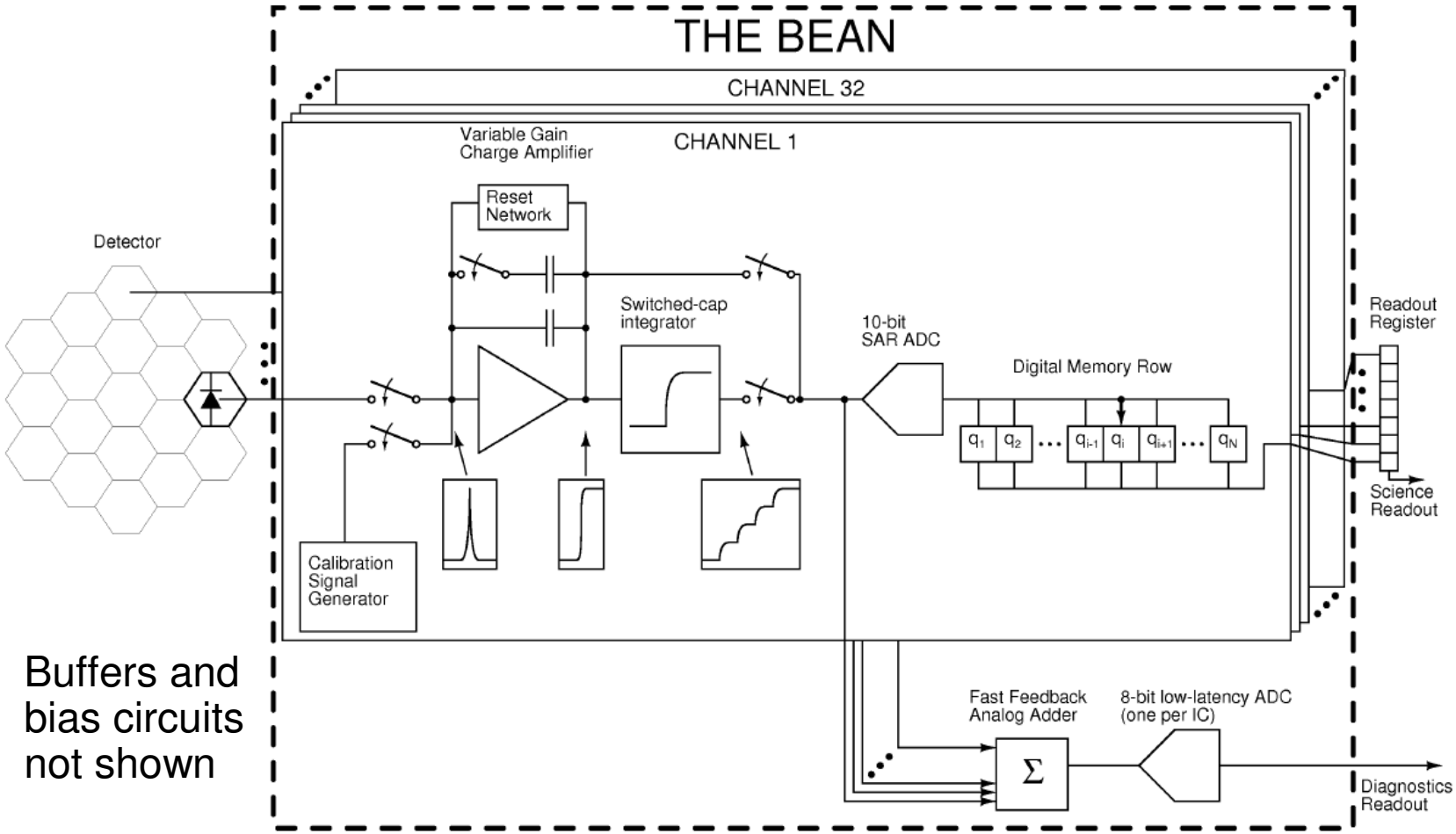
Outline

- BeamCal detector ASIC specs
- System-level design
- Circuit design
- Implementation
- Tests
  - Methodology
  - Results
- Conclusion and future work

BeamCal Detector ASIC Specs

- "High" input rate (3.25 MHz)
- High occupancy (100%)
- Large input signals (~40pC)
- Large input capacitance (~40pF detector + wires)
- High resolution (10 bits)
- Dual gain (50x) for different modes of operation: science and detector calibration
- Low latency (~1μs) output for beam diagnostics
- High radiation (1Mrad total dose)

System-level design: overview

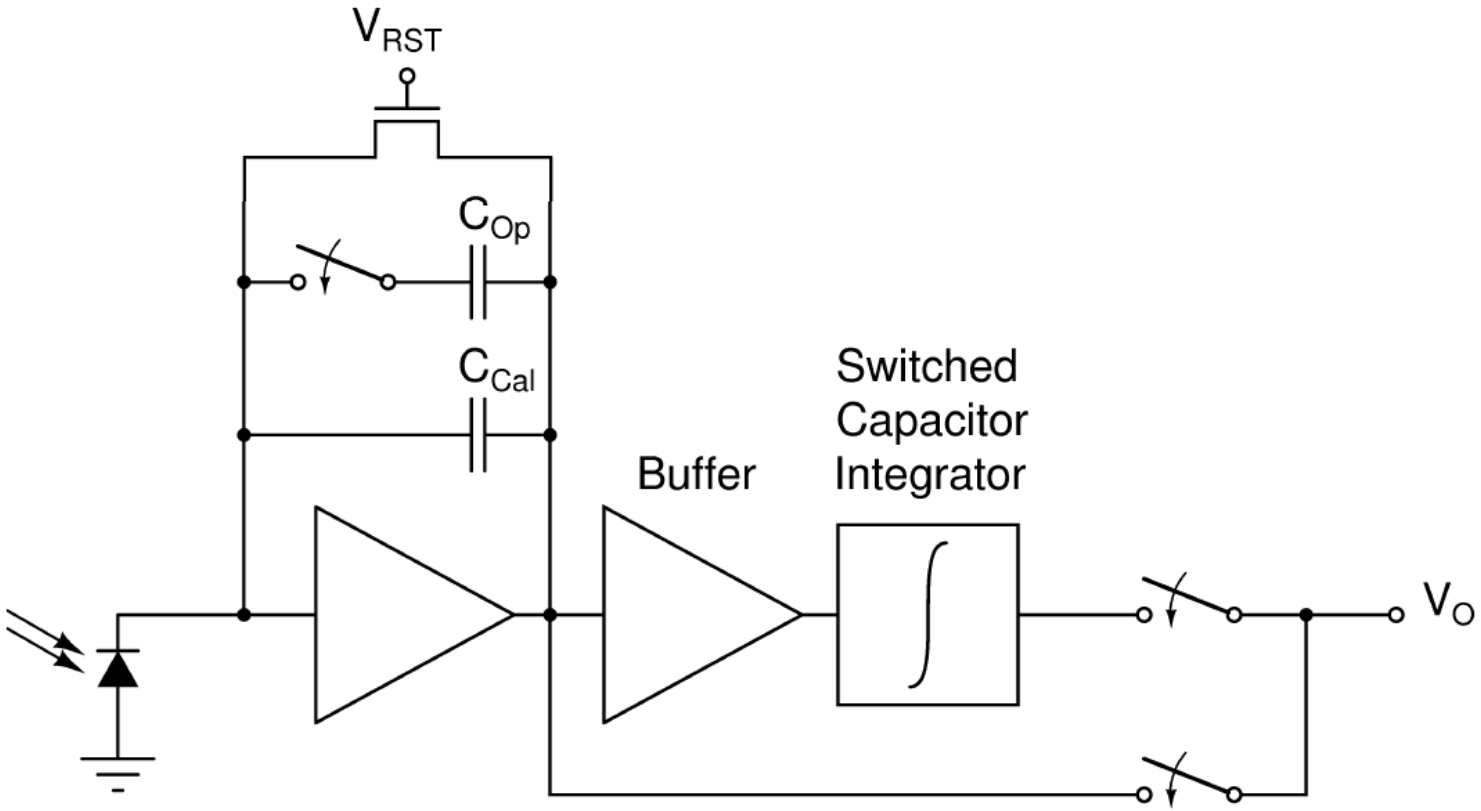


* Buffers and bias circuits not shown

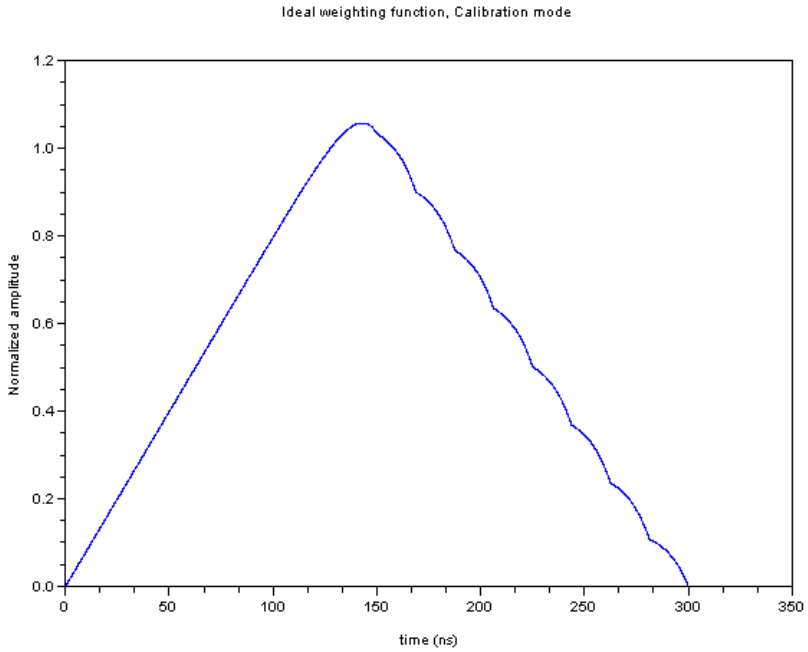
System-level design considerations

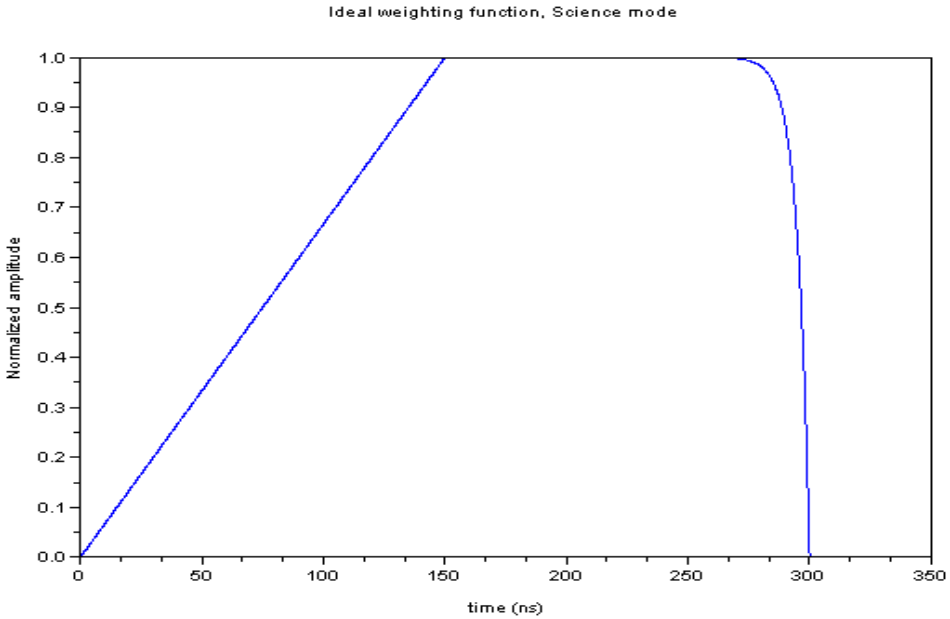
- Considering the system specs:
  - High occupancy → gated system to prevent signal pileup
  - Only 308 ns to process each collision→ noise is dominated by charge amplifier voltage noise
  - Careful design of weighting function is necessary (time-variant filter) in calibration mode: limit its slopes
- In practice, this means…
  - Time constants must be precisely defined → switched-cap circuits
  - Perfectly triangular weighting function produces about ½ of tolerable noise
  - Departure from triangular function implies more voltage noise…

System-level design: Front-end



Intended weighting functions

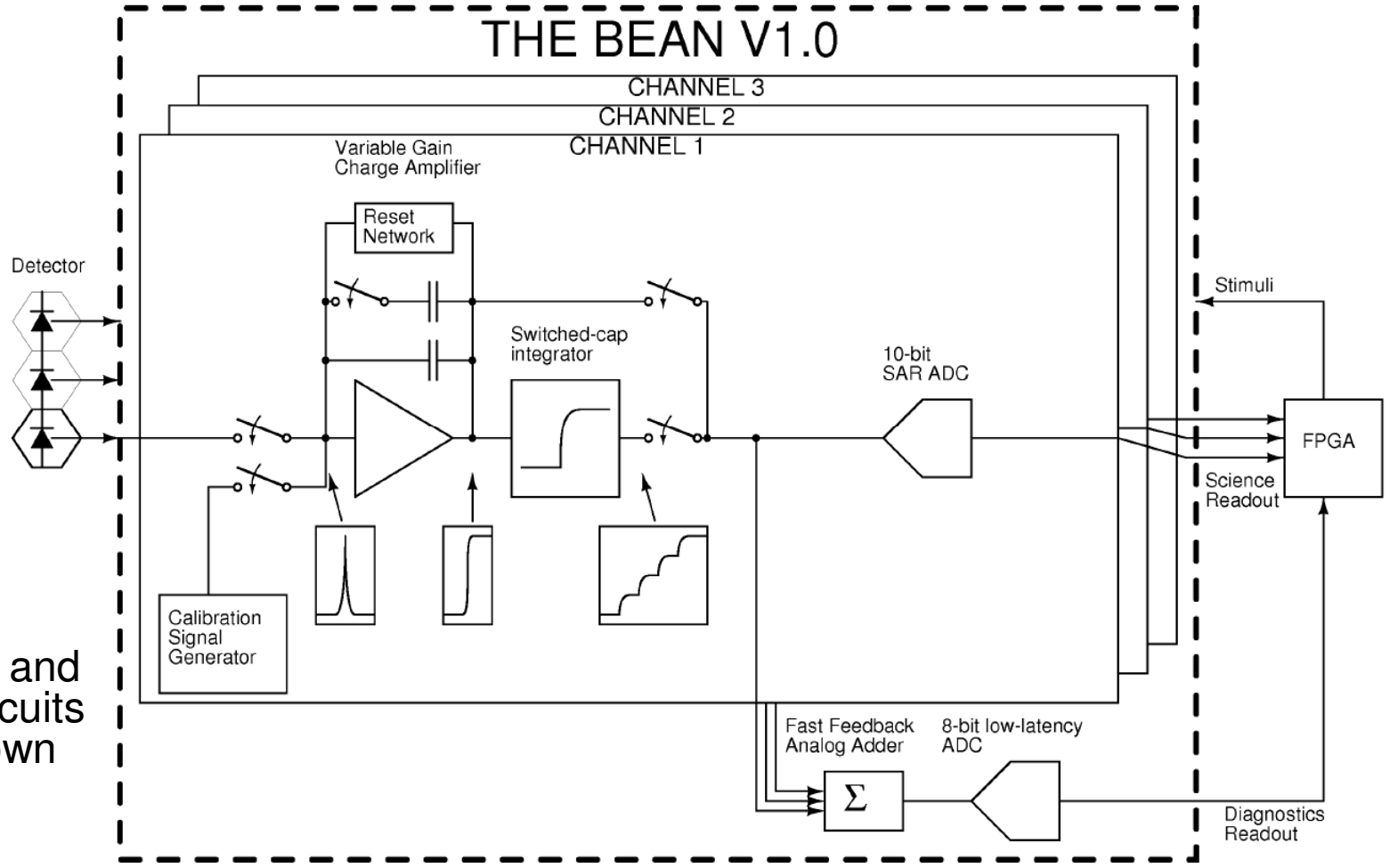




System-level design: ADC

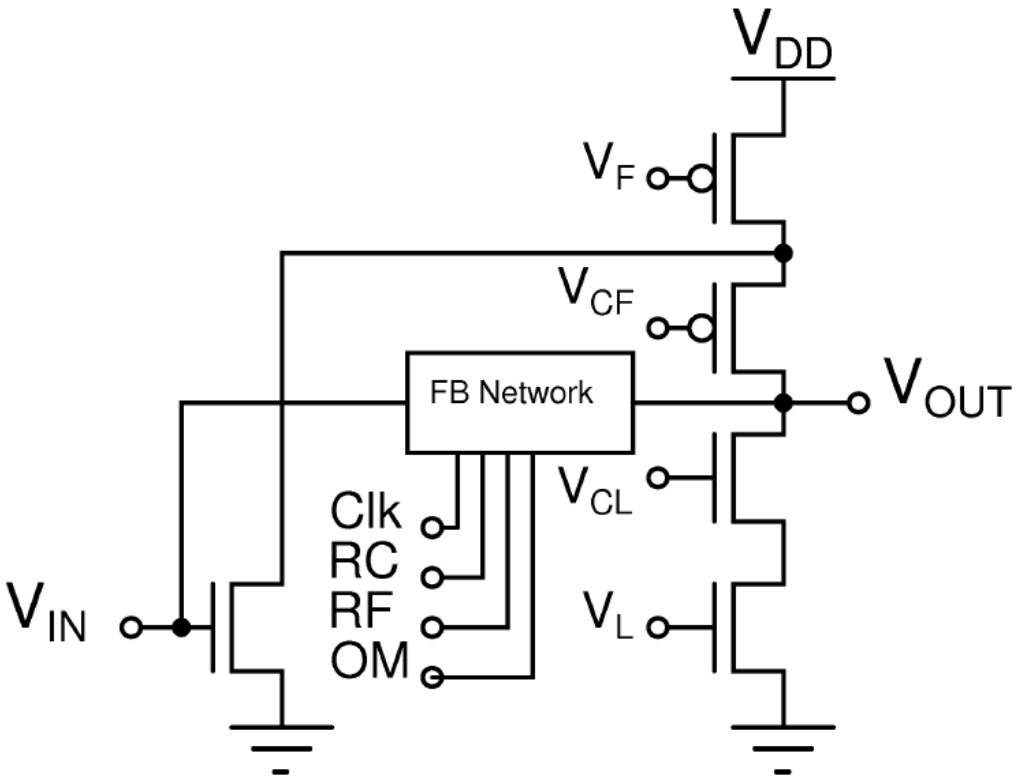
- Required specs:
  - 3.25MS/s
  - 10 bits
  - One ADC per channel
- Successive approximation ADC architecture chosen:
  - Low area
  - Low power consumption
  - Simple design
  - Required specs are achievable

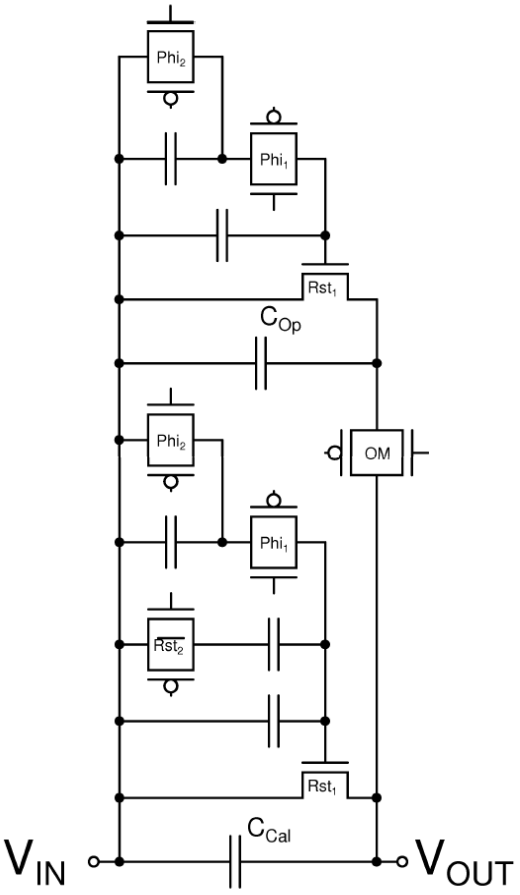
System-level design: prototype ASIC



* Buffers and bias circuits not shown

Circuit design: CSA

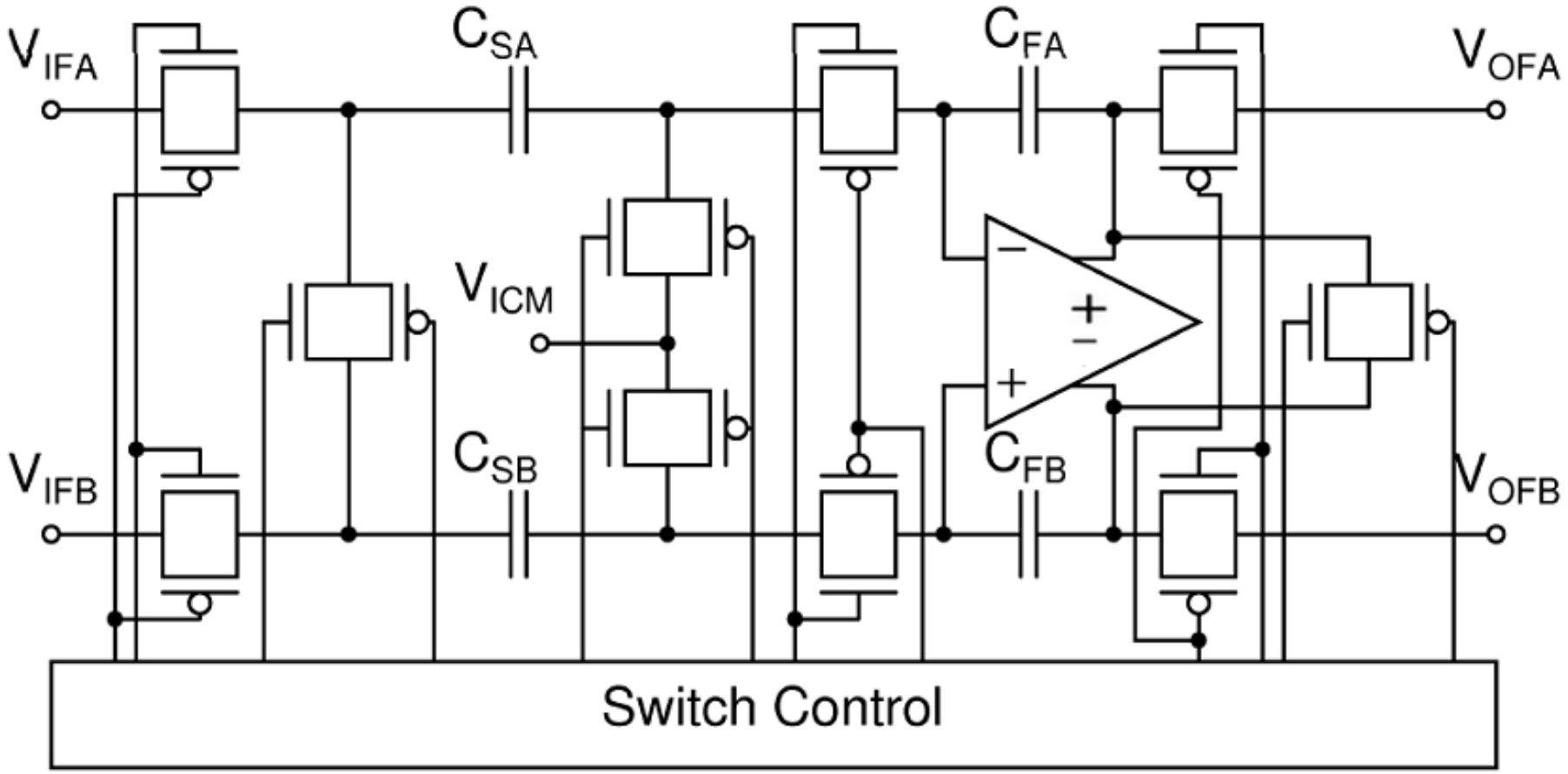




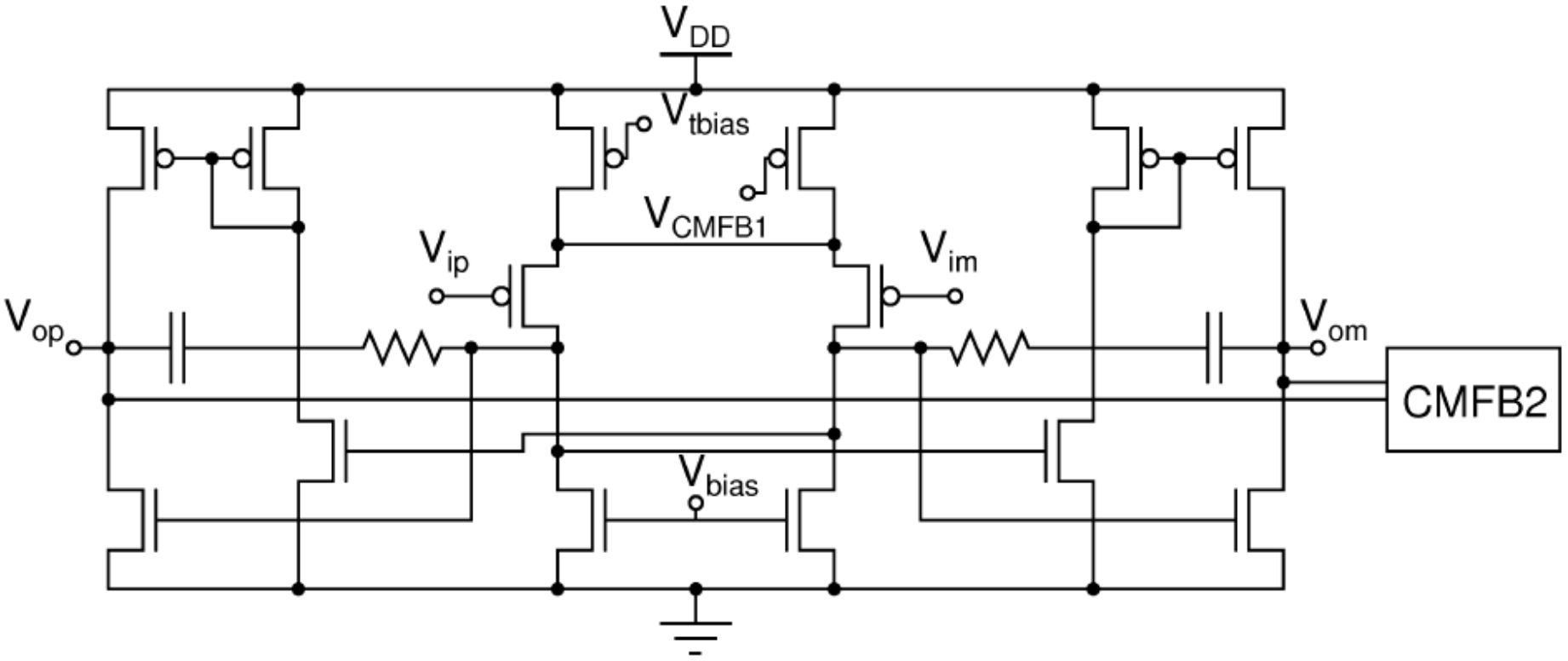
CSA and feedback network

* Some logic has been omitted

Circuit design: Filter (1/2)



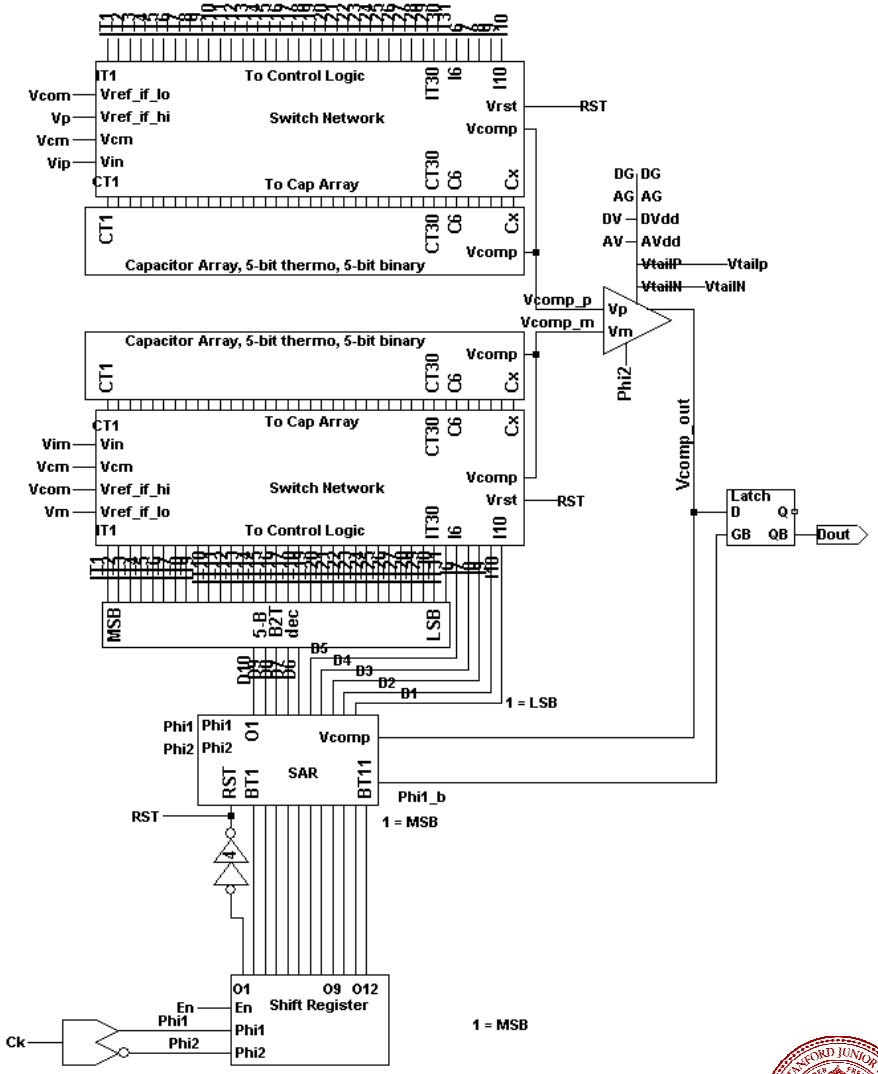
Circuit design: Filter (2/2)



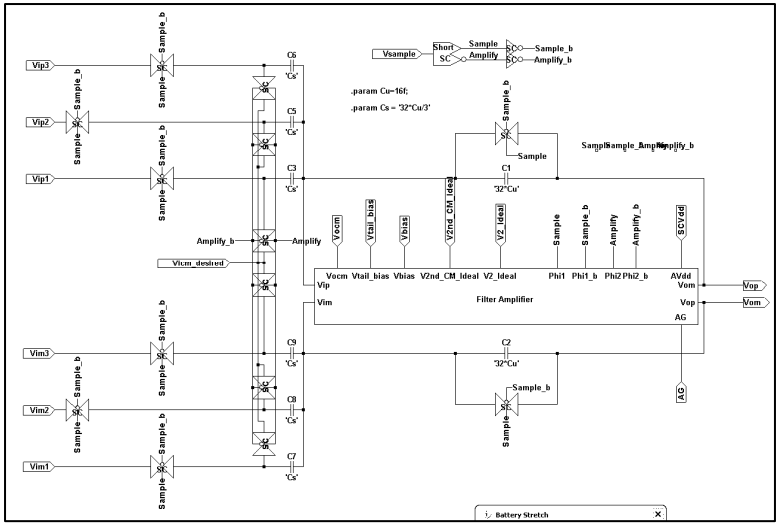
Filter amplifier

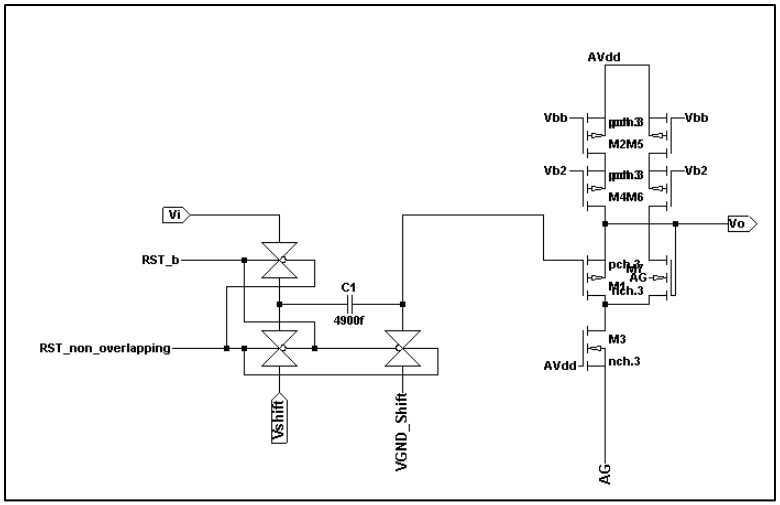
Circuit design: ADC

- Fully differential architecture
- Using 16-fF MIM unit capacitors
- 5 MSB bits: thermometer encoded
- 5 LSB bits: binary coded
- Pavg = 200uW @ 3.25MS/s
- FOM: 6pJ per bit

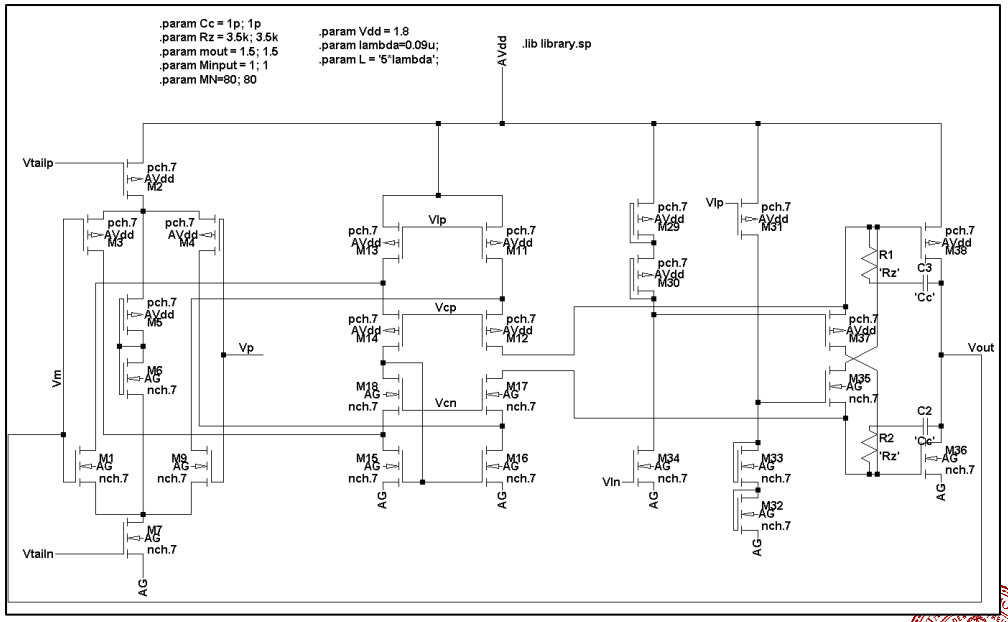


Circuit design: auxiliary circuits

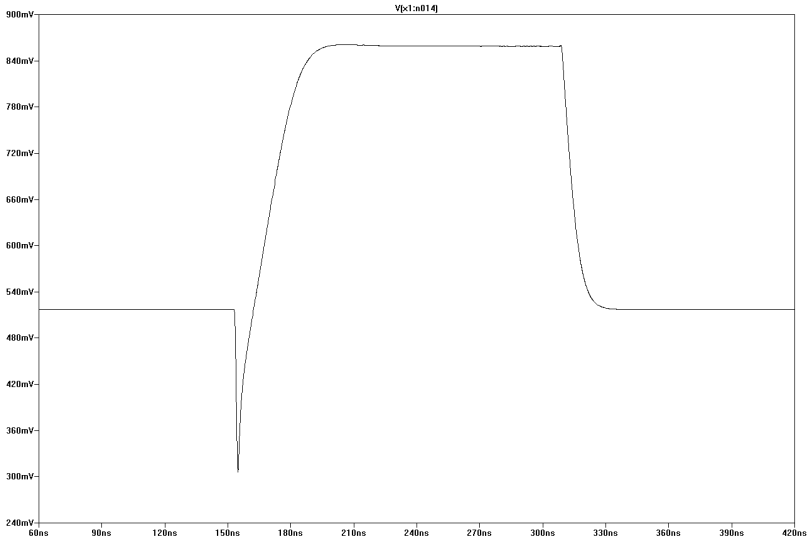


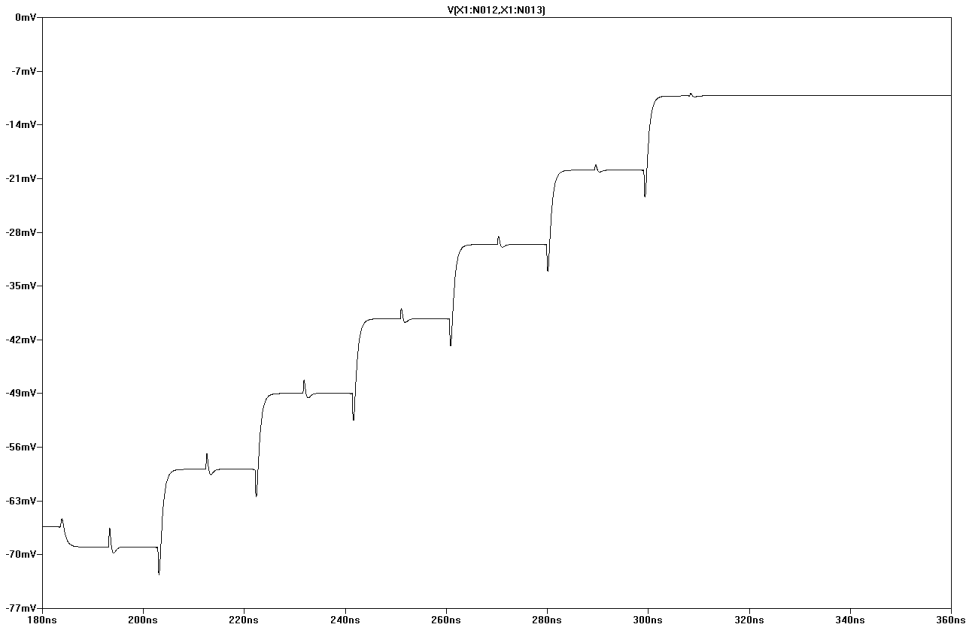


- Signal buffers,
- Switched-capacitor adder
- Rail-to-rail buffers
- Bias circuits
- Etc…

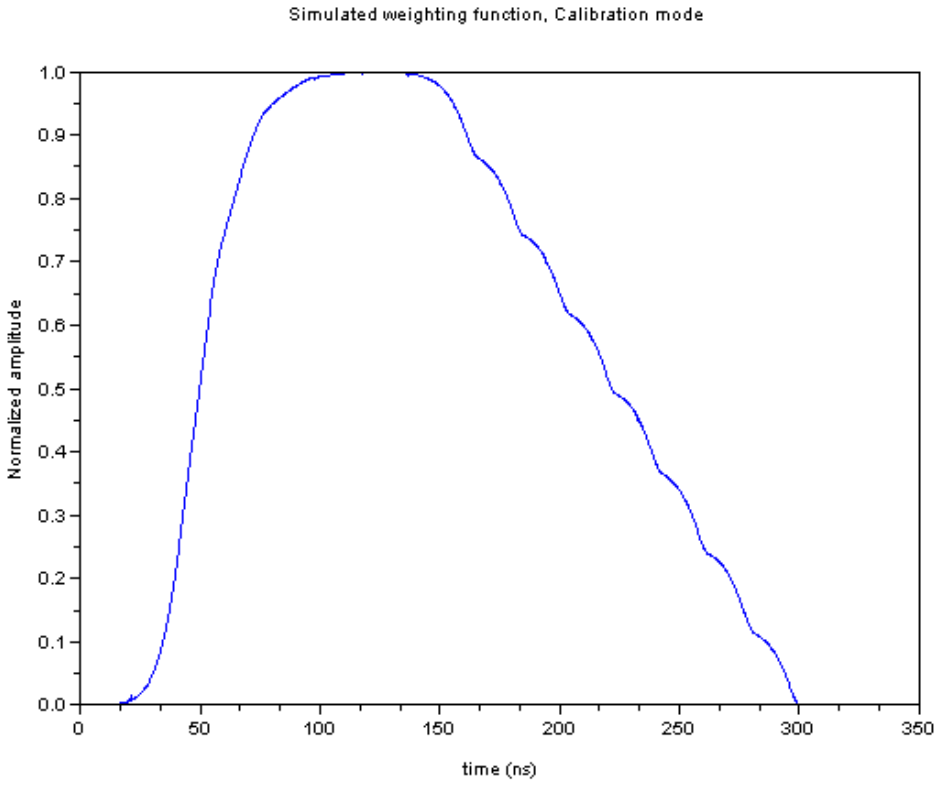


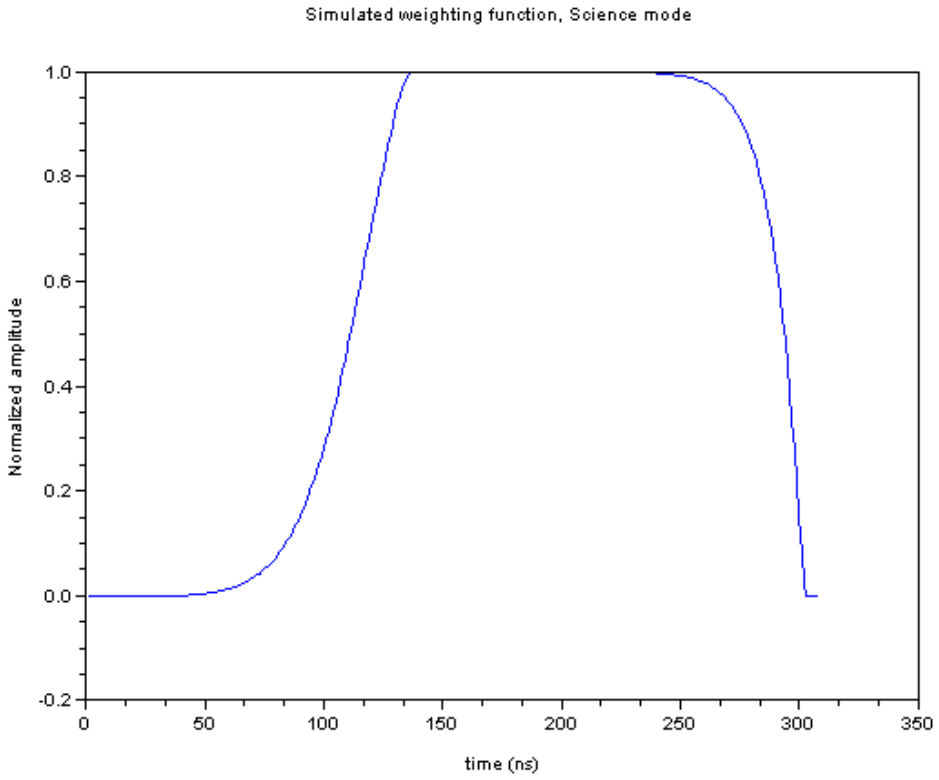
Circuit simulations: waveforms



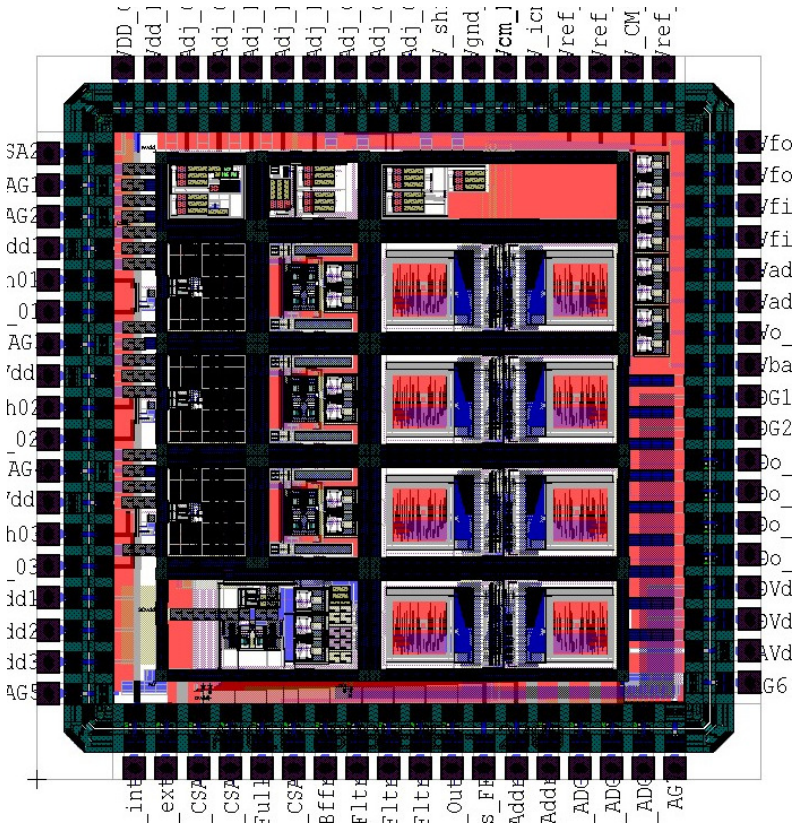


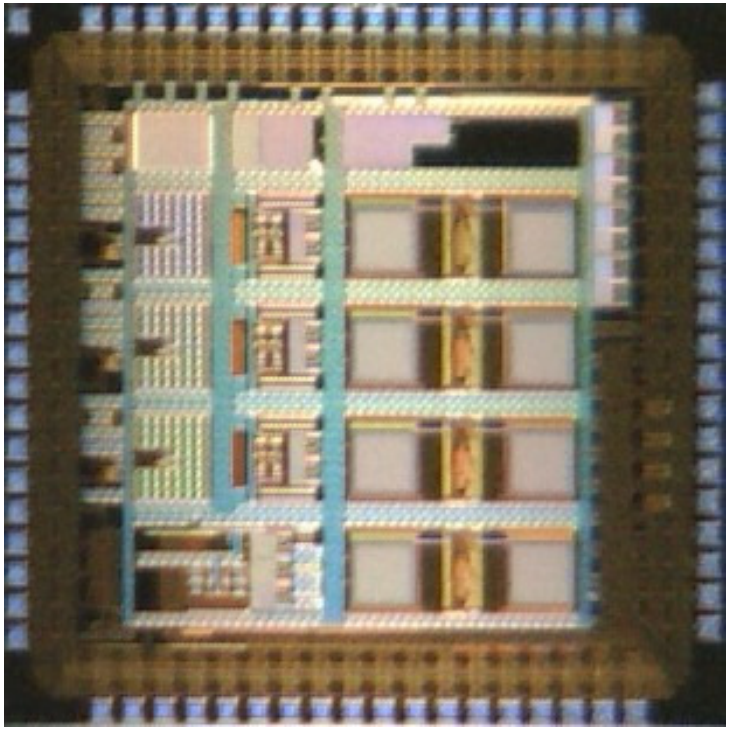
Circuit simulations: weighting functions





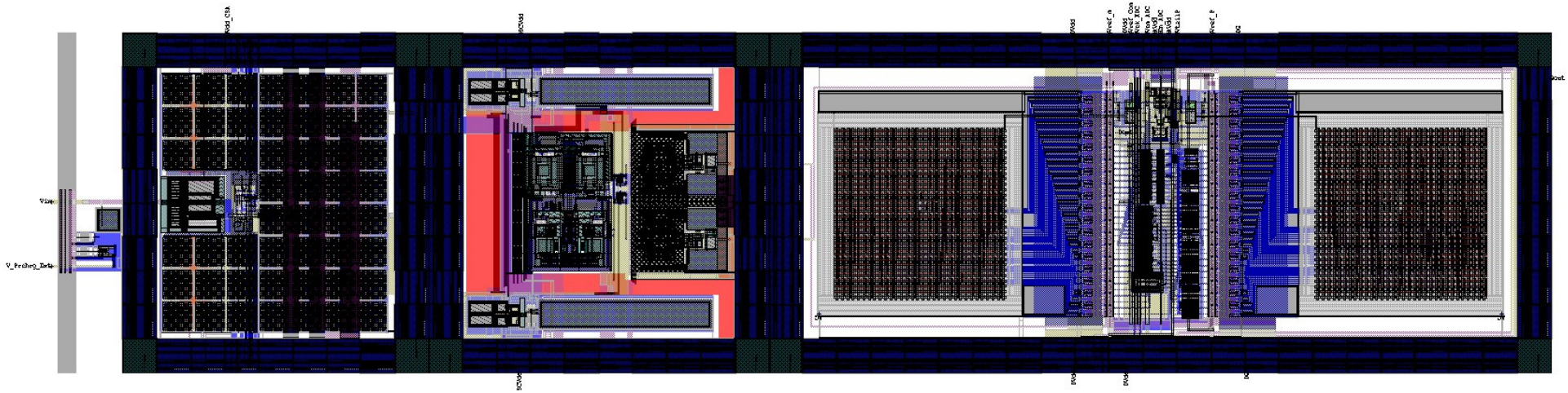
Implementation: full ASIC





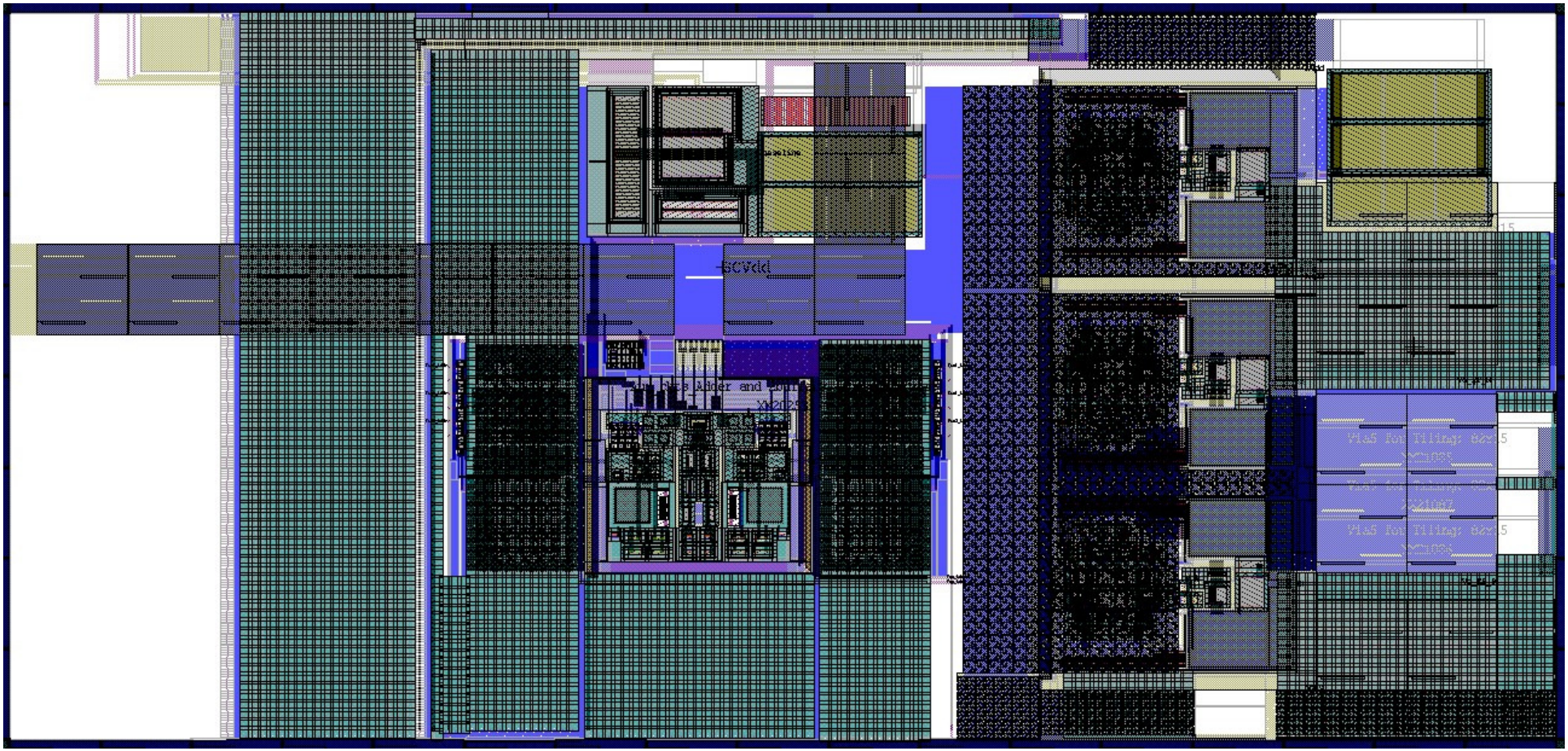
- TSMC 0.18um, 1.8V
- 72 pads, 2.4mm x 2.4mm (incl. pads)
- 7306 nodes, 35789 circuit elements
- 3 charge amplifiers, 4 x 10-bit, fully diff. SAR ADCs, 1 SC adder, 3 SC filters

Implementation: Channel



- From left to right: Calibration circuits; charge amplifier; signal buffers, fully-differential filter and output buffers; SAR ADC
- Channel pitch: 360um, including power bus

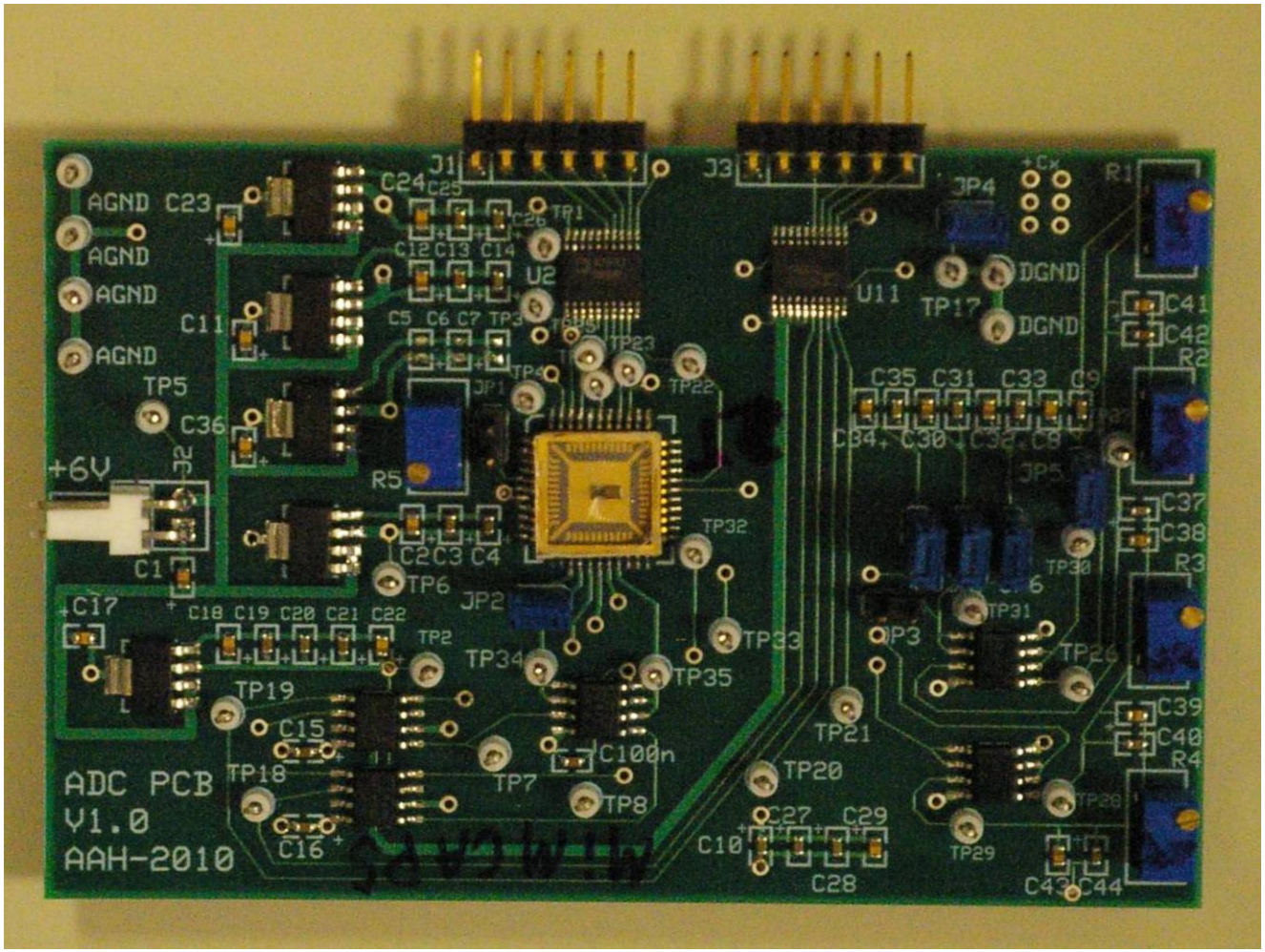
Implementation: Fast feedback



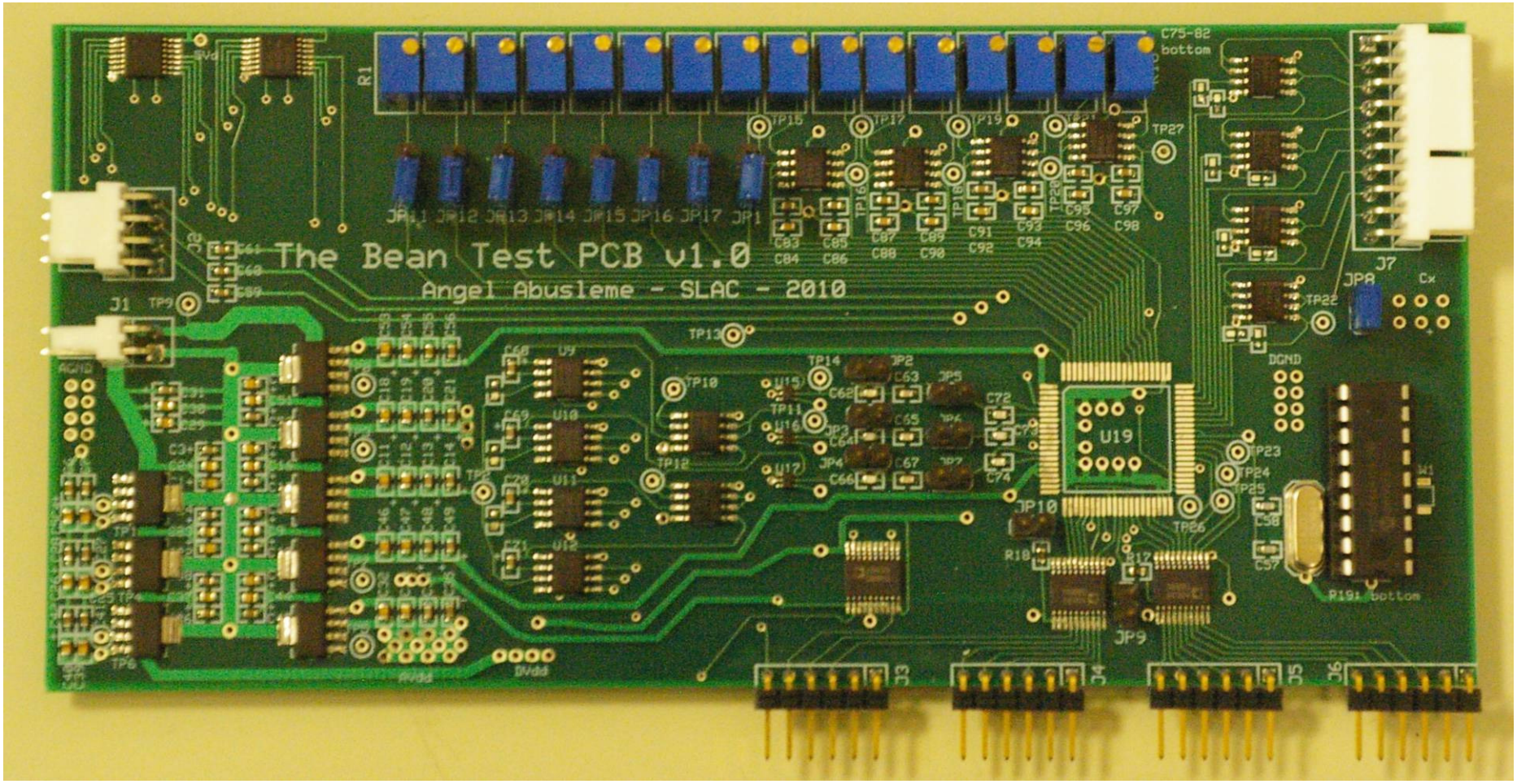
Tests: Methodology

- ASIC is mounted in a test PCB
- Test PCB includes supply voltages, references and DACs for stimuli
- Test PCB is directly connected to FPGA evaluation board
- FPGA provides clocks and stimuli
- FPGA receives a series of commands from a computer; then it executes a test, records a series of measurements, and transfers the results to the computer for further analysis

Tests: ADC board



Tests: ASIC board

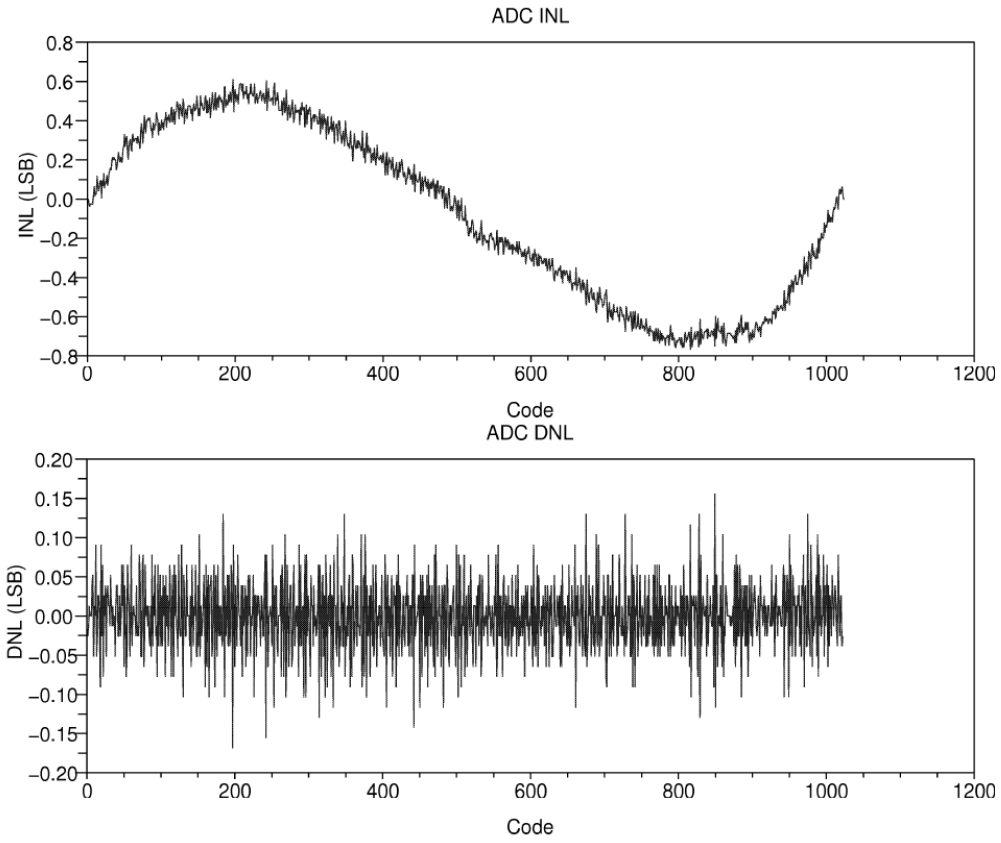


Tests: Results

- As of today, only the ADC has been tested
- Three versions of the ADC were fabricated:
  - 16-fF unit capacitors
  - 4-fF unit capacitors
  - 2-fF unit capacitors
- INL, DNL, noise and sampling rate are within the specs
- Design flaw in bias circuit was detected

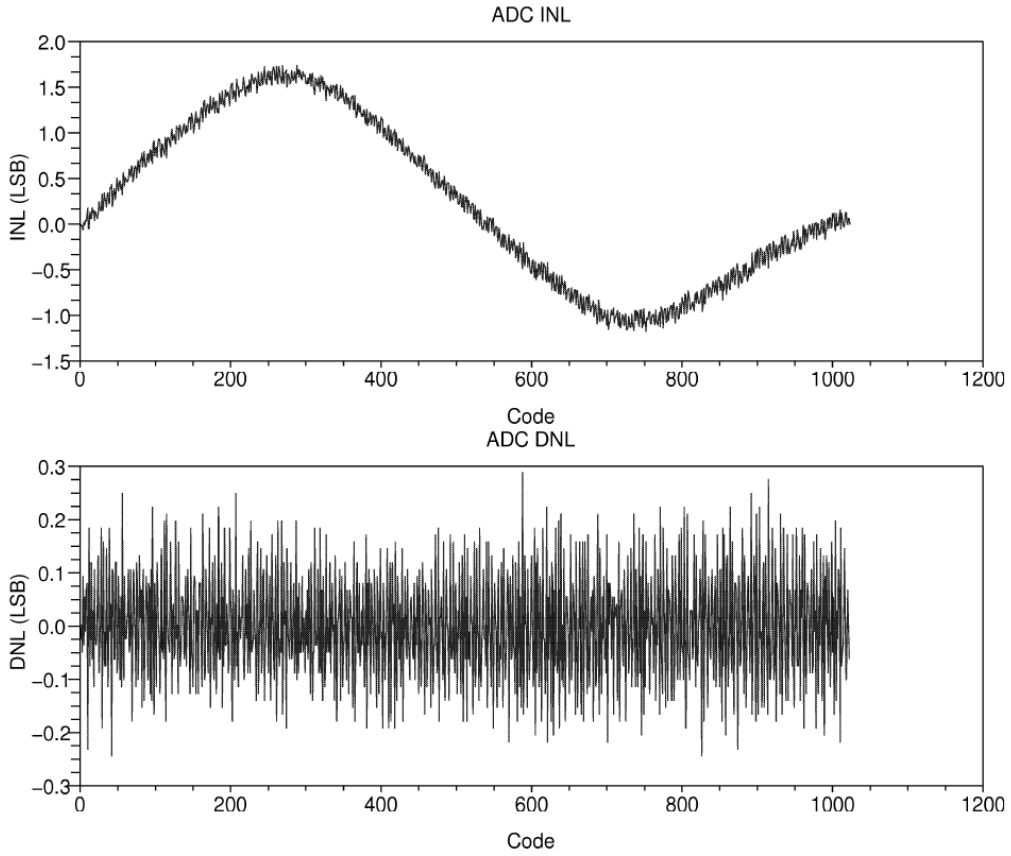
Tests: Results, MIMCaps ADC version

- MIMCaps (16-fF unit capacitance) ADC linearity results:
  - DNL is excellent, no missing codes
  - INL looks strange, but cause has been explained (copper dishing)
  - ADC meets noise and speed requirements



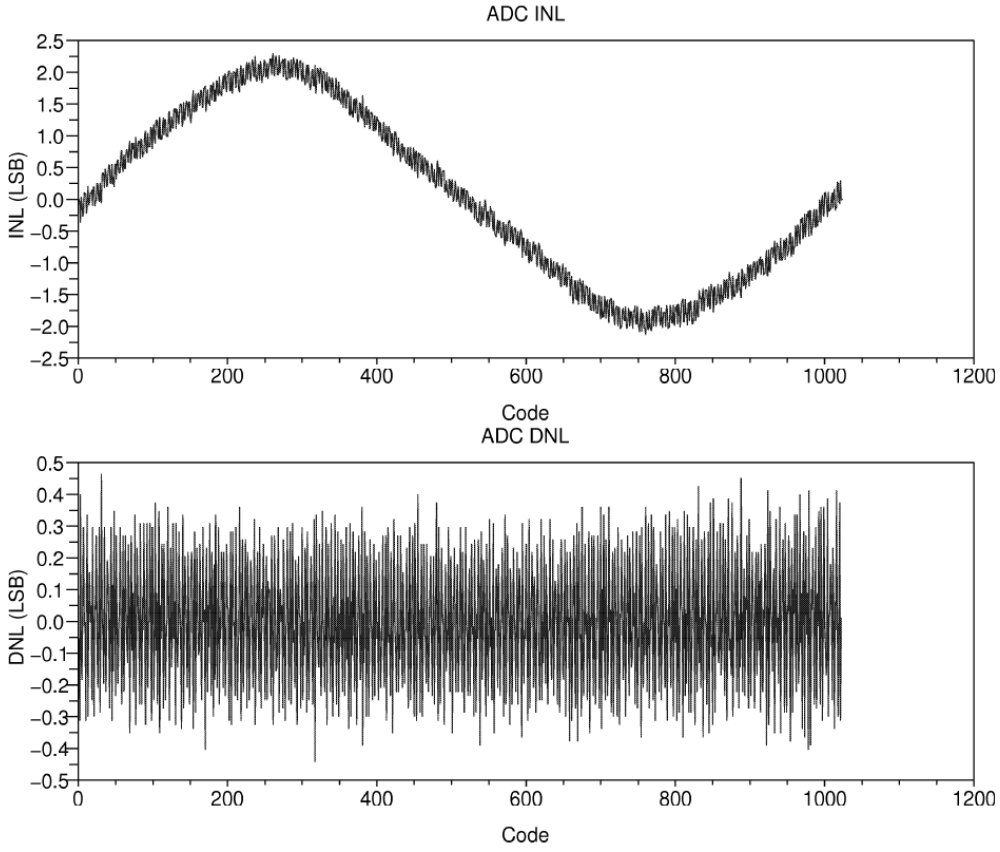
Tests: Results, 2-layer MOMCaps ADC version

- MOMCaps (~4-fF unit capacitance) ADC linearity results:
  - DNL is excellent, no missing codes
  - INL looks strange, but cause has been explained (copper dishing)
  - ADC meets noise requirements
  - We are working to meet speed requirements



Tests: Results, 1-layer MOMCaps ADC version

- MOMCaps (~2-fF unit capacitance) ADC linearity results:
  - DNL is excellent, no missing codes
  - INL looks strange, but cause has been explained (copper dishing)
  - ADC meets noise requirements
  - We are working to meet speed requirements



Conclusion and future work

- Conclusion
  - ADCs work within specs
    - Still pending further analysis and interpretation of the MOMCaps ADC test results (matching estimation)
    - Next version of the ASIC might include MOMCaps-based ADCs
  - Design flaw found in bias circuit does not compromise further testing
  - Front-end ASIC should be fully characterized within the next eight weeks

- Future work
  - Finish tests
  - Perform simple beamline tests
  - Study radiation tolerance
  - Edit front-end to match detector and improve radiation tolerance
  - Plan on full circuit version

Thanks!