ISIS2 as a Pixel Sensor for ILC

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Content

ILC Vertexing

- Requirements:
  - 3 μm resolution
  - 0.1 X_0% per layer
  - ! Huge background
  - Occupancy $< 1\%$
    $\Rightarrow$ Time slicing
- Two solutions offered by LCFI
  - Fast readout: CPCCD
  - Charge Storage: ISIS
- ISIS advantage
  - No need for power cycle, reduced peak power
  - Storage of raw charge

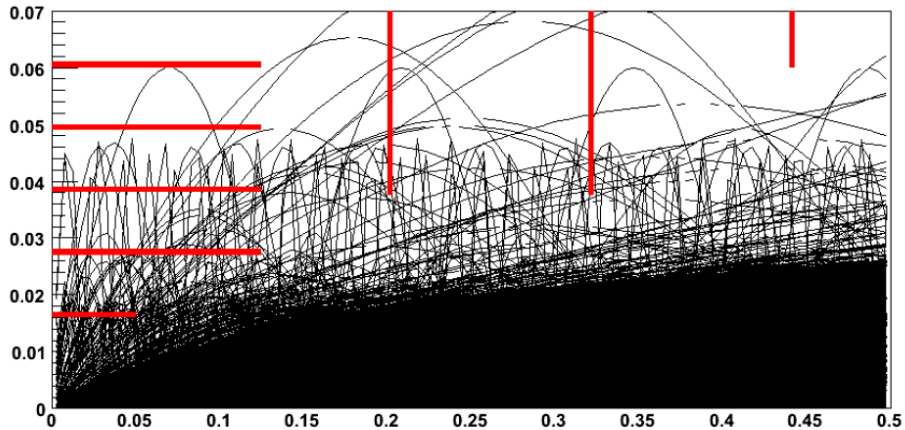


Figure: Simulation of e^+e^- pair production at ILC

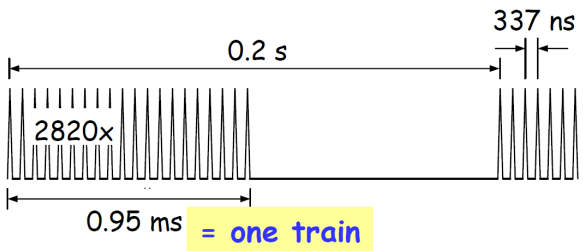
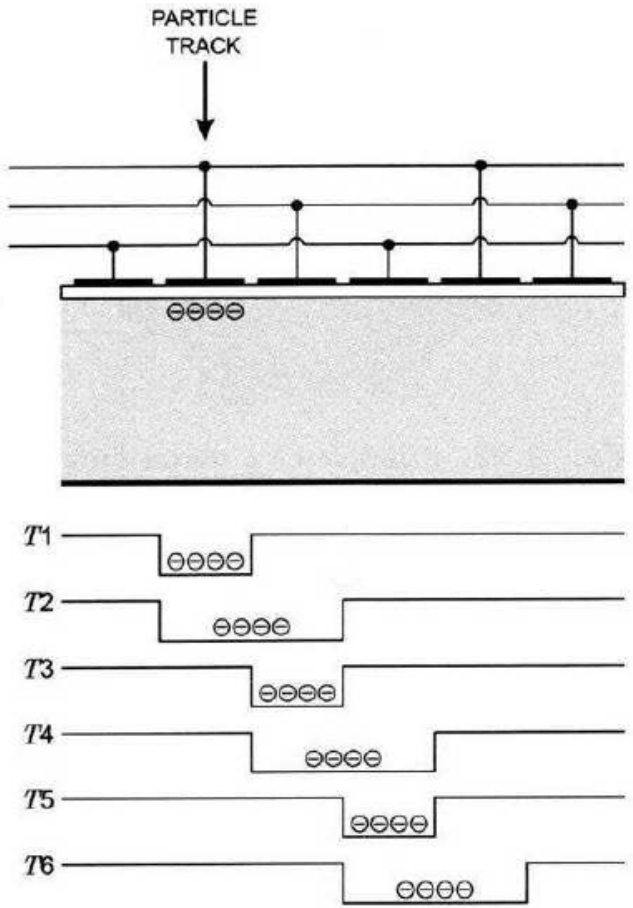


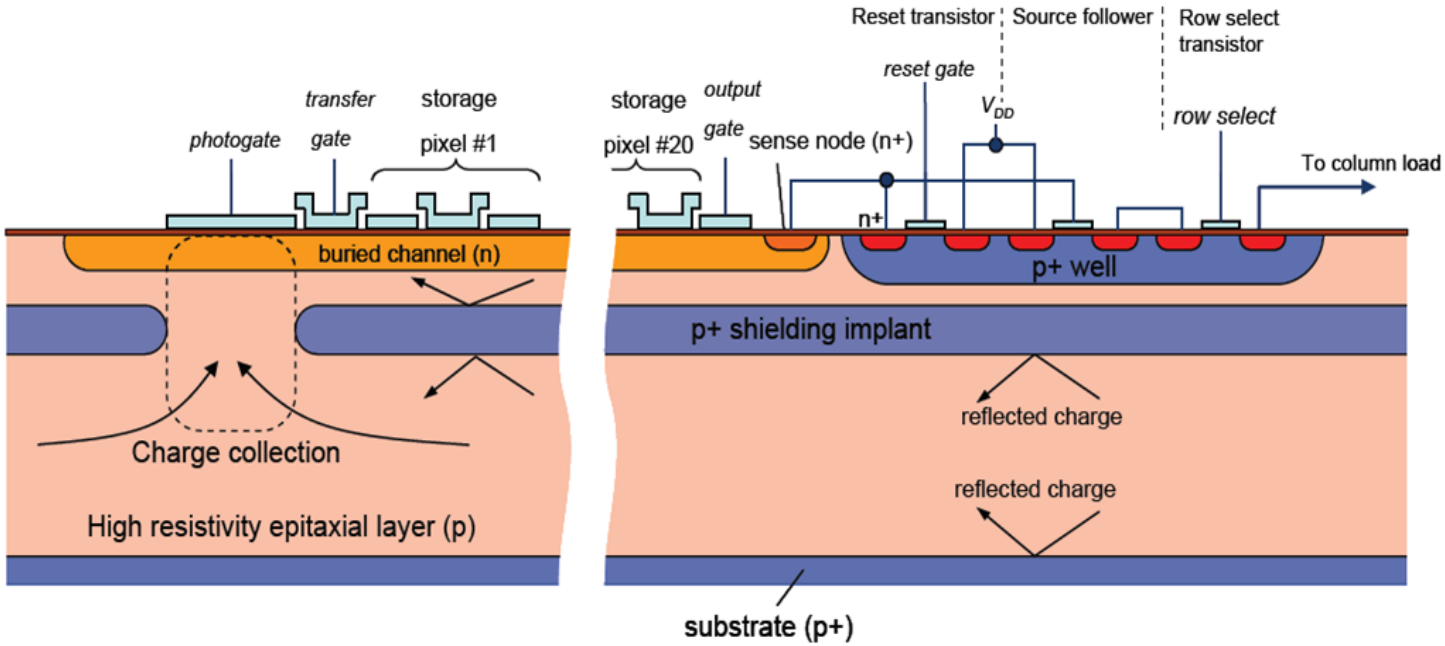
Figure: ILC bunch train

CCD and Charge-Coupled CMOS

- Charge Coupled Device (CCD)
  - Charge is stored inside the pixels
  - Small pixel size $\Rightarrow$ high resolution
- ISIS is produced with CMOS process while uses CCD structures to store signals for multiple time-slices



In-situ Storage Image Sensor



- Charge is collected under photogate
- Charge is transferred into 20 in-situ storage pixels
- During the quiet time between bunch trains the charge is converted to voltage and read out

Possible Application Beyond ILC Vertexing

Buried Channel in CMOS process is of interest in general

- Decouples charge storage and charge-to-voltage conversion ⇒ low noise & CDS
- Efficient charge collection from large area ⇒ LC Tracking
- Silicon Pixel Tracker (SPT)

- Barrel: SiC foam ladders, linked mechanically to one another along their length (*Low-Mass Collaboration UK*)
- Tracking layers: 5 closed cylinders (incl endcaps), $\sim 50\mu m$ square pixels
- $\sim 0.6\%X_0$ per layer, $\sim 3.0\%X_0$ total, over full polar angle range, plus $< 1\%X_0$ from VXD
- Timing layers: one (double) as an envelope for general track finding, and one between VXD and tracker, to tag large angle loopers, $\sim 150\mu m$ square pixels
- Amenable to the fast-growing charge-coupled CMOS pixel technology C architecture offering large area coverage at minimal thickness and cost, due to simplicity of the monolithic process

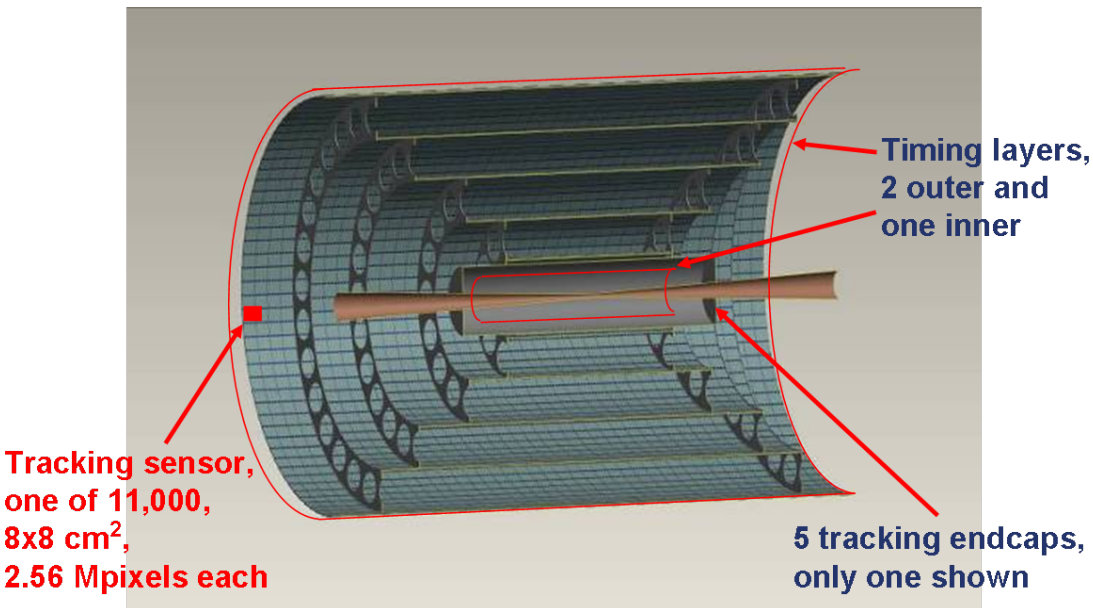


Figure: SPT at ILC/CLIC suggested layout (Chris Damerell)

ISIS History

- Fast framing CCD cameras based on ISIS principle has been developed (G. Etoh et al)
  - Max frame rate $\sim$ 100 Megaframes/s !
- ISIS for ILC development started in LCFI $\sim$ end 2003
- ISIS1 was produced and successfully tested to prove the feasibility of local charge storage
- ISIS2 was received after the termination of LCFI but the testing has been going on nonetheless.

Proof-of-principle Device: ISIS1

- e2V CCD $\sim 2\mu m$ process
- $160 \times 40\mu m^2$ pixel, 5 storage cells
- successfully tested with ^{55}Fe and testbeam

Z. Zhang et al. NIM A 607(2009)538
D. Cussans et al. NIM A 604(2009)393
J. J. Velthius et al. NIM A 599(2009)161

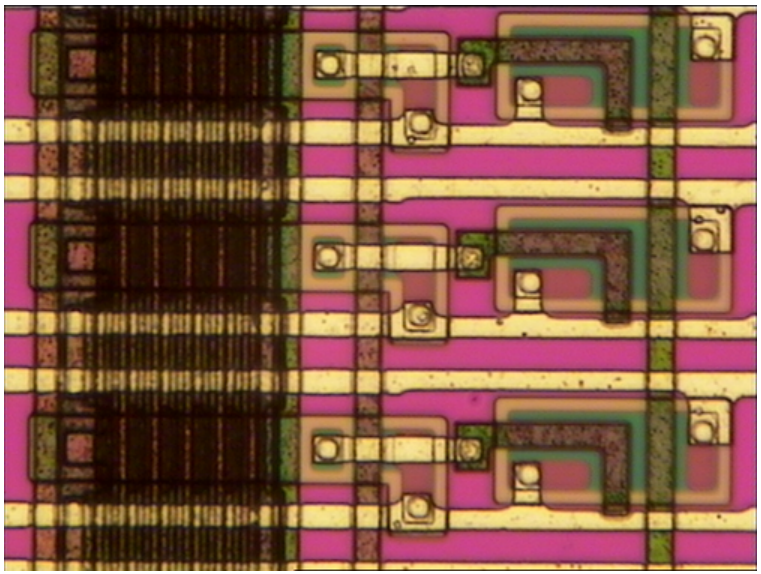
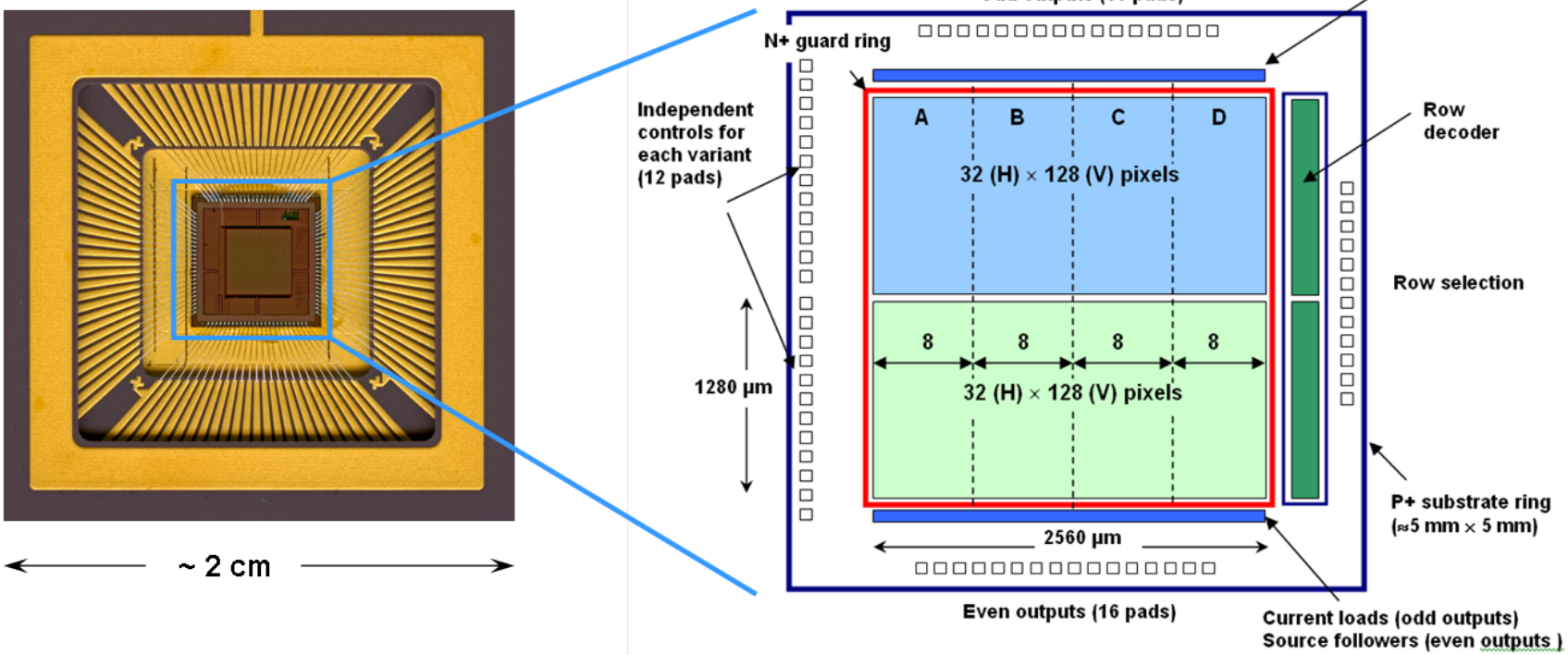


Figure: Three pixels on ISIS1

ISIS2 Design

- ISIS2 received from Jazz Semiconductor in Oct. 2008
- CCD buried channel in a CMOS process!
  - $0.18 \mu m$ CMOS process
  - $3 \times 5\,\mu m^2$ storage pixel (ISIS1: $20 \times 40\,\mu m^2$)



ISIS2 Pixels Layout

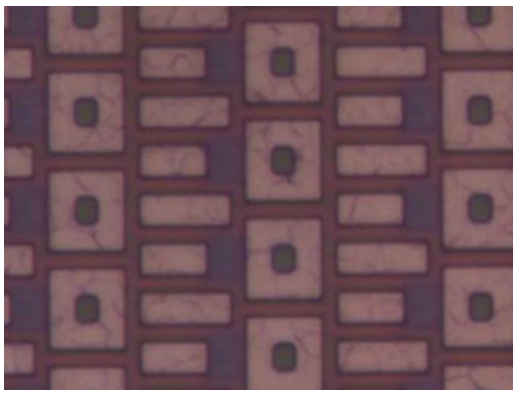


Figure: ISIS2 pixels under microscope

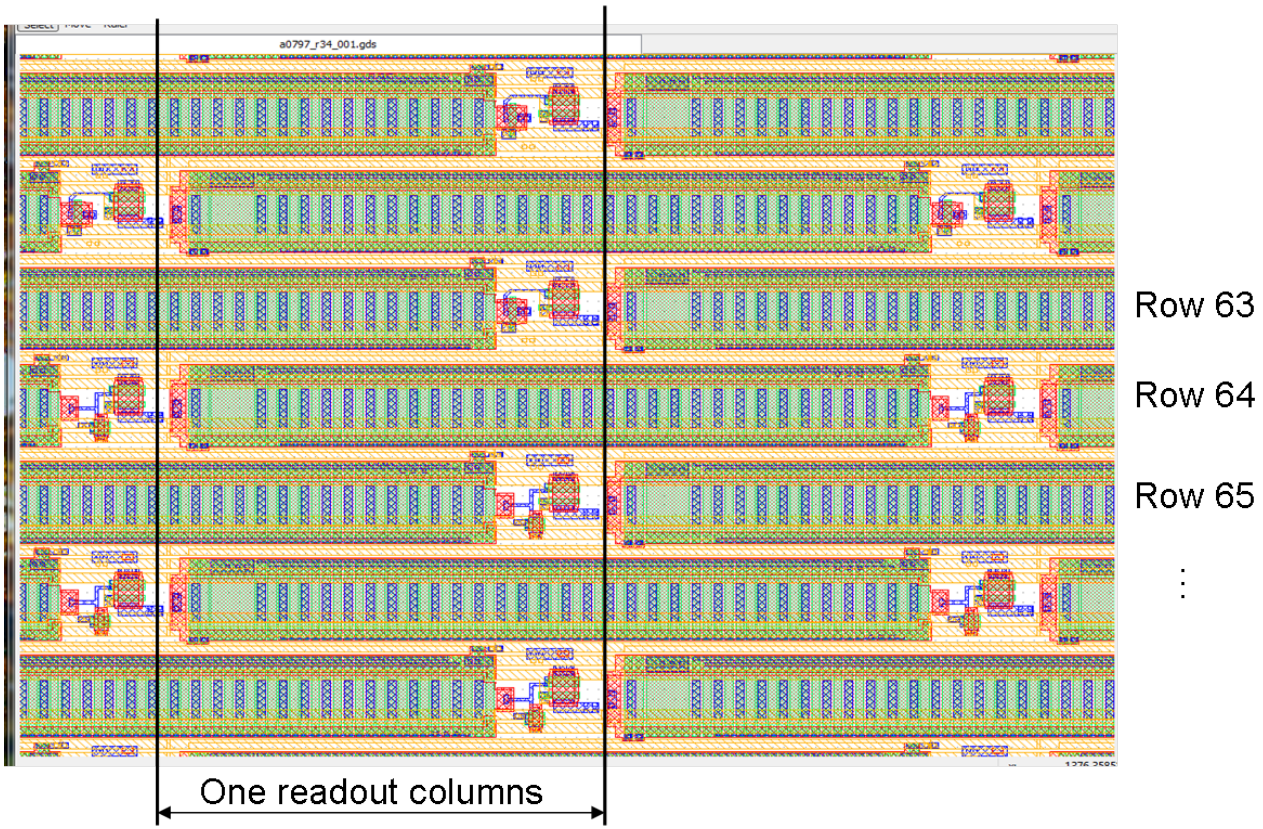


Figure: ISIS2 pixel layout. (K. Stefanov, P. Murray)

ISIS2 Variations

- Reset transistor
  - Surface Channel
  - Buried Channel
- Deep p^+ well
  - With/w.o. aperture under PG
  - Size of aperture
- Pixel variations
  - CCD gate width
  - CCD intergate gap
- Process options: doping concentration

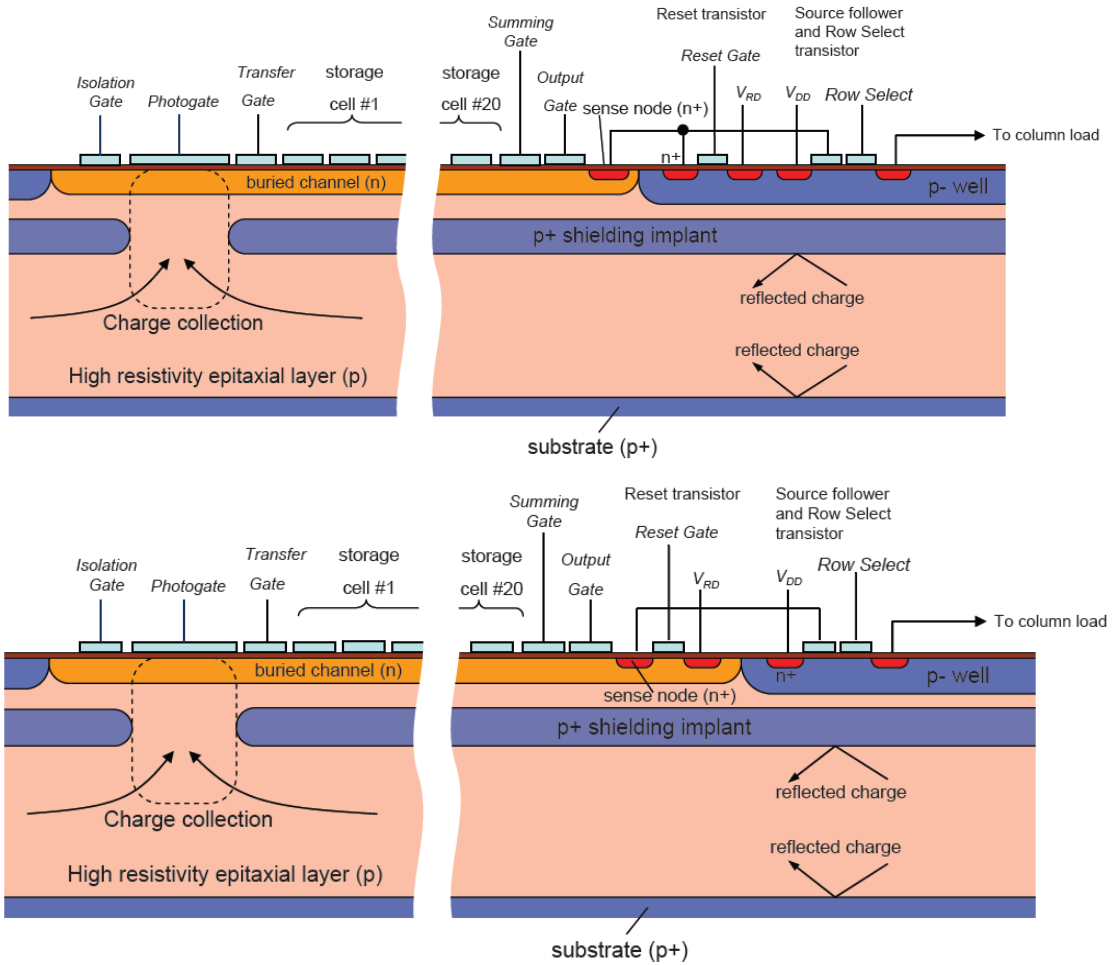
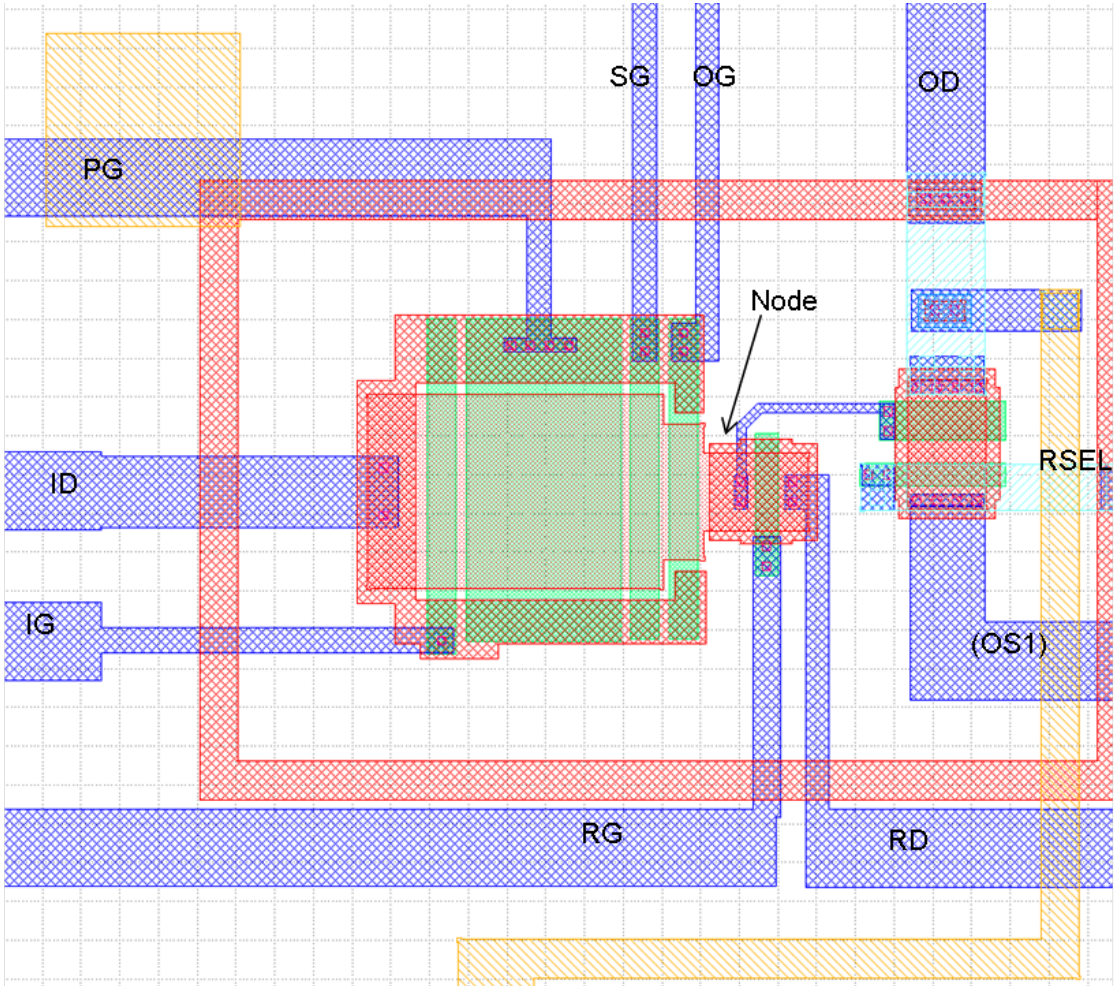


Figure: Upper: Surface Channel reset transistor; Lower: Buried Channel reset transistor. (K. Stefanov)

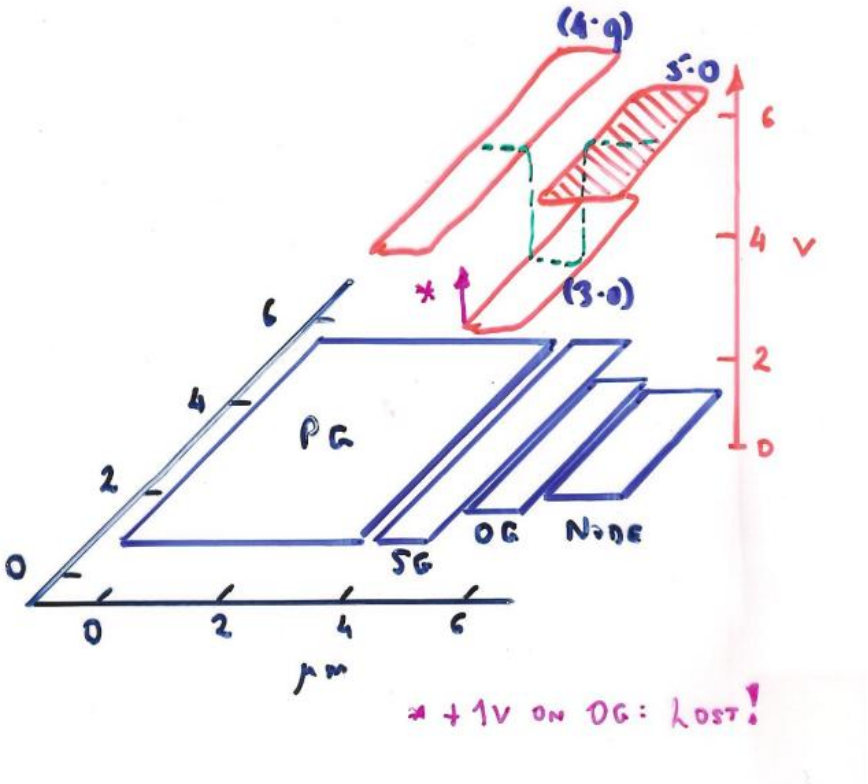
Test Structure

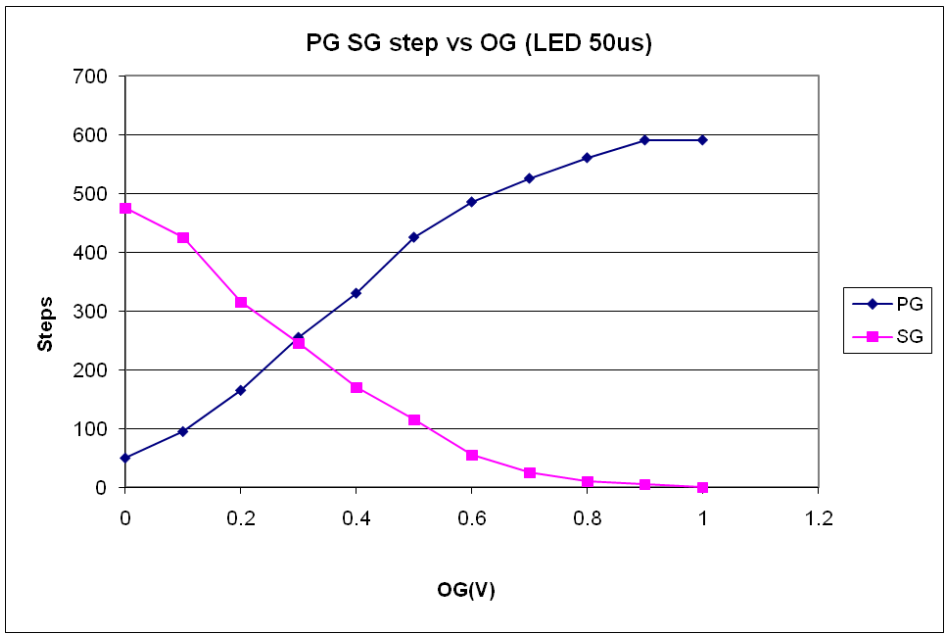


- Same as full array but without CCD transfer gates
- Allows to establish operating conditions
- Small feature size
  - Small capacitance of output node $\Rightarrow$ excellent noise performance
  - Edge effects and 3D fringe fields are important

Figure: ISIS2 test structure. (K. Stefanov, P. Murray)

Fringe Effects

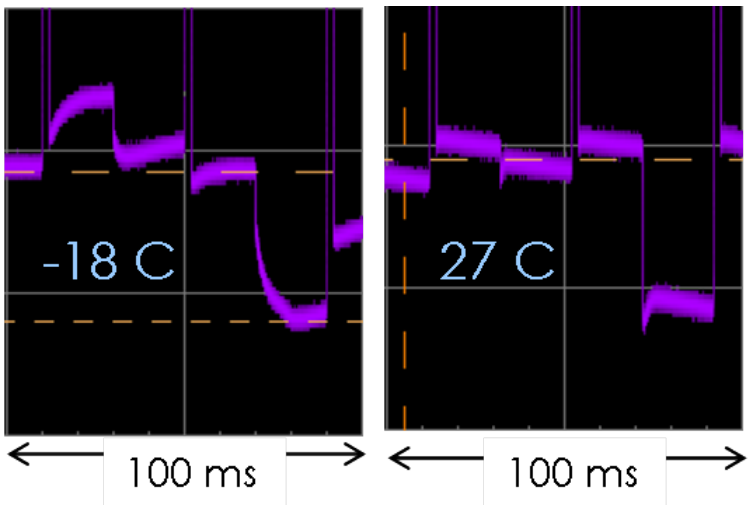




C. Damerell, Z. Zhang

- Potential under the output gate is pulled up by output node at 5 V
  $\Rightarrow$ Charge leaking to output node directly from photo gate

Slow Readout Rate



- Processing/design flaw: Large resistance of polysilicon gates
- It takes a few ms per transfer (between gates) $\Rightarrow$ Large dark current accumulated
- Low temperature: dark current $\downarrow$, gate resistance $\uparrow$

- Bright side: charge lives in CCD for seconds $\Rightarrow$ can be manipulated

X-ray Calibration

- Calibration with ^{55}Fe (1620 e^- K_α and 1780 e^- K_β lines)
  - direct hits on output node
  - hits from photo gate
- CTE and Noise Measured
  - Sensitivity 24 $\mu V e^-$
  - Best noise 6 e^-
  - 5% loss of CTE due to tapered geometry

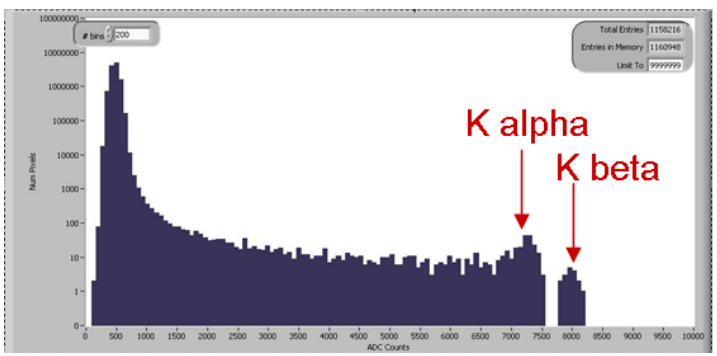
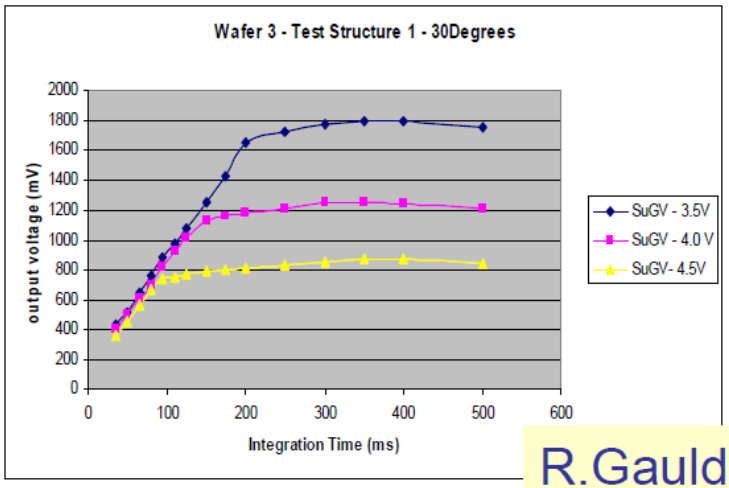
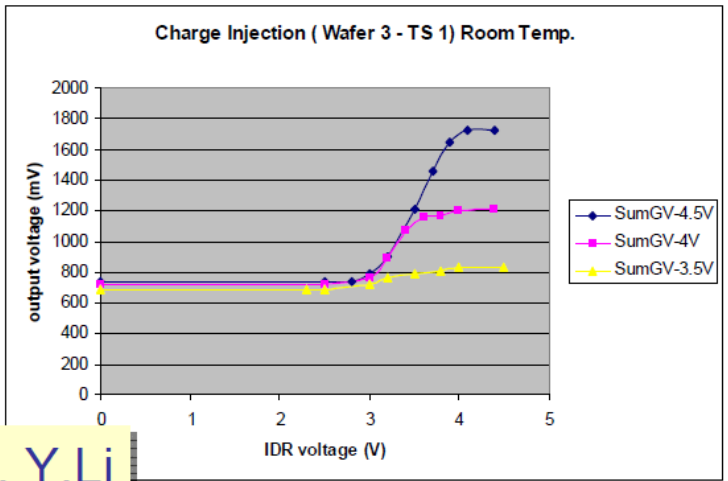


Figure: ^{55}Fe hits on output node at 31 °C

	-10 °C	31 °C
CTE	94.2%	94.5%
OD Noise	20 e^-	14 e^-
PG Noise	27 e^-	66 e^-

Charge Transfer





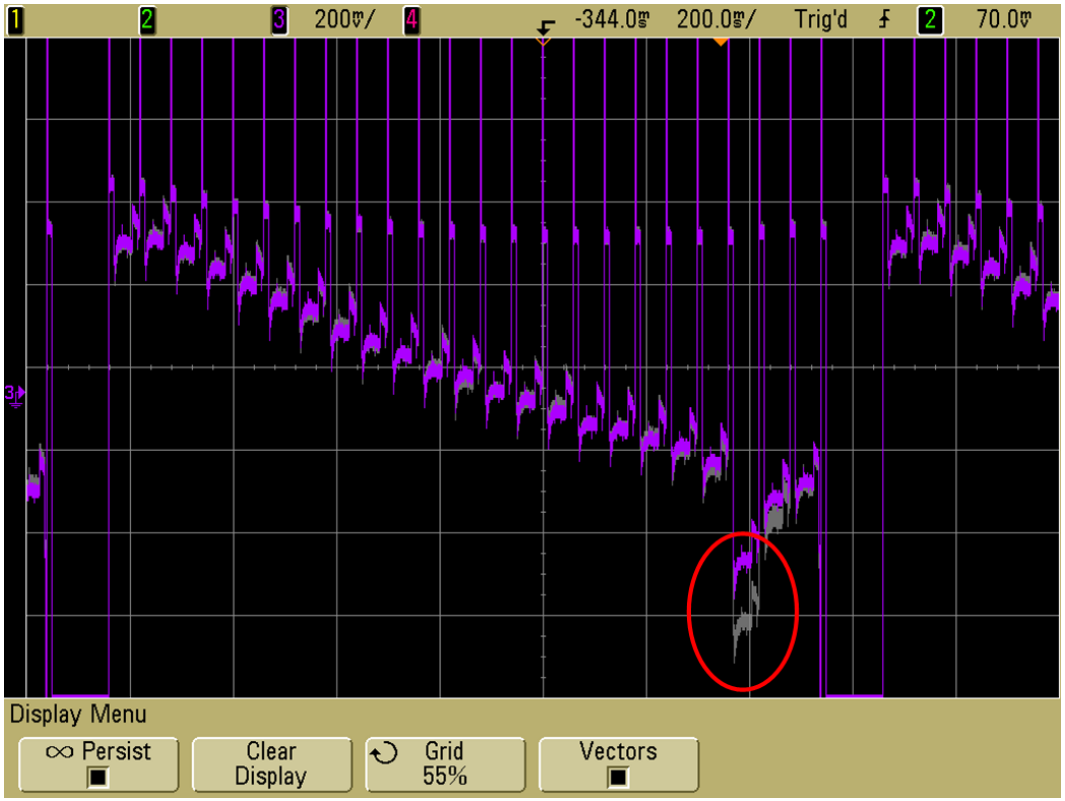
R.Gauld, Y.Li

Leakage current

IDR: charge injection

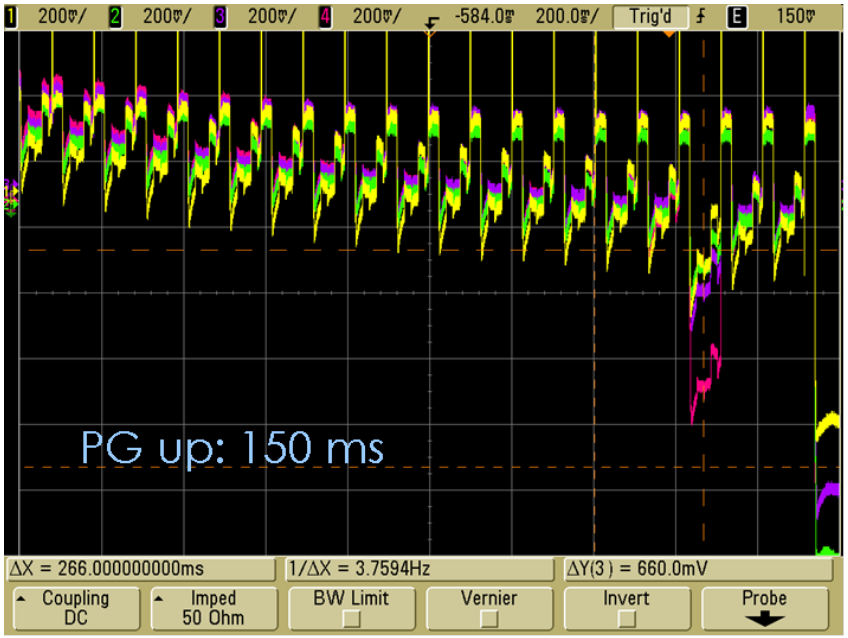
- Charge transferred from: dark current, LED or charge injection
- Well capacity is limited by Summing Gate
  - 5000 $\sim$ 10000 e^- depending on SG bias

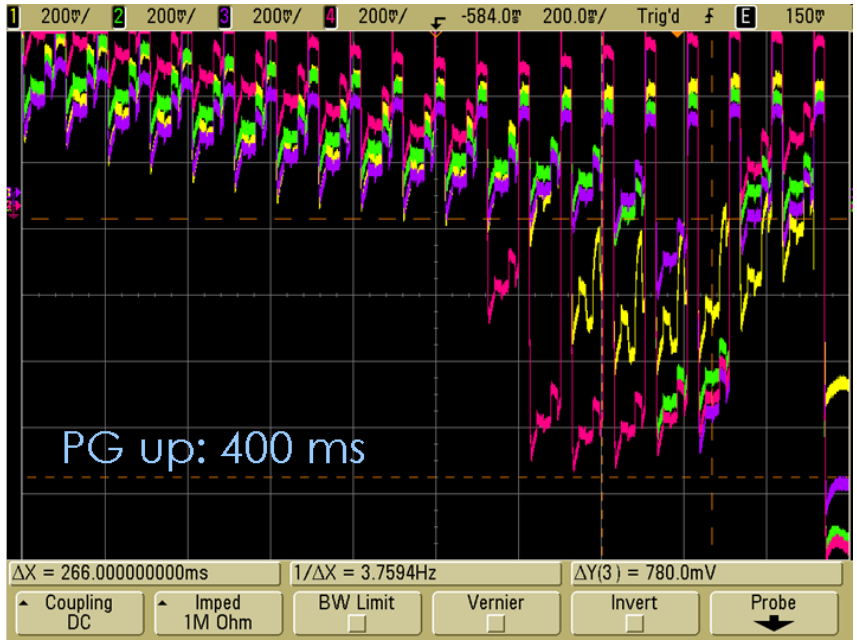
Full Array



First successful charge transfer in main array in July 2009!

Deep p^+ Splits





No deep p^+ shield (YELLOW)

Deep p^+ with aperture (GREEN)

Deep p^+ with wider aperture (PURPLE)

Deep p^+ without aperture (PINK)

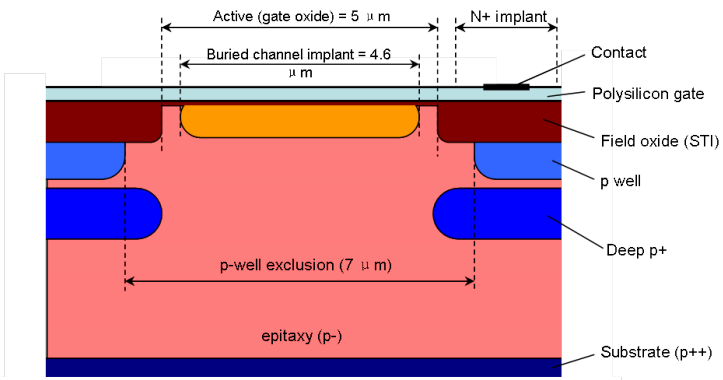
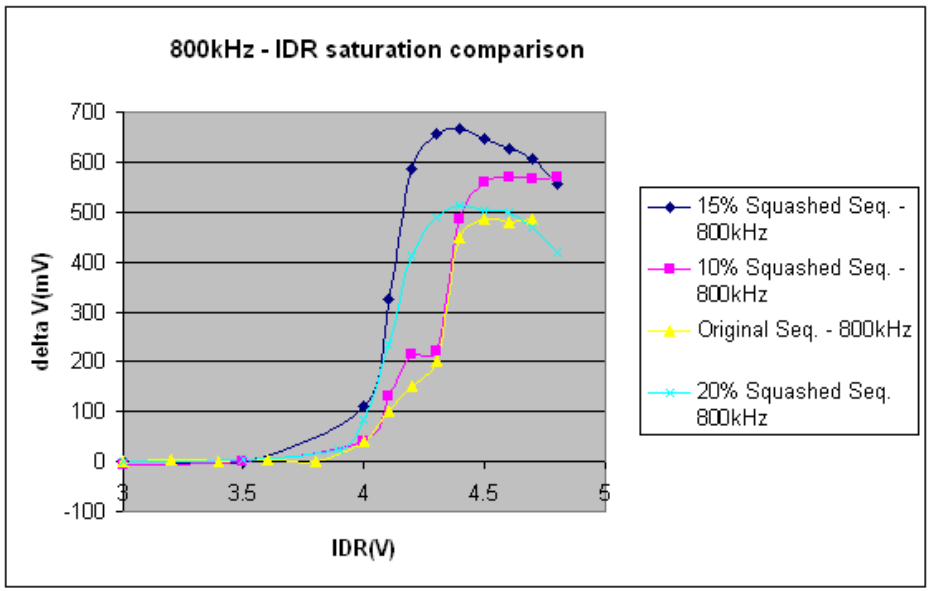
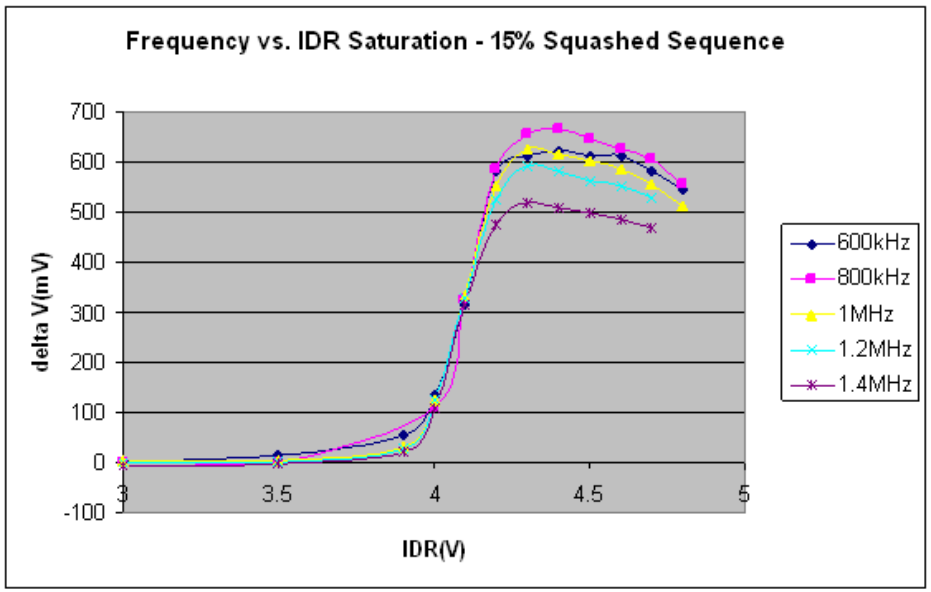


Figure 4. Channel cross section.

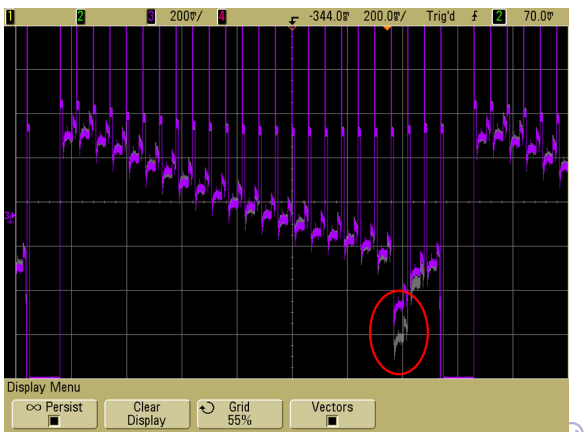
Readout Time Minimization





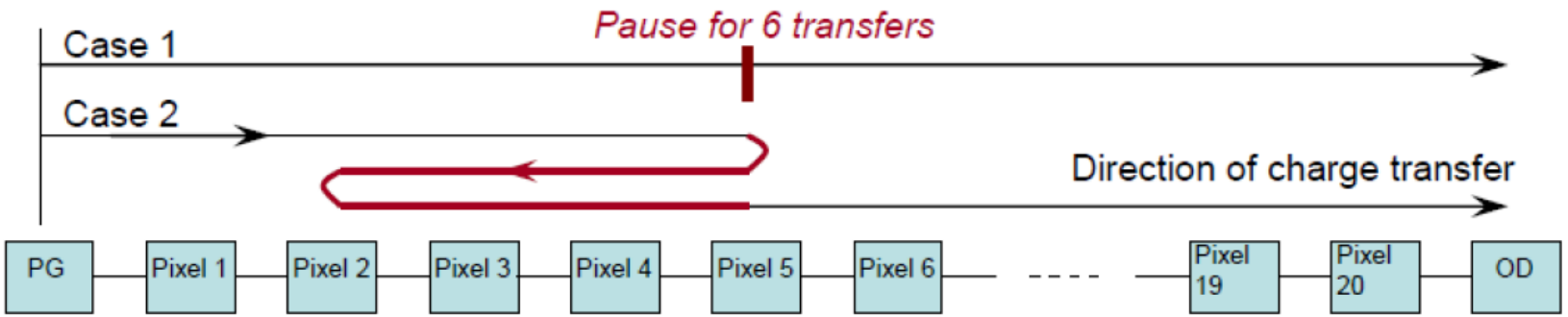
Efforts to minimizing the readout time:

- (left)Sequence of the transfers (excluding SG) is squashed, eg. The time between transfer gates are decreased
- (right)Trying to run at highest frequency



Charge Transfer Efficiency (1)

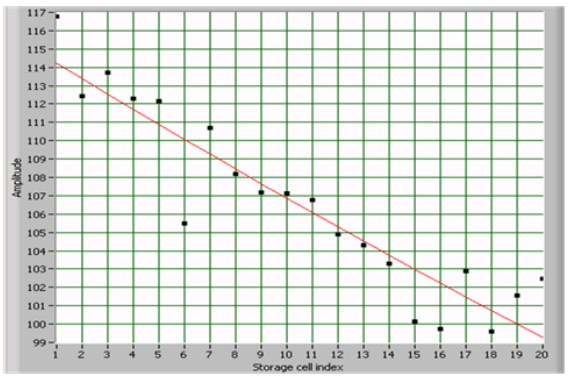
- 3 phase CCD $\Rightarrow$ charge can be transferred in both directions
- CTE is measured by comparing Case 1 and Case 2
- CTE $\gtrsim$ 99% limited by temperature instability

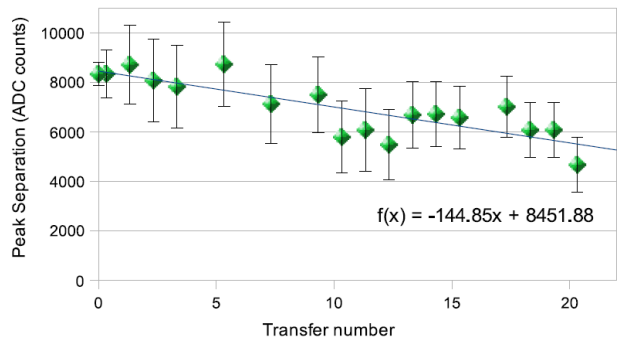


Y.Li, J.J.John

Charge Transfer Efficiency (2)

- CTE is also measured by comparing the charge from each individual storage cell.
- Final charge $S_N = S_0 \times (1 - CTI)^N \approx S_0(1 - N \times CTI)$
- Two different method to achieve hits on individual cell:





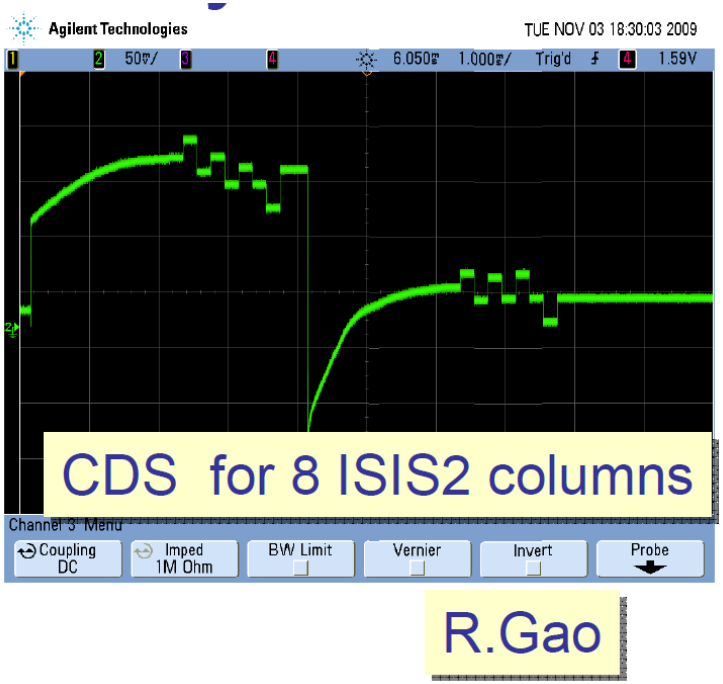
- by moving the source (Z. Zhang)
- CTE 99.3%

- with an optical shutter (H. Wilding, Y. Li)
- CTE 98.4%

- Two numbers are measured using different sensor splits from different wafers, yet still very similar

Full Array Readout

- 128 rows $\times$ 32 columns
- 32 columns serialized into 4 outputs
- Rolling shutter readout
- $\times$ Logic bug - cannot single out one row for pixel-level correlated double sampling



Future

- Design bugs of ISIS2 to be fixed
  - buried channel reset transistor
  - resistive polysilicon gate
  - logic of rolling shutter
- ISIS3: larger sensor with more compact pixel geometry and data serialization.

Summary

- ISIS Approach has its advantage for ILC vertexing and beyond
- ISIS2 successfully demonstrated feasibility of multiple charge storage and transfer in CMOS process
- A few defects in ISIS2 design/manufacture, but well understood and easy to fix in future iteration