Institut Pluridisciplinaire Hubert CURIEN STRASBOURG

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Development of fast and high precision CMOS pixel sensors for an ILC vertex detector

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Outline

- *MIMOSA26 design and test results*
  - *Comparison normal and high resistivity EPI*
- *Sensor design plan for the coming 2-3 years*
  - *Innermost layer sensors design*
  - *Outer layer sensors design*
- *Conclusion*

cnrs IN2P3 Les deux infinis

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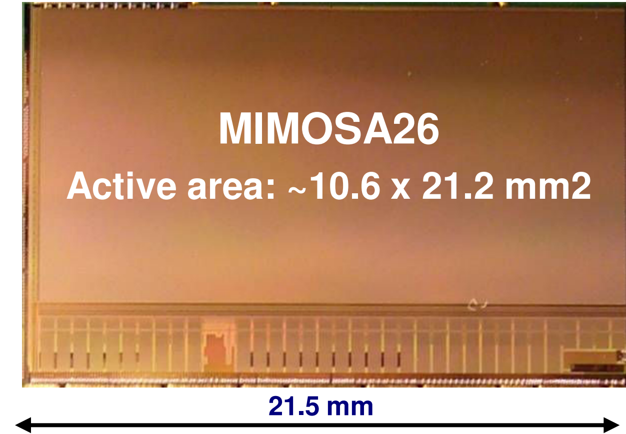
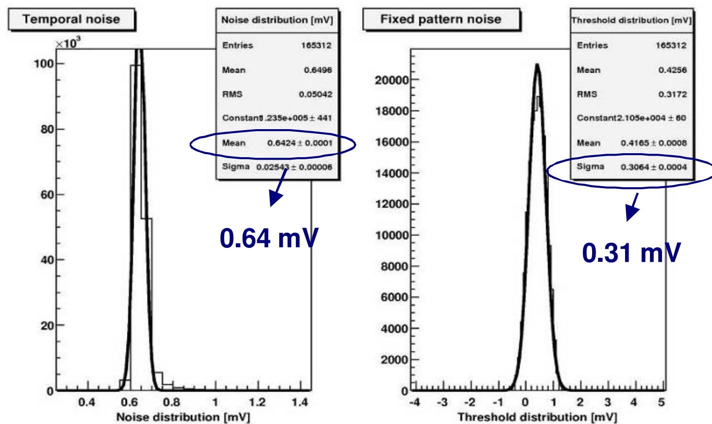
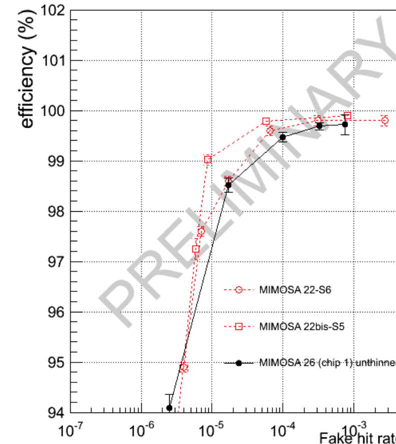
Development of CMOS Pixel Sensors for Charged Particle Tracking

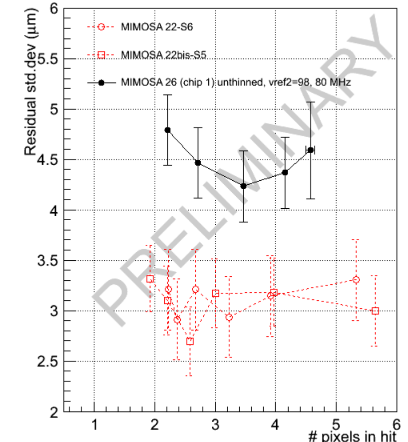
- *2009, an important year for CMOS pixel sensors R&D: MIMOSA26 has been designed, fabricated and tested within the EUDET program*
- *MIMOSA26 is a reticule size MAPS with binary output, 10 k images / s*
  - *Pixel array: 1152 x 576, 18.4 µm pitch*
  - *Architecture:*
    - *Pixel (Amp+CDS) array organised in // columns r.o. in the rolling shutter mode*
    - *1152 ADC, a 1-bit ADC (discriminator) / column*
    - *Integrated zero suppression logic*
    - *Remote and programmable*



- *Lab. and beam tests: 62 chips tested, yield ~75%*





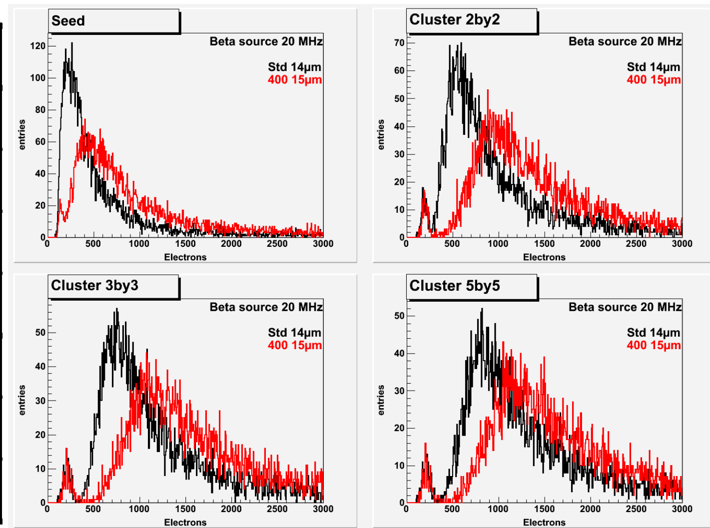


ENC ~ 13-14 e^- **Efficiency 99.5% for fake rate 10^{-4}** **Single point resolution ~4 µm**

MIMOSA26 Test

- *Standard EPI layer (fab. end 2008) v.s. high resistivity EPI layer (fab. end 2009)*
  - *Charge collection & S/N (Analogue output, Freq. 20 MHz)*

EPI layer	Standard (~10 Ω.cm) 14 µm			High resistivity (~400 Ω.cm)			
	Seed	2x2	3x3	EPI	seed	2x2	3x3
Charge Collection (^{55}Fe source)	~21%	~ 54 %	~ 71 %	10 µm	~ 36 %	~ 85 %	~ 95 %
				15 µm	~ 31 %	~ 78 %	~ 91 %
				20 µm	~ 22 %	~ 57 %	~ 76 %
S/N at seed pixel (^{106}Ru source)	~ 20 (230 e^-/11.6 e^-)			10 µm	~ 35		
				15 µm	~ 41		
				20 µm	~ 36		



  - *Radiation test under way for applications more demanding than ILC*
    - *Ionising TID: 150 K , 300 K, 1M Rad*
    - *Non Ionising NIEL: $3x10^{12}$, $6x10^{12}$, $1x10^{13}$, $3x10^{13}$ N_{eq}/cm^2*

- *MIMOSA26 can be operated at a high readout speed*
  - *Clock frequency: from 80 $MHz_{typ.}$ (~110 µs) up to 110 MHz (~80 µs)*

➔ *MIMOSA26: design base line for STAR Vx upgrade, CBM MVD*
Its performances are close to the ILD vertex detector specifications

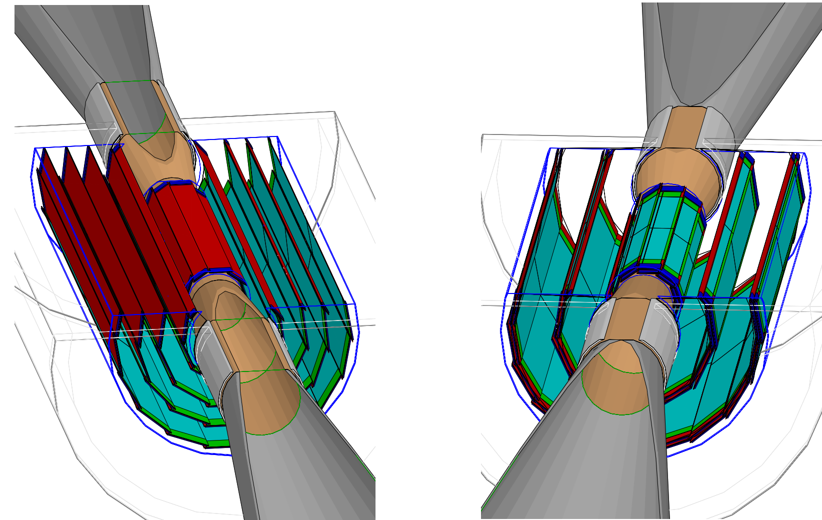
ILC VTX : R&D of CMOS Sensors

- ***Innermost layer sensors:***
  - $t_{int.}$ ~ 25 µs
    σ_{sp} < 3 µm
    R&D effort on high readout speed design
    - *Double-sided readout (for both design options)*
    - *Elongated pixels (for 3 double layers option: time stamp tier)*

- ***Outer layer sensors:***
  - $t_{int.}$ <~ 100 µs
    σ_{sp} ~ 3-4 µm
    R&D effort on low power consumption design
    - *Single-sided readout (for both design options)*
    - *4-bit column-level ADCs*

- ***Power consumption:***
  - P_{diss} < 0.1–1 W/cm² (× ~ 1/50 duty cycle)

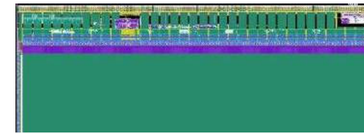
ILD design: 2 options

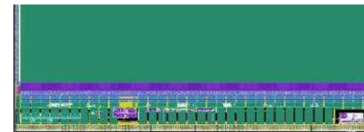


5 single layers **3 double layers**

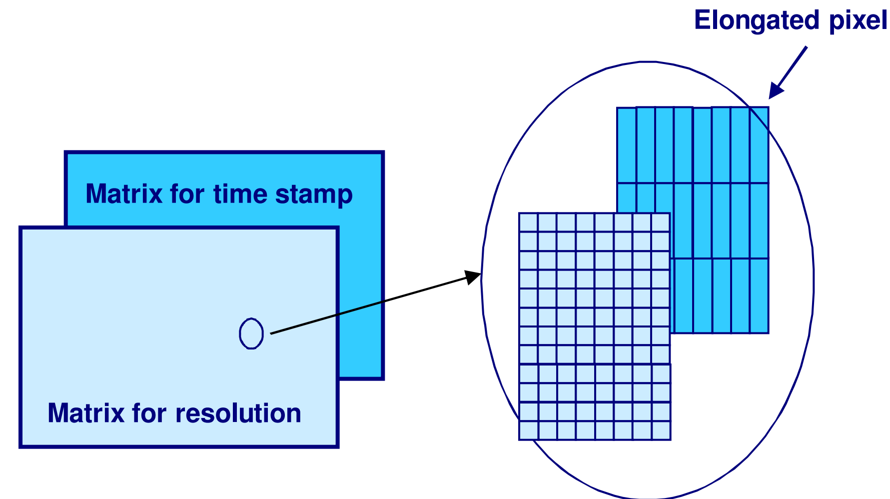
Innermost Layer CMOS Sensor's Development

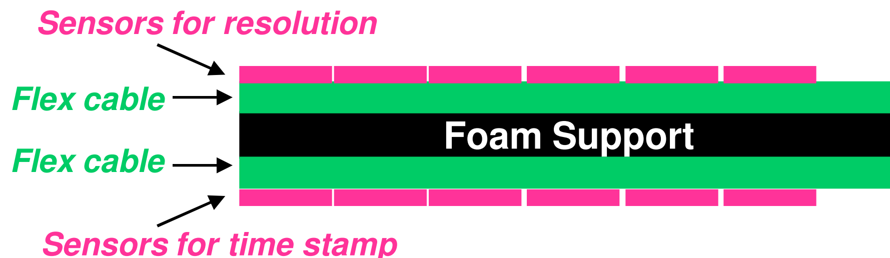
- *1st R&D line: double-sided readout*
  - *Based on architecture of MIMOSA26*
    - *Rolling shutter readout mode + A/D conversion ➔ binary output + zero suppression*
  - *Pixel array: ~ 14 µm pitch*
  - *Active area: ~ 9 x (~ 20) mm²*
  - *$t_{int.}$ <~ 40-60 µs*
  - *P_{diss} <~ 1 W/cm² (× ~ 1/50 duty cycle)*





- *2nd R&D line: elongated pixels*
  - *Time stamp tier for 3 double layers option*
    - *Ex: 14 x (4 x 14 µm)*
  - *$t_{int.}$ <~ 10-15 µs*
  - *High resistivity EPI process useful*
    - *High charge collection efficiency*





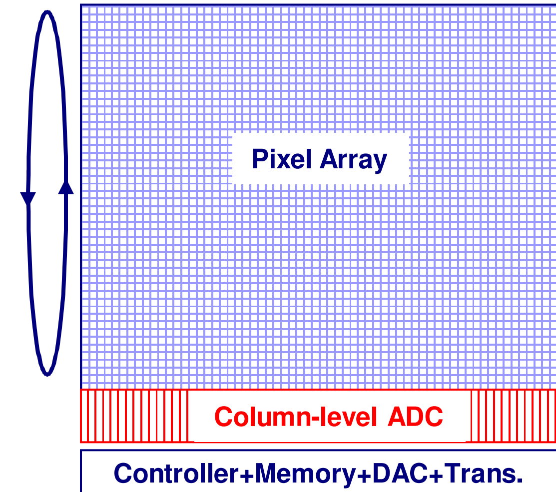
"Plume" Project ➔ Integration topic

Collaboration: Strasbourg, DESY, Oxford, Bristol, ...

See Nathalie Chon-Sen's talk:

ILC Outer layer CMOS Sensor's Development

- *Large pitch pixels associated with column-level ADC*
  ➔ power consumption reduction
- *Single-sided readout*
  - *Pixel array: 576 x 576, pitch 35 µm*
  - *4-bits ADC / column*
  - $t_{int.}$ *~ 60 - 100 µs*
  - P_{diss} *<~ 0.2 W/cm² (x ~ 1/50 duty cycle)*



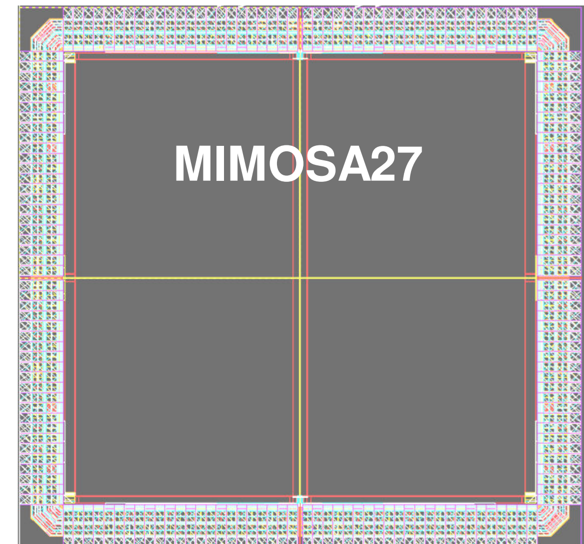
- *Different column-level ADC architectures have been investigated in IN2P3-CEA collaboration*
- *Taking integration experience of MIMOSA26, ADC's architecture will be extended to several hundreds ADCs converting all signals of a row simultaneously*
  - *Noise from substrate coupling*
  - *Coupling between ADC*
  - *Long common reference line (~2 cm) for whole chip*
  - *Offset compensation*
  - *Clock and control signals management*

  ➔ Submission of a small sensor but a sizable prototype: pixel array + column-level ADC

Exploration of new process

- ➔ *Using a smaller feature size CMOS technology: 0.18 µm*
  - *High speed operation inside chip*
  - *Surface reduction in digital design*
  - *Reduce power consumption …*
  - *Offer more metal layers for interconnection ➔ decrease dead zone*

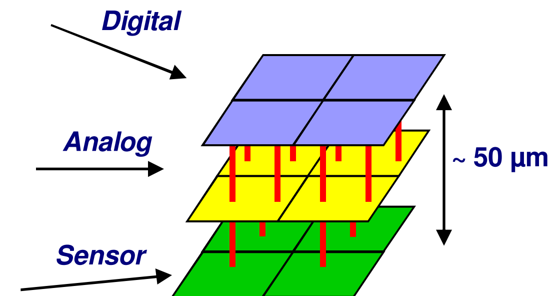
- *MIMOSA27 in a 0.18 µm process (up to 6 metal layers) will be submitted on April 9th, 2010*
  - *10 mm², 20 µm pitch, 4 sub-matrices of 64 x 64*
    - *Up to16 options:*
      - *Diode size and type of configuration*
      - *3 T and self-bias*
      - *In pixel amplification*
    - *Study:*
      - *Charge collection efficiency*
      - *Technology features*
      - *Signal to noise ratio*
      - *Radiation hardness*
      - *…*



Using 3DIT to improve MAPS performances (1)

- ***3DIT are expected to be particularly beneficial for MAPS :***
  - ***Combine different fabrication processes*** ➔ *Split signal collection and processing functionalities* ➔ *use best suited technology for each Tier :*
    - *Tier-1: charge collection system ➔ Epitaxy (depleted or not) ➔ ultra thin layer➔ X_0* ↓
    - *Tier-2: analogue & mixed signal processing➔ analogue, low I_{leak}, process (No. of metal layers)*
    - *Tier-3: digital signal processing & data transmission*
    - *(Tier-4: data transmission, electro-optical conversion ?)*

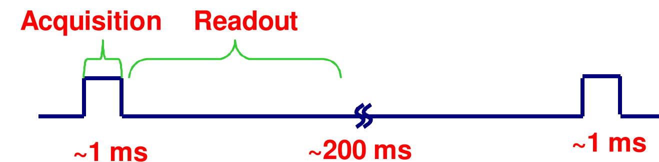
    > *digital process (number of metal layers) feature size➔ fast laser driver, etc.*
  - ***Resorb most limitations specific to 2D MAPS***
    - *Dead surface* ↓
    - *Power consumption*↓
    - *Readout speed*↑
    - *…*



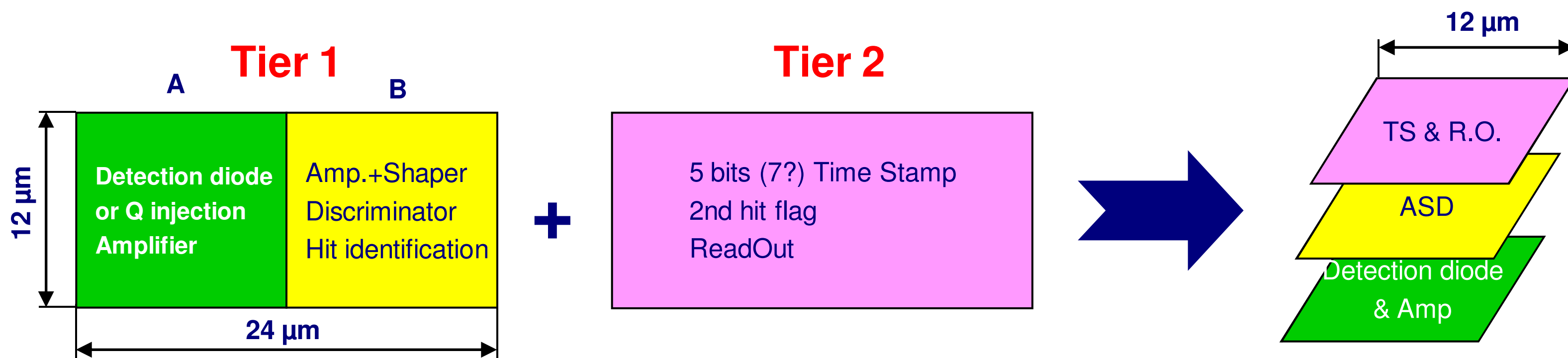
- ***2009: run in Chartered - Tezzaron technology***
  - *3D consortium: coordinated by FermiLab*
  - *130 nm, 2-Tier run with "high"-res substrate (allows m.i.p. detection)*
    - *Tier A to tier B bond➔ Cu-Cu bond*

Using 3DIT to improve MAPS performances (2)

- *Delayed R.O. Architecture for the ILC Vertex Detector (designed & submitted)*
  - *Try 3D architecture based on small pixel pitch, motivated by :*
    - *Single point resolution < 3 µm with binary output*
    - *Probability of > 1 hit per train per pixel << 10 %*
    - ➔ *12 µm pitch :*
      - σ_{sp} *~ 2.5 µm*
      - *Probability of > 1 hit/train/pixel < 5 %*



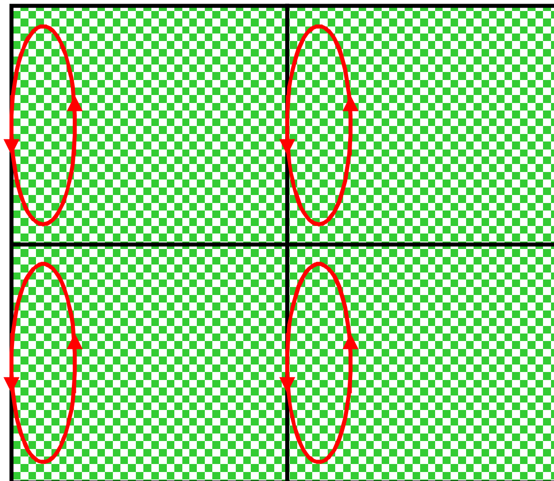
  - ***3D 2-tier process***
    - *Tier-1: A: sensing diode & amplifier, B: shaper & discriminator*
    - *Tier-2: time stamp (5 bits) + overflow bit & delayed readout*
  - ➔ *Architecture prepares for 3-Tier perspectives : 12 µm*
    - *Tier-1: CMOS process adapted to charge collection*
    - *Tier-2: CMOS process adapted to analogue & mixed signal processing*
    - *Tier-3: digital process (<< 100 nm ?)*

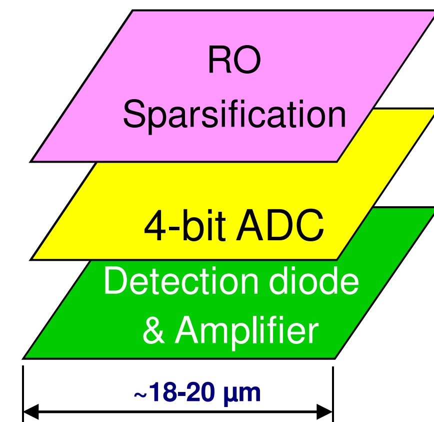


Using 3DIT to improve MAPS performances (3)

- ***MAPS with fast pipeline digital readout aiming to minimise power consumption (R&D in progress)***
  - *Subdivide sensitive area in "small" matrices running individually in rolling shutter mode*
  - *Adapt the number of raws to required frame readout time*
    - ➔ *few µs r.o. time may be reached*
  - *Design in 20 µm²:*
    - *Tier 1: Sensor & preamplifier (G ~ 500 µV/e⁻)*
    - *Tier 2: 4-bit pixel-level ADC with offset cancellation circuitry (LSB ~ N)*
    - *Tier 3: Fast pipeline readout with data sparsification*

➔ σ_{sp} ~ 2 µm
$T_{int.}$ < 10 µs





Conclusion

- ***MIMOSA26's performances are close to ILD vertex detector specifications***
  - ➔ ***Architecture will evolve to meet VTX performances***
  - *Innermost layer: double sided readout ➔ readout speed trade-off*
  - *Outer layer: matrix + column-level ADC➔ power consumption trade-off*

- ***Fabrication processes with high resistivity EPI layer will improve read-out speed and radiation tolerance***
  - *Time stamp layer*

- ***Integration of column-level ADCs with pixel array in progress***

➔ ***Prototyping of inner and outer layer sensors expected to be nearly finalised by 2012 for ILD-DBD***

- ***Translation to 3DIT will resorb most limitations specific to 2D MAPS***
  - *Still many difficulties to overcome*
  - *Offer an improved read-out speed : O(μs) + Lower power consumption*