# CALICE Second Generation AHCAL Developments

Riccardo Fabbri

**on behalf of the *CALICE* Collaboration**

**LCWS/ILC 2010** **Beijing, 28 March 2010**

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- **Prototypes for the AHCAL Calorimeter**
- **Mechanical Concept**
- **System Subcomponents**
- **Test Beam Campaign at DESY**
- **Commissioning: Preliminary Results**
- **Conclusions and Outlook**

# Prototypes for the Analogue HCAL

- **Physics ($1^{st}$ generation) prototype successfully used in test-beam campaigns at DESY, CERN & FNAL (2006-09)**

  **$\Longrightarrow$ to evaluate the calorimetry technology for ILC**

  — $1m^2$ **instrumented volume,** $38$ **layers with** $2cm$ **absorber per layer**

  — **Active layers made of scintillating tiles;** $216$ **cells per layer, ranging from** $3x3cm^2$ **to** $12x12cm^2$**, individually readout by SiPMs**

  — $7608$ **channels in total; detailed** $3D$ **reconstruction of hadronic showers**

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  — $7608$ channels in total; detailed $3D$ reconstruction of hadronic showers

- Technological ($2^{nd}$ generation) prototype under development/commissioning

  $\Longrightarrow$ Demonstrate feasibility to build calorimeter with fully integrated electronics meeting constraints of a real detector

  — Milions of channels to be handled (high-granularity calorimeter)

  — Non-invasive integration needed; as close as possible to active area in detector

  ✥ compact design with integrated sensors & electronics

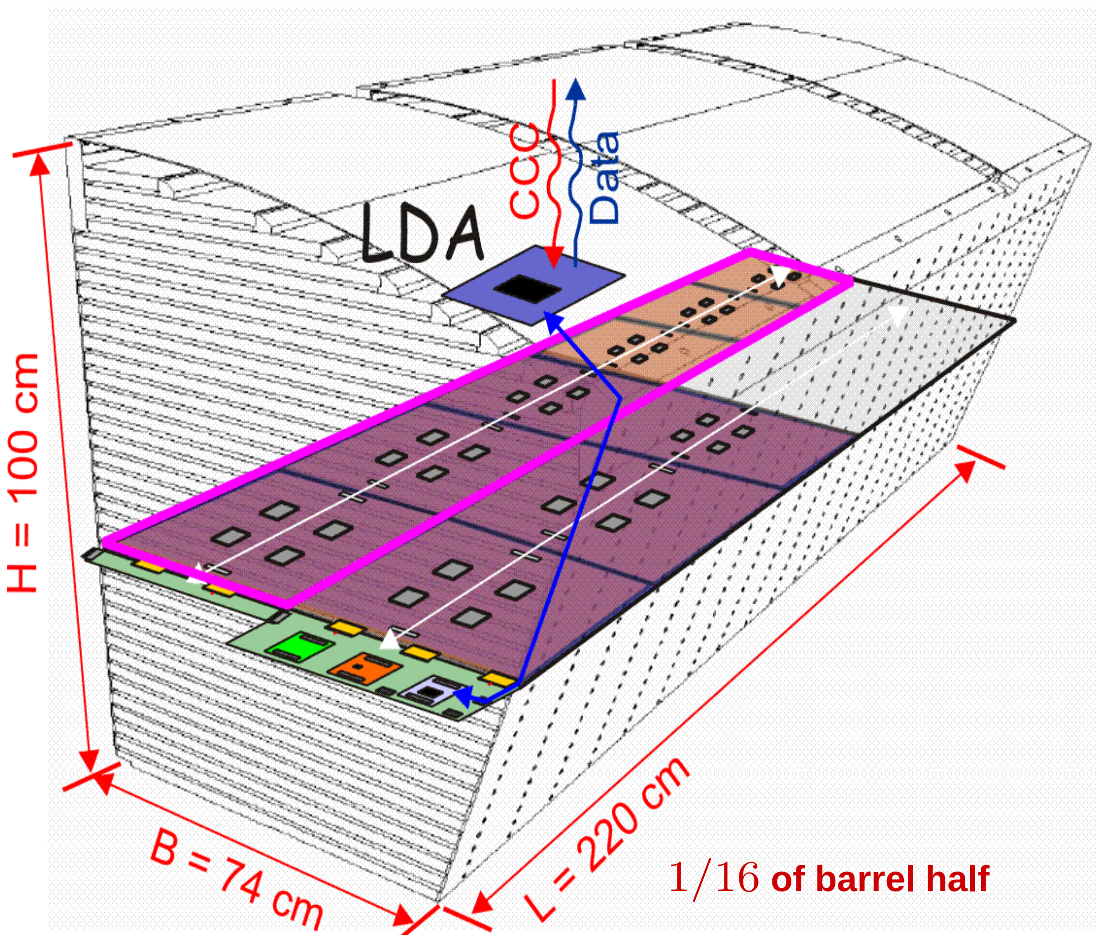
  ✥ minimum dead areas and power consumption

  ✥ maximum compactification

# Mechanical Concept

**Barrel of HCAL architecture:**
- — scintillator-based calorimeter
- — granularity: $3x3$ cm$^2$ tiles
- — SiPM readout (one per tile)

**DIMENSIONS ARE APPROVED/FIXED**



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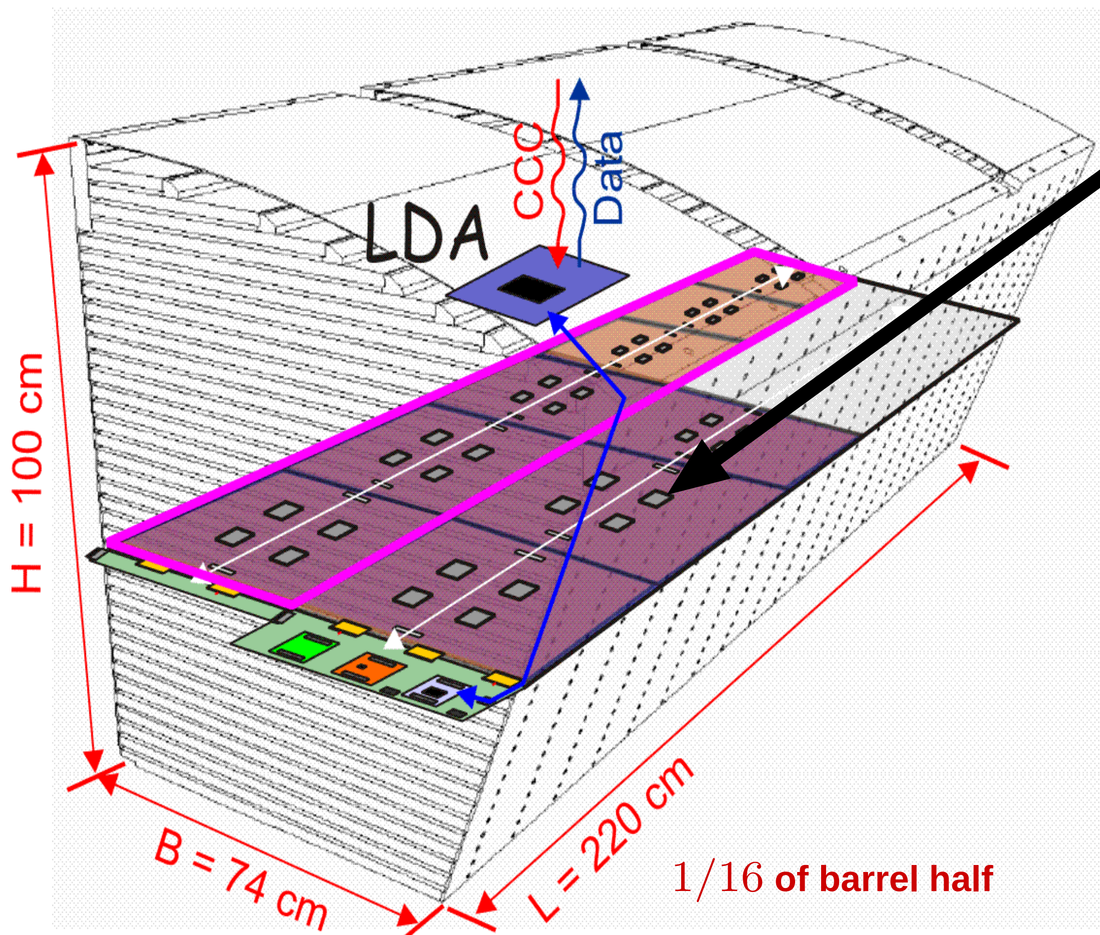


$1/16$ of barrel half

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  handles signal from $36$ SiPMs

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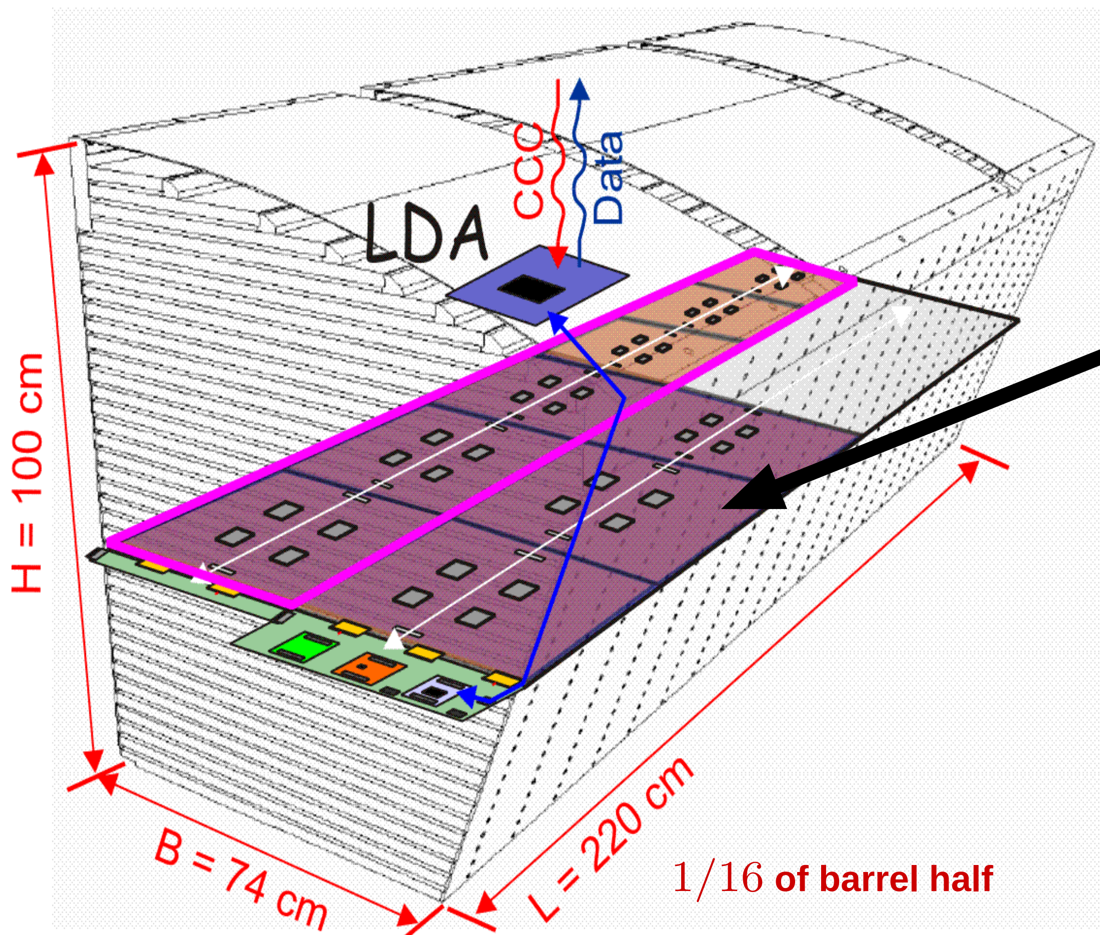


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  hosts up to $12x12$ tiles/$4$SPIROCs

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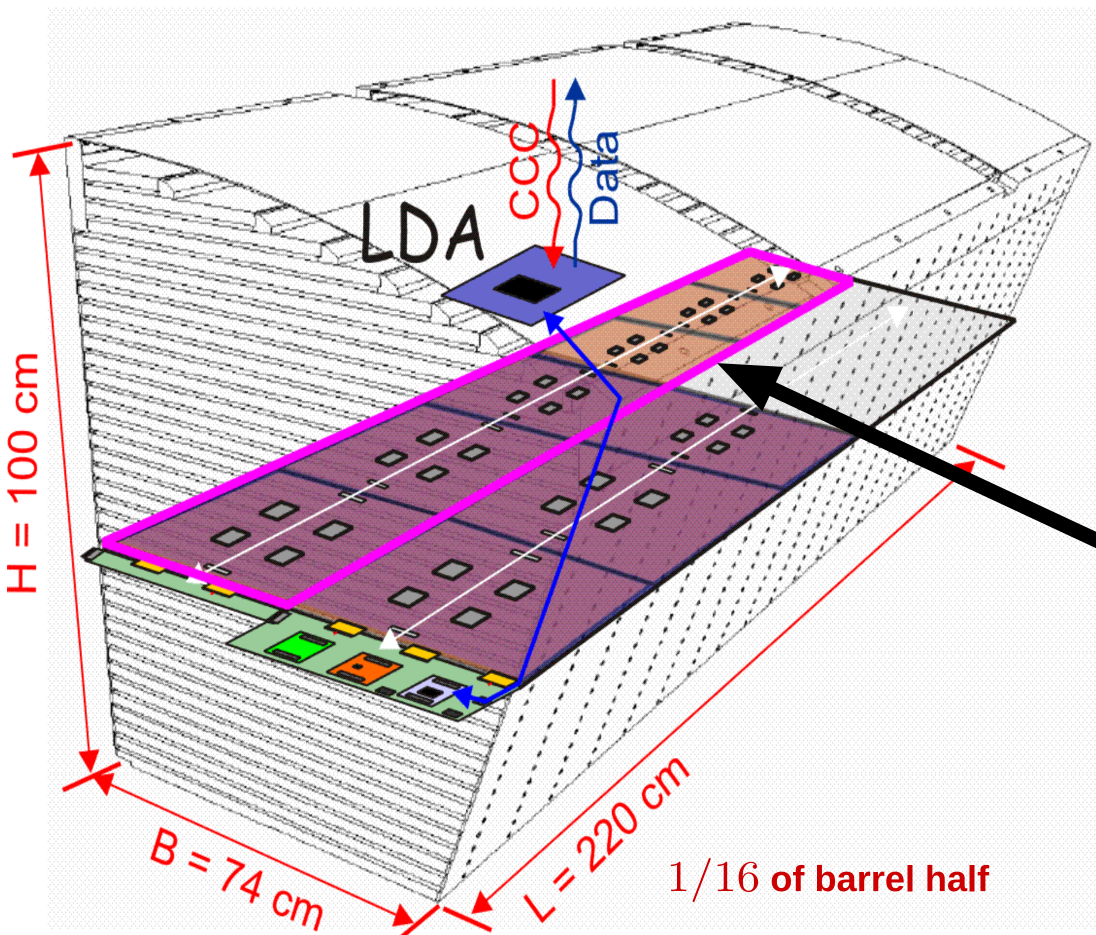


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  hosts $6$ HBUs in a row

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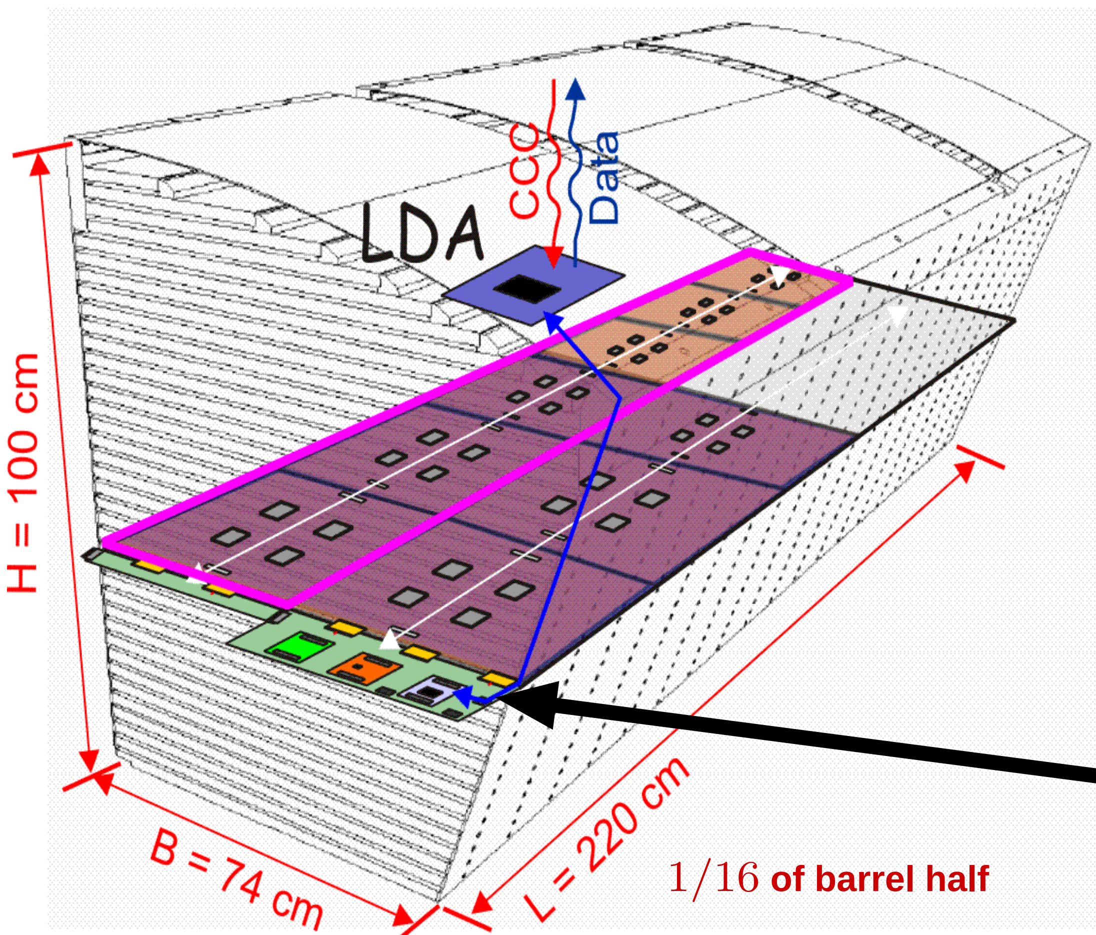


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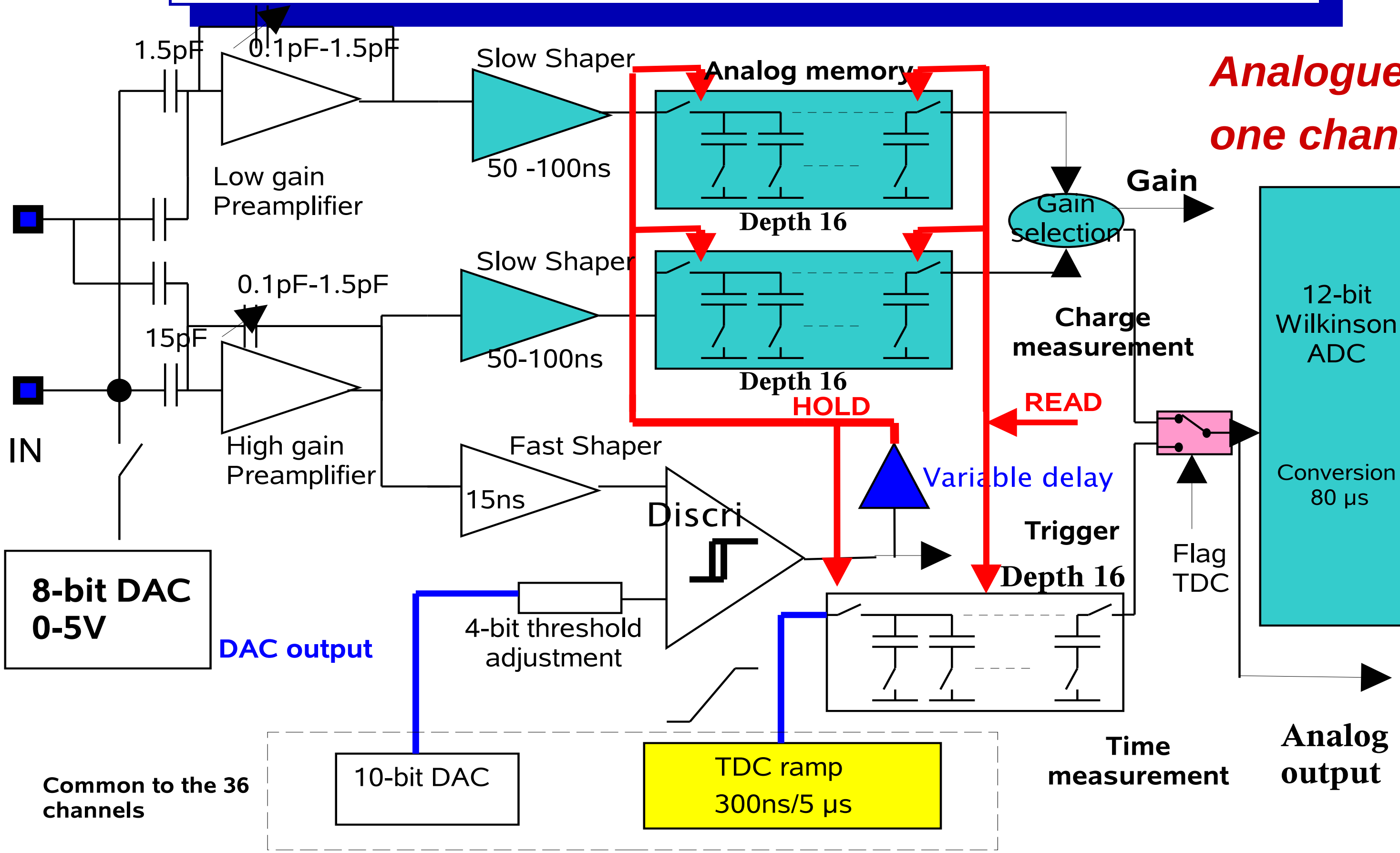
- **CIB (Central Interface Board):**
  hosts $DIF$ $CALIB$ $POWER$ modules

# Subcomponents: SPIROC ASIC

*Analogue part: one channel layout*



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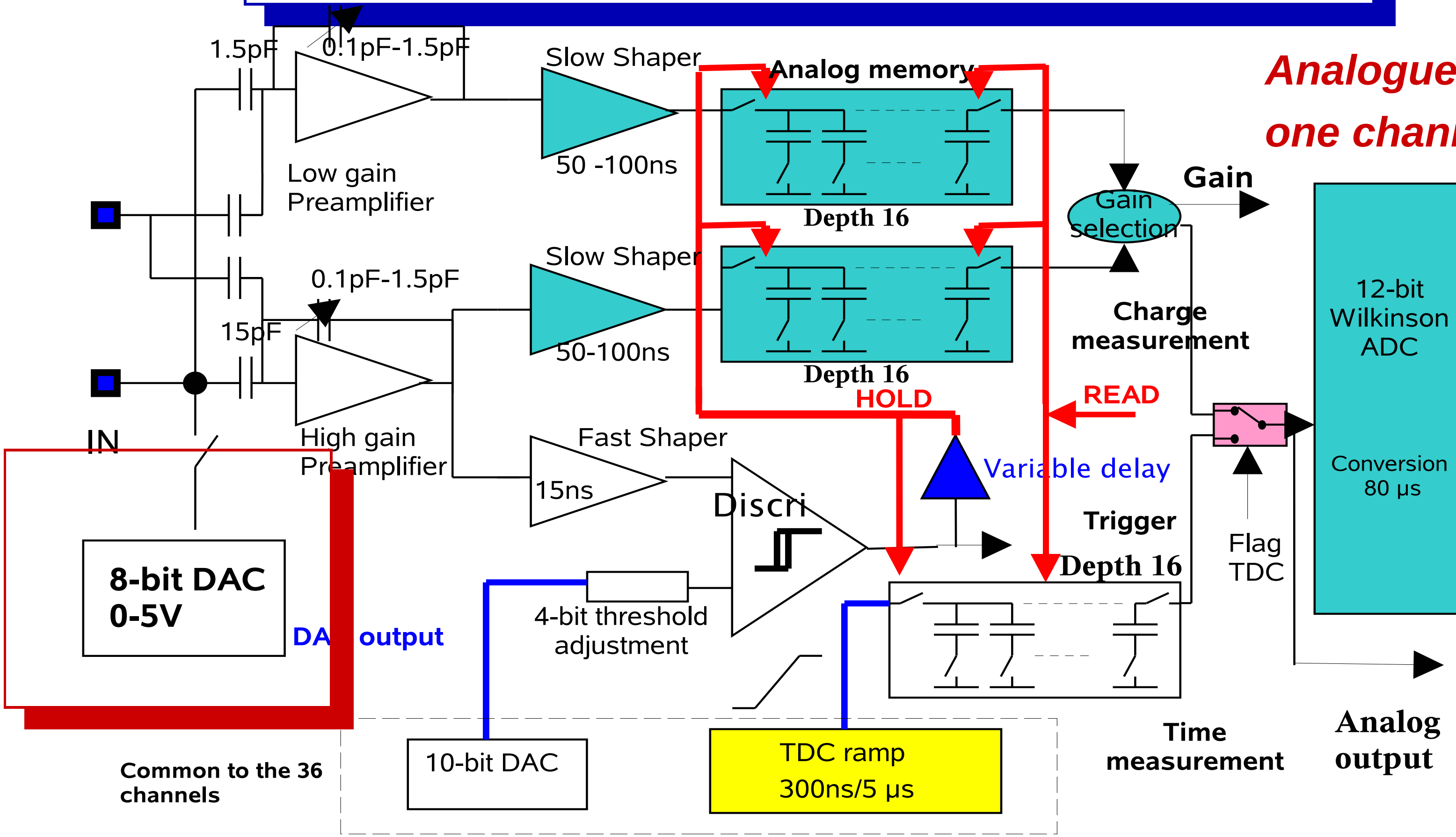
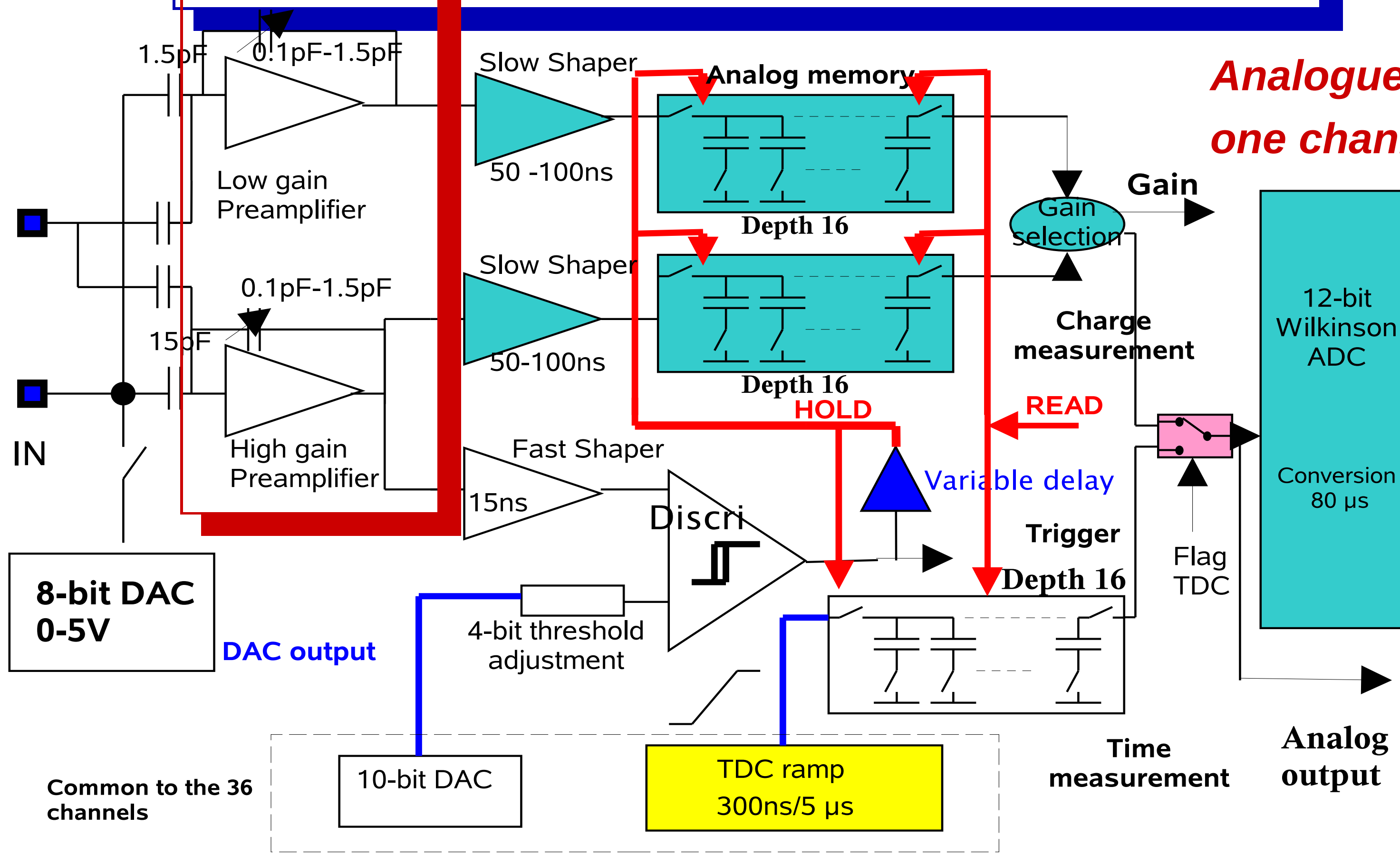



***Adjustable bias voltage for each SiPM***

# Subcomponents: SPIROC ASIC

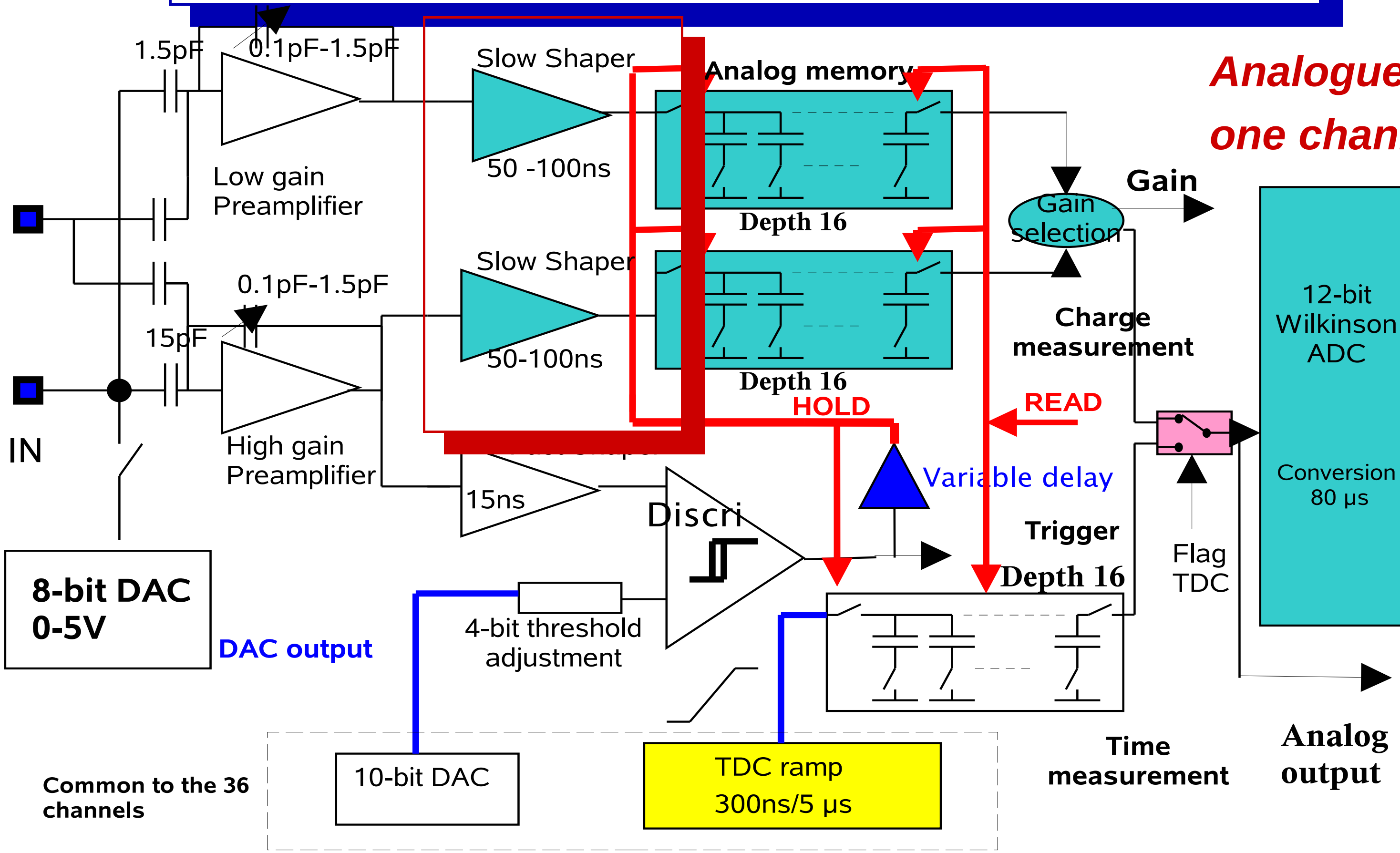



***Analogue part:***

***one channel layout***

***Separate channels for adjustable pre-amplification in low/high gain mode of input signal***

# Subcomponents: SPIROC ASIC

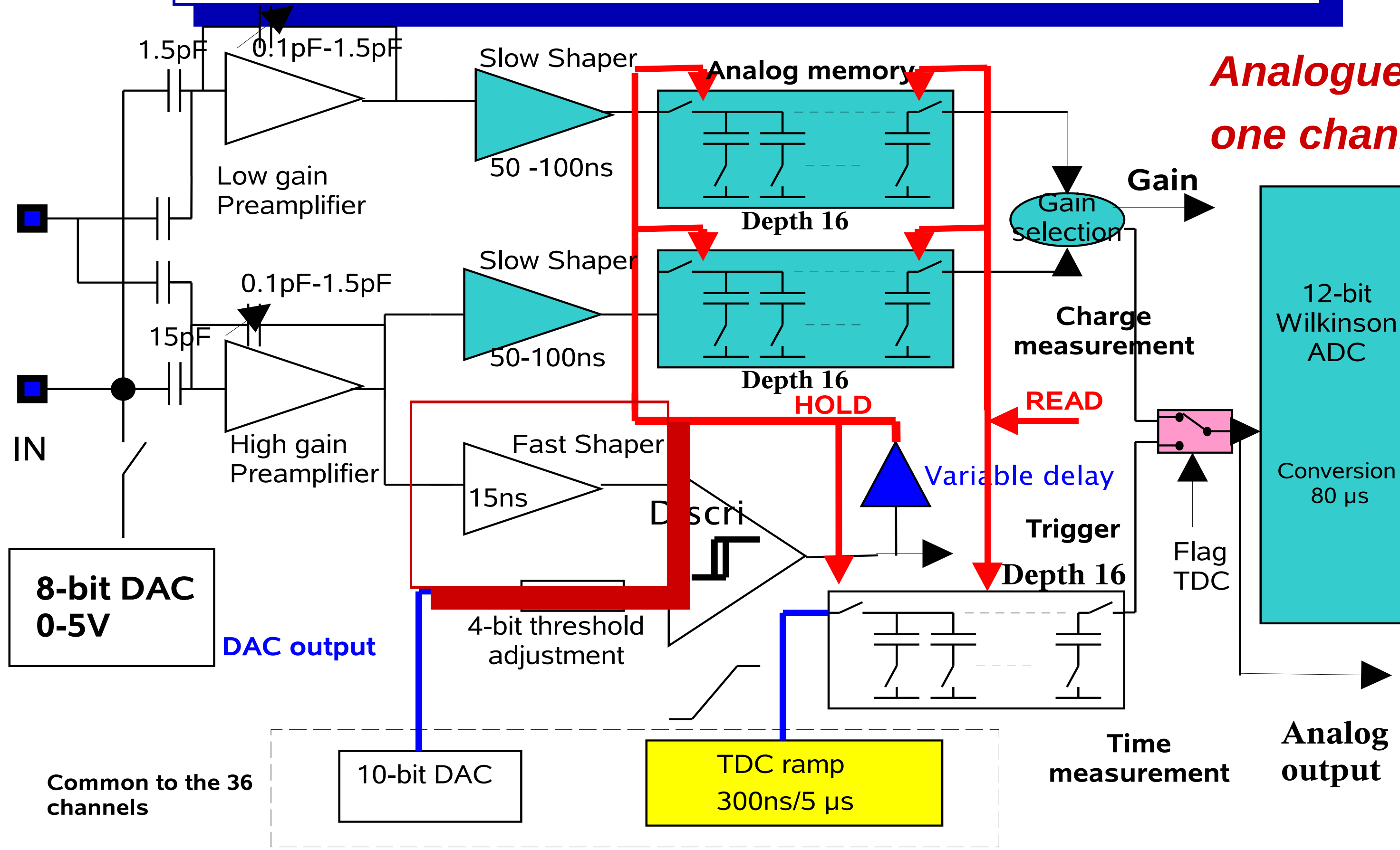



***Analogue part: one channel layout***

***adjustable shaping time***

# Subcomponents: SPIROC ASIC

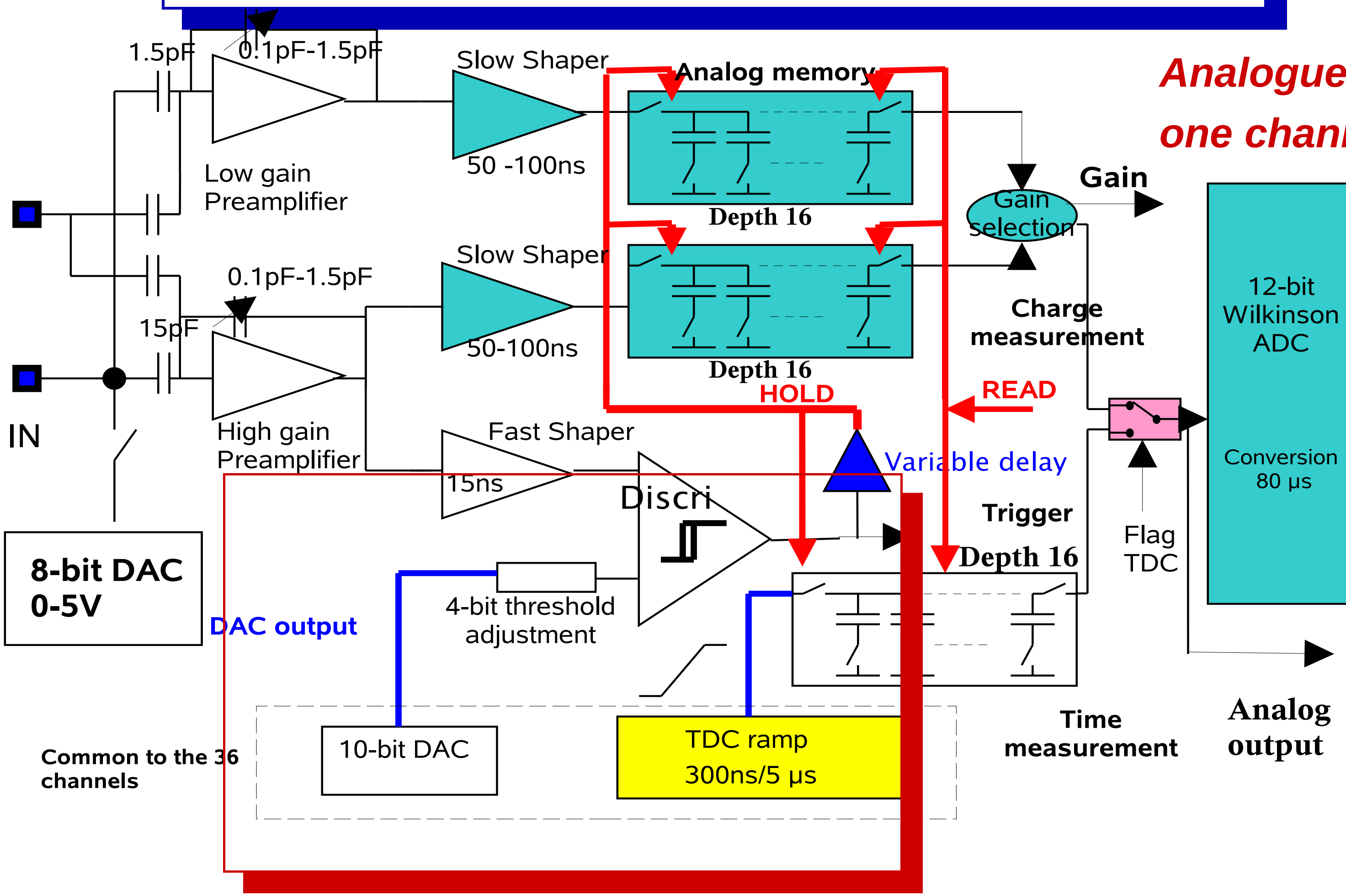
*Analogue part: one channel layout*




*fast shaper for ...*

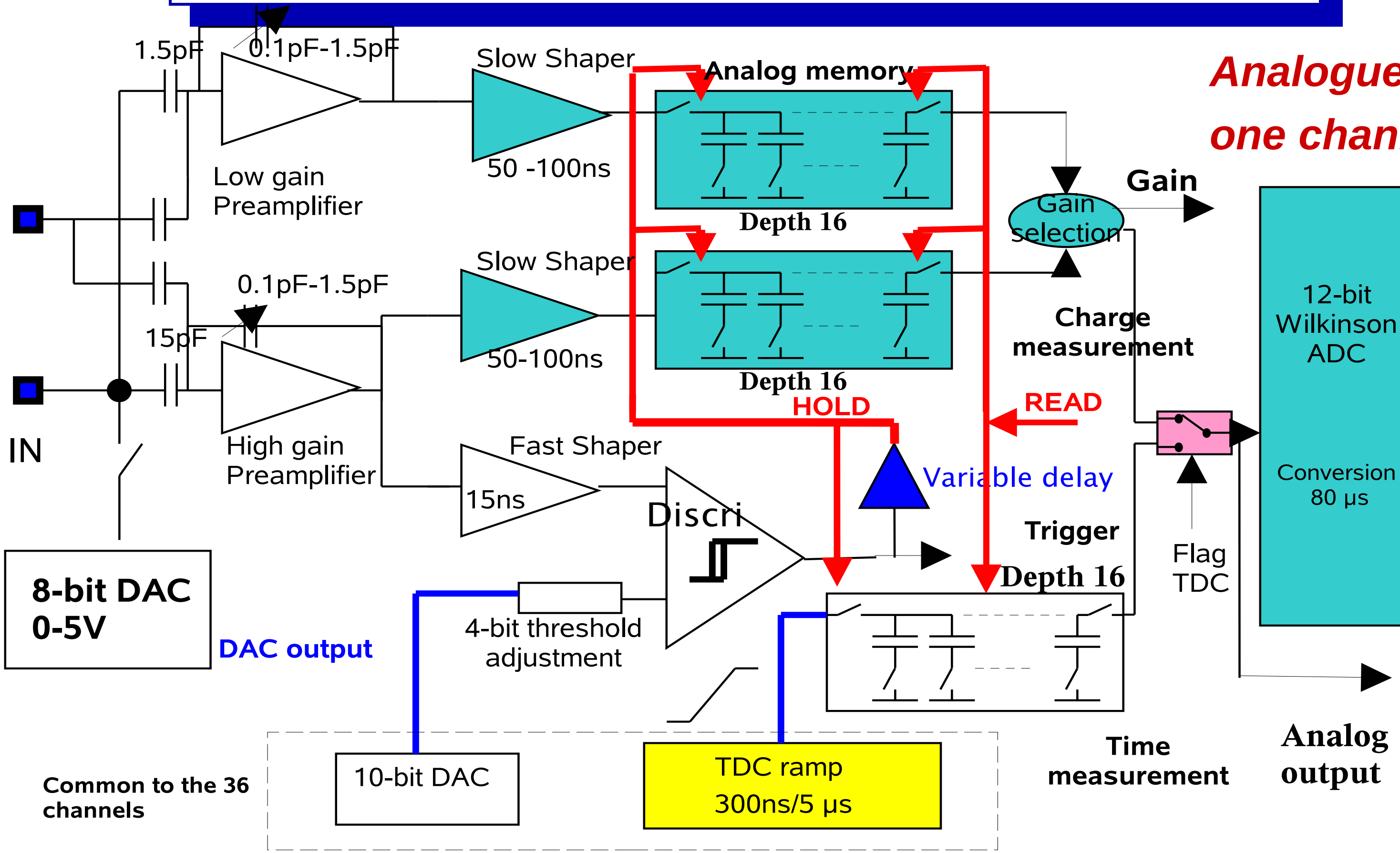
# Subcomponents: SPIROC ASIC

*Analogue part: one channel layout*




*...autotrigger (to eventually hold the analogue shaped signal)*

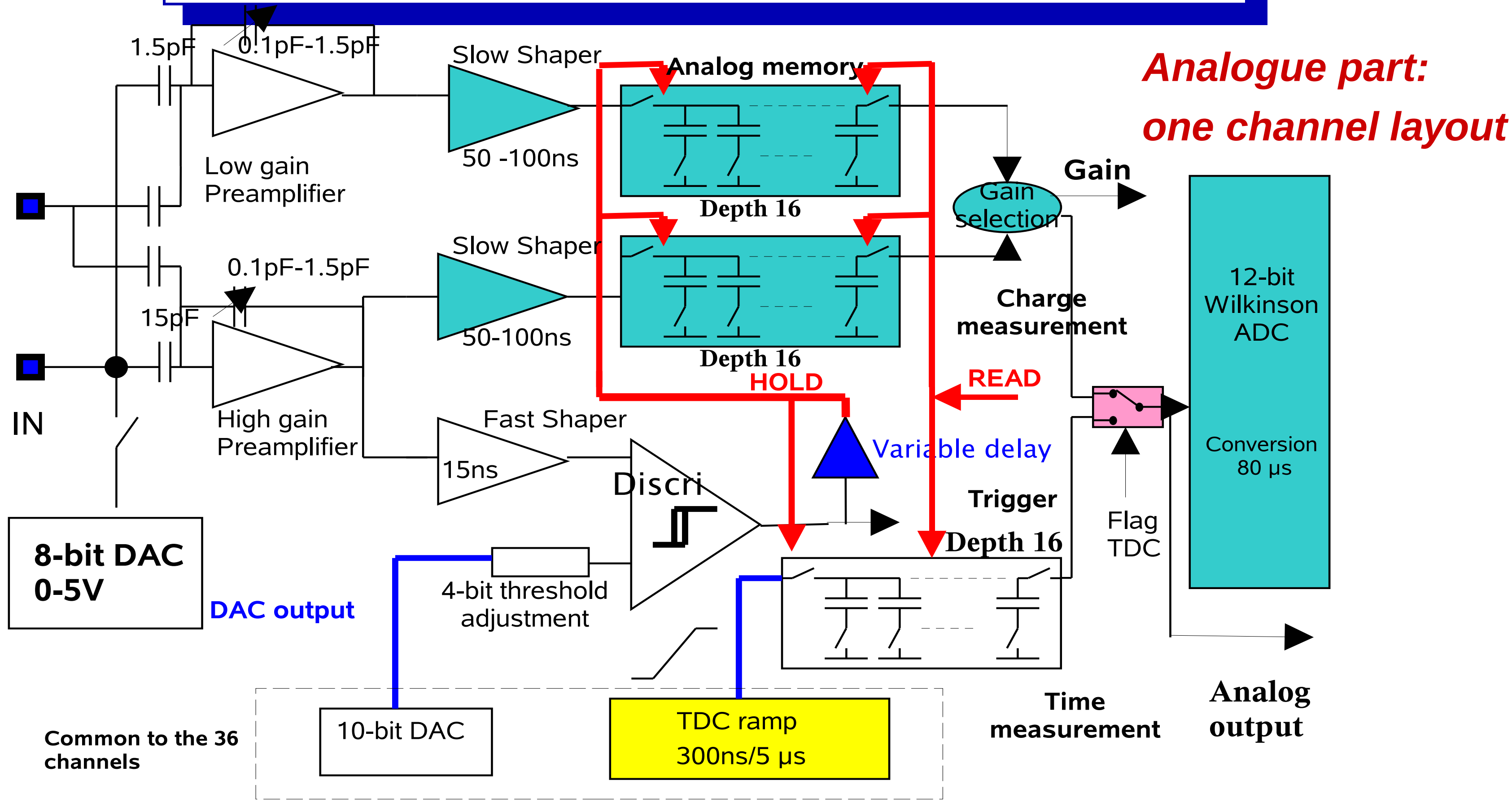
# Subcomponents: SPIROC ASIC




*Analogue part: one channel layout*

*plus digital stage (not shown here) to synchronise acquisition/readout with ILC timing*

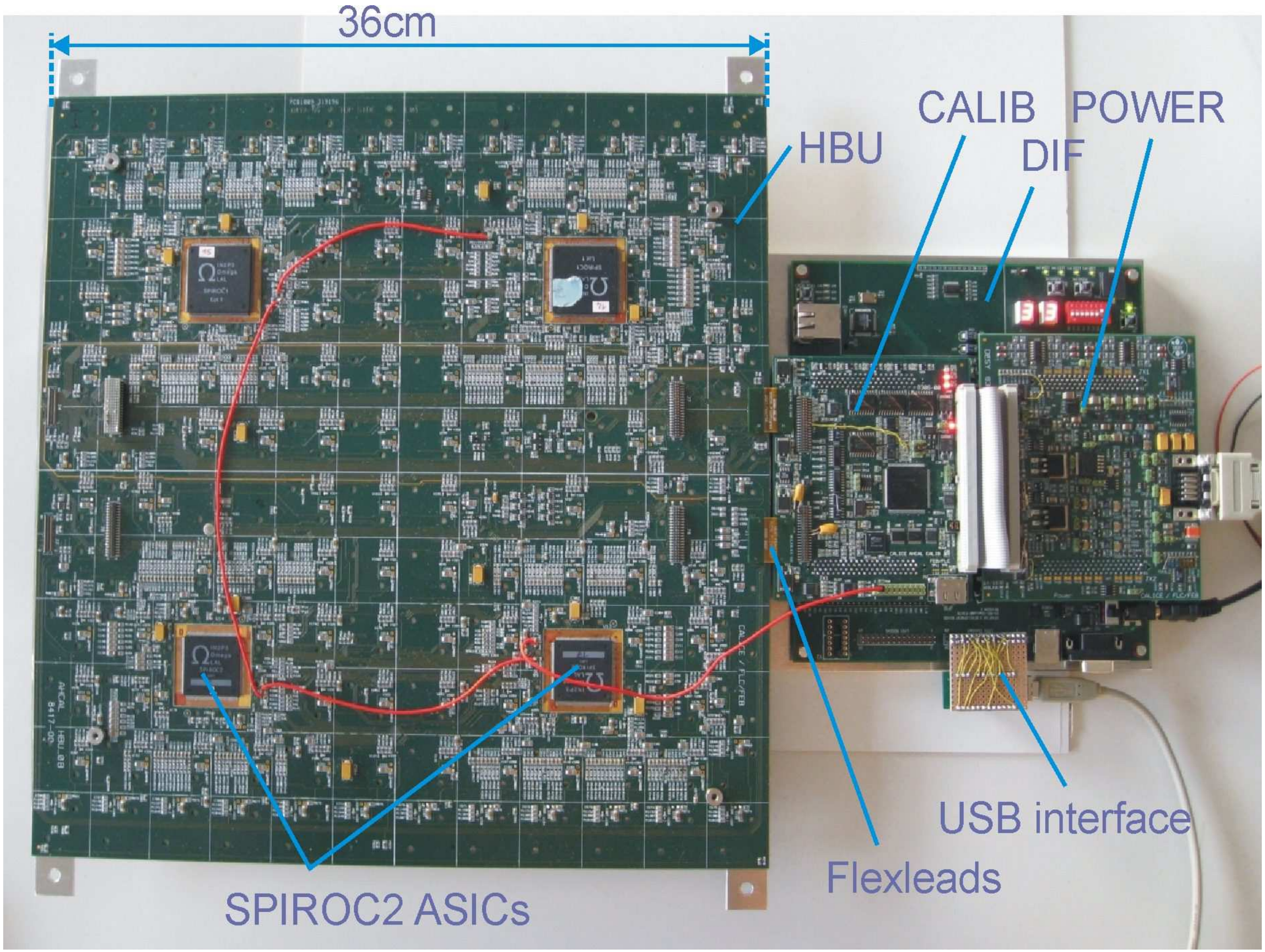
# Subcomponents: SPIROC ASIC




- **Designed/developed by LAL (Paris)**
- **Handle $36$ input signals ($36$ SiPMs)**
- **Internal ADC, autotrigger mode, low power dissipation**
- **Commissioning ongoing at DESY (strong support from LAL and Heidelberg)**

$\Longrightarrow$ **Results on analogue part finalized in arXiv:0911.1566/EUDET-Report-2009-05**

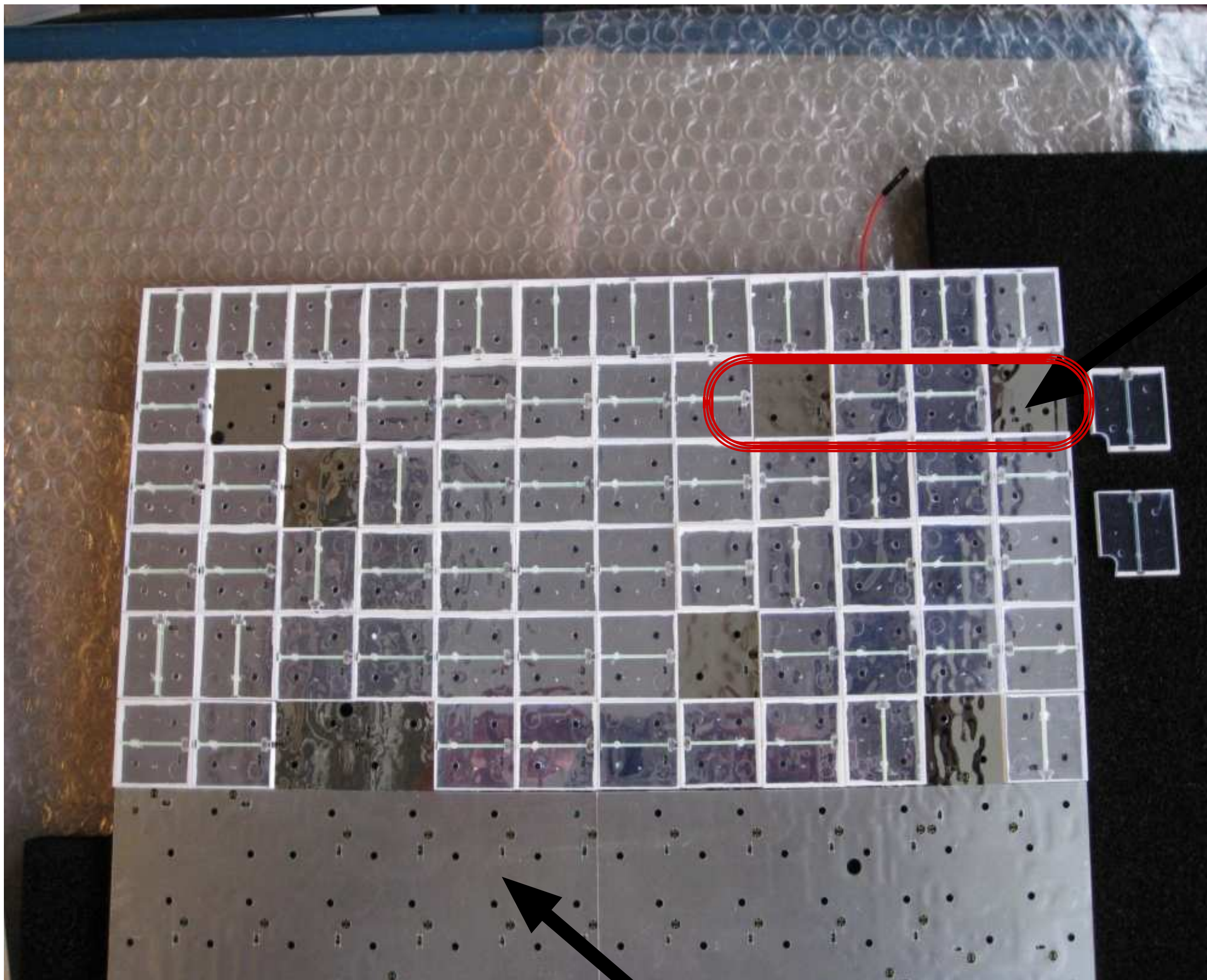
# Subcomponents: HBU (HCAL Base Unit)




- Two setups in operation (one in Lab., one in Test-beam area)

# Subcomponents: HBU (HCAL Base Unit)

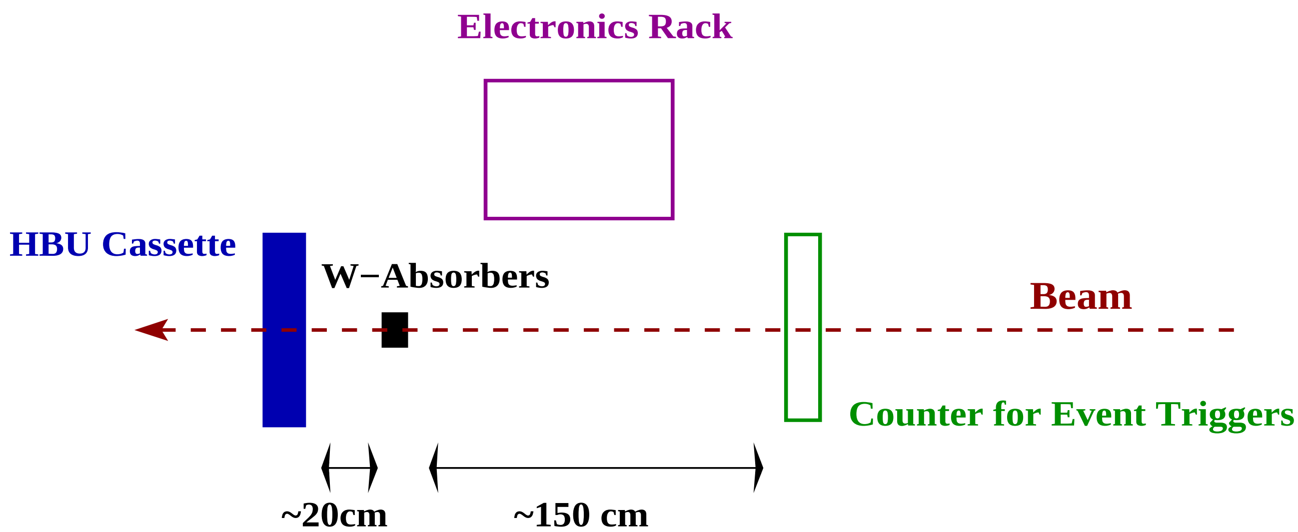
- **Both HBUs assembled with tiles in the SPIROC 2 regions**

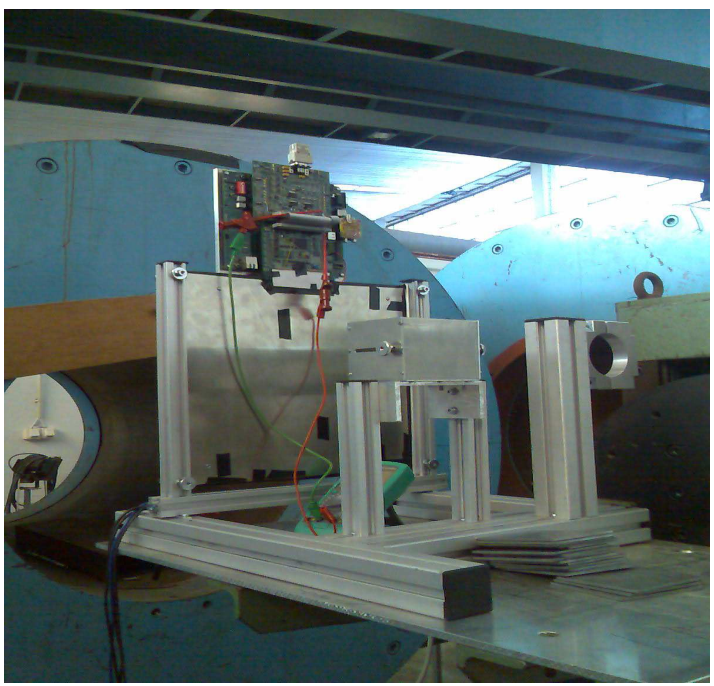


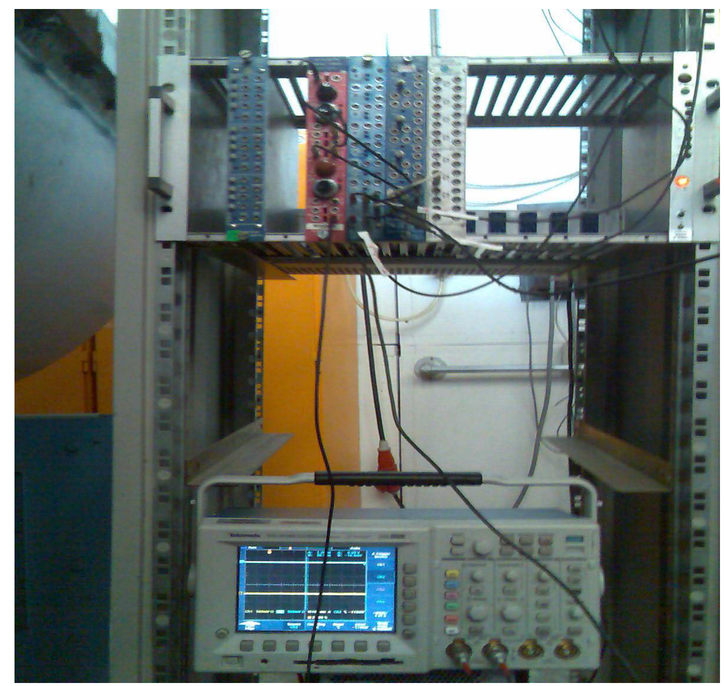
**Some positions are empty (tiles do not fit!)**

**Reflecting foil**

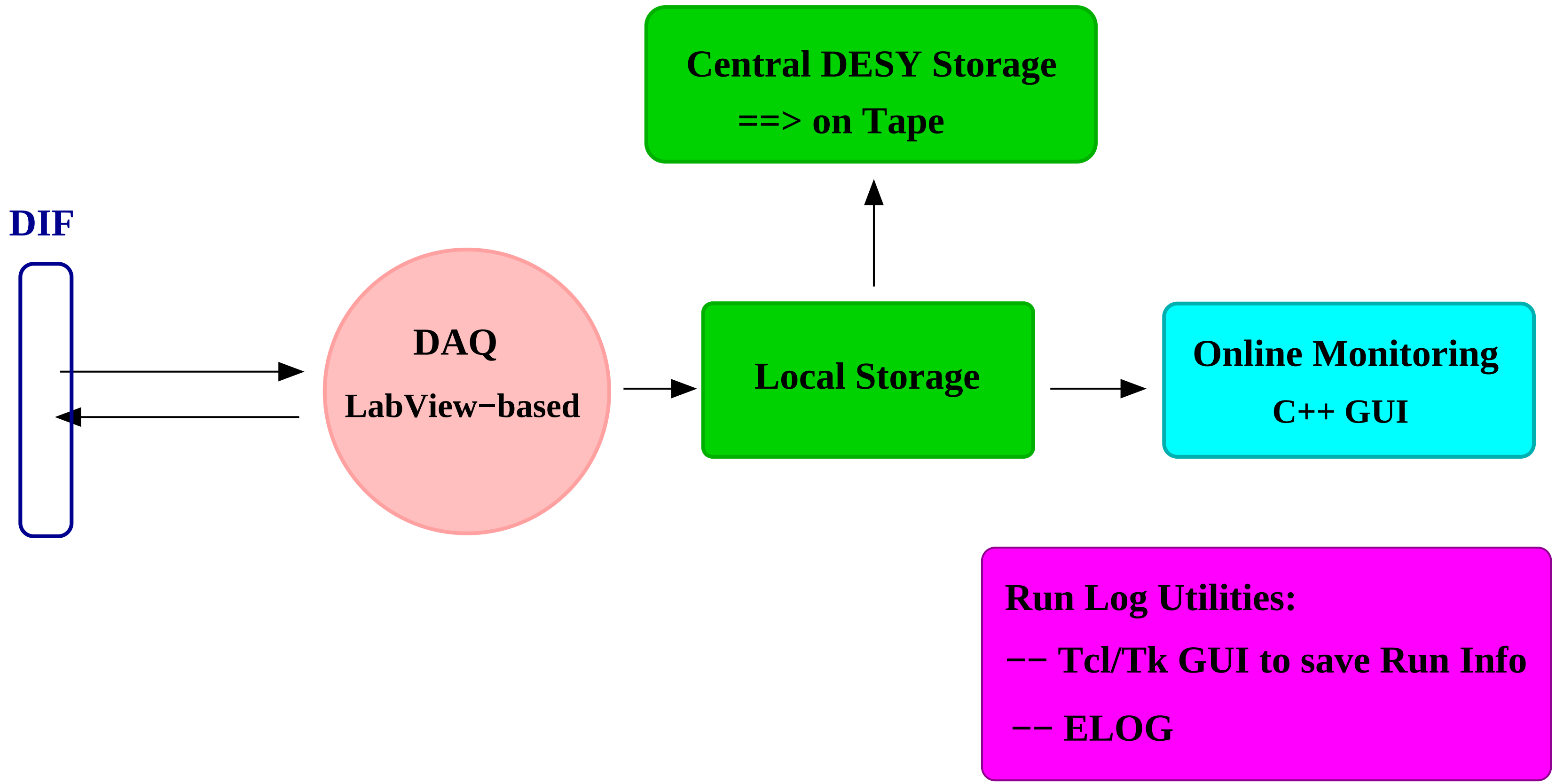
# Test Beam Campaign at DESY (2010)



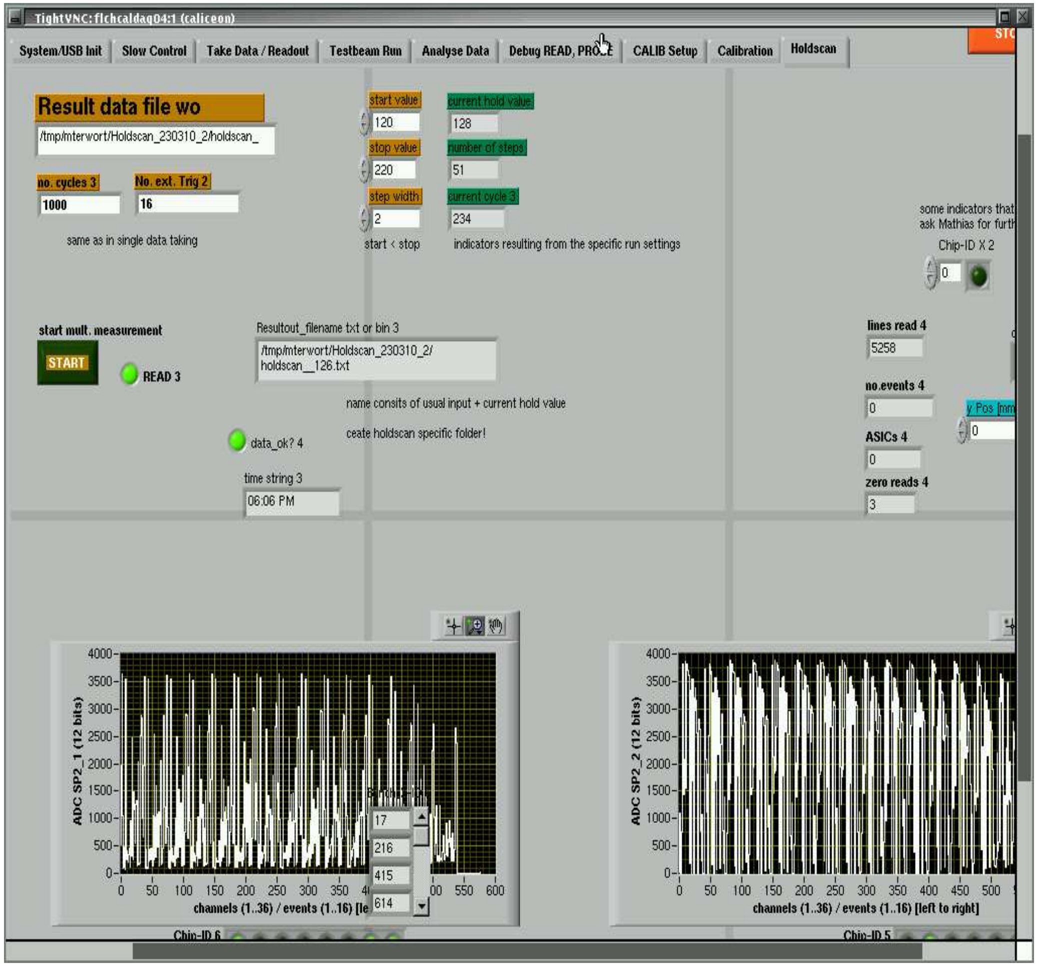


# Data Acquisition Chain




- All system running under Linux (SL5)
- DAQ performed through VNC connections

# DAQ and Online Monitoring




- **LabView Based**
  - $\Longrightarrow$ **Temporary solution until official CALICE DAQ is ready**
  - $\Longrightarrow$ **Readout speed dominated by serial2USB interface in DIF (forseen for debugging)**

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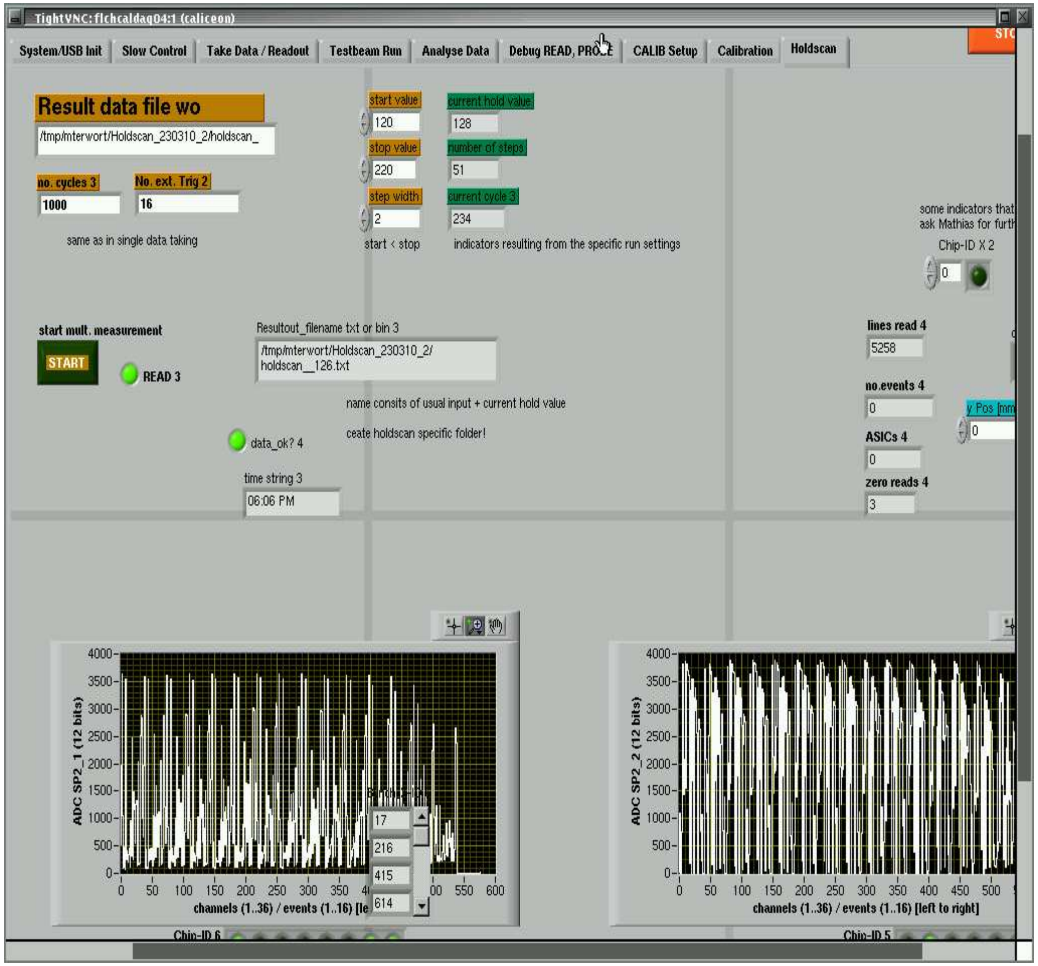
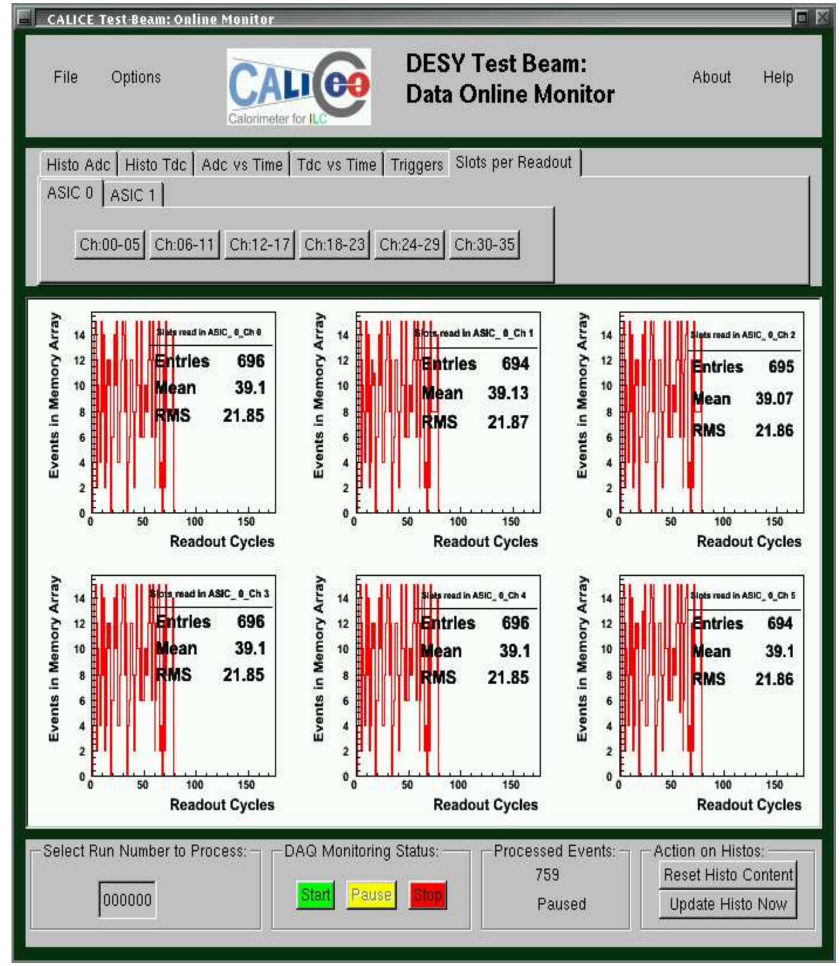



- **LabView Based**
  - $\Longrightarrow$ **Temporary solution until official CALICE DAQ is ready**
  - $\Longrightarrow$ **Readout speed dominated by serial2USB interface in DIF (forseen for debugging)**

- **Written from scratch to fit current test-beam data scructure**
  - $\Longrightarrow$ **Scalable with nr. of SPIROCs**

# DAQ Operational Modes

Three major trigger modes forseen

- External Trigger (start of Spill sequence) to validate events
  - $\Longrightarrow$ generates gate to accept trigger events
  - $\Longrightarrow$ mode for commissioning setup in test-beam
- ASIC in auto-trigger mode
  - $\Longrightarrow$ every event above $1/2$ MIP is collected
    - — SPIROC read out when all $16$ memory slots are filled
  - $\Longrightarrow$ Scheme to test ILC mode
- Internal trigger to validate events
  - $\Longrightarrow$ Calibration mode (as for LED-induced single-pixel spectra )

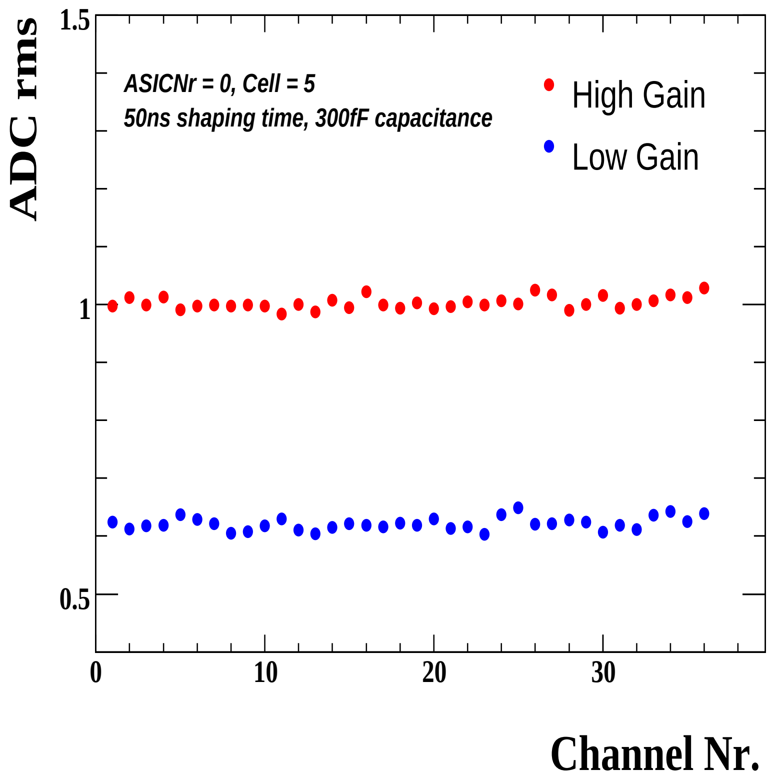
<u>In the following, preliminary results in calibration</u>

<u>mode and with external trigger are presented</u>

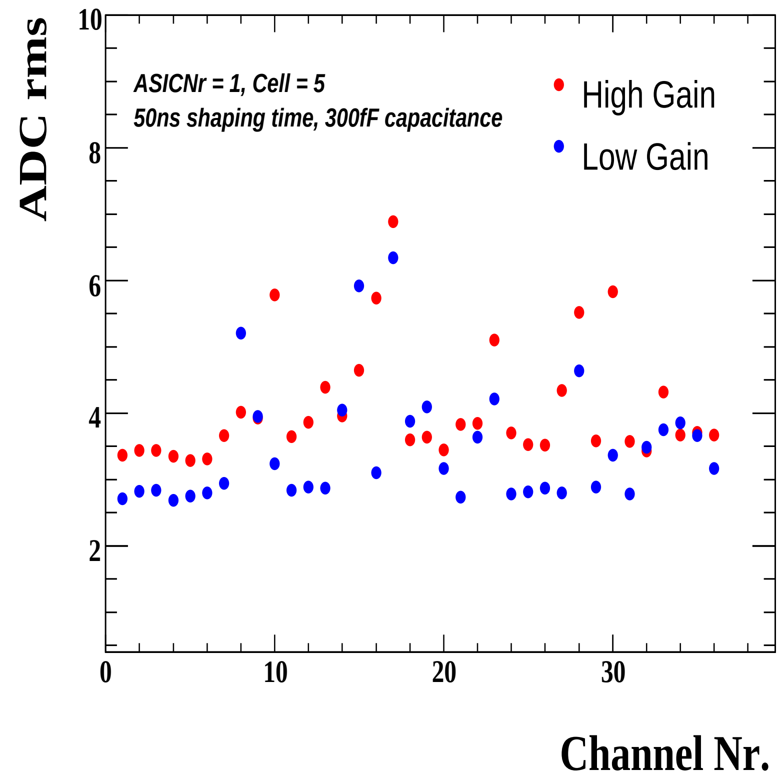
# Commissioning: Preliminary Results

## Noise Measurements

**Need also to check uniformity between channels**




**2 ADC = 0.68 mV**



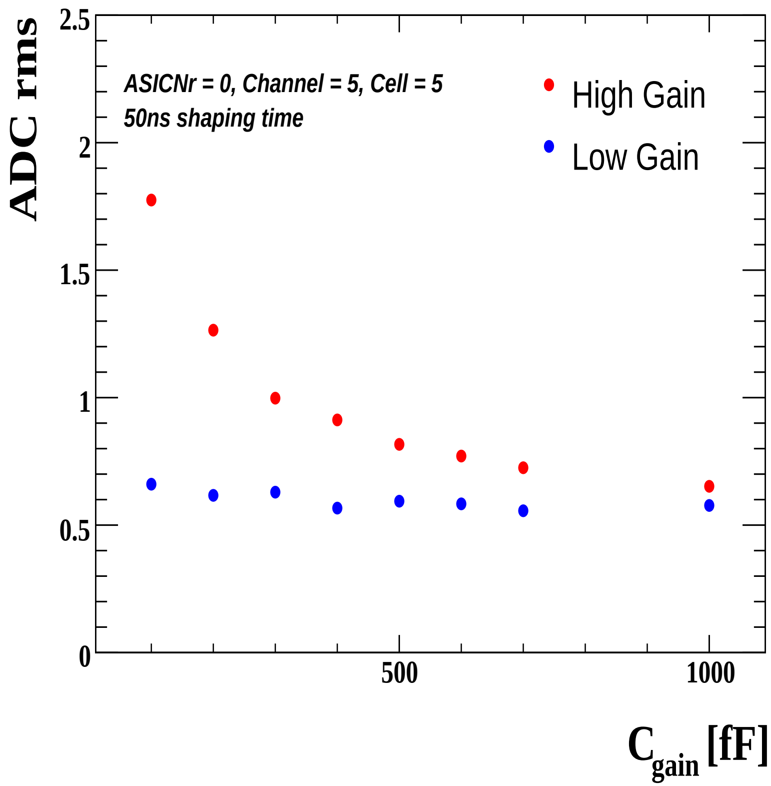

- **Overall characteristic is fine, but much higher noise on ASIC 1**
- **To be done:** **mV conversion to charge (from datasheet: $4 \cdot 10^5 e \approx 26$ ADC)**

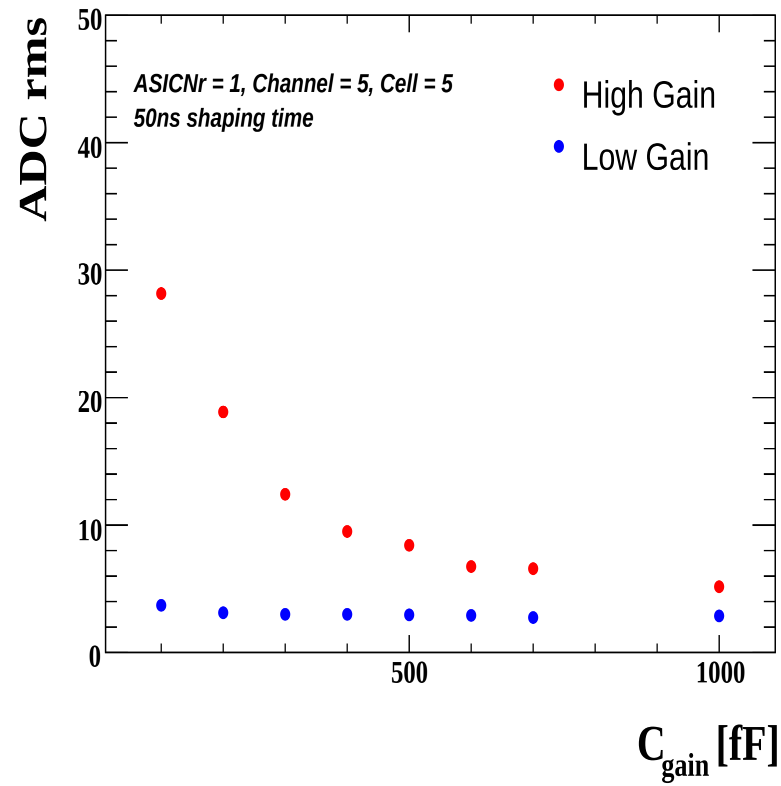
  **Understand ASIC 1 high-noise**

# Commissioning: Preliminary Results

## Noise Measurements

### Dependence on the ASIC gain (feedback capacitance)

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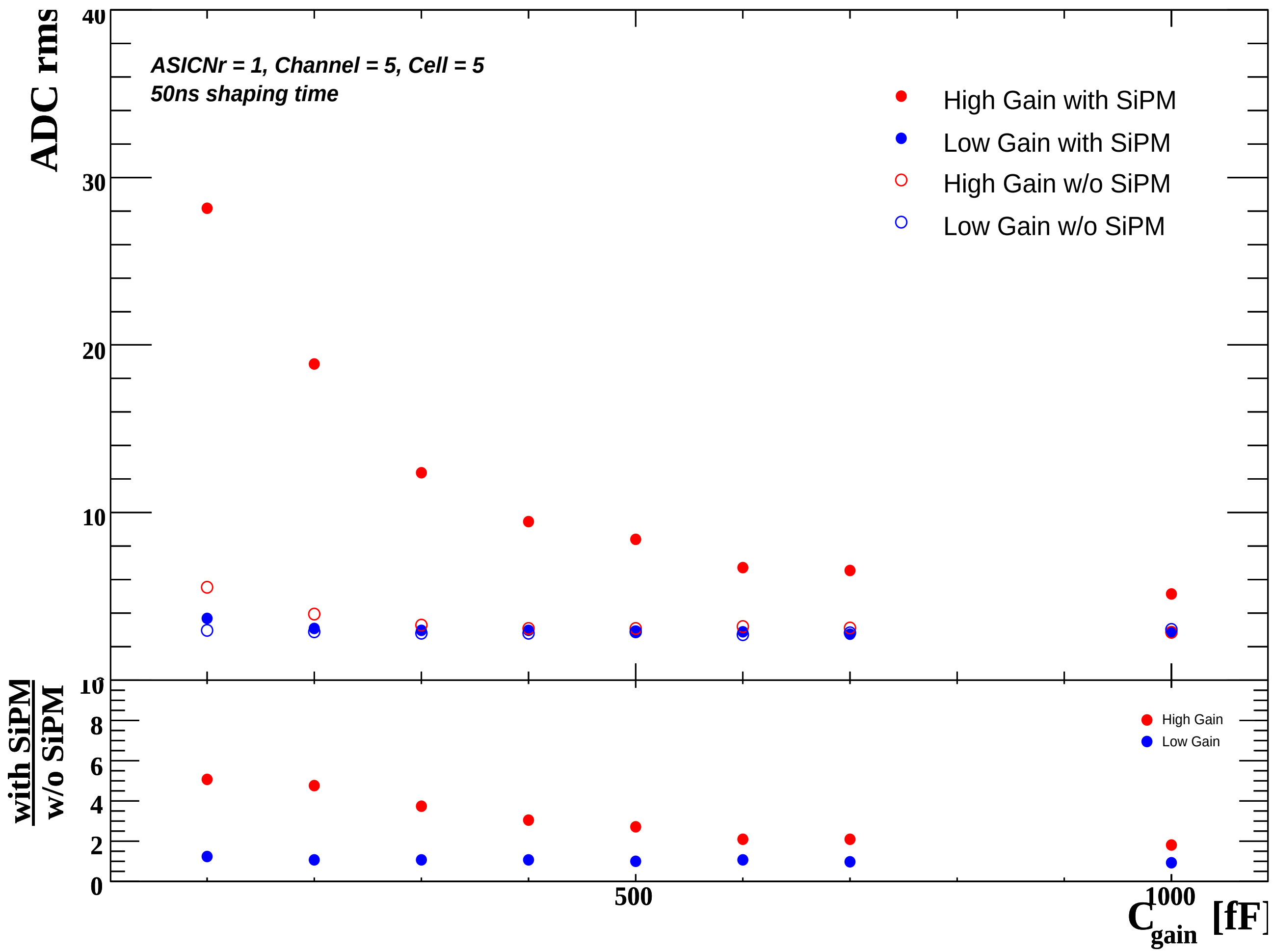
# Commissioning: Preliminary Results

## Noise Measurements

### Noise with and without SiPM switched on

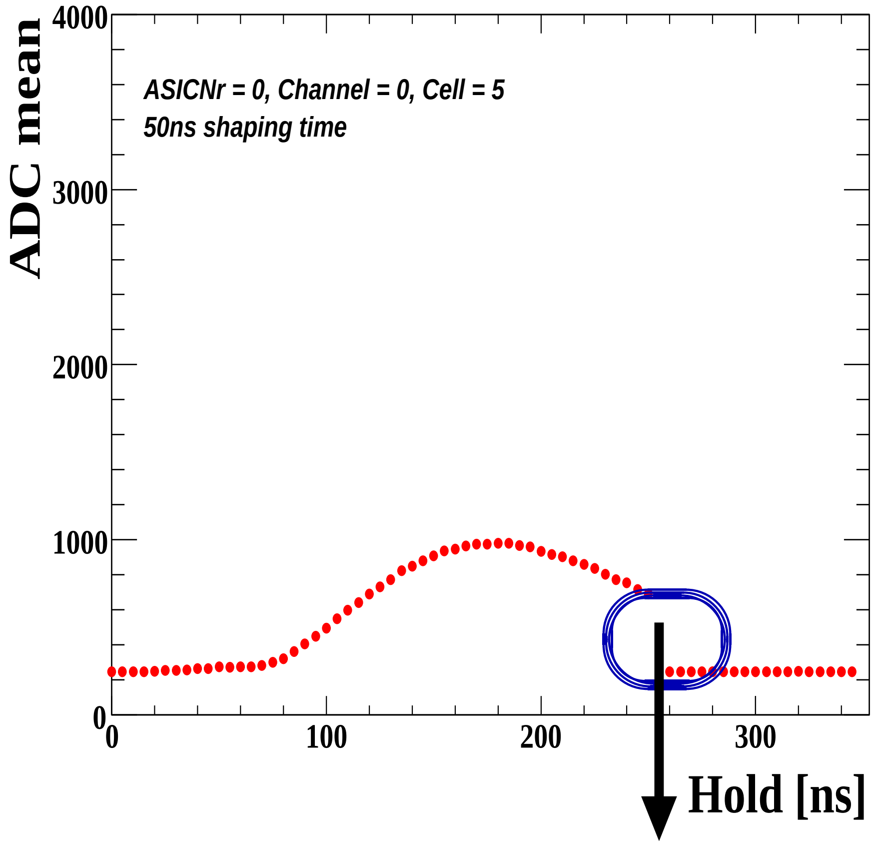



- Noise is SiPM dominated

# Commissioning: Preliminary Results

## Determination of the peaking time

**Using LED light (with MIPs on-going)**




**Due to setting hard-coded in FPGA**

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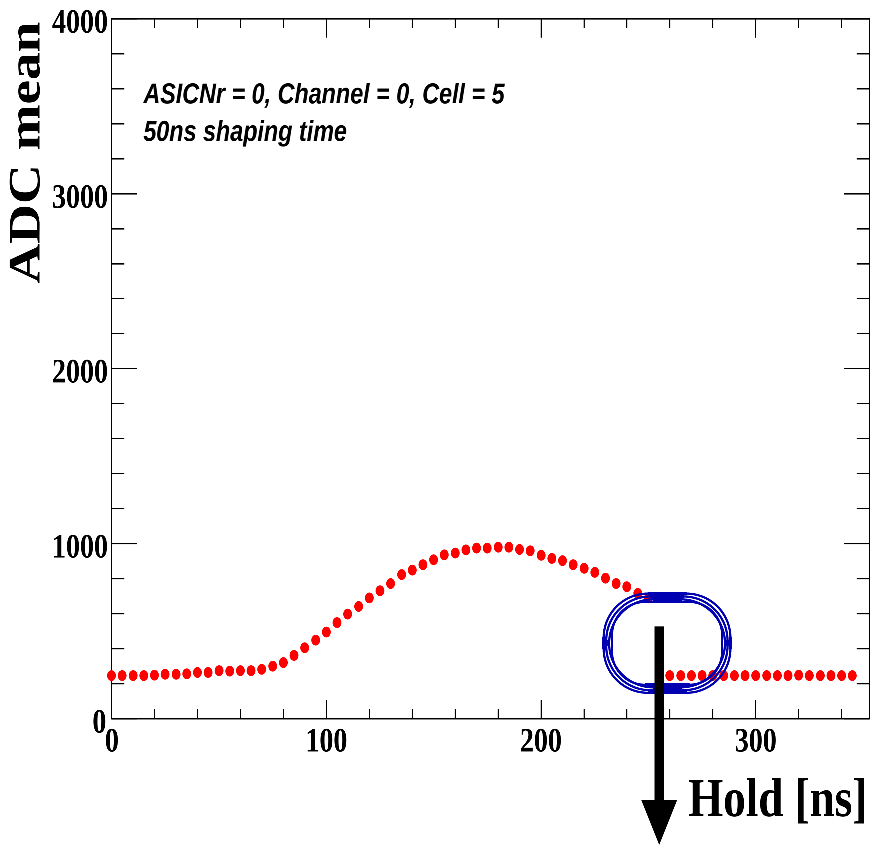
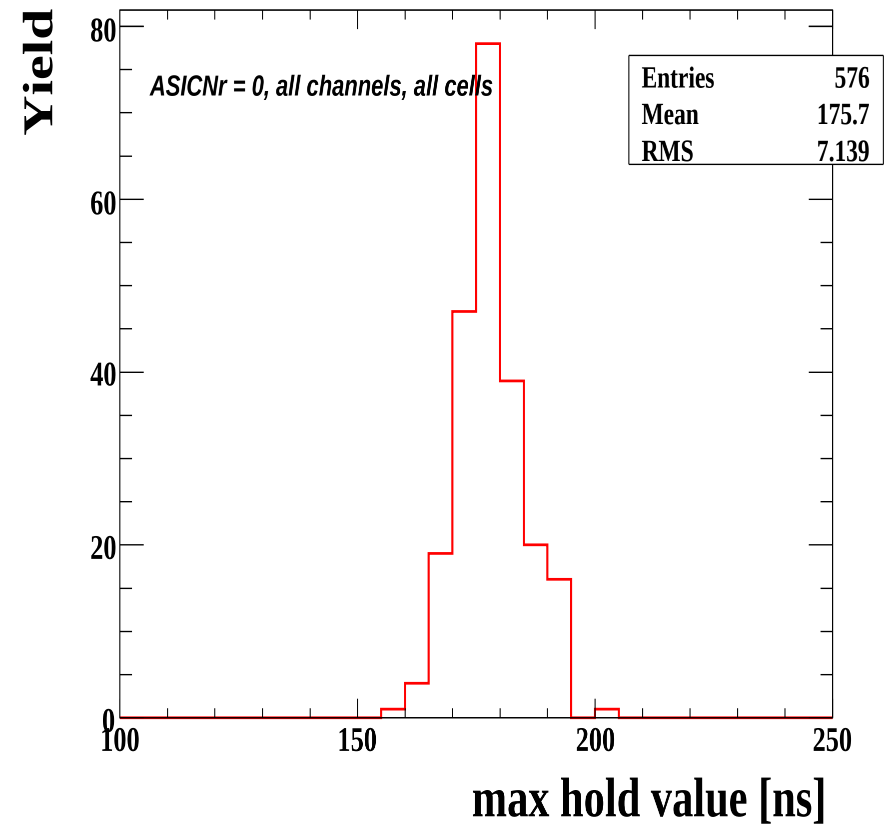


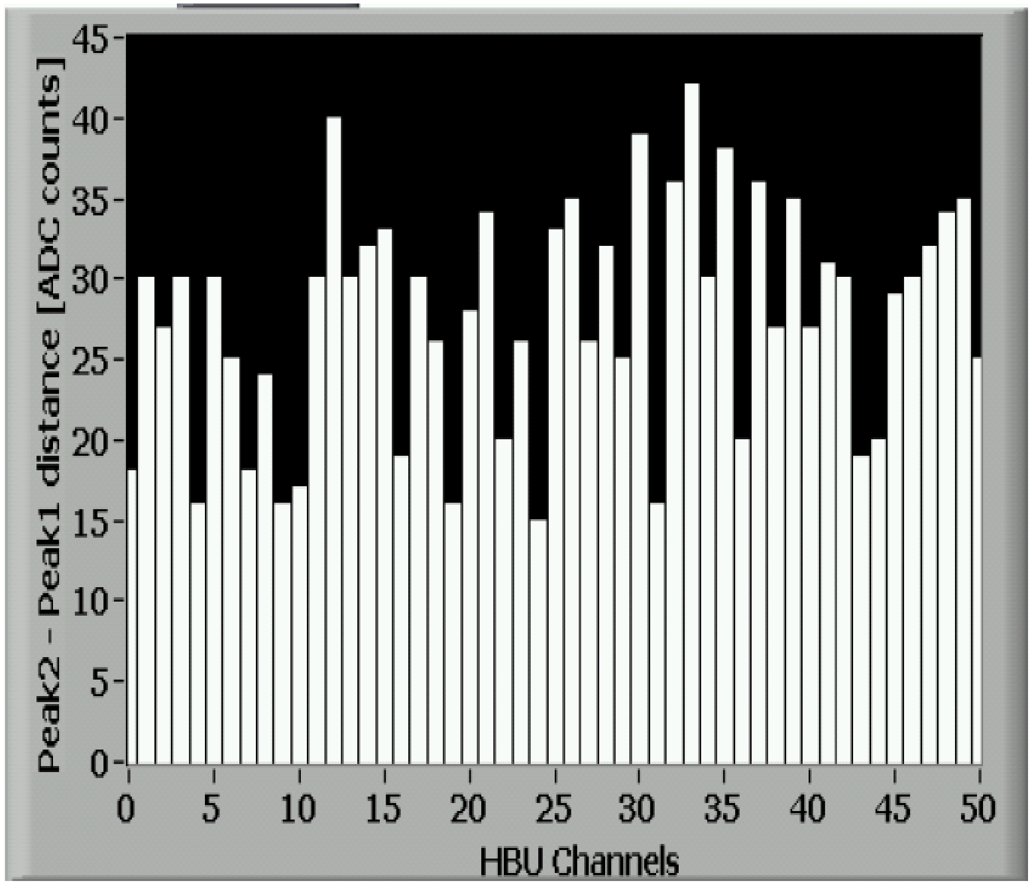




**Due to setting hard-coded in FPGA**

- **Uniformity appears reasonable (scan performed with coarse $5$ ns steps)**

# Commissioning: Preliminary Results

## Gain Measurement for $51$ channels: in lab. test-bench

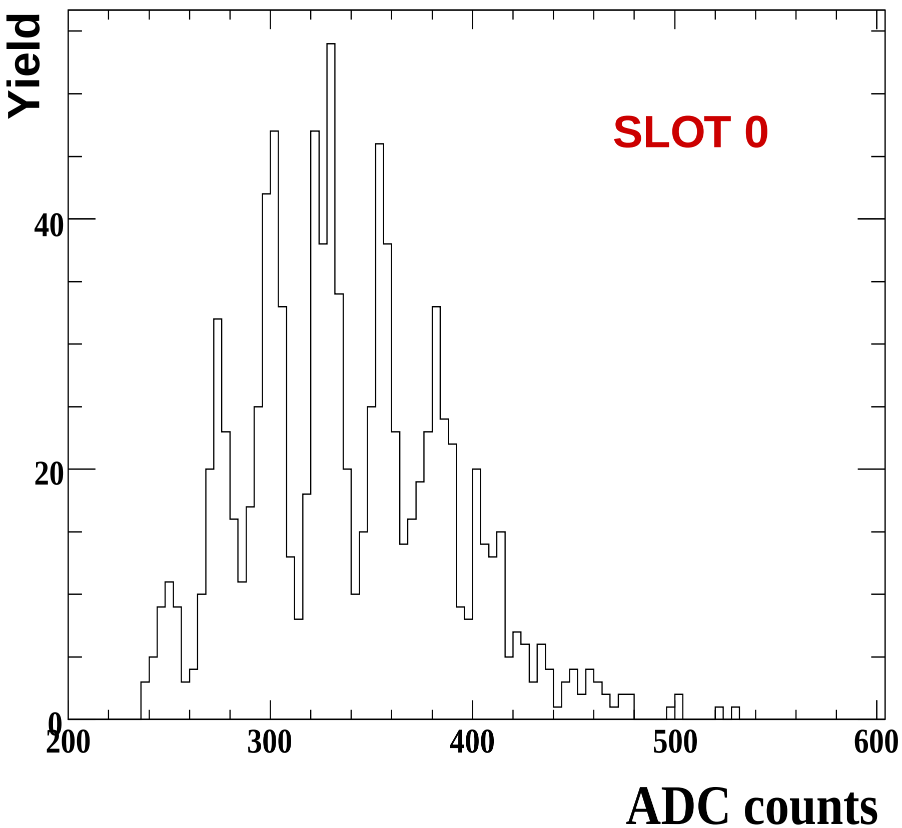


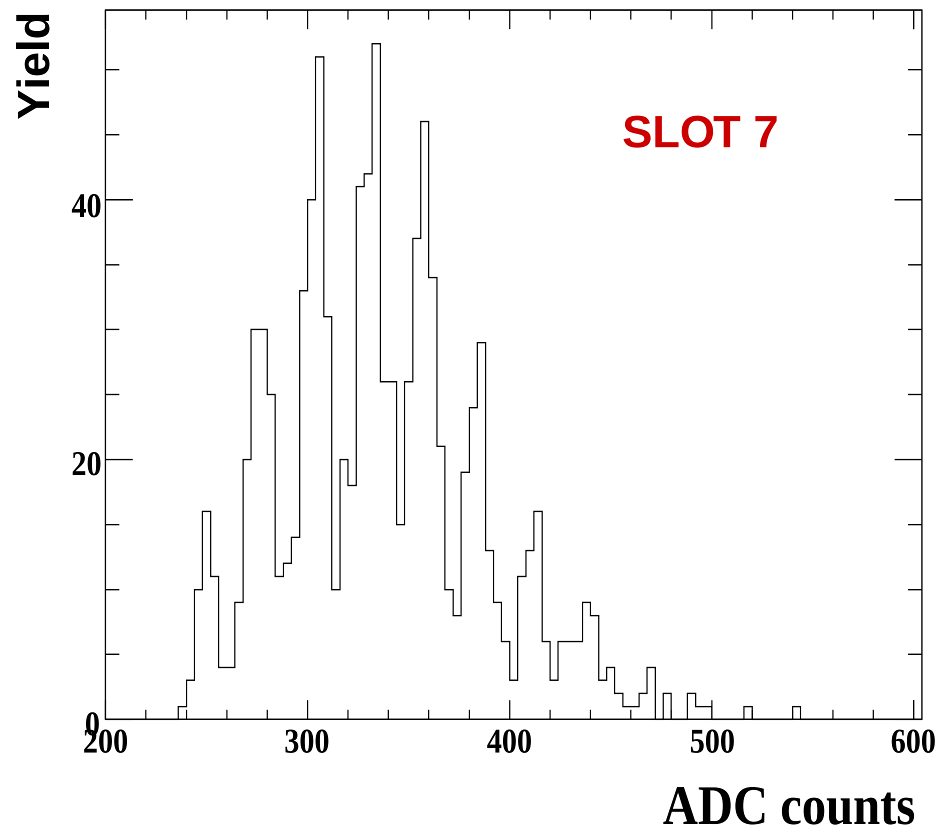

- **Large spread in gain $\Longrightarrow$ consistent with ITEP datasheet on SiPMs**

# Commissioning: Preliminary Results

## Single Pixel Spectra

### Using LED light for Gain determination




**ASIC 0; Channel 11**

- **More statistics planned for a stable and precise multi-gaussian fit**

# Redesigns and Planned Replacements

- HBU to be redisigned according to size of tiles arriving from ITEP

  $\Longrightarrow$ tiles better shaped; no more size mismatch

  $\Longrightarrow$ will host 4 SPIROC2 (new subversion from LAL)

  $\longrightarrow$ See De La Taille's presentation at this Workshop

  $\Longrightarrow$ new LED system (optimized by Wuppertal Group)

- CIB redesigned according to 'agreed/fixed' board dimensions

- Goal to have an entire slab readout to commission

  $\Longrightarrow$ Eventually, within the EUDET project, a detector layer with about 2200 channels will be realized to investigate e.g.

  — Electronic signal transport and integrity over full length of readout lines

  — Calorimeter signal uniformity over the full area

**A lot of work ahead!!**

# Summary and Outlook

- Technological prototypes for the AHCAL in full operation
  - $\Longrightarrow$ two HBU setups ready
  - $\Longrightarrow$ one setup already in test-beam area at DESY for commissioning
  - $\Longrightarrow$ Labview-based DAQ used; waiting for the official CALICE DAQ
  - $\Longrightarrow$ software for monitoring data-taking developed
  - $\Longrightarrow$ preliminary results presented

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  - $\Longrightarrow$ Labview-based DAQ used; waiting for the official CALICE DAQ
  - $\Longrightarrow$ software for monitoring data-taking developed
  - $\Longrightarrow$ preliminary results presented
- Power-cycling should be tested
- Redesigning on-going
  - $\Longrightarrow$ implement new LED system
  - $\Longrightarrow$ stick to finalized/approved dimensions
- Modification/improvement of DAQ/Monitoring software according to needs of the test-beam campaign

**More to come from the AHCAL; stay tuned!**

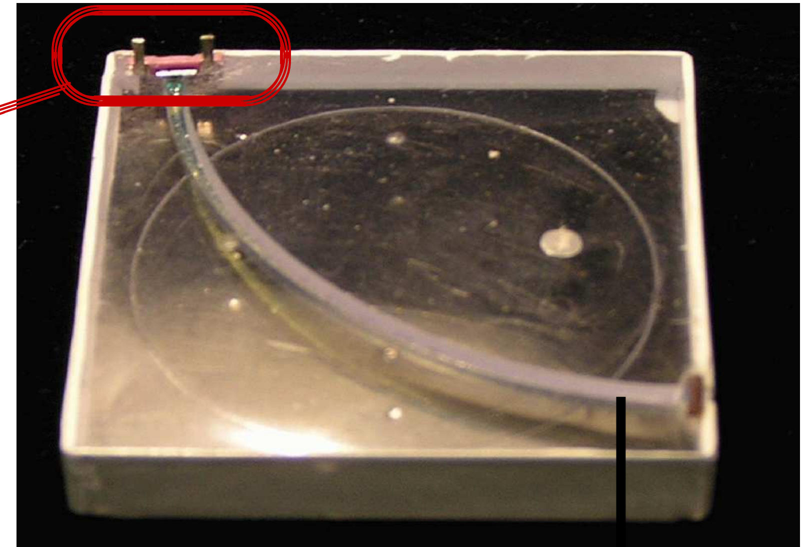
# Back Slides

# SiPM/Scintillator Characteristics

**SiPM: novel multi-pixel photo-multiplier**

**operated in Geiger mode**

$\Longrightarrow$ $B$**-field proof, small**



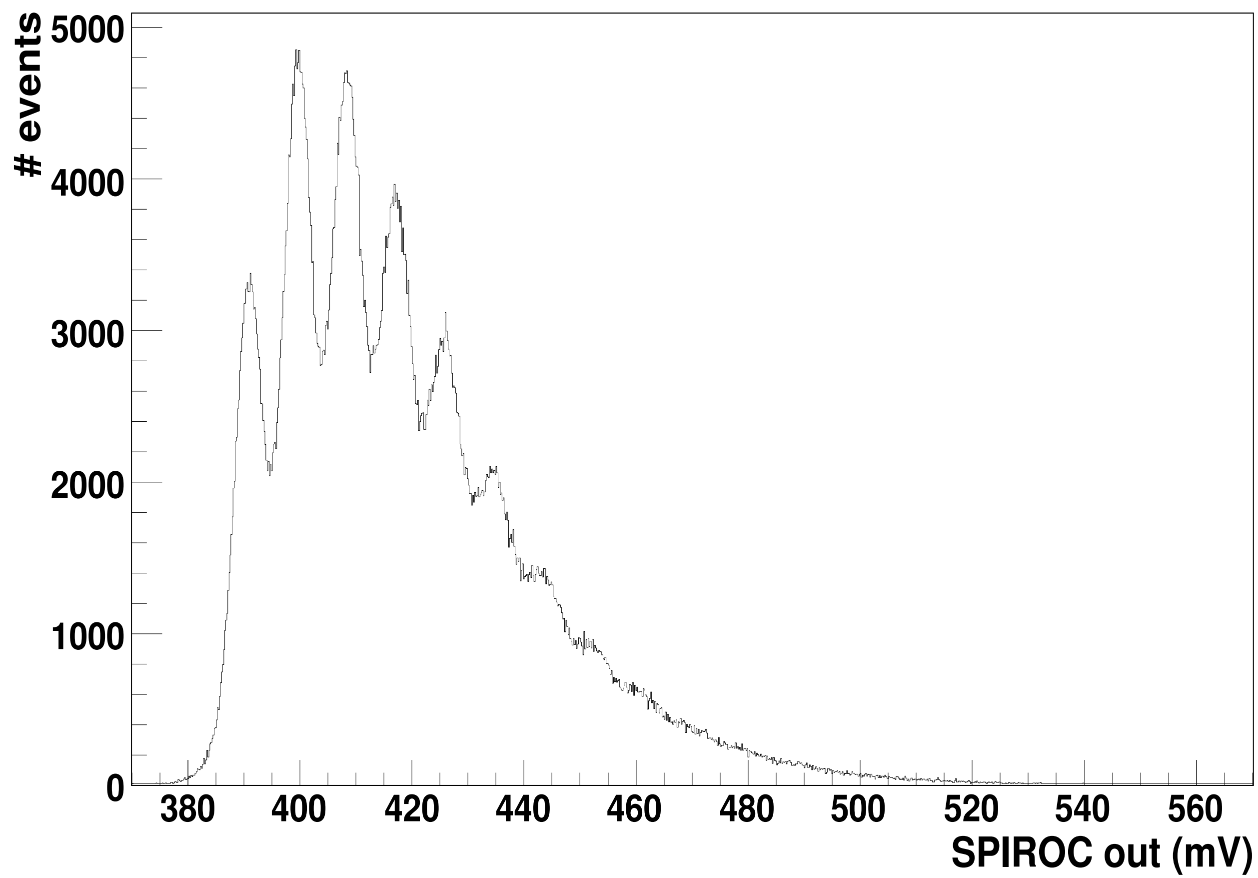
**Optimization of scintillator size to $3x3$ cm$^2$**

$\Longrightarrow$ **confirmed by Monte Carlo simulation**

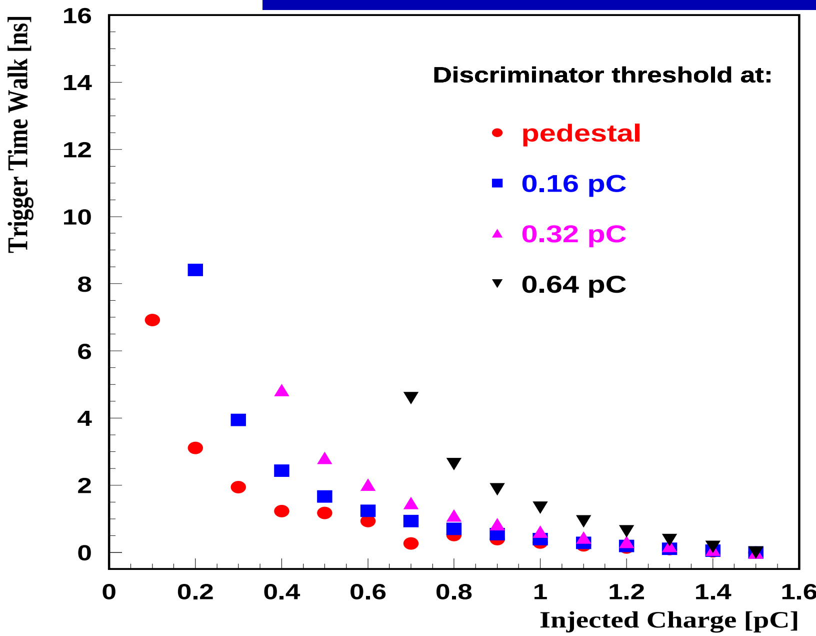
***Wavelength shifter***

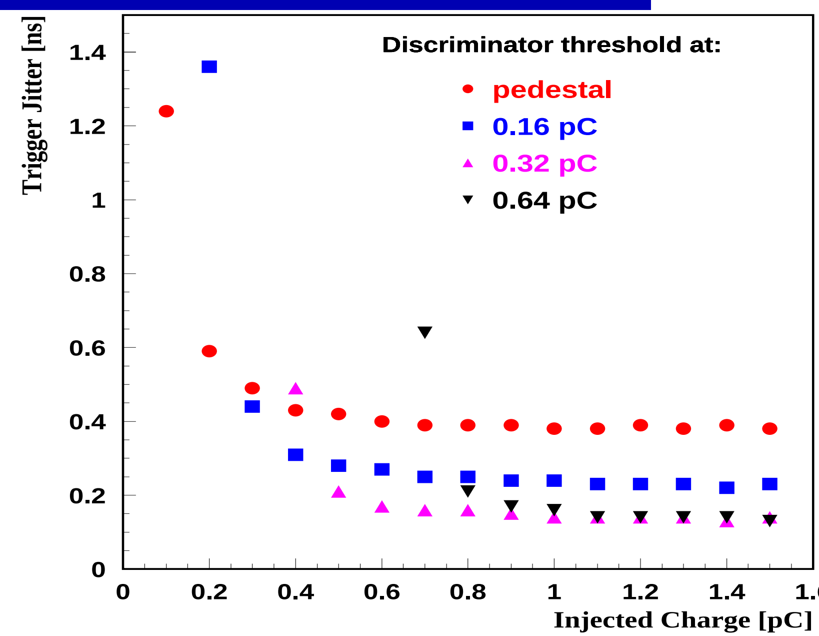
# SiPM: Single-peak spectrum with External Trigger

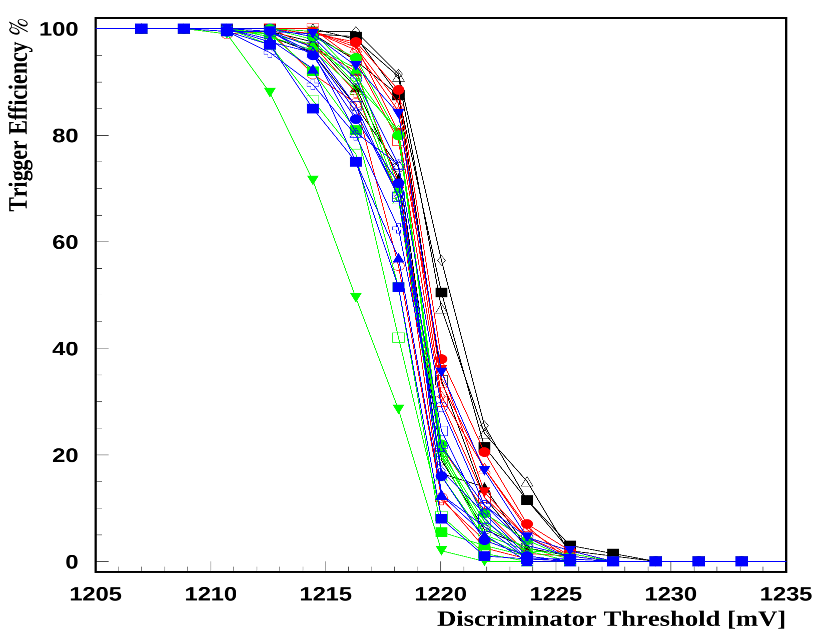
- Measurement done during SPIROC2 commissioning in Lab.; using SiPM Nr. 753
- SPIROC operated in HG mode with $100fF$ variable capacitance and $25ns$ shaping time
- External hold (from pulse generator)

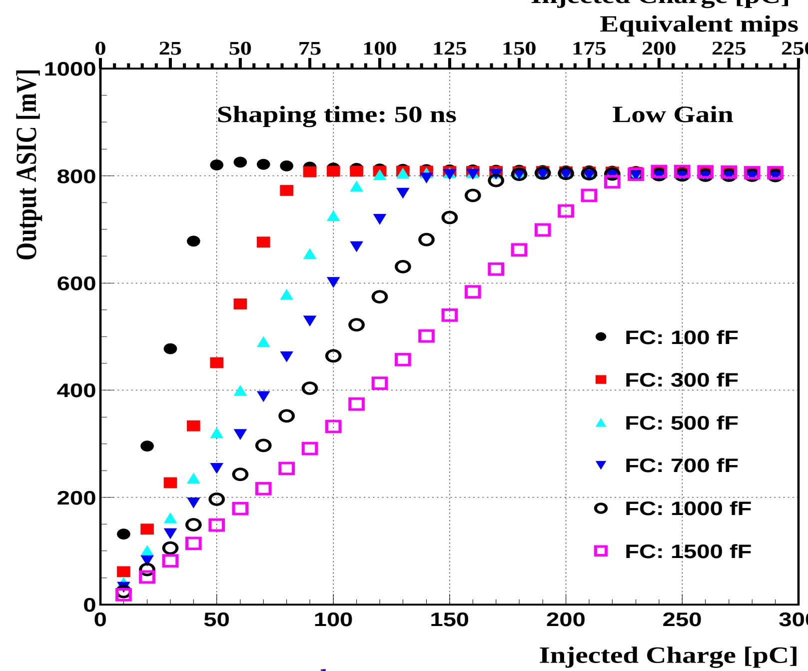


# SPIROC 2 Commissioning (2009)

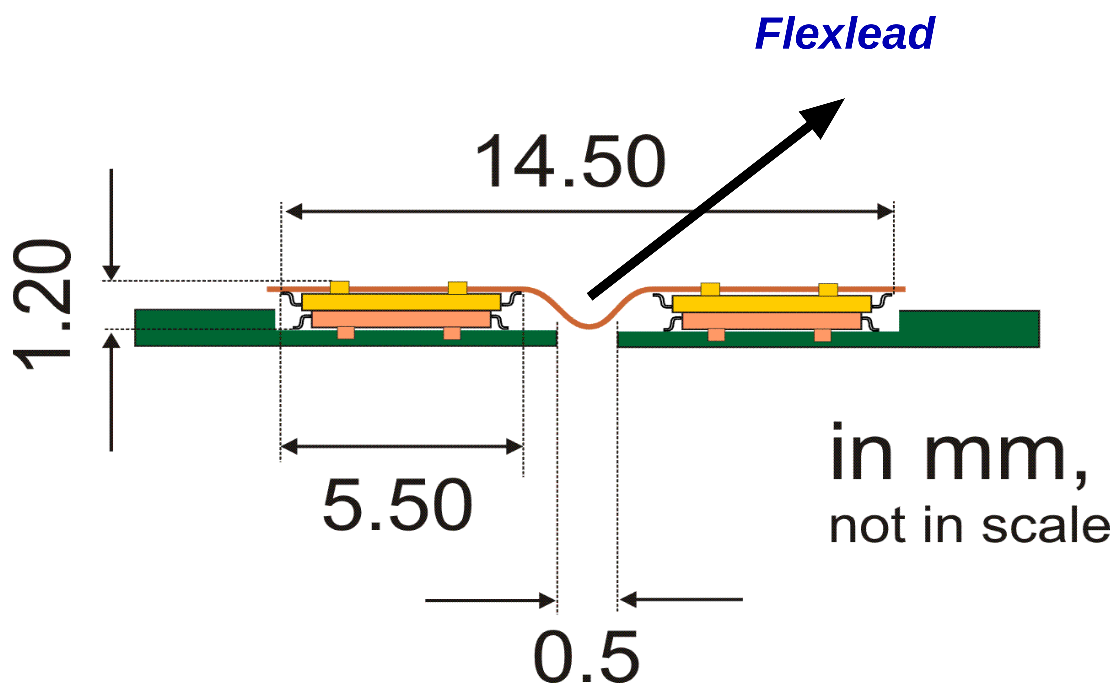


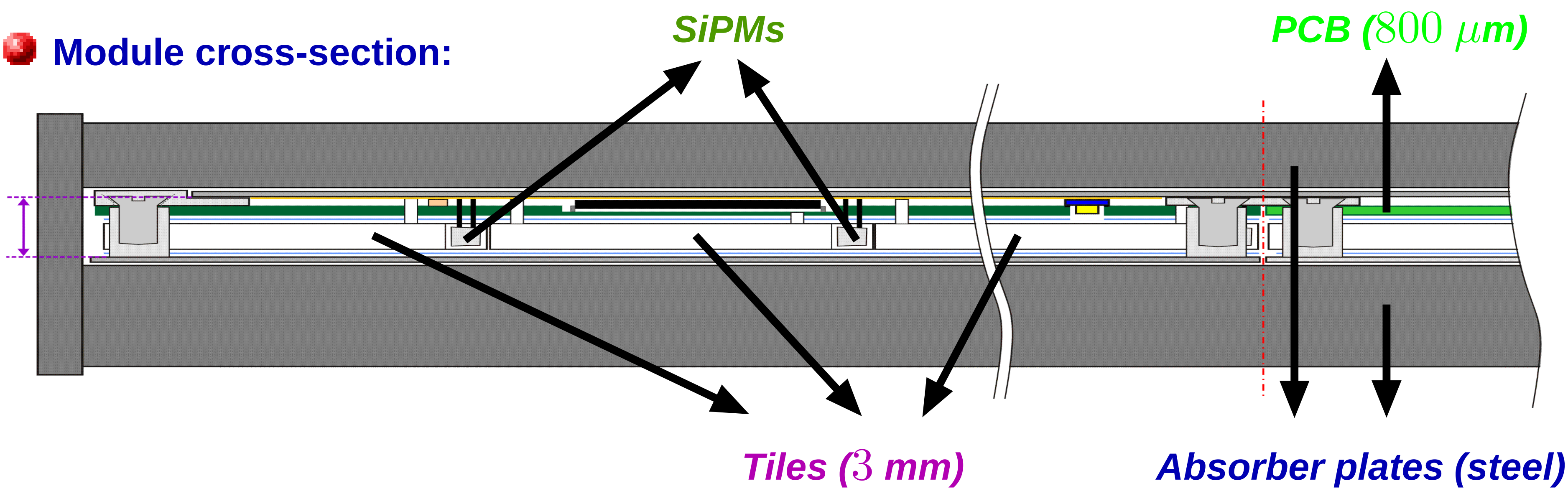
# HBU-HBU Interconnection




- **Flexlead:**
  - **rigid at connector ($80$ pins) sides**
  - **flexible in between HBUs**
  - **bended flexlead allows HBU-HBU displacement of $\pm100\mu$m**

# Subcomponents: HBU (HCAL Base Unit)

- **Module cross-section:**



# Subcomponents: HBU (HCAL Base Unit)

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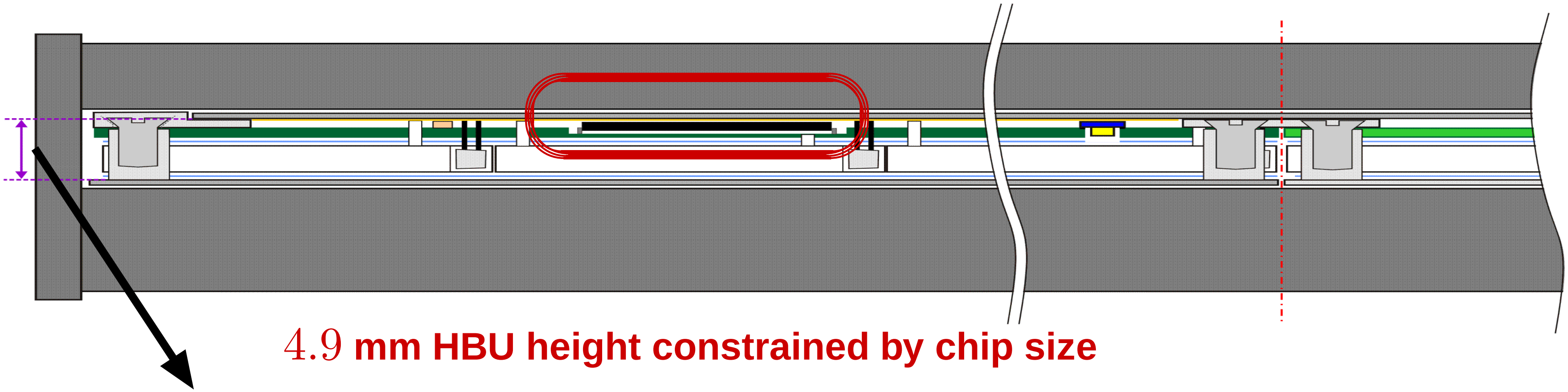


$4.9$ mm HBU height constrained by chip size

$\Longrightarrow$ reduction obtained using SPIROC2 (with height $1.4$ mm)

(SPIROC2 here shown with $1$ mm; SPIROC1 = $4.3$ mm)

- **Power dissipation: cooling system not forseen**

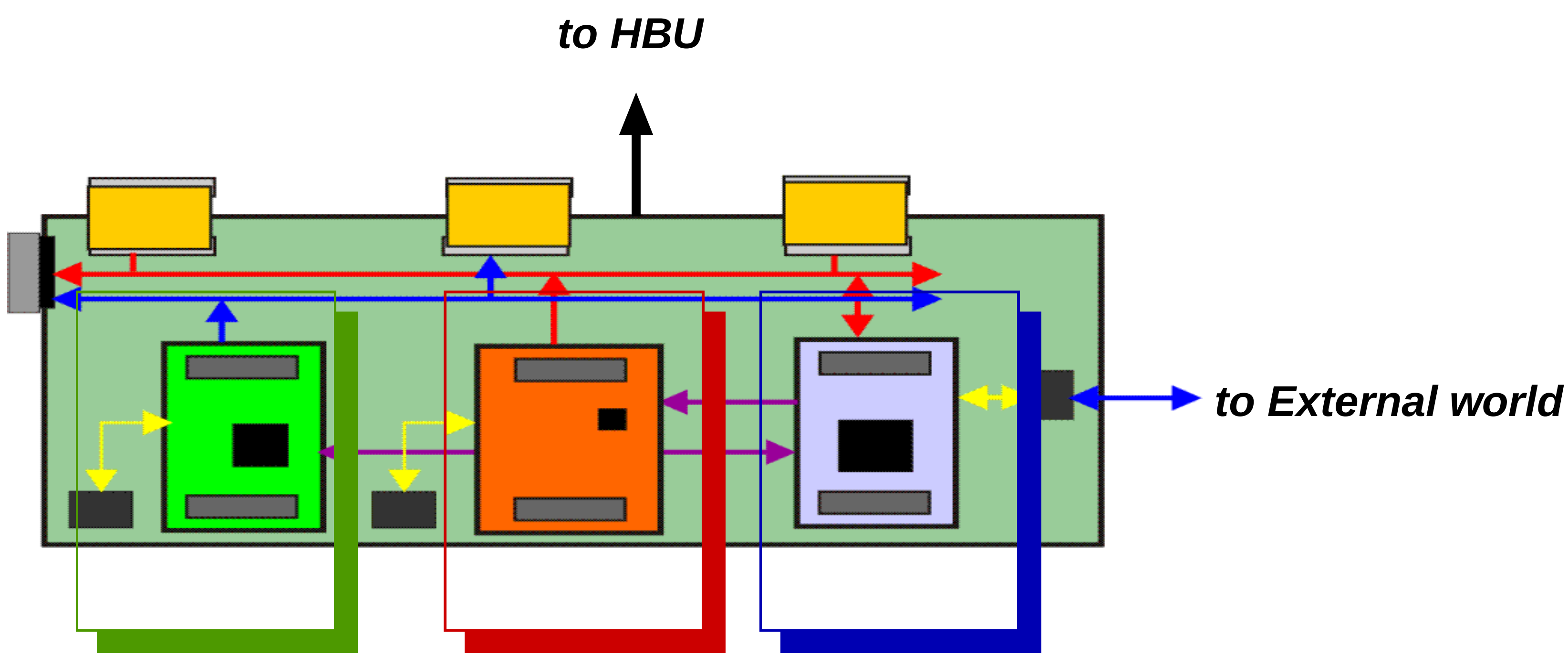
*per channel*:

— SiPM: $15\mu$W (always on) — SPIROC: $25\mu$W — calibration electronics: $23\mu$W

$\Longrightarrow$ effective dissipation sizably reduced keeping SPIROC/calib. electronics off between two ILC train crossing (on during $1\%$ of ILC duty time)

✔ even more, considering calibrations done realistically only every few minutes

# Subcomponents: CIB (Central Interface Board)




*POWER module*

— Provides $+3.5$, $+5$ V, bias voltages & ground to HBUs (and SiPMs therein)

*CALIB(ration) module*

— Drives/regulates calibration electronics (LED + charge injection) inside HBUs

*DIF module*

— External world $\leftrightarrow$ HBU interface

— Readout/control of ASICs

- Differently from HBU case, here cooling is forseen (it is located outside detector)