IN2P3

Omega

2nd generation ASICs

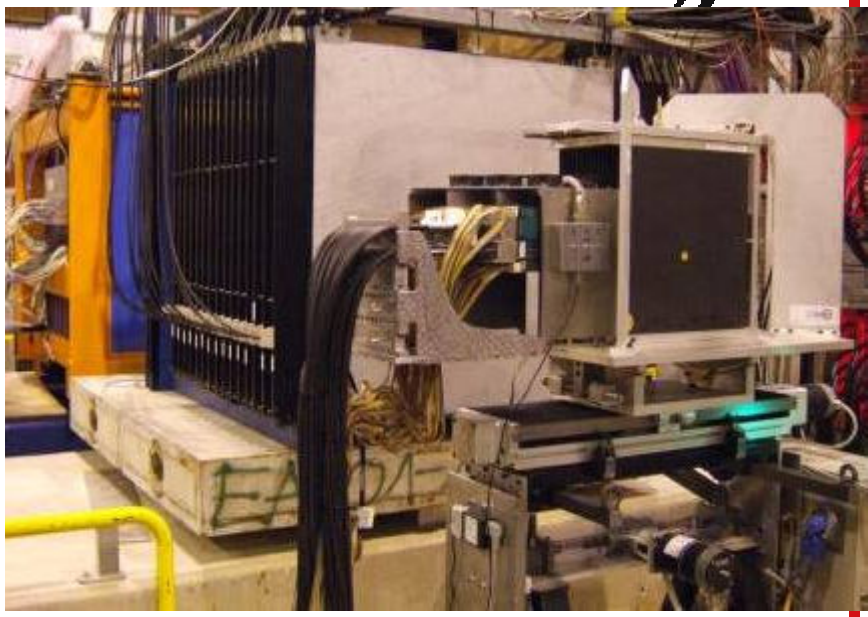
for CALICE/EUDET

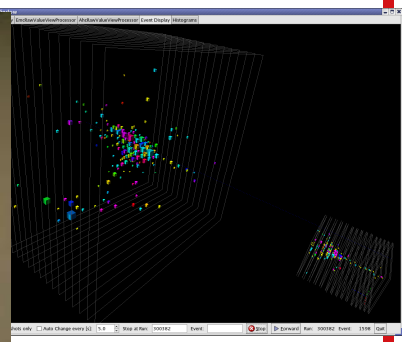
LA TAILLE

Orsay MicroElectronic Group Associated

CALICE physics prototypes

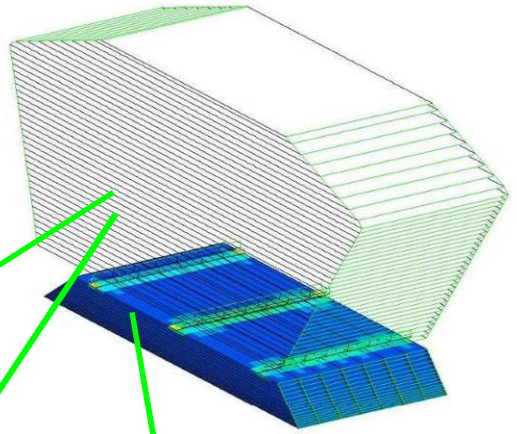
- 1 m^3 **prototype for physics** tests
  - Goal : study particle flow algorithm and validate Geant 4
- SiW ECAL
  - 9 600 readout channels since 2004
  - FLC_PHY3 chip [LAL] 18ch analog
- 1 m^3 Analog HCAL : tiles + SiPM
  - 8400 channels since 2005
  - FLC_SiPM chip [LAL]
- 1 m3 Digital HCAL : RPCs
  - 400 000 readout channels
  - DCAL chip [FNAL], 64ch 0.25µm
  - In fabrication, see talks by J. Repond and H. Weerts
  - Alternative R&D with GEMs & µMegas : see talks by A. White and M. Chefdeville



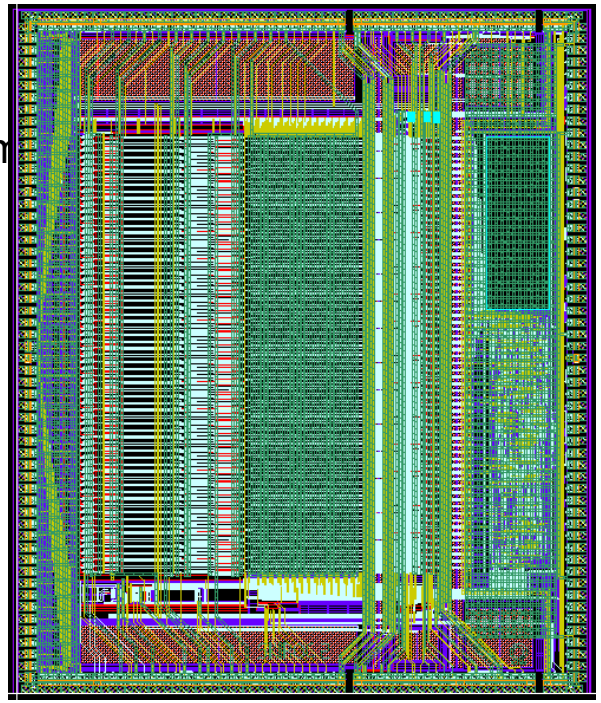


Second generation ASICs

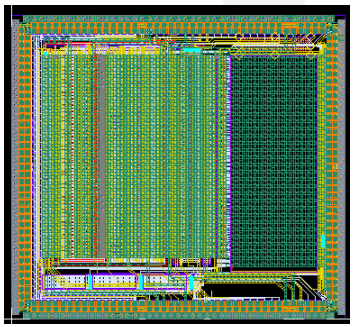
- Add auto-trigger, analog storage, digitization and token-ring readout !!!
- Include power pulsing : <1 % duty cycle
- Address integration issues asap
- Optimize commonalities within CALICE (readout, DAQ…)



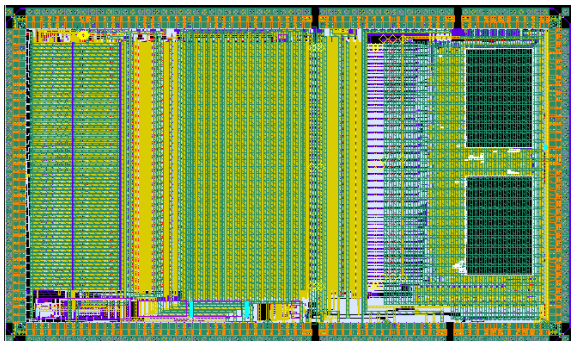
SKIROC2
ECAL Si
64 ch. 70 mm



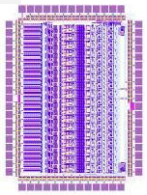
HARDROC2
SDHCAL RPC
64 ch 16 mm²



SPIROC2
AHCAL SiPM
36 ch 30 mm²

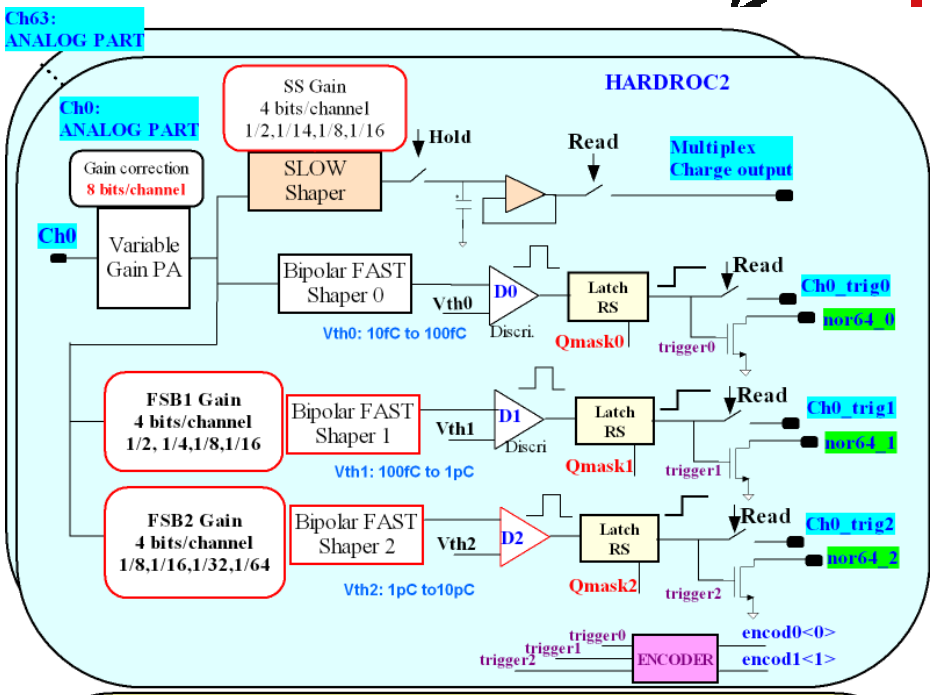


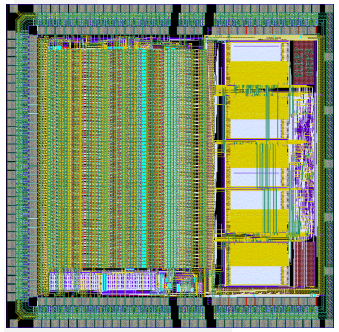
FLC_PHY3 (2003)

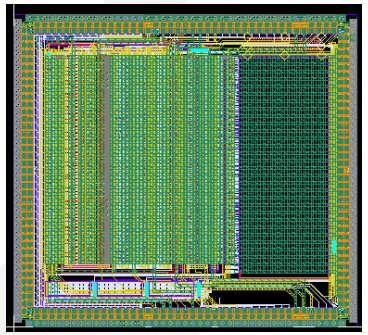


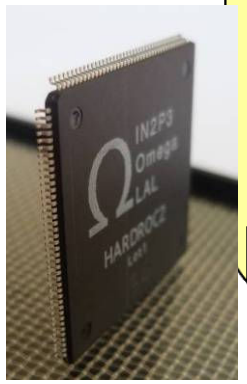
HARDROC: HAdronic Rpc Digital ReadOut Chip

- Variable gain (6bits) current preamps (50Ω input)
- Auto-trigger on ½ MIP
- Store all channels and BCID for every hit. Depth = 128 bits
- Data format : 128(depth)*[2bit*64ch+24bit(BCID)+ 8bit(Header)] = 20kbits
- Power dissipation : 1.5 mW/ch (unpulsed)-> 7 µW with 0.5% cycle
- Large flexibility : >500 slow control settings
- SiGe 0.35µm sept 06 and june 08

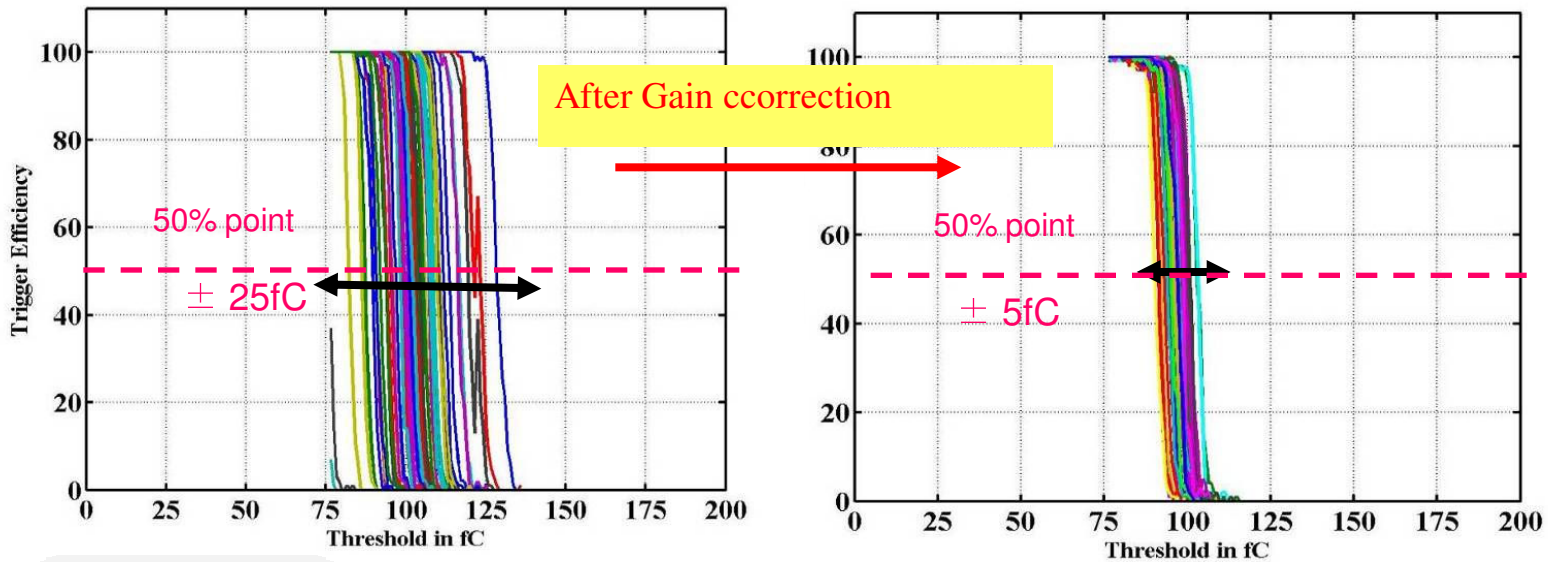


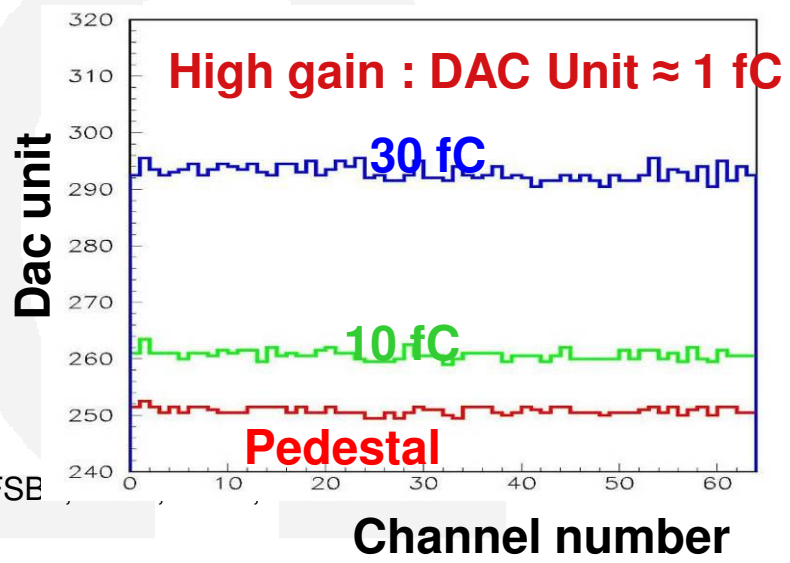


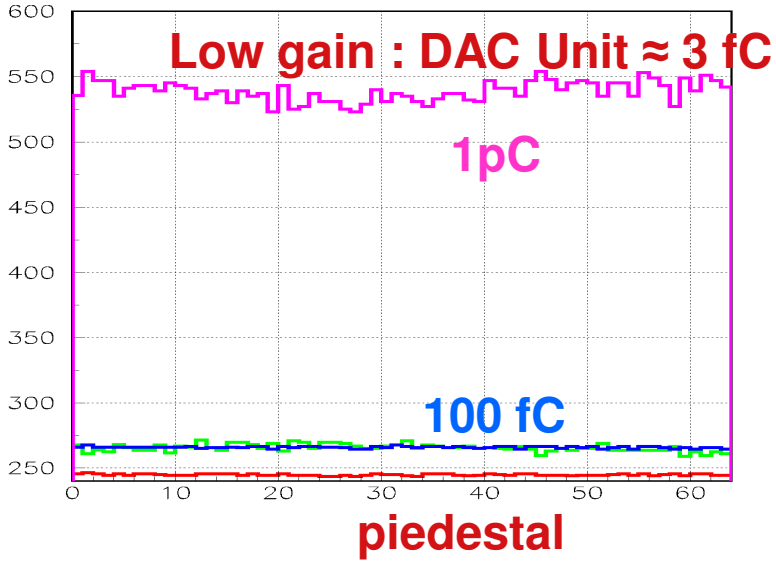




Trigger efficiency measurements

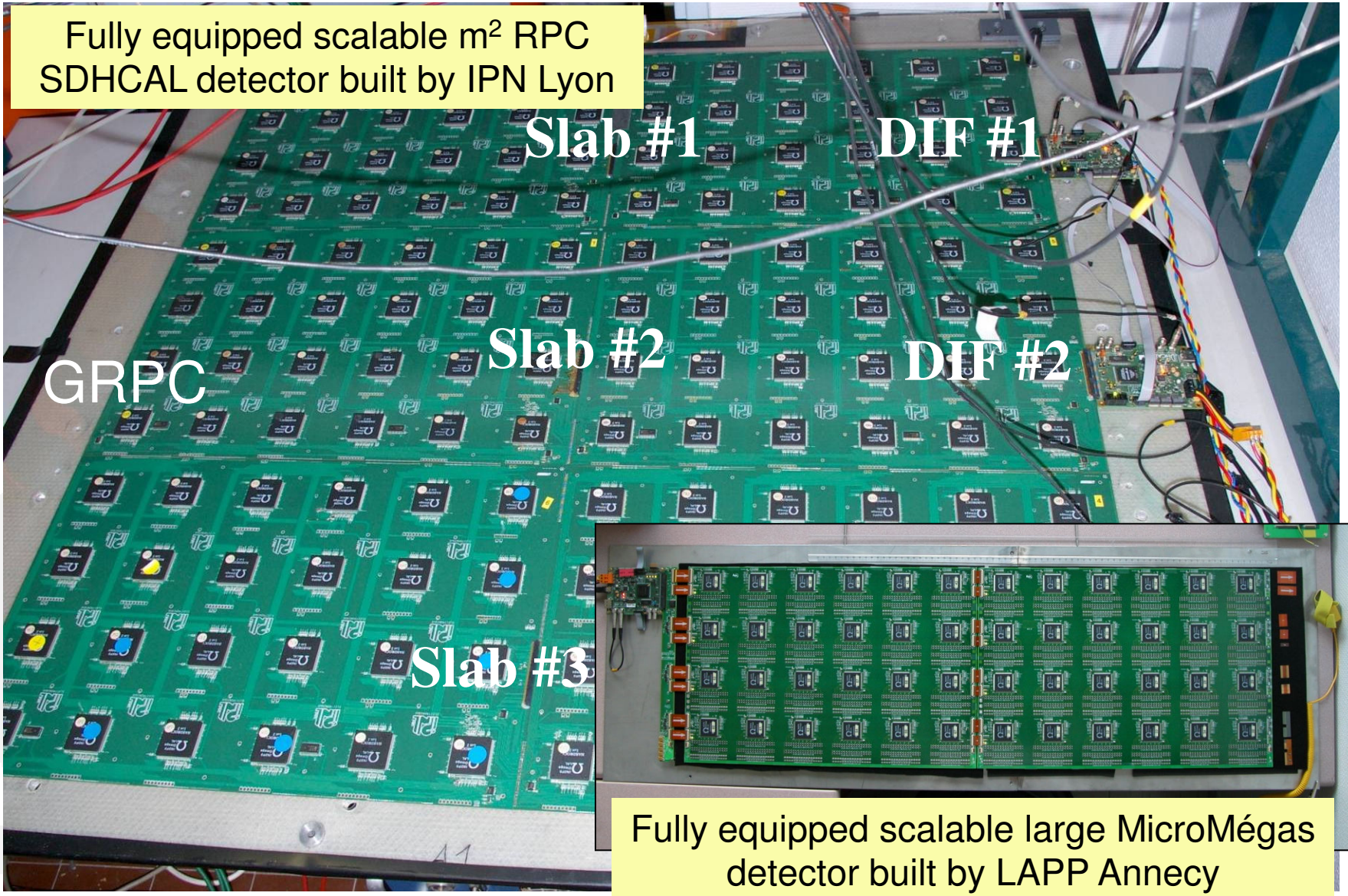






TOWARDS A TECHNOLOGICAL PROTOTYPE

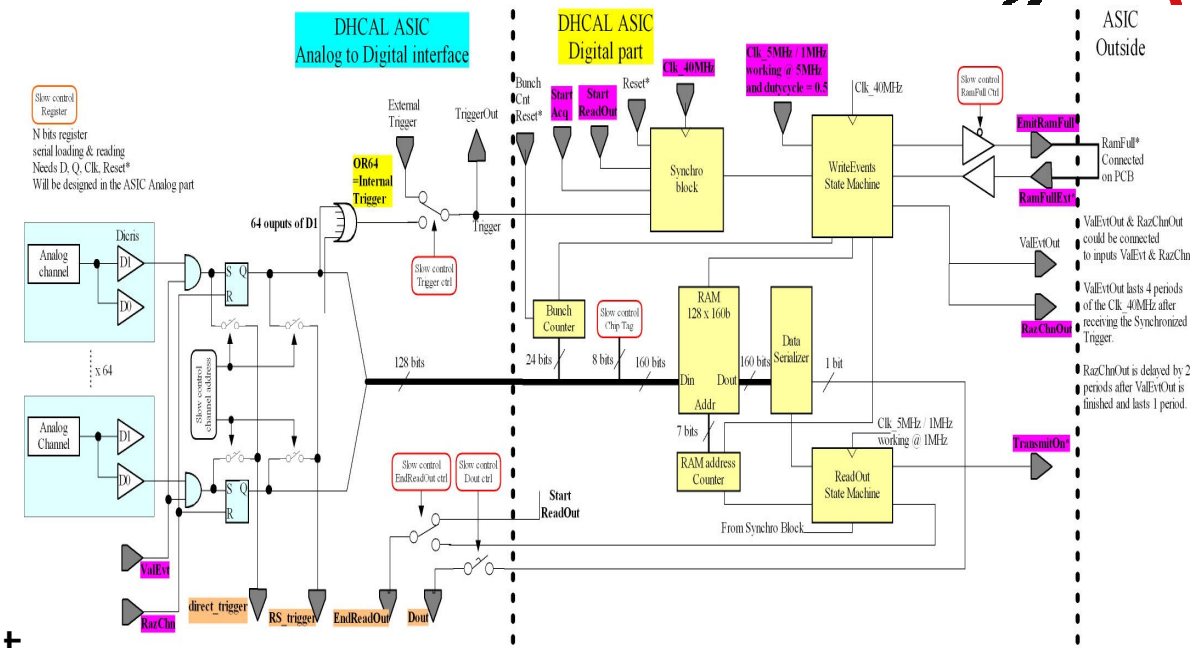
Fully equipped scalable m² RPC
SDHCAL detector built by IPN Lyon

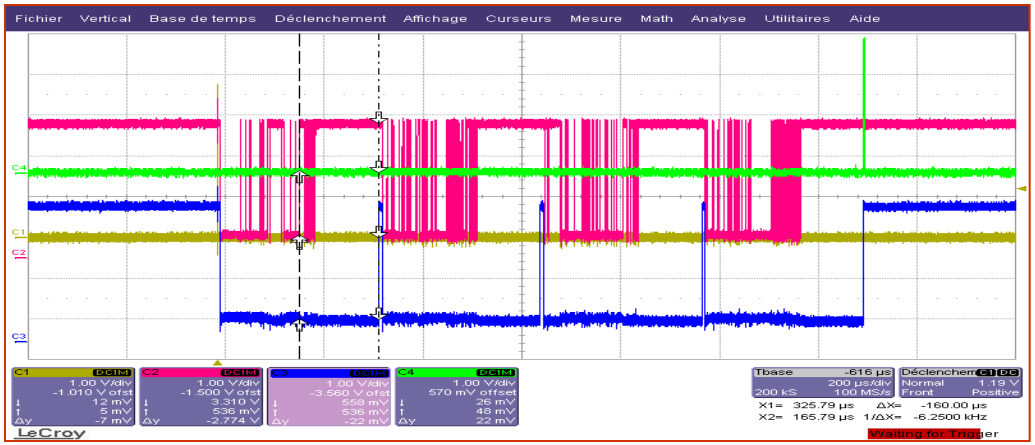


Fully equipped scalable large MicroMégas
detector built by LAPP Annecy

Digital data path

- Low power token ring transmission
- Open collector bus, scalable to several meters. 1 V swing.
- Redundant data lines
- Clock power management incorporated in chip
- **Readout and DAQ2 validated with µMegas and RPC m² detectors**
- Important issues with PCB design





Power pulsing on Hardroc 2 ASU : Power consumption

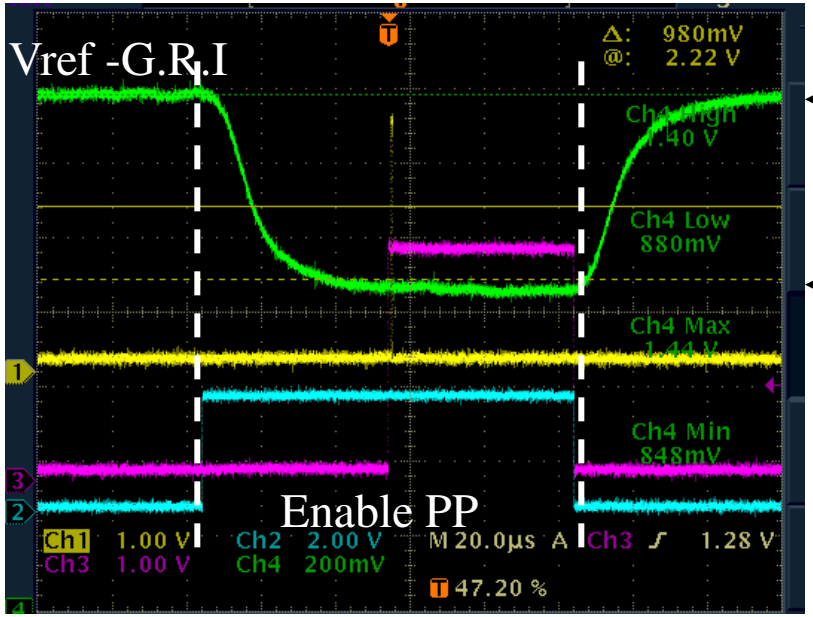
Power pulsing tested at detector level by IPN Lyon

Bias decoupling capacitors removed : performance unchanged

“Awaking time” = 20 µs

Power pulsing gives 80% power reduction. Goal is 99.5 !

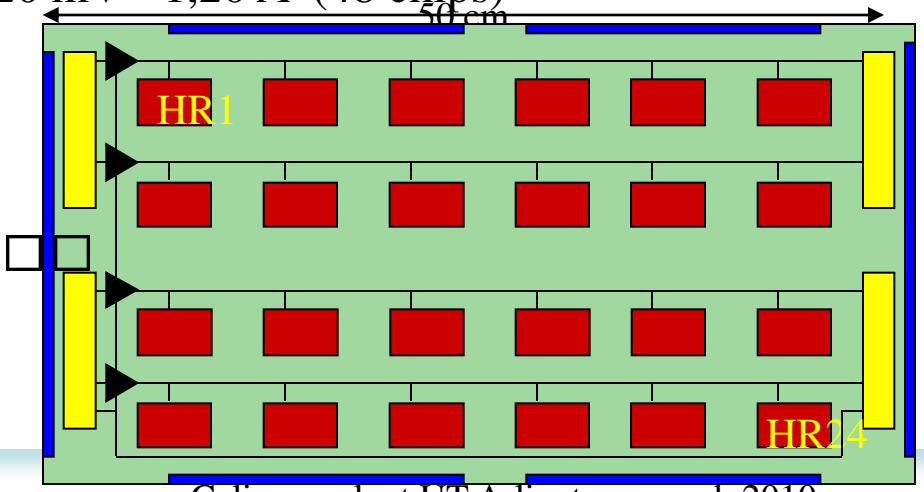
10 µW/ch => 24h operation of full slab with 2 AAA batteries !



100 mV - 200 mA

Permanent consumption due to off-chip LVDS drivers !

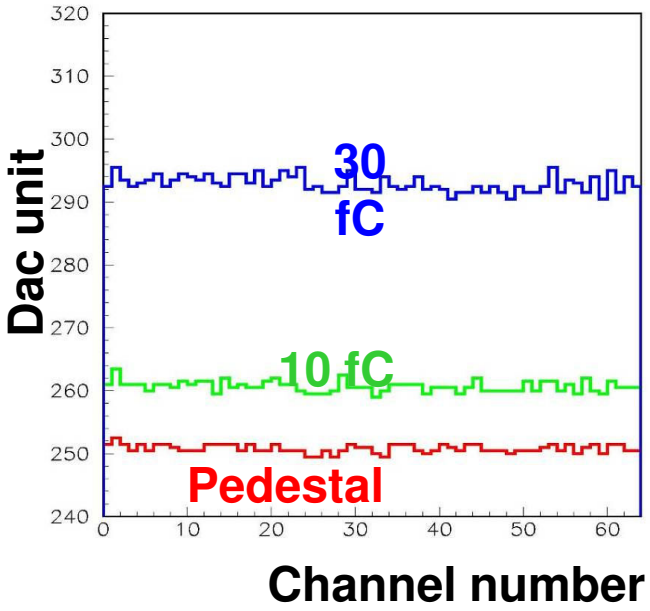
620 mV - 1,20 A (48 chips)



HaRDROC status

- 10000 HARDROC2B in production in march10
  - Ready to equip one large m^3 RPC prototype
  - See talks by K. Belkadhi and N. Lumb
  - Chips expected in june 2010
  - Detector assembly by autumn 2010

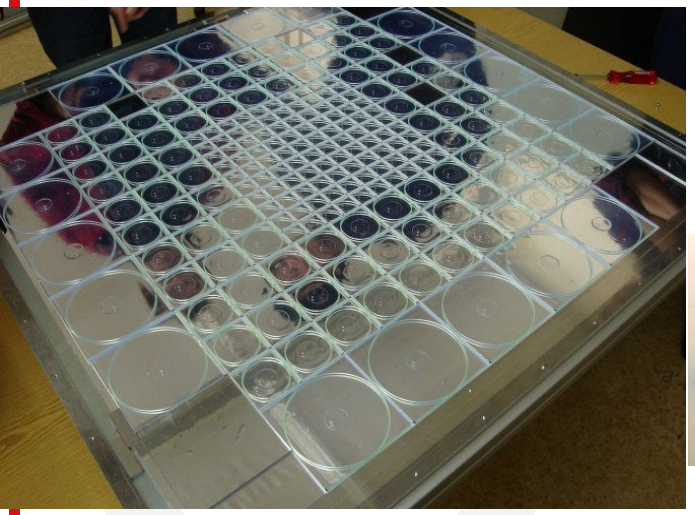
- HR2B not optimized for micromegas
  - Late information on signal amplitude and speed (150 ns)
  - => Thresholds around 2 fC
  - => slower "fast" shaper needed
  - Needs charge preamp
  - => High voltage protection studies are mandatory, combined with preamp
  - Joint development with LAPP Annecy of chip combining DIRAC front-end preamplifier and HR2B backend, expected for june 2010
  - See talk by M. Chefdeville



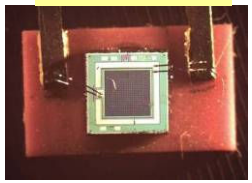
AHCAL: Technological prototype

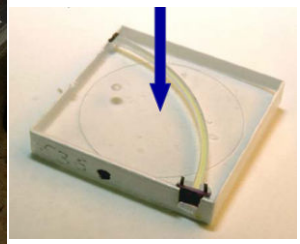
- SiPM detector: 40 layers of 1.5 m^2 2 cm thick steel plates interleaved with cassettes of 296 scintillating tiles (3x3 cm^2) readout by SiPMs

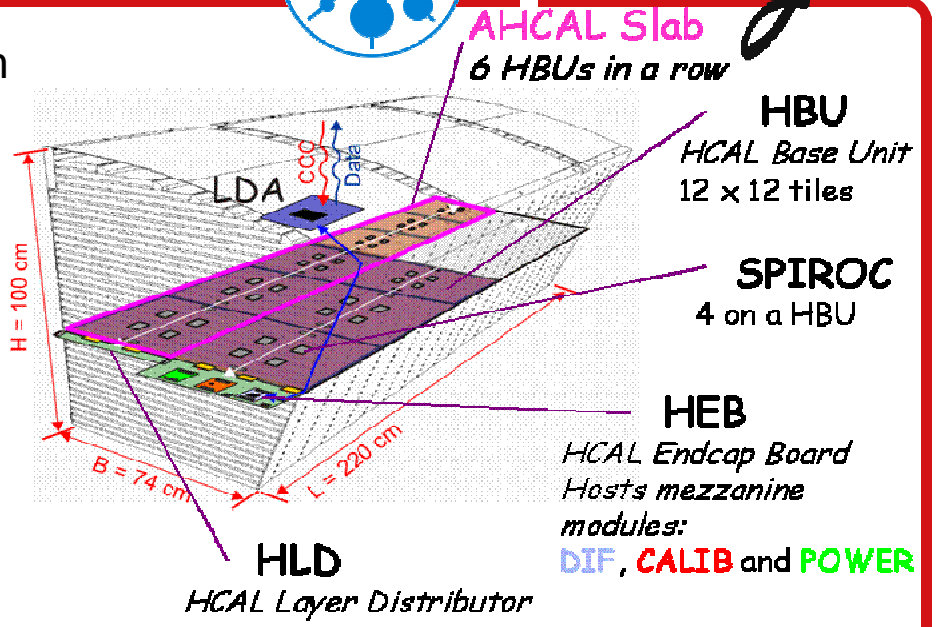
- FE Chip embedded inside the detector
  - Thickness:critical issue: Mother boards (HBU) are sandwiched between 2 absorber plates

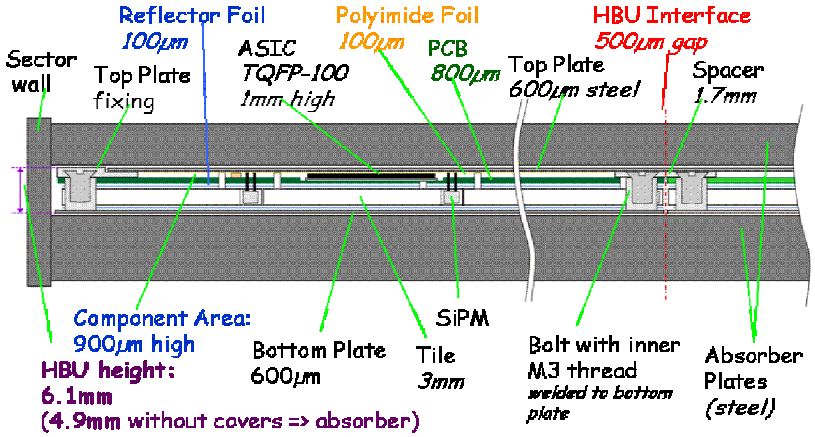


Mephy SiPM



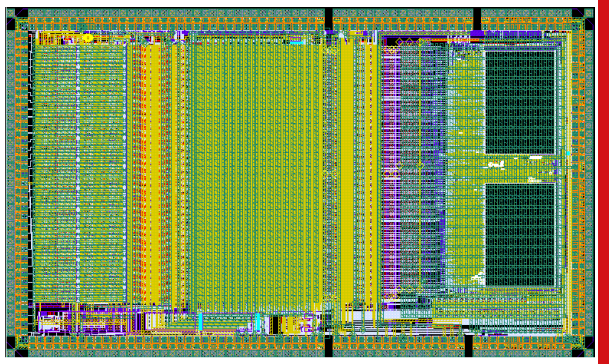




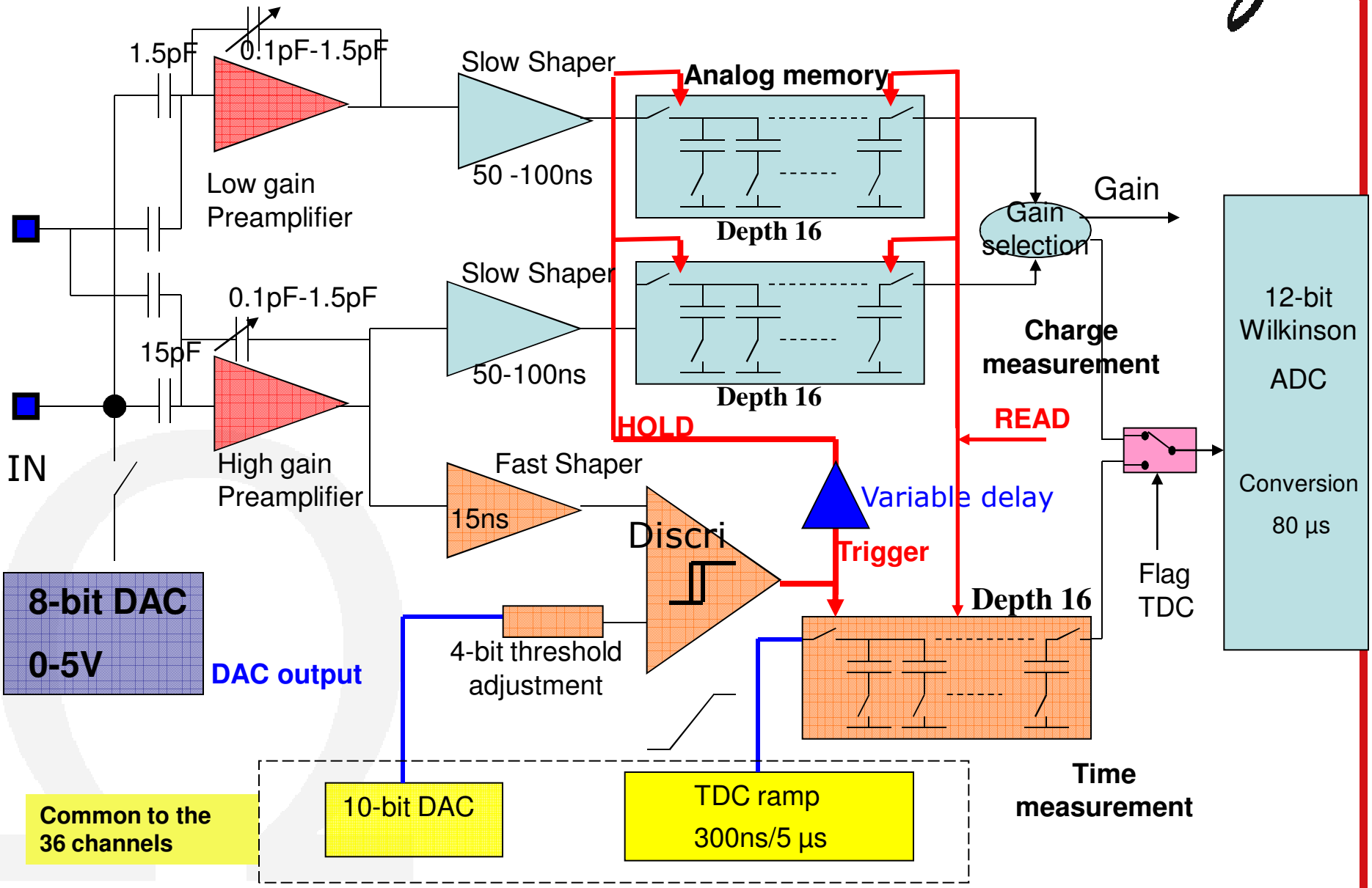


SPIROC main features

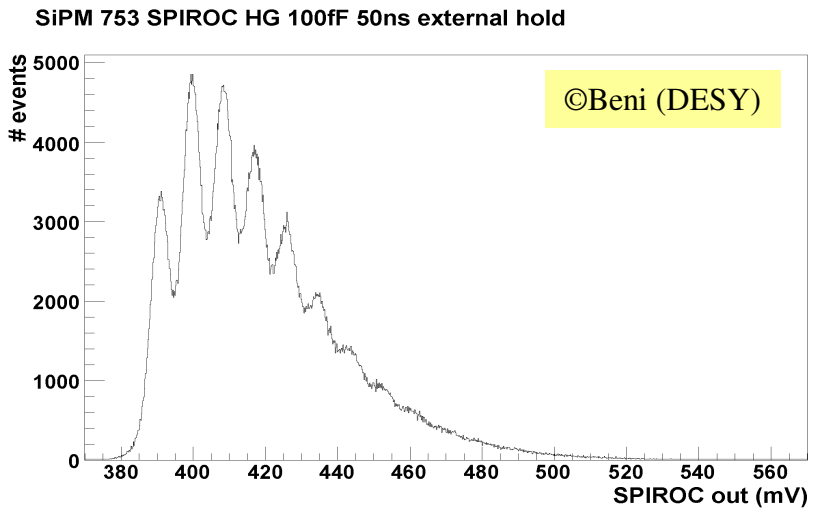
- Internal input 8-bit DAC (0-5V) for individual SiPM gain adjustment
- Energy measurement : 14 bits
  - 2 gains (1-10) + 12 bit ADC: 1 pe → 2000 pe
  - Variable shaping time from 50ns to 100ns
  - pe/noise ratio : 11
- Auto-trigger on 1/3 pe (50 fC)
  - pe/noise ratio on trigger channel : 24
  - Fast shaper : ~10 ns
  - Auto-Trigger on ½ pe
- Time measurement : 1 ns
  - 12-bit Bunch Crossing ID
  - 12 bit TDC step~100 ps
- Analog memory for time and charge measurement : depth = 16
- Low consumption : ~25 µW per channel (in power pulsing mode)
- Individually addressable calibration injection capacitance
- Embedded bandgap for voltage references
- Embedded 10 bit DAC for trigger threshold and gain selection
- Multiplexed analog output for physics prototype DAQ
- 4k internal memory and Daisy chain readout

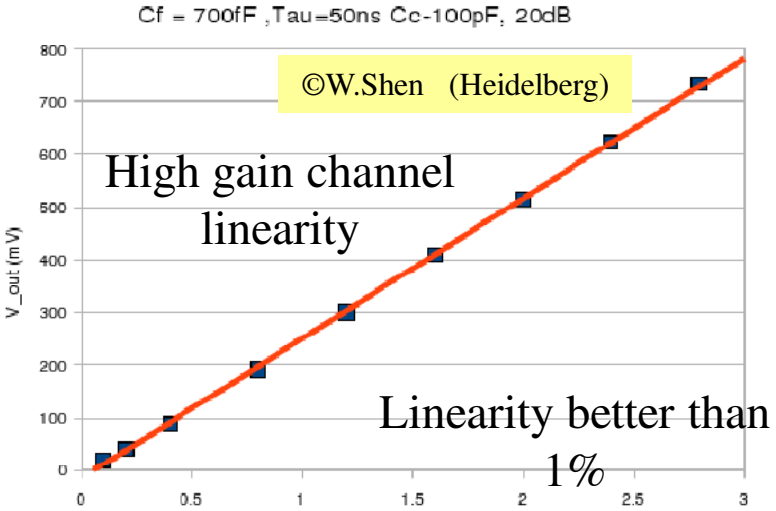


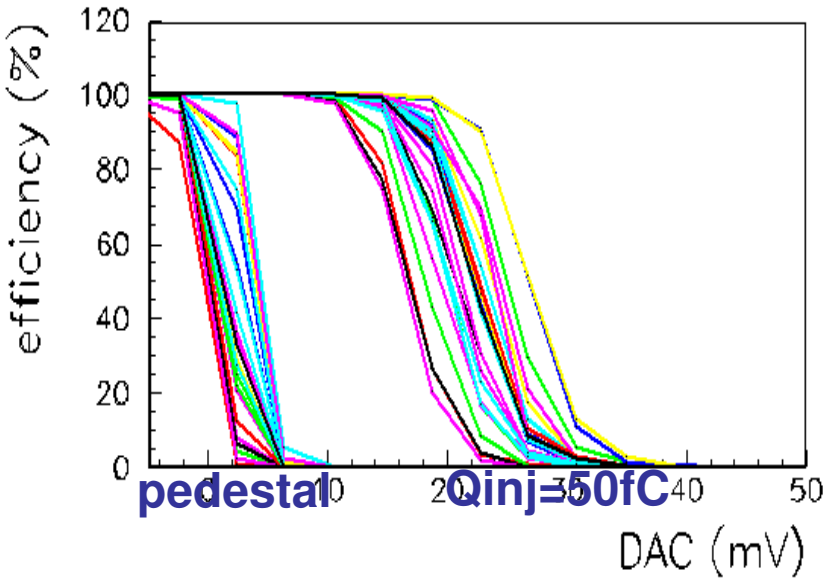
SPIROC : One channel schematic

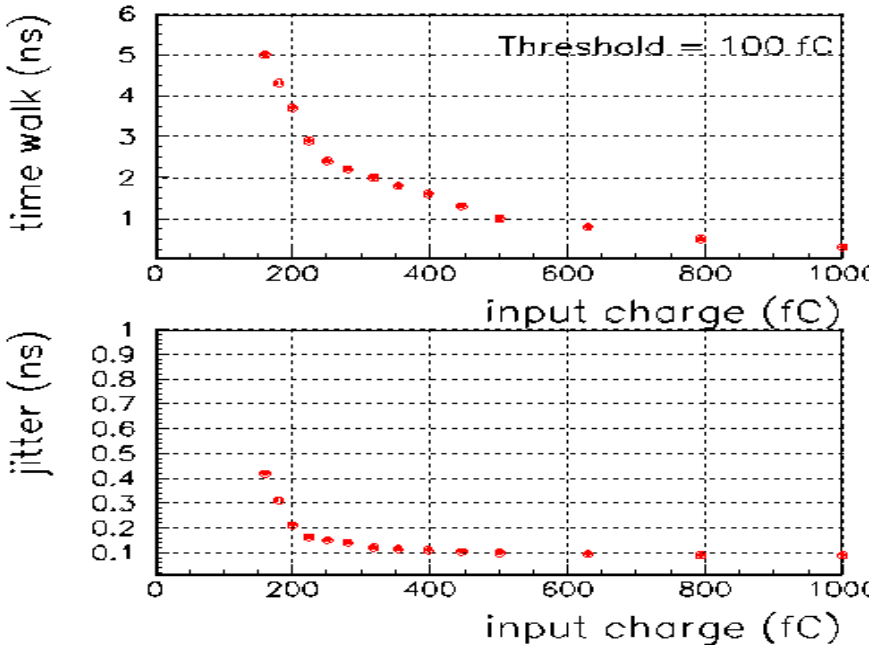


Analog Performance

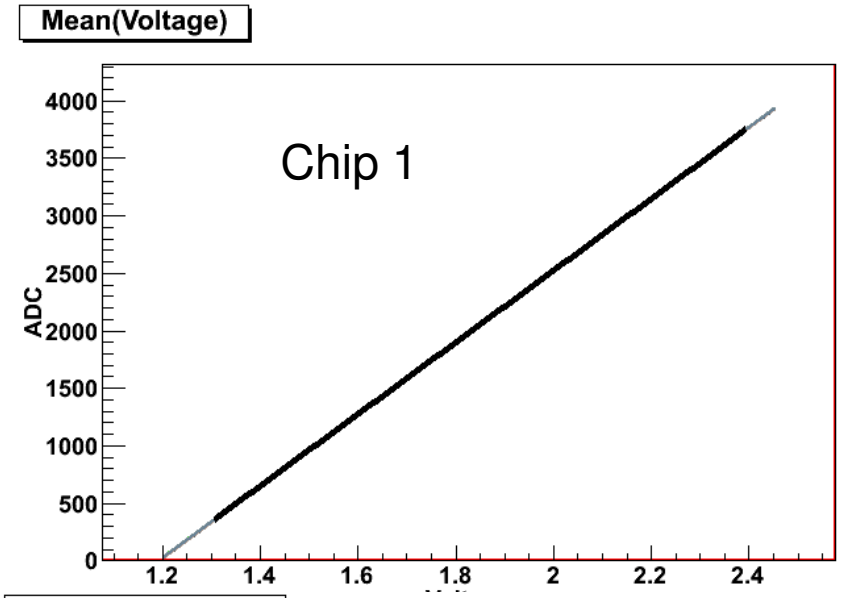


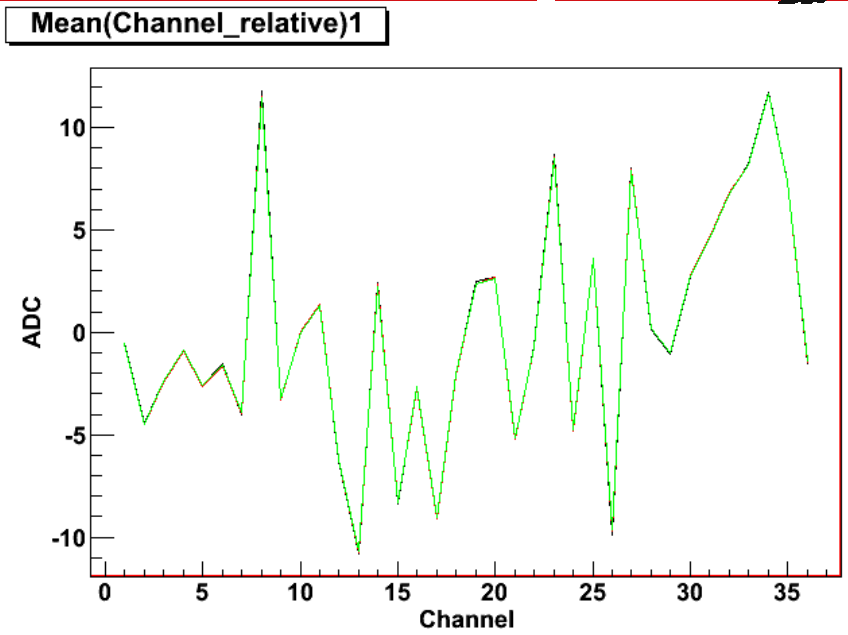


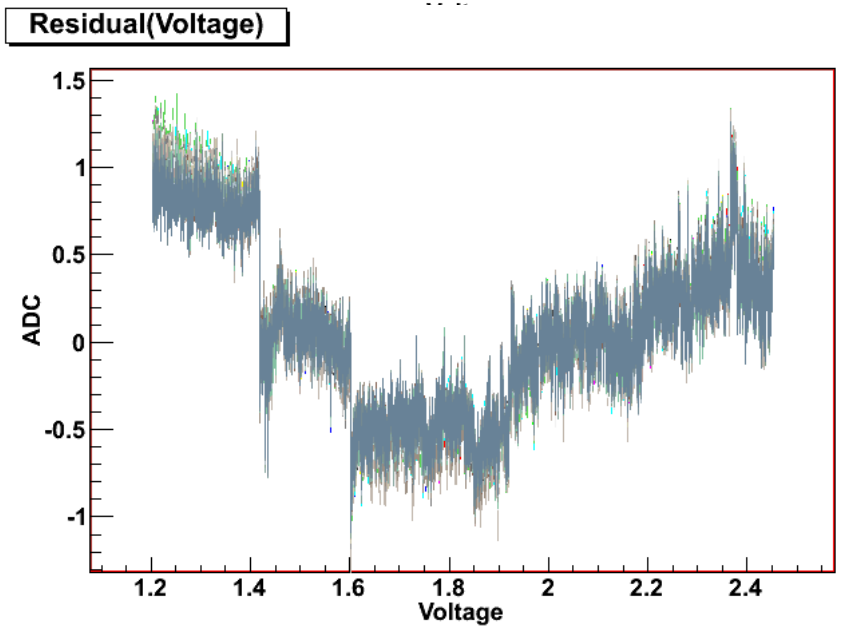


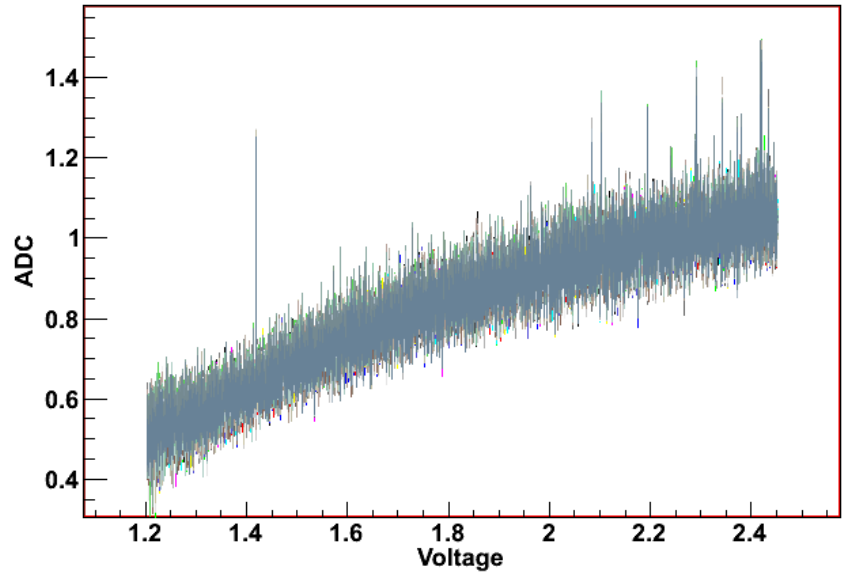


Internal 12-bit ADC performance



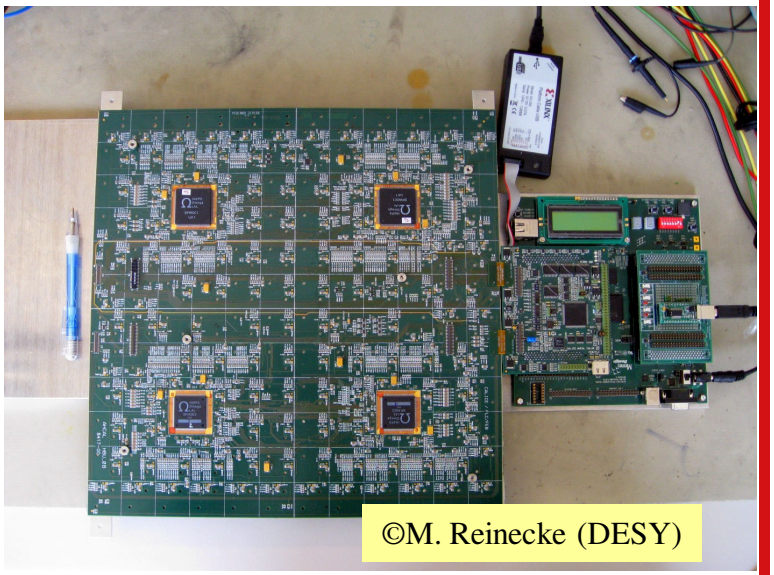




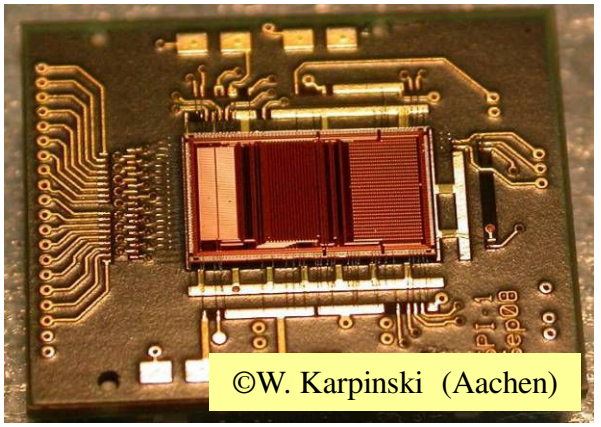


SPIROC status

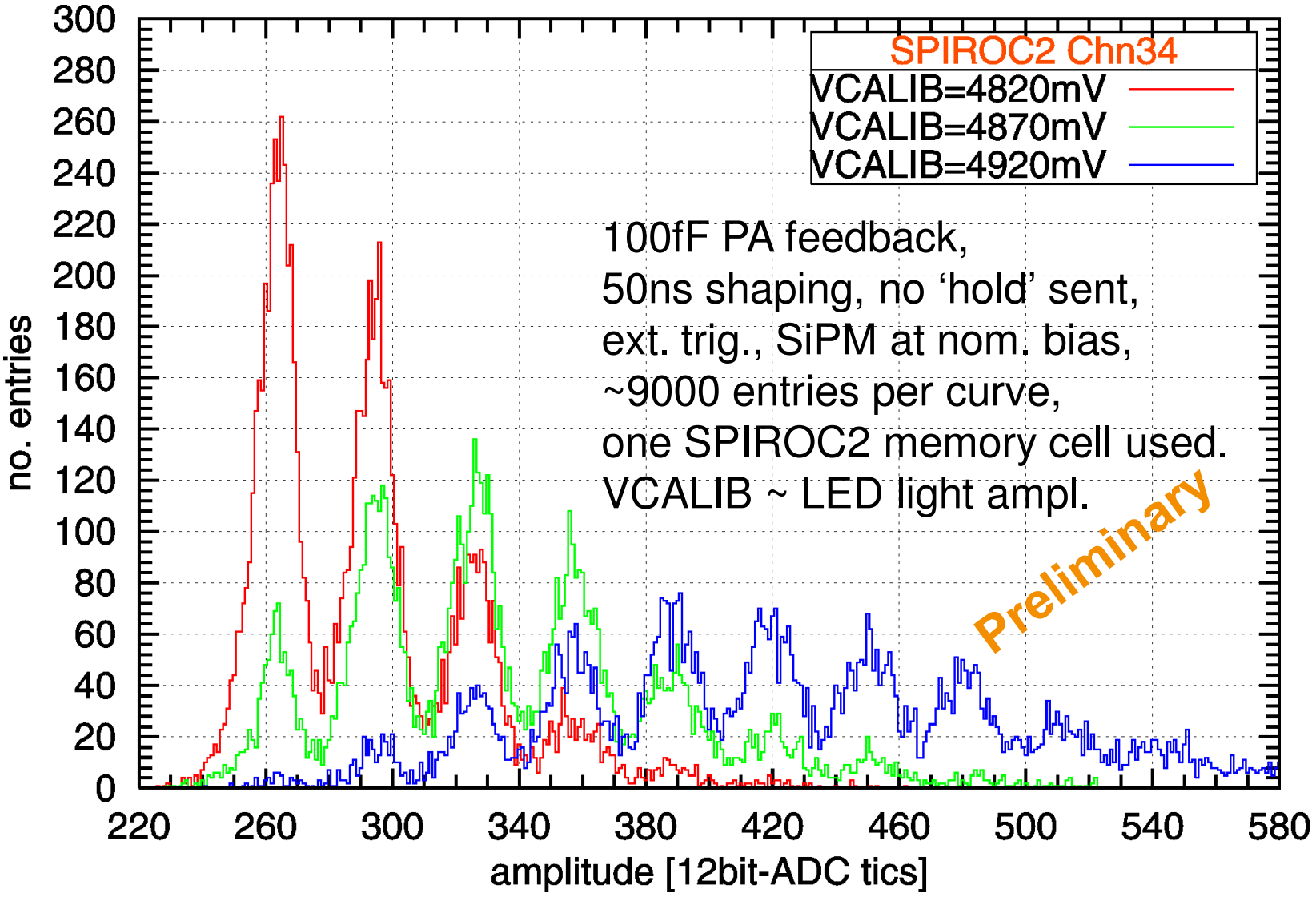
- 50 chips **SPIROC2** produced in june 2008 to equip AHCAL and ECAL EUDET modules
  - Package TQFP208 (w=1.4 mm)
  - Difficult slow control loading (cf HR2b)
  - Measurements gradually coming in
  - Collab LAL, DESY, Heidelberg
  - New preamp developed in Heidelberg [Wei Shen] for lower gain SiPM
  - See talk by R. Fabbri


©M. Reinecke (DESY)

- External users :
  - astrophysics PEBS (Aachen), medical imaging (Roma, Pisa, Valencia…), nuclear physics (IPNO), Vulcanology (Napoli)

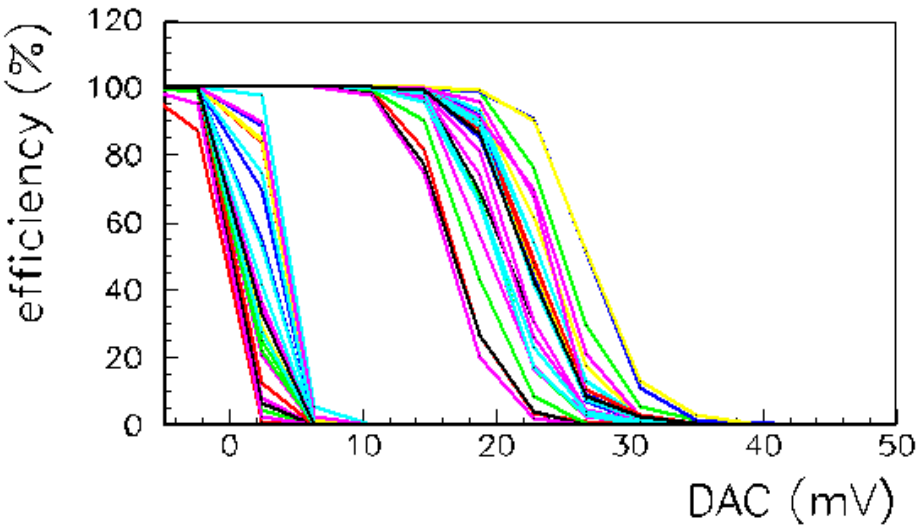

©W. Karpinski (Aachen)

Single-Photon Peaks I



Spiroc pending issues

- Autotrigger mode
- Linearity
- Power pulsing
- Time measurement

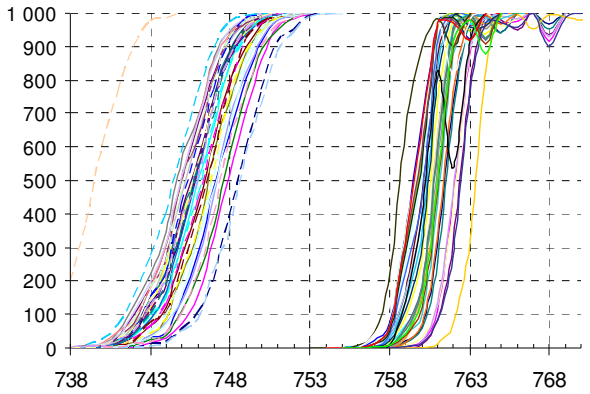


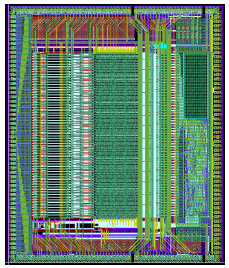
- 2 versions have been fabricated for EUDET
  - SPIROC2A : same as v2, slow control fixed
  - SPIROC2B : individual gain adjustment

SKIROC status

- SPIROC2 used as SKIROC emulator
  - only preamp differs
  - 36 channels instead of 64
  - Limited dynamic range (~500 MIPs)
  - Tests starting with FEV7 to address embedding issues
  - Noise tests on testboard proceeding (ENC ~ 1 ke-)

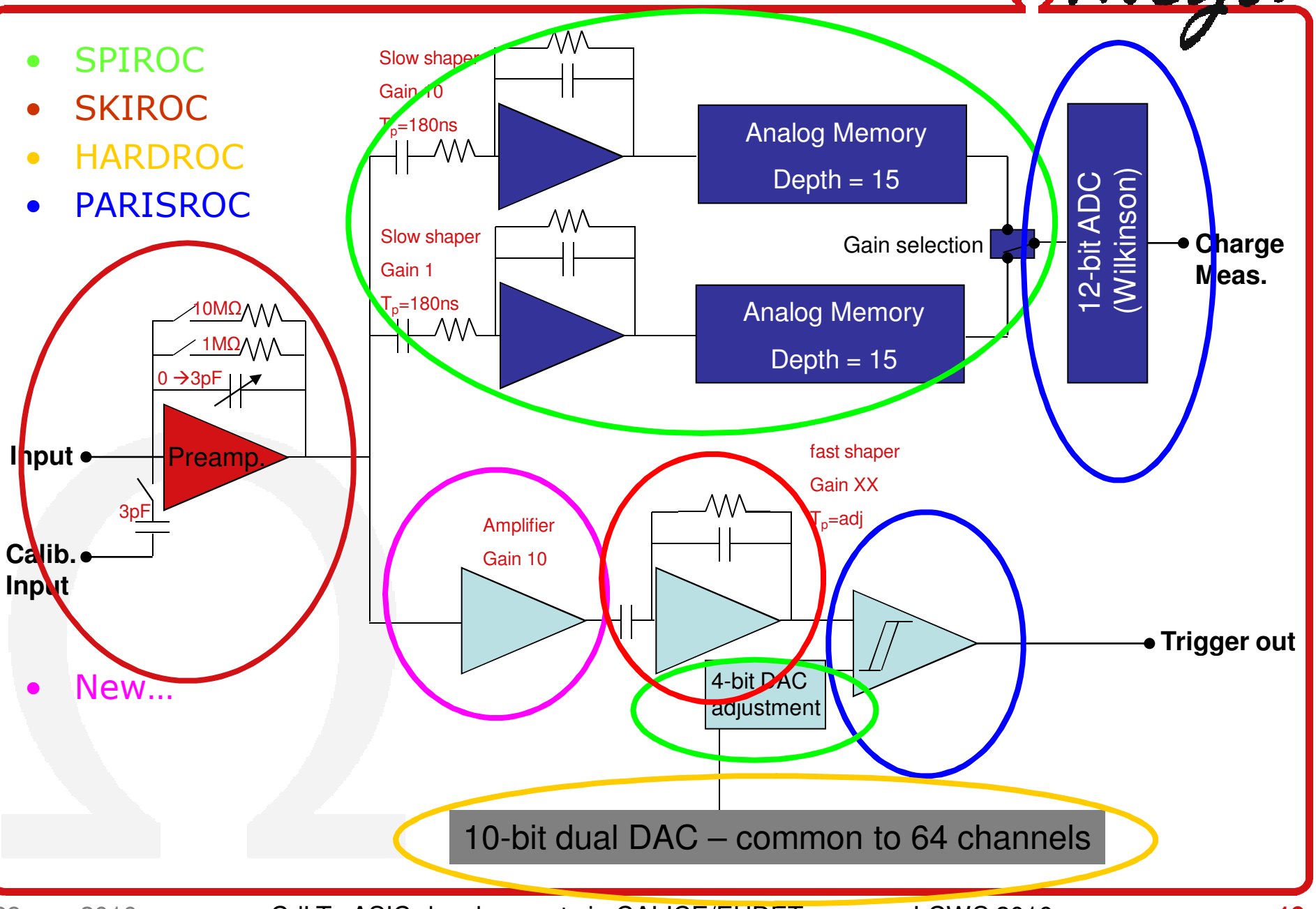
- SKIROC2 submitted with production run
  - 64 channels, 70 mm^2
  - Very large dynamic range: HG for 0.5-500 MIP, LG for 500-3000 Mip
  - Testability at wafer level





SKIROC2 One channel block scheme

- SPIROC
- SKIROC
- HARDROC
- PARISROC



- New…

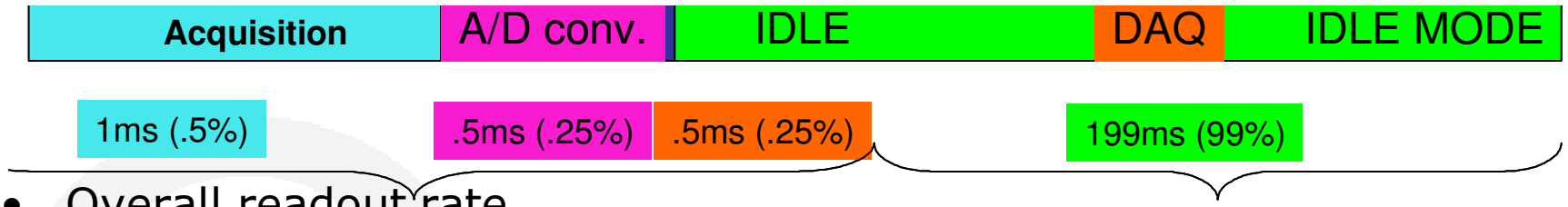
Conclusion

- Chips in production for technological prototypes
  - Chips expected june 2010
  - Detector assembly fall 2010

- Lots of important tests ahead
  - Power pulsing
  - Coherent noise
  - Power dissipation
  - timing
  - System aspects
  - DAQ

Test beam with technological prototype

- Data rate (Spiroc/Skiroc) : naive estimate
  - Volume : 36ch*16sca*50bits=30 kbit/chip
  - Conversion time : 16*100 µs = 1.6 ms
  - Readout speed 5 MHz (could be increased to 10-20 MHz)
  - 8 chips/DIF line (one FEV only)
  - Total : 1.5ms + 30000*200ns*8 = 50 ms/16 events = 3 ms/evt => 300 Hz during spill



- Overall readout rate
  - « Add » 1-10% power pulsing : 3-30 Hz effective rate
  - Pessimistic as assuming all chips full
  - **interesting tests to be done**

- Note : readout electronics designed for ILC low-occupancy, low rate detector **≠Testbeam** !!

Read out: token ring

- Readout architecture common to all calorimeters
- Minimize data lines & power