Status of the MICROMEGAS semi-DHCAL

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LAPP, Annecy, France

LCWS, 27th March 2010, Beijing

Overview

- The 1 m^3 semi-DHCAL project & MICROMEGAS

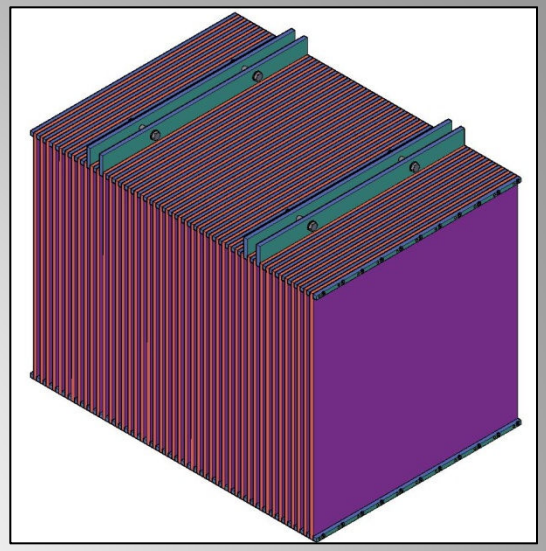
- Simulation
- Test beam and ASIC
- DAQ

- The 1 m^2 MICROMEGAS prototype

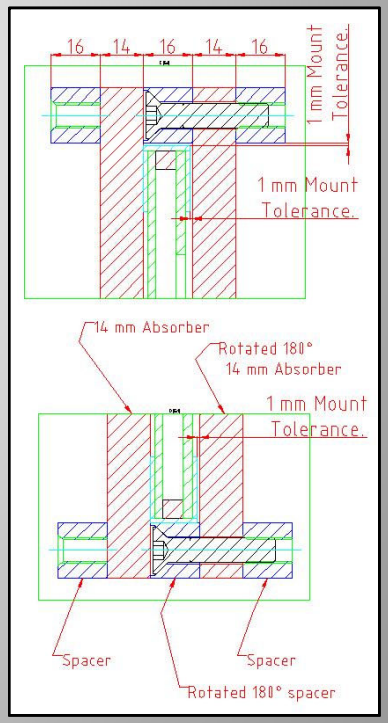
The 1 m^3 semi-DHCAL

- Calorimetry based on Particle Flow
  - Granularity more important than resolution → digital option
  - Loss of linearity at high energy (100 GeV/c) → 2 bit readout → semi-digital HCAL
- 1 m^3 semi-DHCAL project in France
  - Funded by CNRS/IN2P3 + "Agence Nationale de la Recherche" (ANR) + Rhone-Alpes region (chip development)
  - Several labs involved
    LAL (Orsay) → HARDROC
    IPNL (Lyon) → RPC
    LLR (Palaiseau) → CALICE DAQ
    LAPP (Annecy) → MICROMEGAS
- Choice of active media (required by ANR schedule)
  - 3 physicist committee
  - RPC favored but production of MICROMEGAS m^2 planes should be pursued

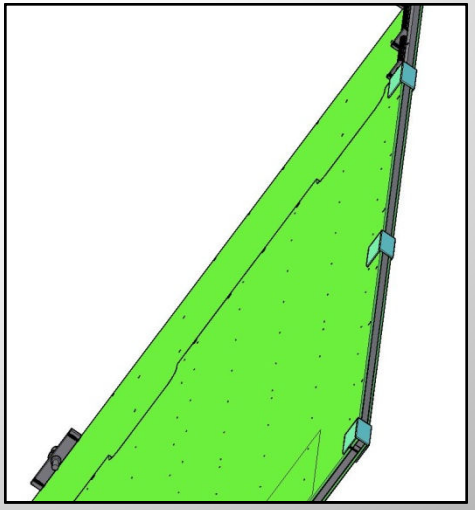
The 1 m^3 structure



- Design proposed by CIEMAT group
  - In collaboration with LAPP engineer
  - 2 different mechanical pieces
    minimum machine operation on each piece
  - Deformation and stress simulation
- From Enrique Calvo Alamillo talk,
  Madrid, 1st March 2010



- Compatible with RPC and MICROMEGAS
  - 44 planes
  - 16 mm between absorbers
    1 mm tolerances



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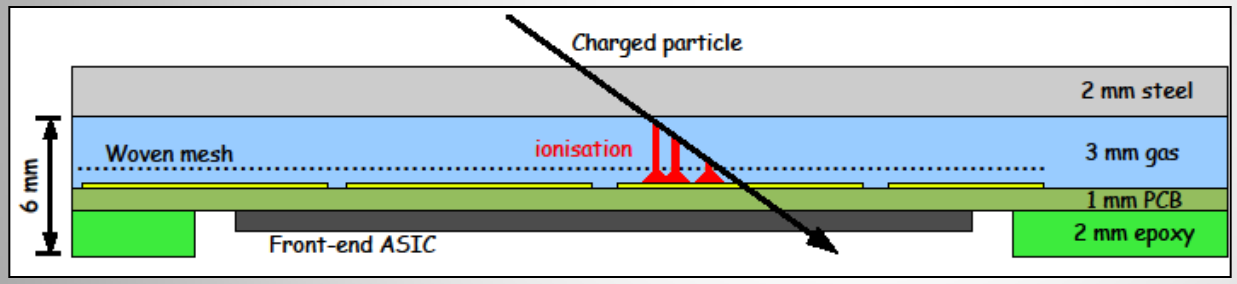
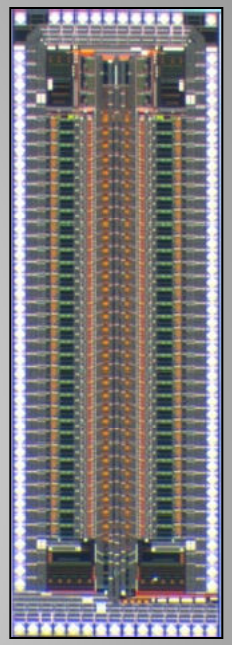
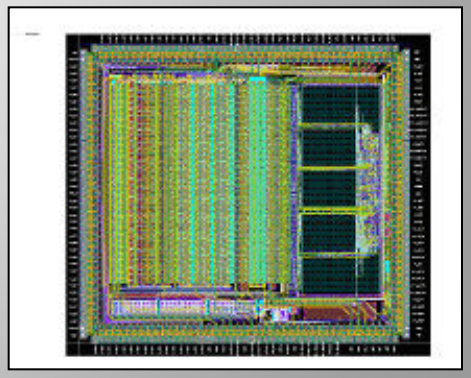
Detector planes

- RPC VS MICROMEGAS
  - Large VS small signals, low VS high rate capability
  - Limited proportionality VS proportional mode
    → MICROMEGAS best suited for semi-DHCAL



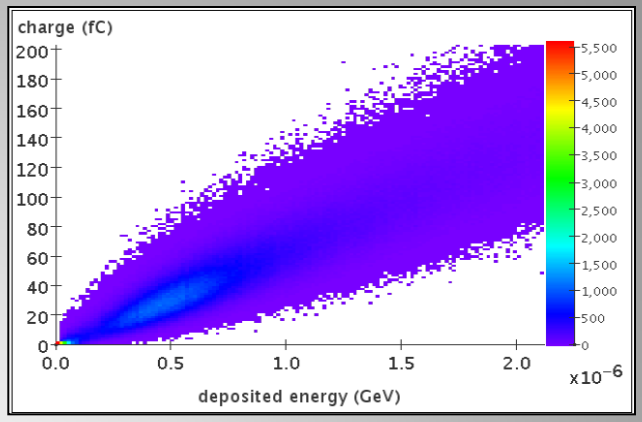


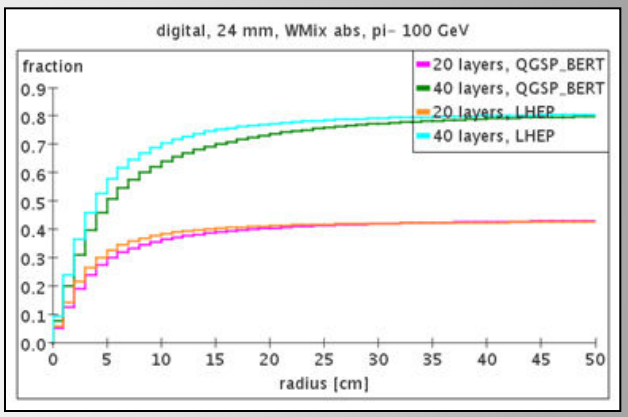
- Semi-digital readout
  - HARDROC or DIRAC ASIC (3 thresholds)
  - What should the threshold be?
    → detailed simulation

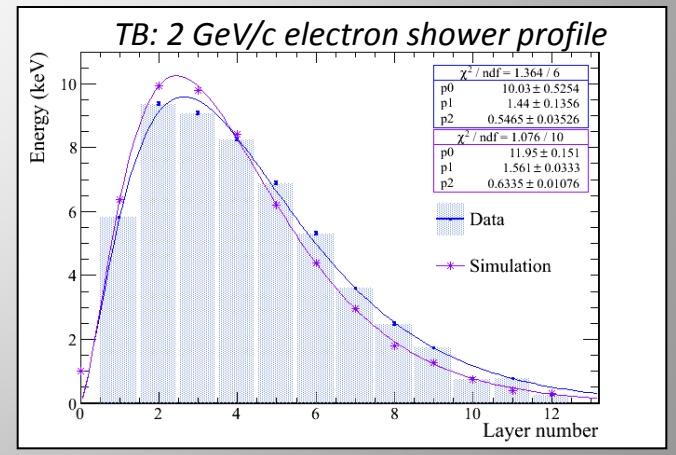


Simulation (I)

- Comparison analogue/digital readout for 1 m^3 steel, applying 1 energy threshold
  - Energy resolution, linearity, shower shapes
    → 2009 *JINST* **4** P11009
- Digitization, from GEANT4 energy deposits in gas layers to hits, applying charge thresholds
- Simulation for CLIC:
  - Definition of HCAL;
  - Definition of small prototype for beam test:
    → J. Blaha, CLIC Physics and Detector Meeting, 15 Sep. 2009, CERN
- TB setup simulation and comparison with data
  → shower profile study to be published

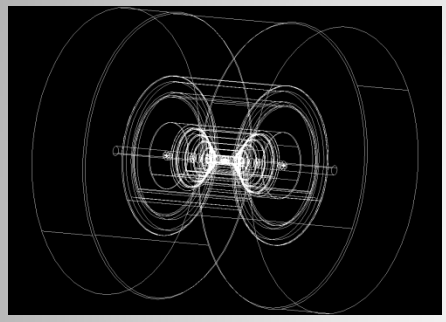


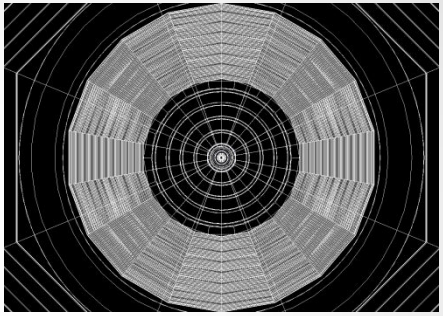


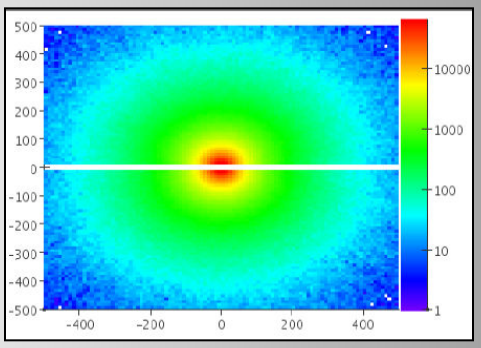


Simulation (II)

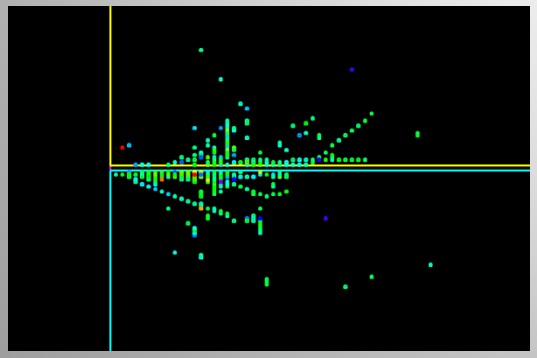
- Implementation of MICROMEGAS DHCAL in CLIC and SiD detector geometry

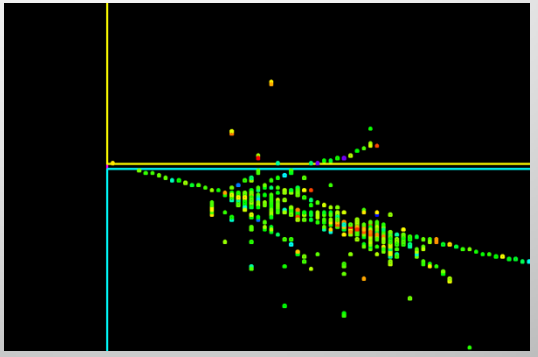


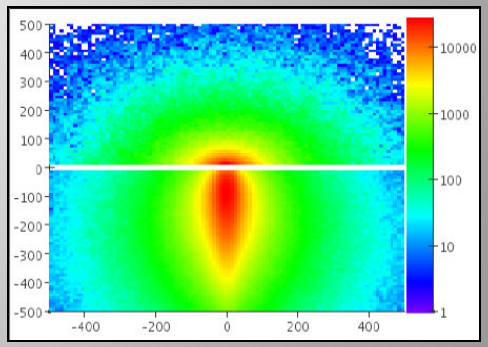




- Study of crack effects on HCAL performance
  - Projective and tilted geometries





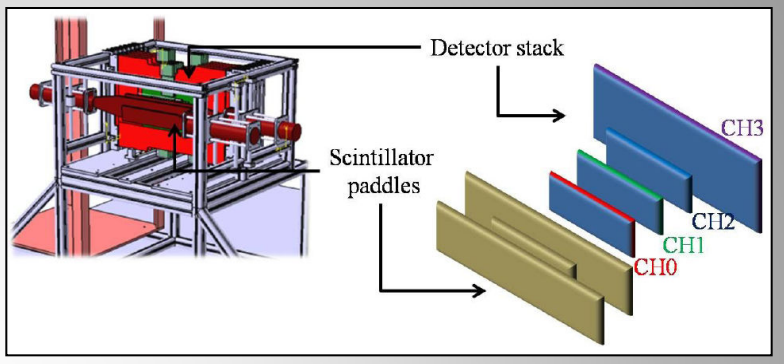


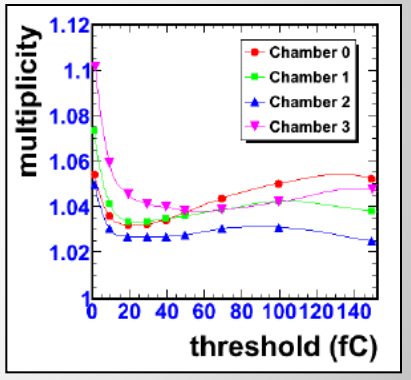
TB and ASIC developments

- Detector characterisation done with analogue readout prototype (GASSIPLEX)
  - Carried out with Irfu collaborators

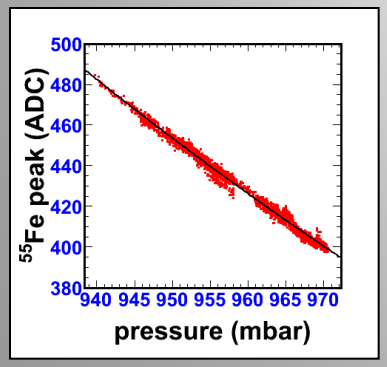
  → 2009 *JINST* **4** P11023

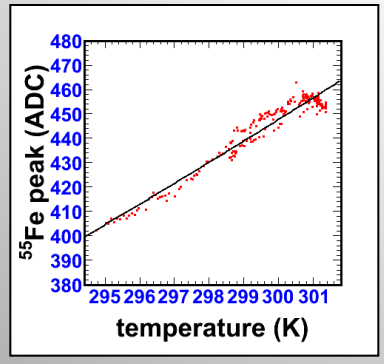
- Signal MPV of 20 fC (with 10 % variations)
- Sensitivity to P, T (2 % / K & -0.6 % / mbar)
- At a threshold of 1.5 fC
  - 97 % efficiency with variations < 1 %
  - Hit multiplicity below 1.12

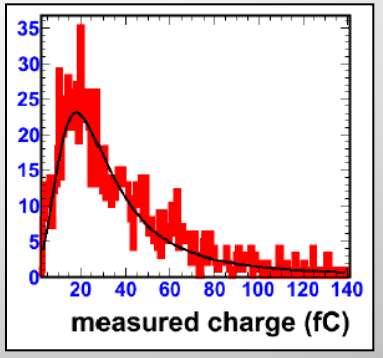


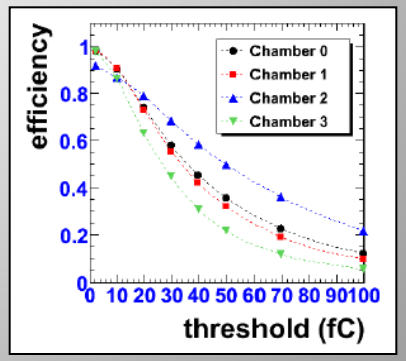


irfu cea saclay









TB and ASIC developments

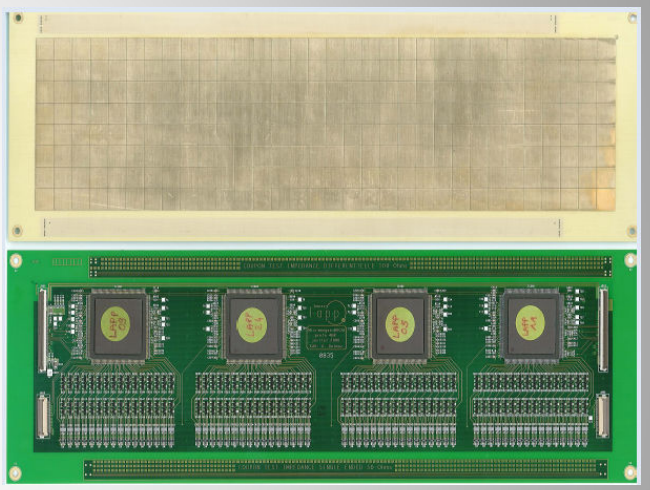
- Now focus on test of digital readout prototypes with embedded electronics
  - ASIC and spark protection components on PCB
  - Bulk lamination on PCB using a mask at CERN workshop
  - RD51 collaboration (*http://rd51-public.web.cern.ch/RD51-Public*) asked for a new location: increased production capability

- 2 different chips (64 channel each)
  - HARDROC (LAL/Omega group), asynchronous functioning, shape signals
  - DIRAC (IPNL/LAPP), synchronous functioning, integrate signals

2009 TB with HARDROC1

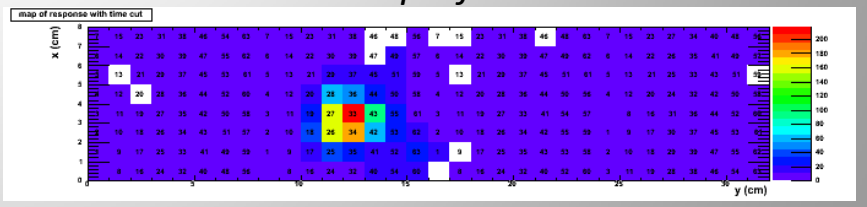
- 3 chambers of 32x8 cm^2 (3 mm gas gap)
  4 chips & 1 DIF / board

32x8 cm^2 ASU with 4 HARDROC



- May 09 @ PS/T10
  - Hard times with DAQ:
    DIF synchronicity
    no acquisition software expert available
    USB data readout problems…
  - No quantitative study: beam profile
    → it works

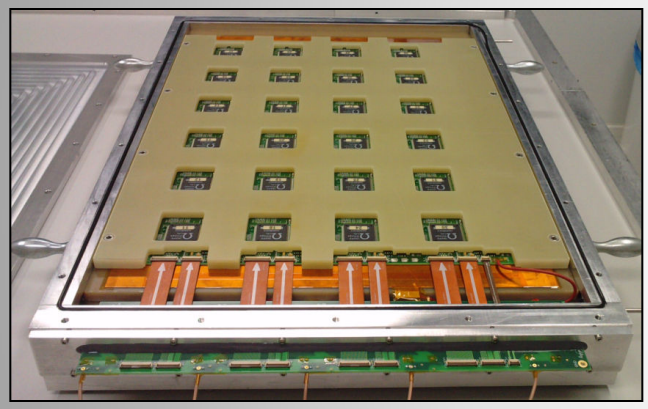
Hadron beam profile in one chamber

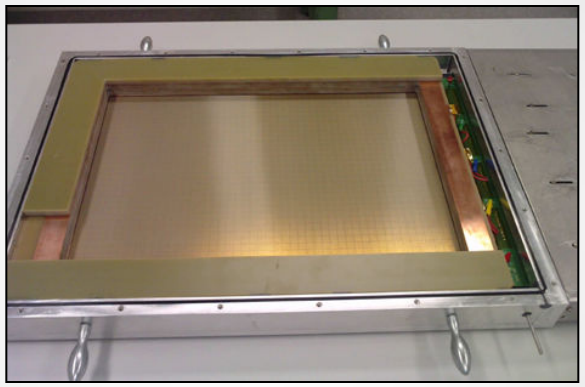


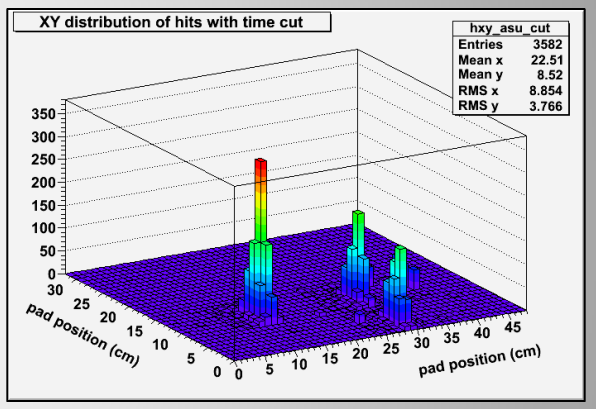
- Sep 09 @ PS/T10 (DAQ OK)
  - Very low efficiency (5-10 %)
  - Understood as too short shaping time

2009 TB with HARDROC2

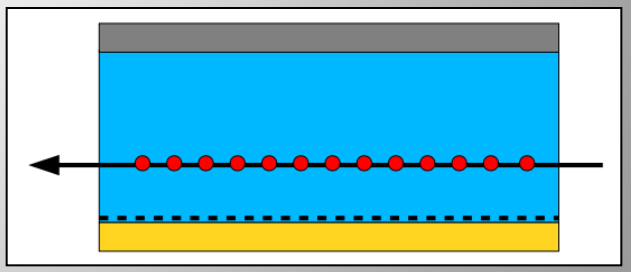
- 1 board of 48x32 cm^2 (unit of future 1 m^2) inside a gas test box with 3 cm gas gap, equipped with 24 chips & 1 DIF





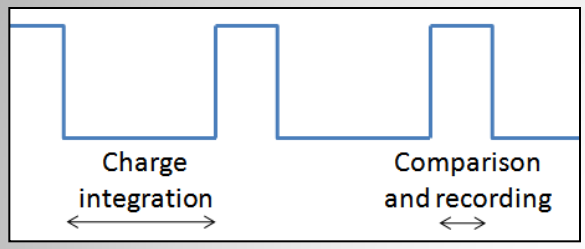


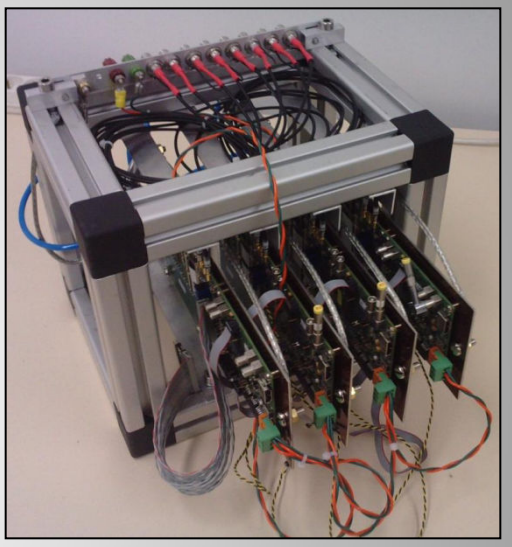
- Test with chamber (perpendicular and) // to beam
  - Faster signals at the pads
  - Larger signals (1 cm)
  - Efficiency between 10-90 % depending on chip threshold



2008-09 TB with DIRAC

- Synchronous chip functioning (ILC-like)





- First chamber with embedded ASIC (ASU)
  - 8x8 cm^2 tested in SPS beam in 2008

- Stack of 4 chambers (8x8 cm^2)
  - PS/T9 in Nov. 2009
  - Short life-time in beam
    → chip design improvement
  - Small statistics but promising results
    → multiplicity 1.06-1.13
    → efficiency 45-50 %

Chamber 1: 12 / 27 = 0.44
Chamber 2: 14 / 29 = 0.48
Chamber 3: 14 / 30 = 0.47
Chamber 4: 14 / 30 = 0.47

To be corrected for synchronous functioning

Future plans for front end electronics

- HR input stage not suited for the detection of MICROMEGAS signals

- Promising results obtained with DIRAC chip

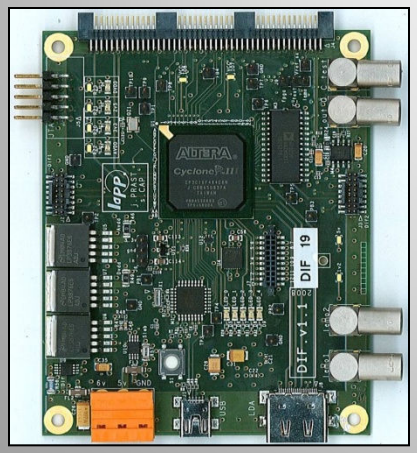
→Development of a new chip from existing ones, in collaboration with LAL/Omega group

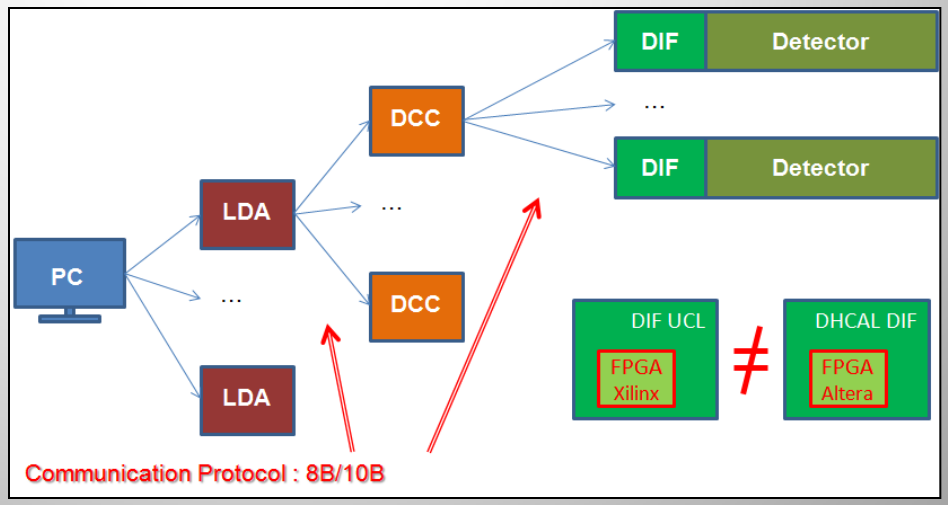
→ Work on spark protection
spark proofness test setup @ LAPP
innovative solutions studied within RD51

Contribution to CALICE DAQ

- Detector Interface (DIF) developed at LAPP is ready for production
  - A batch of 20 DIF should be available end of March
  - 150 board production planned for this summer, all available in Sept.

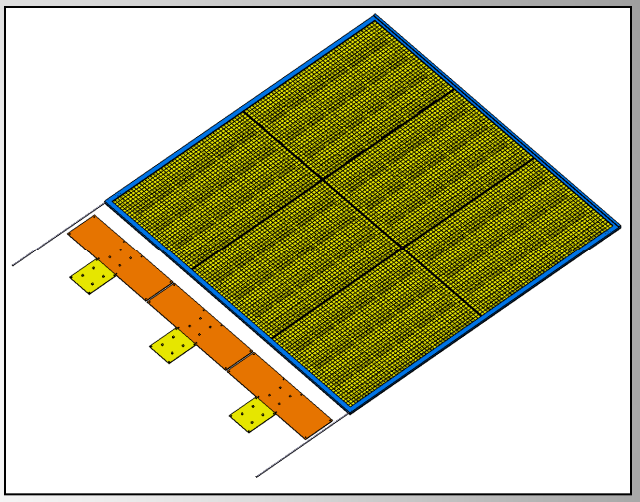
- Important milestones
  - 8B/10B communication protocols validated (LAPP/LLR)
  - CCC (Clock and Control Card) integration in work at LAPP

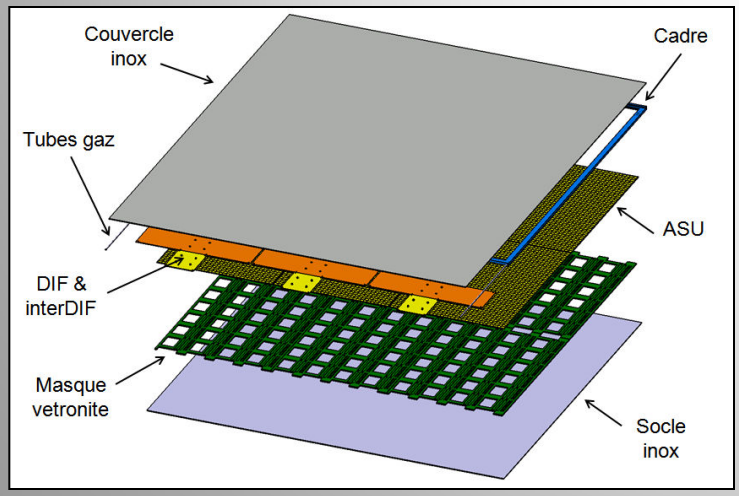




The 1 m^2 MICROMEGAS prototype

- Features
  - 6 ASU of 48x32 cm^2
  - 24 ASIC / ASU
    → 1536 * 6 = 9216 channels
  - Dead areas < 10 %
  - Total thickness of 1.15 cm (incl. steel covers)
  - 3 DIF boards
- Test of each ASU separately
- Assembly procedure validated



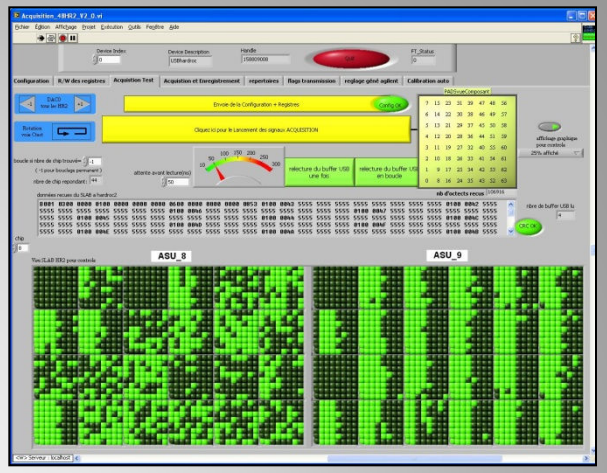


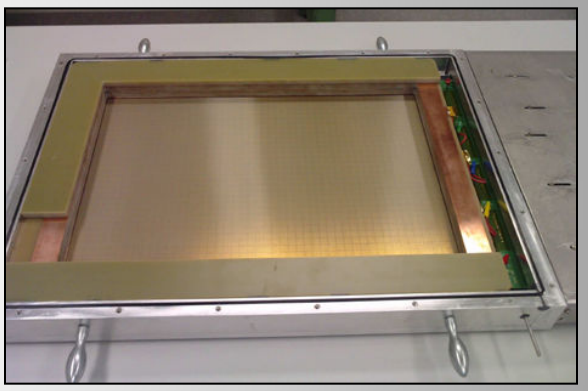
Status and future plans

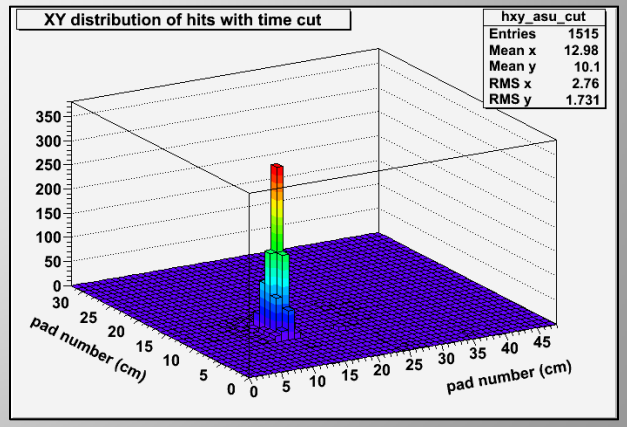
- ASU test on-going
  - Measurement of ASIC performance
    - Noise, gain, uniformity, equalization
  - Response to ^{55}Fe X-rays and cosmics in gas box @ LAPP

- 4 ASU with HR2, 1 ASU with HR2b + 1 dummy
  Assembly foreseen in April
  Cosmics tests @ LAPP until June

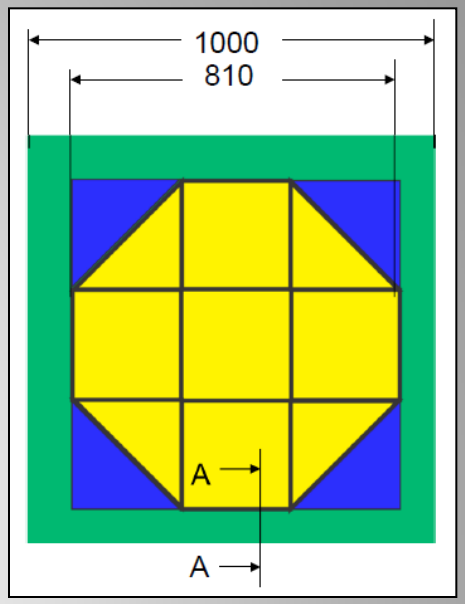
- 2-3 weeks of beam in SPS/H4 end of June
  - Efficiency, multiplicity, uniformity
  - Spark study (beam intensity)







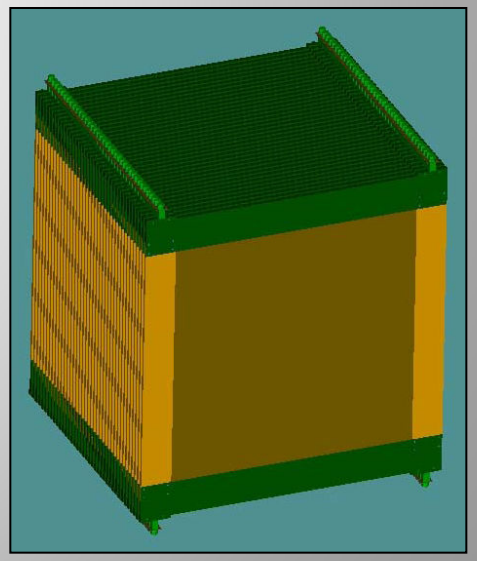
Test inside W-structure



- The LCD-CERN, CALICE-DESY and LAPP groups agreed to work together and construct a W-HCAL prototype starting 2010
  - LAPP contribution on simulation + MICROMEGAS layers
    → see W. Klempt talk at CALICE meeting, Arlington, 12/03/10

- Start with a small prototype
  - 20 W-layers of 81x81 cm^2, 1 cm thick

- 2 weeks of beam inside W-structure with AHCAL in PS/T9 starting mid November 2010
  - Test of scintillator layers + 1 or more MICROMEGAS planes



Conclusions

- MICROMEGAS, as proportional detector, is well suited for a semi-DHCAL
- Very good basic performance for a DHCAL
  but strongly depends on electronics
  - HARDROC input stage not optimized for MICROMEGAS signals
    Work on a new ASIC on-going
  - Several options for spark protection are being investigated
- First 1 m^2 MICROMEGAS prototype available end of April 2010
  and ready for beam test at the end of June
  - Equipped with HR2, so limited performance expected
    However, a lot to learn for next 1 m^2 prototypes
  - Next prototypes should be equipped with a different chip
    - One plane with DIRAC if spark protection issue solved
    - Next planes with a new chip, probably resulting from
      the collaboration between LAL and LAPP

Acknowledgments

the LAPP group

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