R&D of FCAL

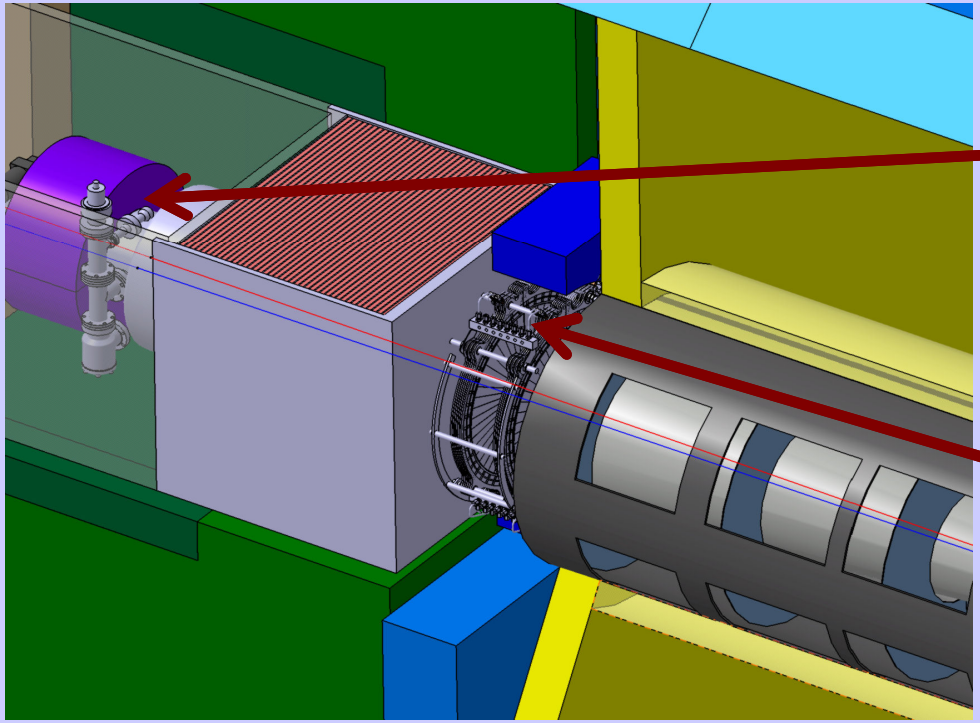
W. Lohmann, DESY,

on behalf of FCAL

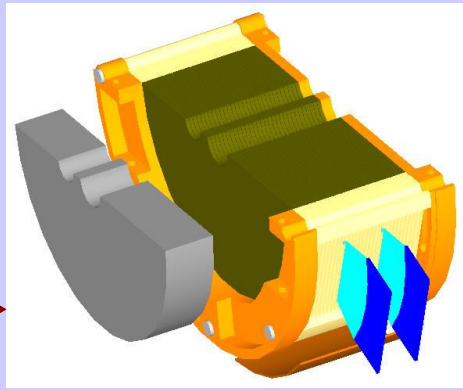
- Simulation studies
- Sensors
- FE ASICs
- System Tests
- short- and midterm plans

Labs involved: Argonne, Vinca Inst, Belgrade, Bukharest, CERN, Univ. of Colorado, Cracow UST, Cracow INP, IKP Dresden, JINR, Royal Holloway, NCPHEP, UC Santa Cruz, Stanford University, SLAC Tuhoku Univ., Tel Aviv , Univ., DESY (Z.)

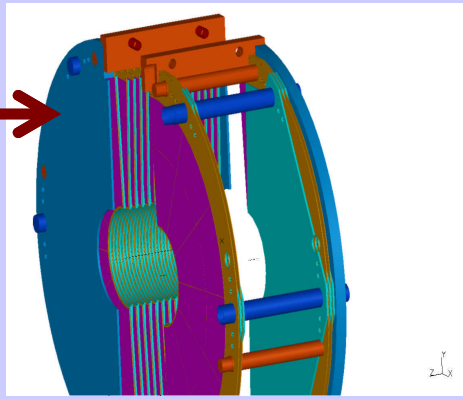
Very forward detectors- challenges



BeamCal + Pair Monitor

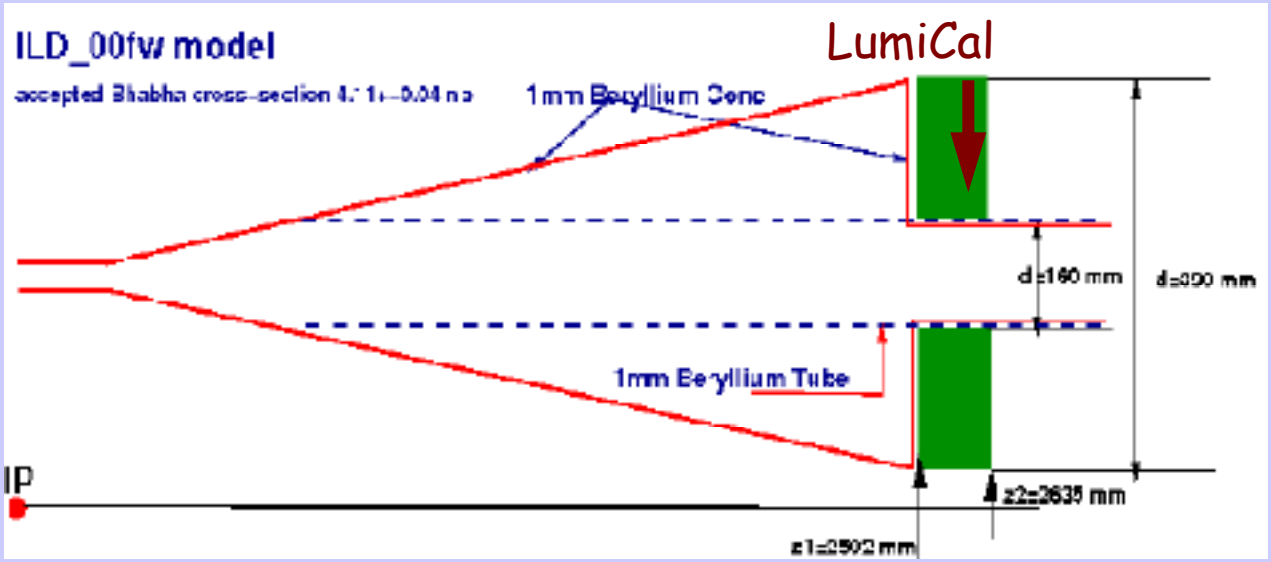


LumiCal



- Ongoing simulations to optimize detector design for
  - precise luminosity measurement,
  - hermeticity (electron detection at low polar angles),
  - assisting beam tuning (fast feedback of BeamCal data to machine)
- Challenges: radiation hardness (BeamCal), high precision (LumiCal) and fast readout (both)

Simulation Studies, example beam-pipe shape



Simulation using 10^6 Bhabha events indicates no impact on the precision of the Lumi measurement

However: keep the conical volume empty

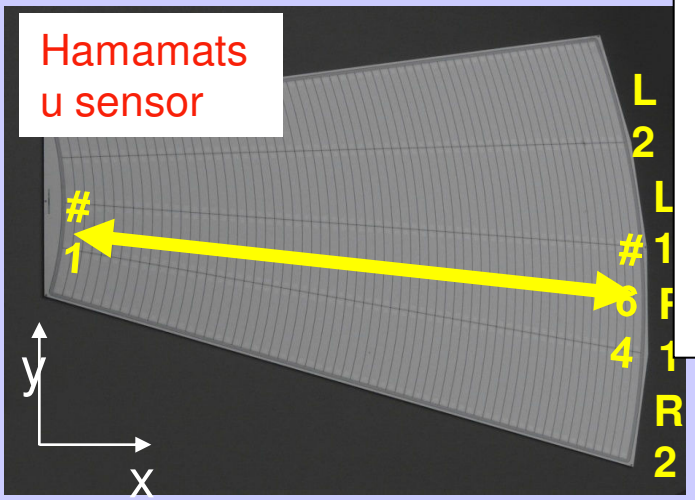
See also the talk by Ivanka Bozovic-Jelisavcic in the MDI session, Monday, March 29, 12.00, and Andre Sailer, BDS_MDI session, Monday 29 March, 2.25

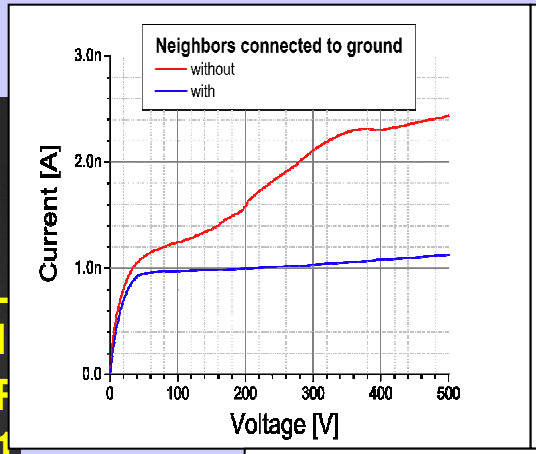
LumiCal sensors

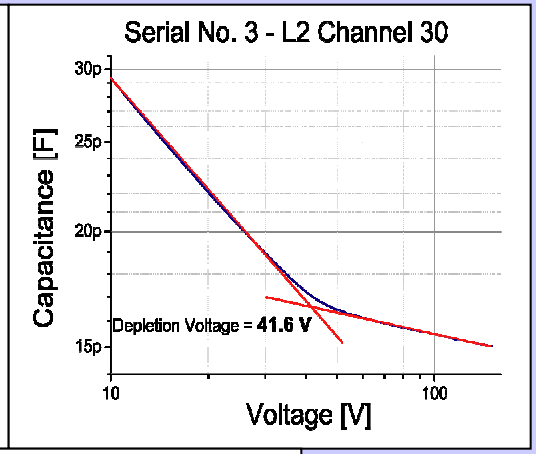
LumiCal: low irradiation load → silicon-tungsten sampling calorimeter

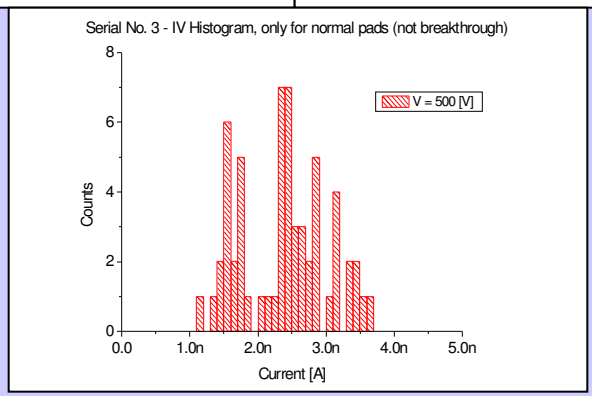
- Design (optimized geometry for luminosity measurement)
- Hamamatsu sensor prototypes (6", p in n, DC-coupled, 350 μm thick)

Measurements in Cracow, DESY, Tel Aviv (cross calibration)









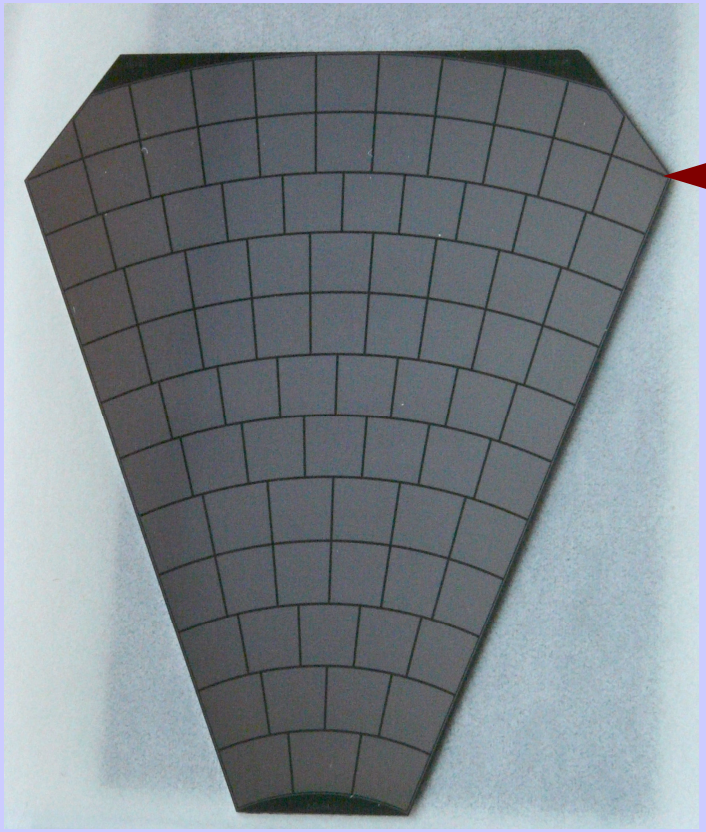
BeamCal sensors

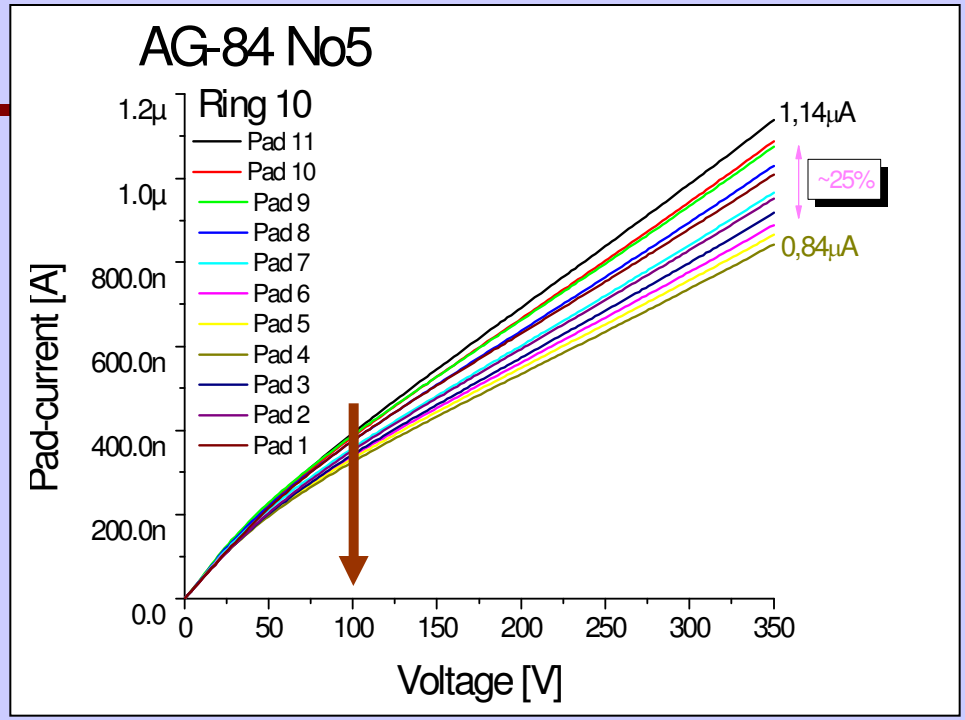
GaAs sensors, delivered by JINR

(produced in Tomsk, Sibirian Academy of Science)

500 μm thickness, 3 inch wafer, Au metallisation

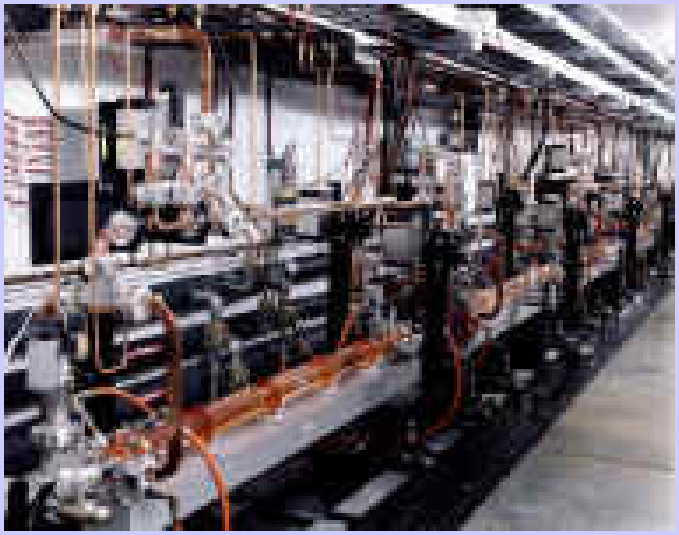
Probe station measurements





BeamCal sensors

Rad. Hard Silicon sensor tests at the NLCTA beam (150-200 MeV electrons)



SLAC and
UC Santa Cruz

SENSOR
DUMMY

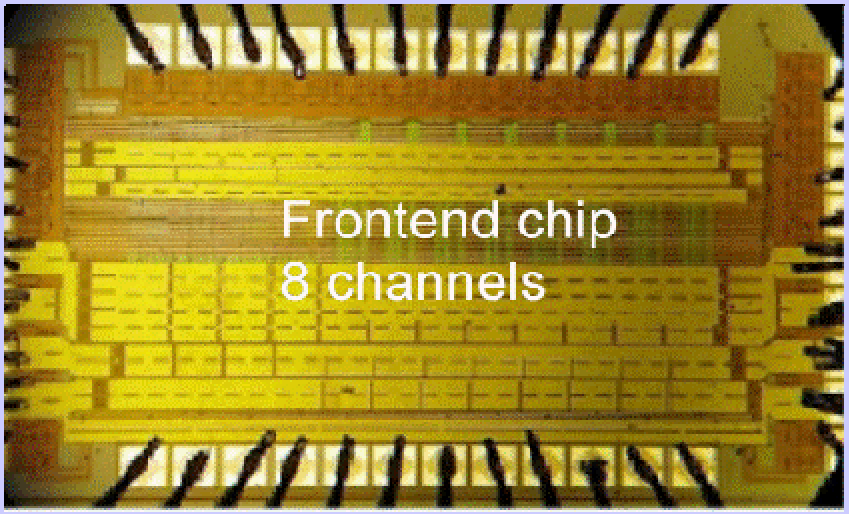
n- and p-type float-zone and magnetic Czochralski sensors

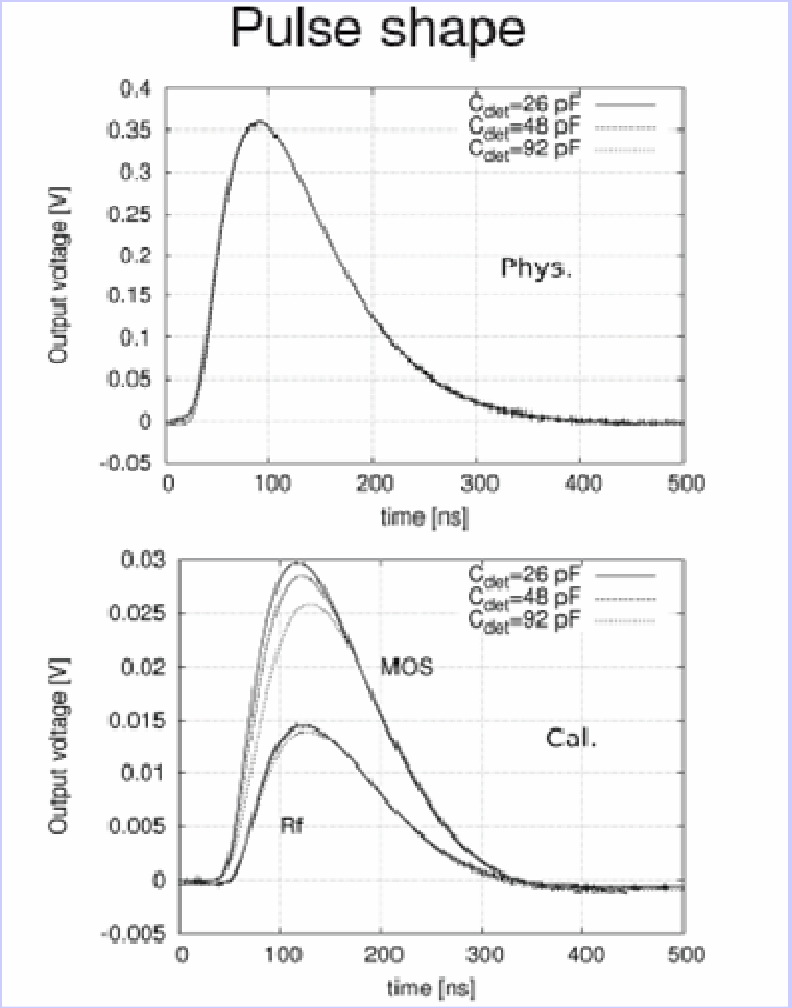
Create neutron flux by absorber

See also the talk by Bruce Schumm in the MDI session

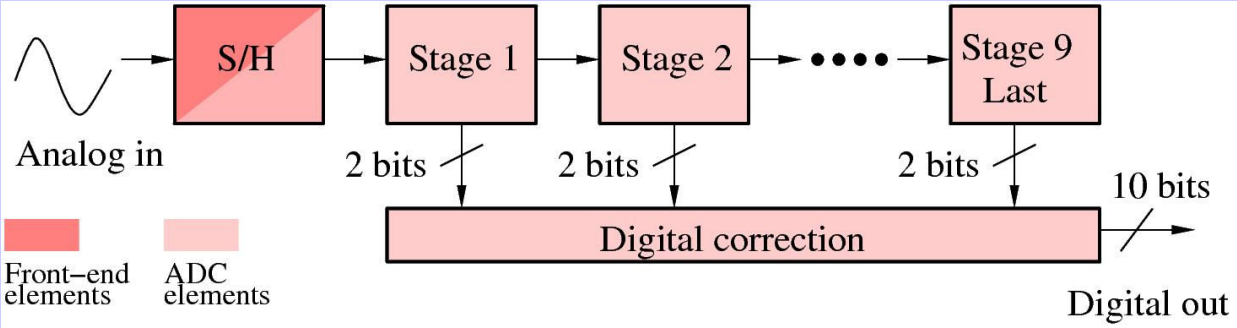
FE ASICs, LumiCal

- Frontend readout prototype chip developed at UST Cracow, manufactured in a MPW run (0.35 μm AMS)
- 8 channels, passive or MOS feedback
- Two amplification ranges (MIP and physics data taking)
- Measured in Cracow and Zeuthen:
  - Noise ≈ 300 e^- (+ 28 e^-/pF),
  - gain ≈ 20 mV/fC (calibration mode), 0.11 mV/fC (data taking)

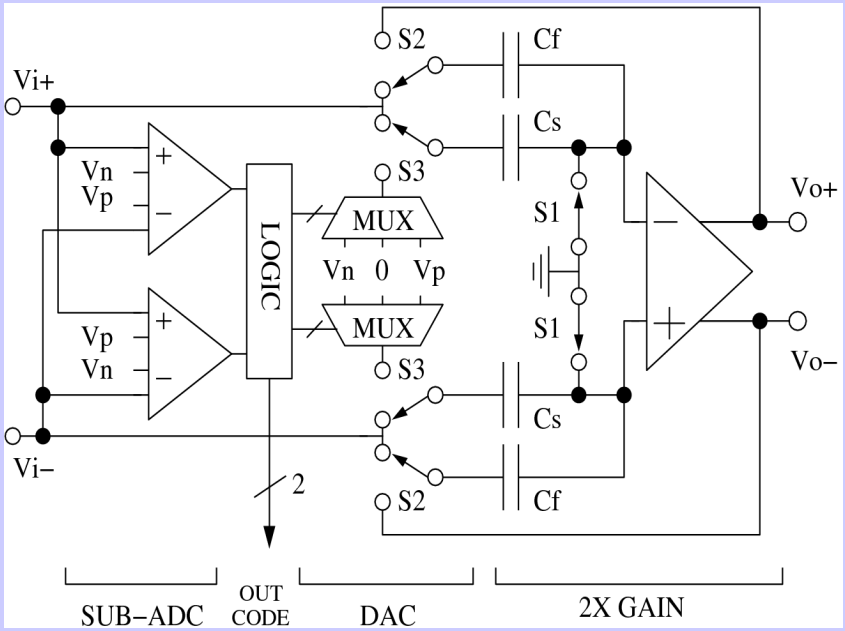




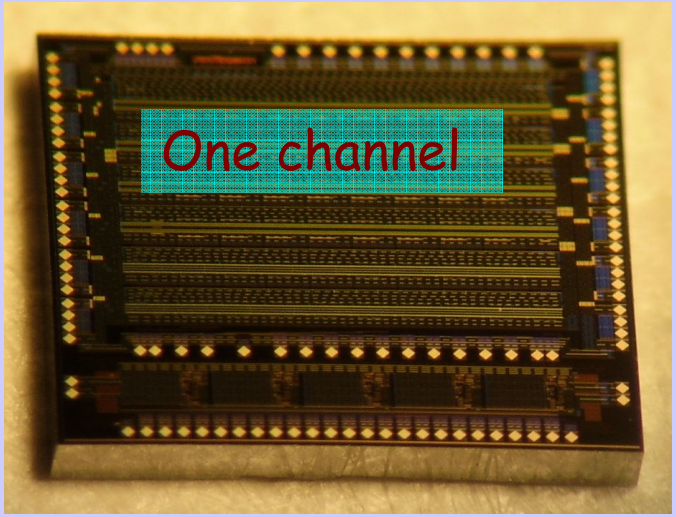
ADC ASICs, LumiCal

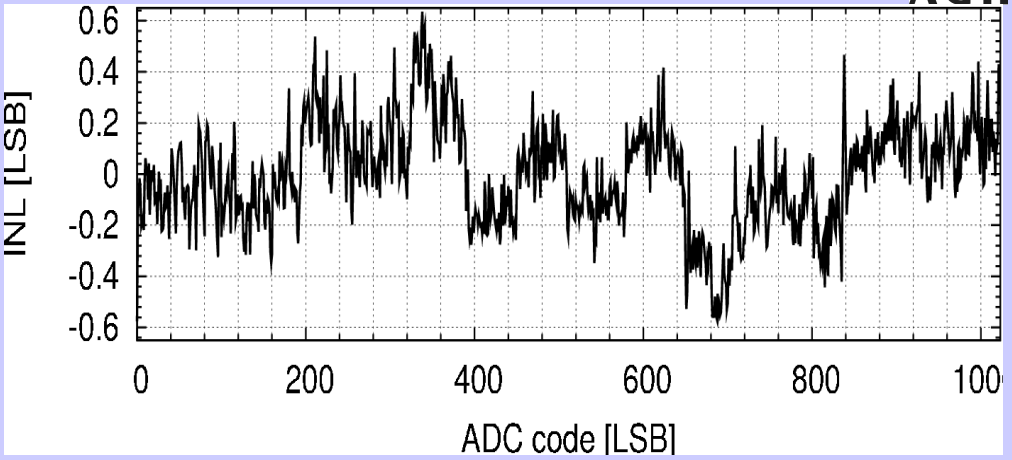


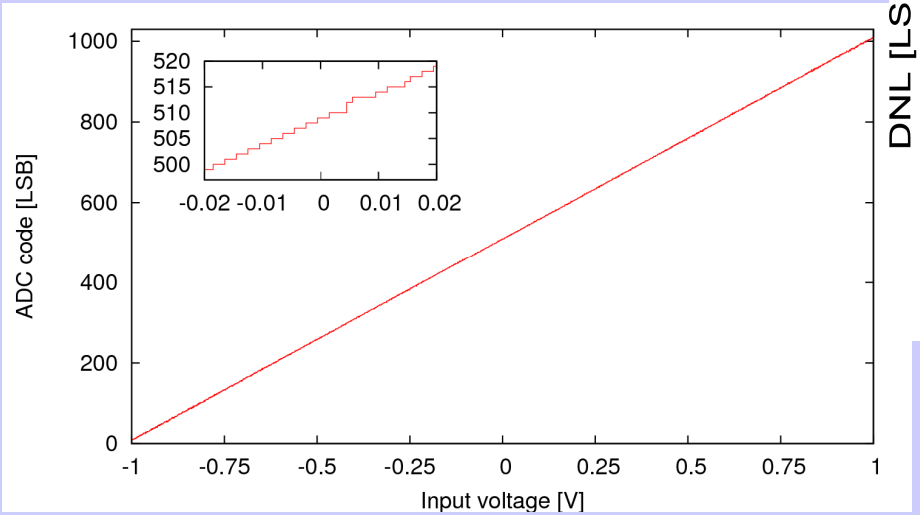
- 10 bit pipeline ADC 1.5 bit/stage
- Variable sampling frequency up to ~25 Ms/s
- Scalable power consumption
- Fully differential
- Power switching OFF/ON (ILC, CLIC beam timing)
- Present version in 0.35 μm AMS, finer pitch technology soon...

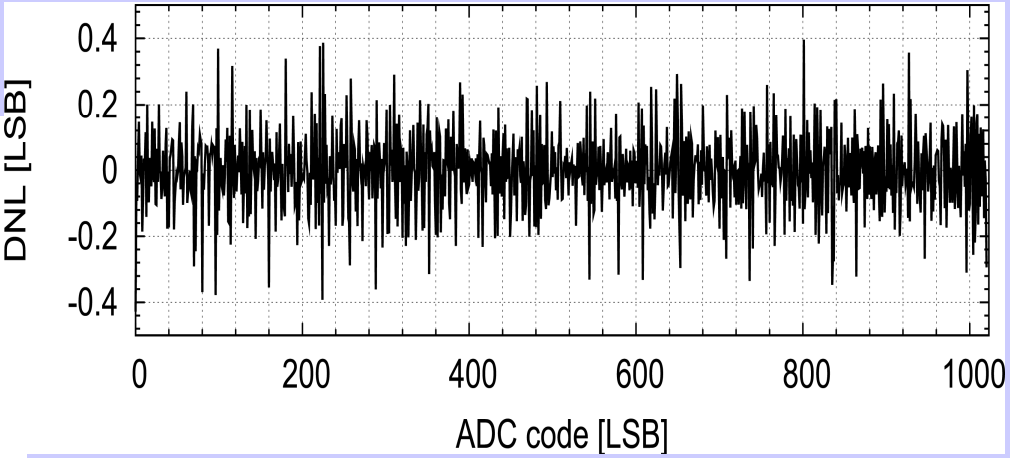


ADC ASIC, static measurements







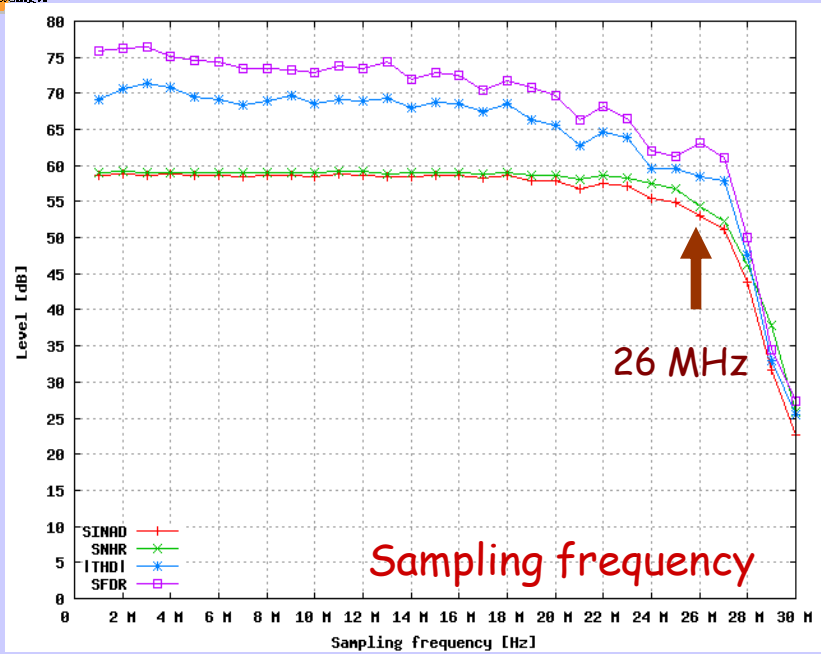


Very good linearity

INL < 0.61LSB, DNL < 0.5 LSB

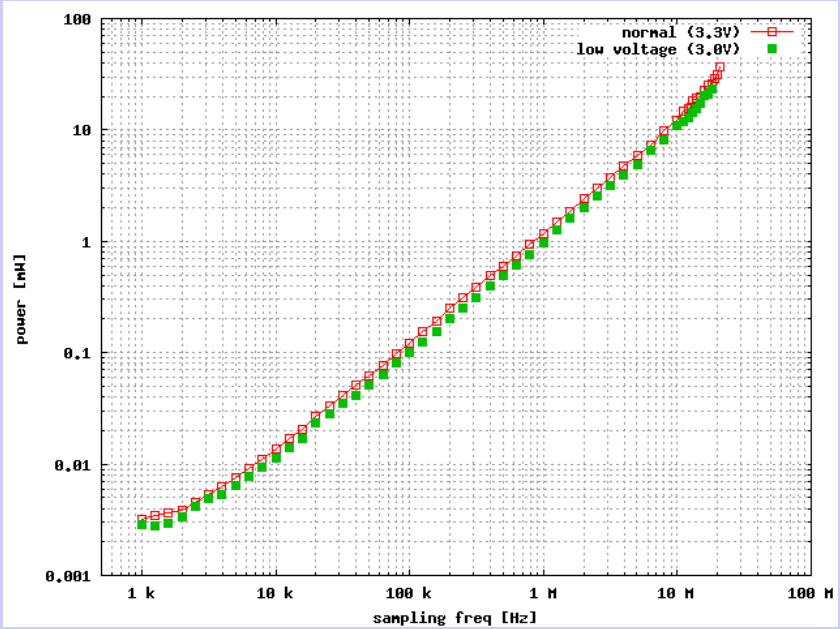
ADC ASIC, power consumption, switching

S/N



ADC dynamic measurements

Good dynamic performance ENOB
~ 9.5 bit



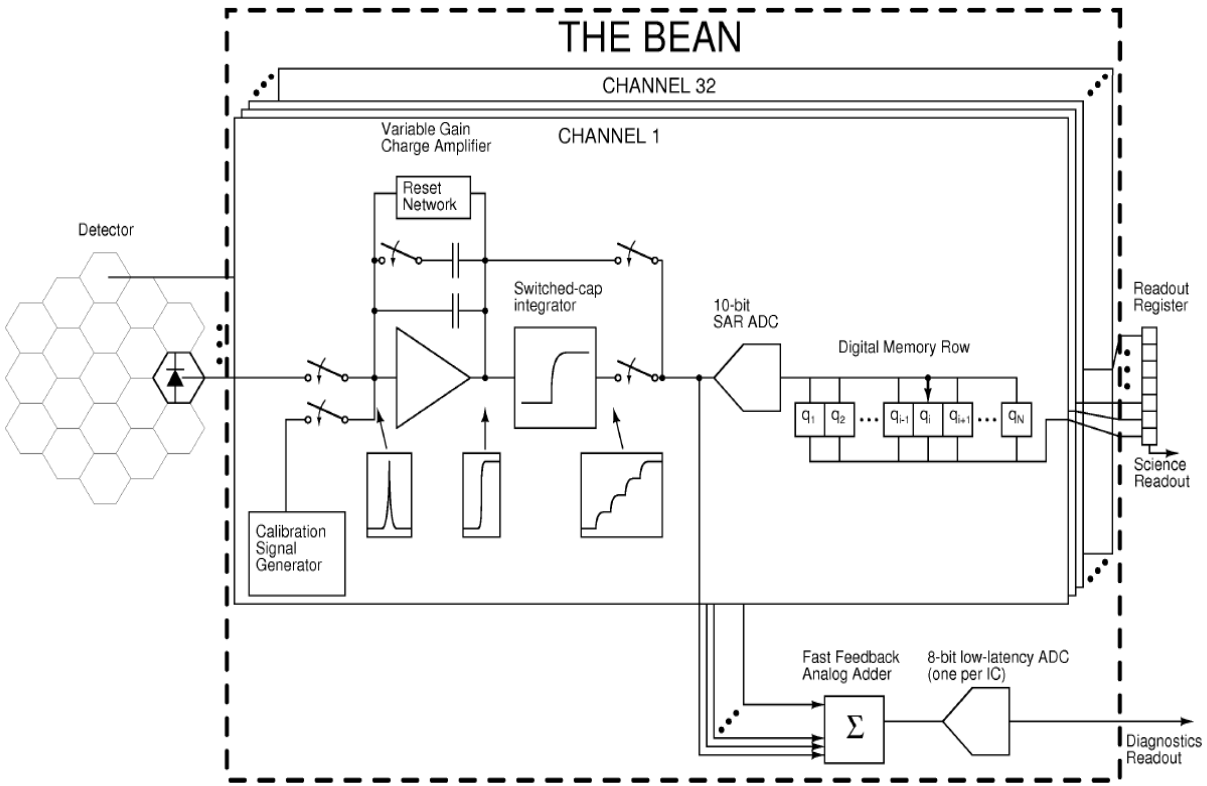
Power consumption is about 1-1.5 mW/MHz at worst case (Nyquist input frequency, including output buffers)

Power switching ON/OFF tested. Depending on sampling frequency 8-16 clocks needed to turn power ON

We have just submitted 8 channels ADC version layout with a pitch 200 µm per channel

FE ASICs, BeamCal

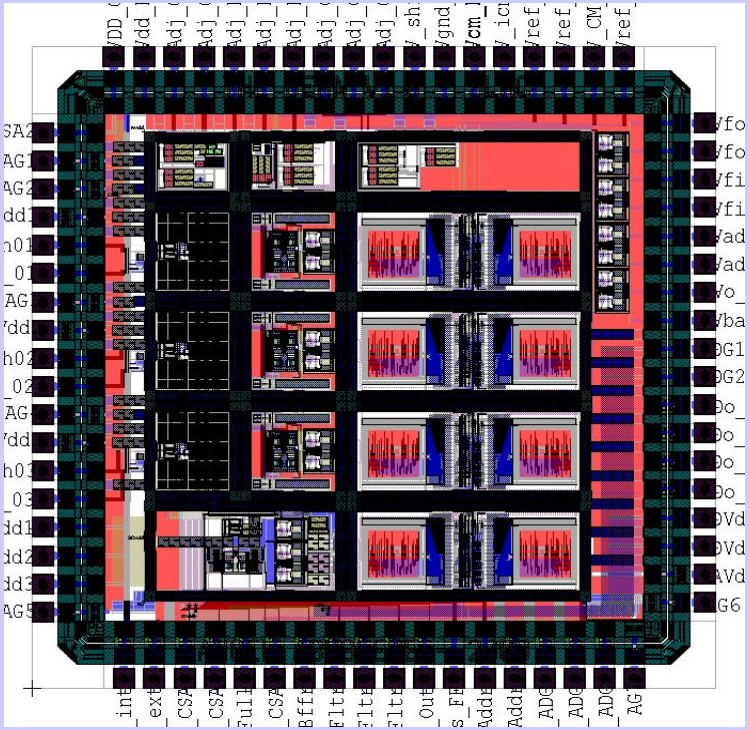
- "High" input rate (3.25 MHz)
- High occupancy (100%)
- Large input signals (~40pC)
- Large input capacitance (~40pF detector + wires)
- High resolution (10 bits)
- Dual gain (50x) for different modes of operation: science and detector calibration
- Low latency (~1us) output for beam diagnostics
- High radiation (1Mrad total dose)

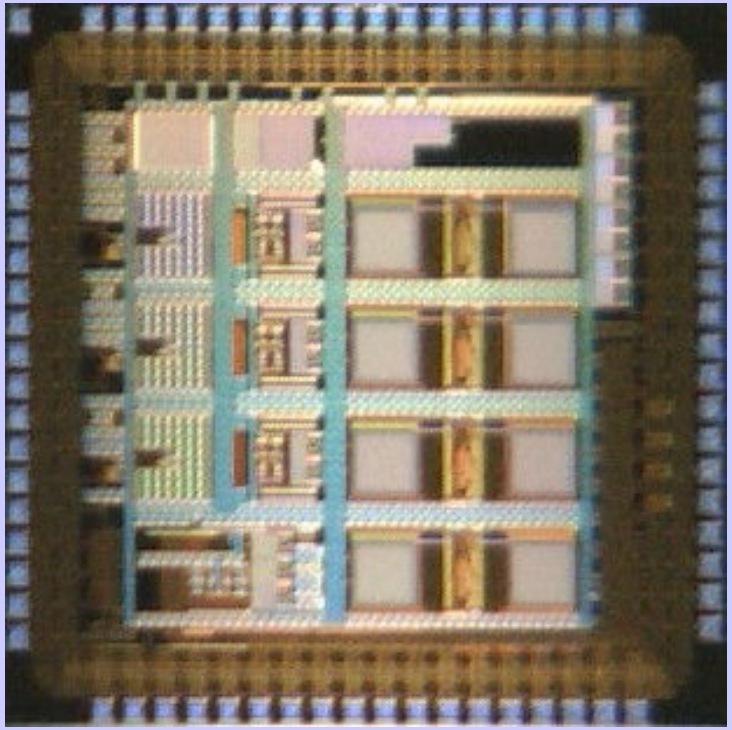


- Design at Stanford University (KPiX technology)
- readout between bunch trains
- prepared for fast feedback (diagnostics readout to machine)
- prototypes now available

See also the talk by Angel Abusleme in the MDI session

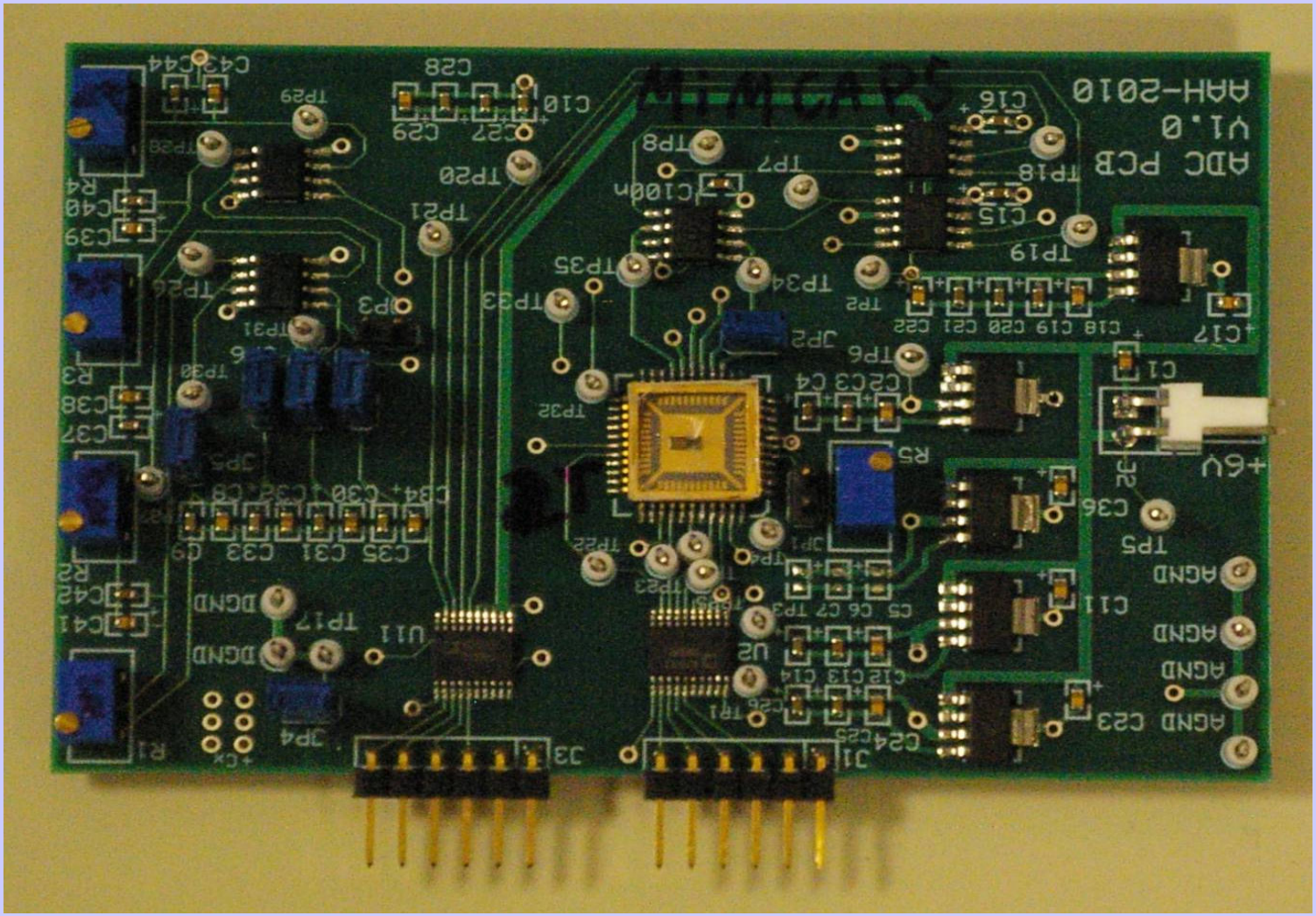
FE ASICs, BeamCal





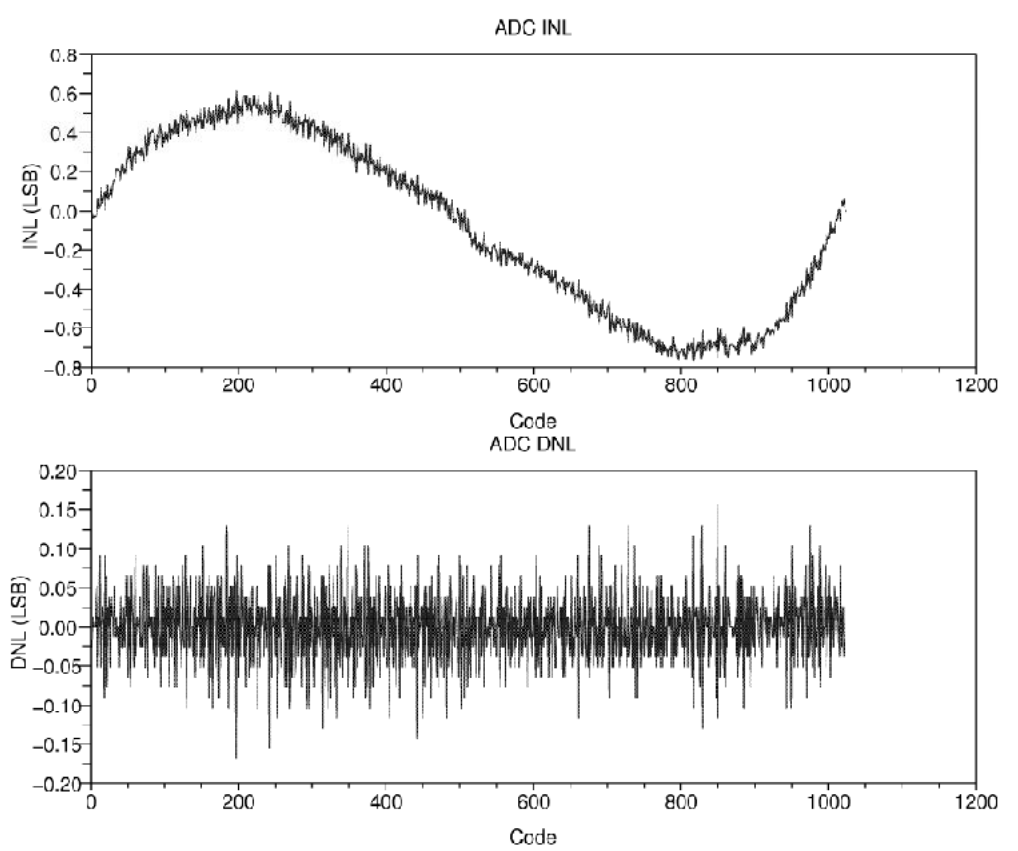
- TSMC 0.18um, 1.8V
- 72 pads, 2.4mm x 2.4mm (incl. pads)
- 7306 nodes, 35789 circuit elements
- 3 charge amplifiers, 4 x 10-bit, fully diff. SAR ADCs, 1 SC adder, 3 SC filters

ADC Test Board

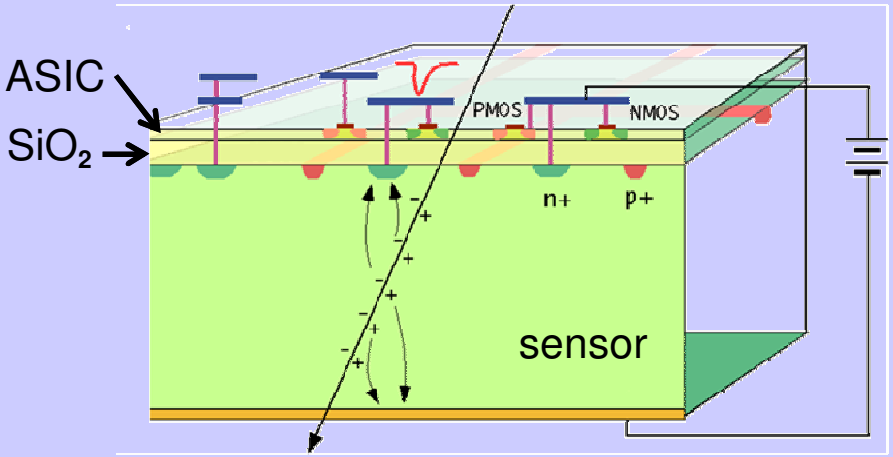


FE ASICs, BeamCal

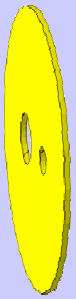
- MIMCaps (16-fF unit capacitance) ADC linearity results:
  - DNL is excellent, no missing codes
  - INL looks strange, but cause has been explained (copper dishing)
  - ADC meets noise and speed requirements



Pair Monitor



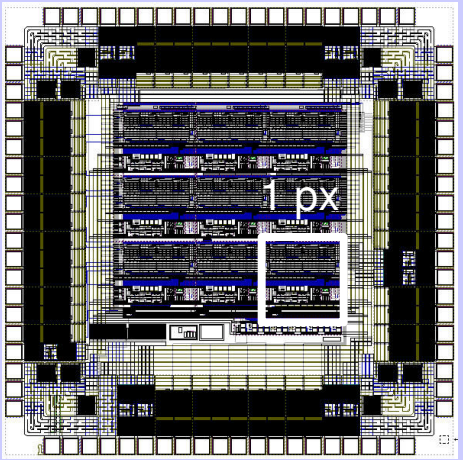
- Pixel size: 400 x 400 μm²
- Radius: 10 cm
- Total number of pixels: **~200,000**



→ Monolithic construction allows the elimination of the bump-bonding process.

- First step: design of a readout prototype ASIC for 3x3 pixels:
- digital readout (preamp, discriminator, counter)

- manufactured chip (CMOS 0.2 μm, SOI technology)
- performance measurements:
  - gain: ~ 17 mV/fC
  - noise: ~ 260 e^- (+ 130 e^-/pF) @ signals ~ 20000 e^-

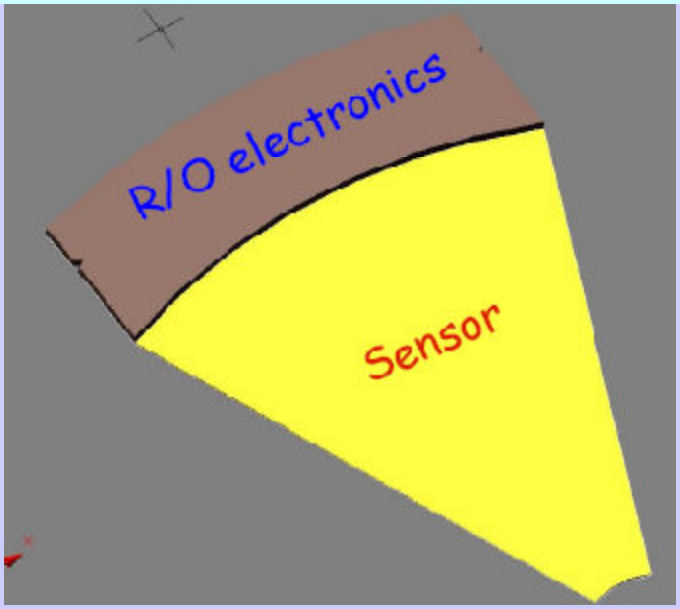


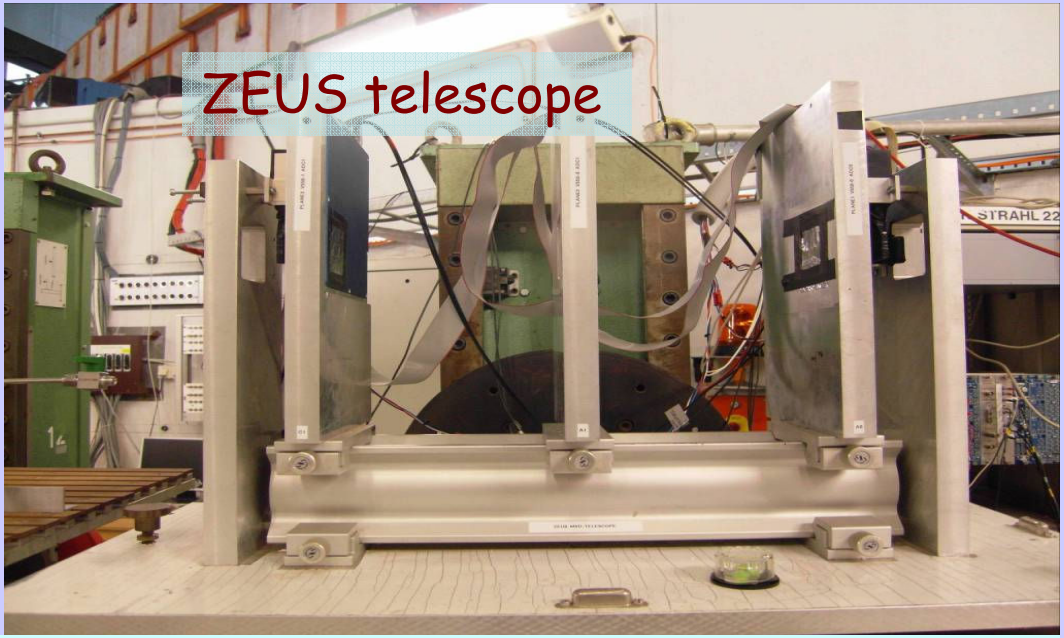
Next steps in FCAL R&D

Shortterm (2012):

Full assembly of a Prototype Sector

- Sensors and ASICs connection (Cracow, DESY, help from other labs)
- DAQ (+Tel Aviv)
- Preparation of a Beamtest in Summer at DESY





- intense simulation effort to understand signal and background in LumiCal and BeamCal at 3 TeV for the CLIC detector CDR April 2011

Midterm (>2012):

FP7 application (AIDA)

- Infrastructure to allow 'Physics studies" after 2012
- Cracow (2x), DESY, Tel Aviv (from EUDET)
  + VINCA and IFIN-HH (associats)

FP7 Partners:

AGH-UST Cracow (Marek Idzik)
CERN Geneva (Lucie Linssen)
DESY Zeuthen (W. Lohmann)
IFJPAN Cracow (L. Zawiejski)
TAU Tel Aviv (H. Abramowicz)

FCAL Specific infrastructure:

- Flexible, high precision tungsten structure
- Fast FE Readout
- Module construction and test devices (jigs, mechanics and electronics test facilities)
- Position control devices