



Pixel readout for a TPC

LCWS 2010 – Tracking TPC R&D session
27 March 2010

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On behalf of the Bonn/CERN/Freiburg/Nikhef/Saclay groups

Full post-processing of a TimePix

· Timepix chip + SiProt + Ingrid:

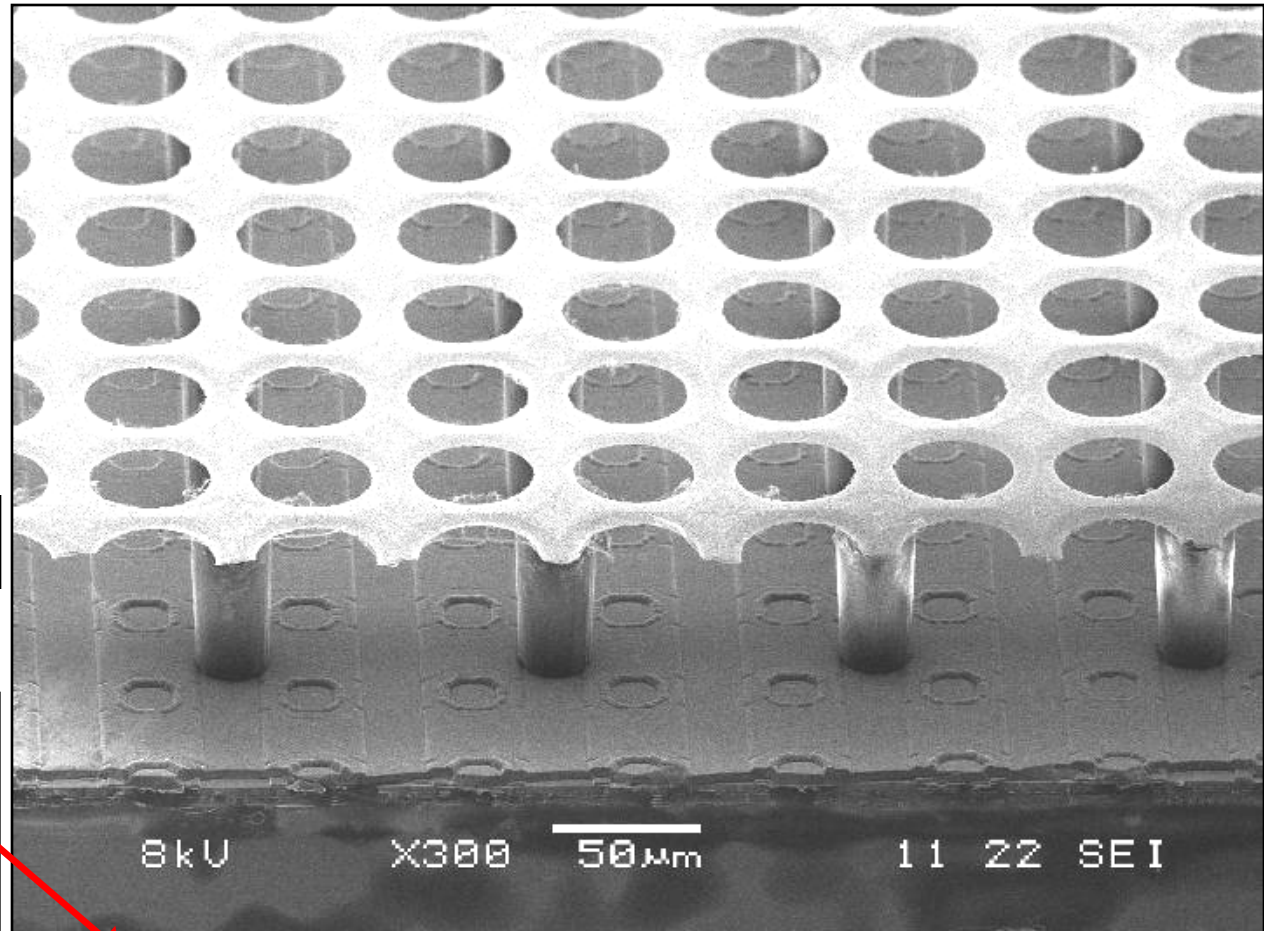
Timepix chip:

- 256x256 pixels
- pixel: $55 \times 55 \mu\text{m}^2$
- active surface: $14 \times 14 \text{ mm}^2$

MESA+: Ingrid

IMT Neuchatel:

15 or 20 μm highly resistive aSi:H protection layer

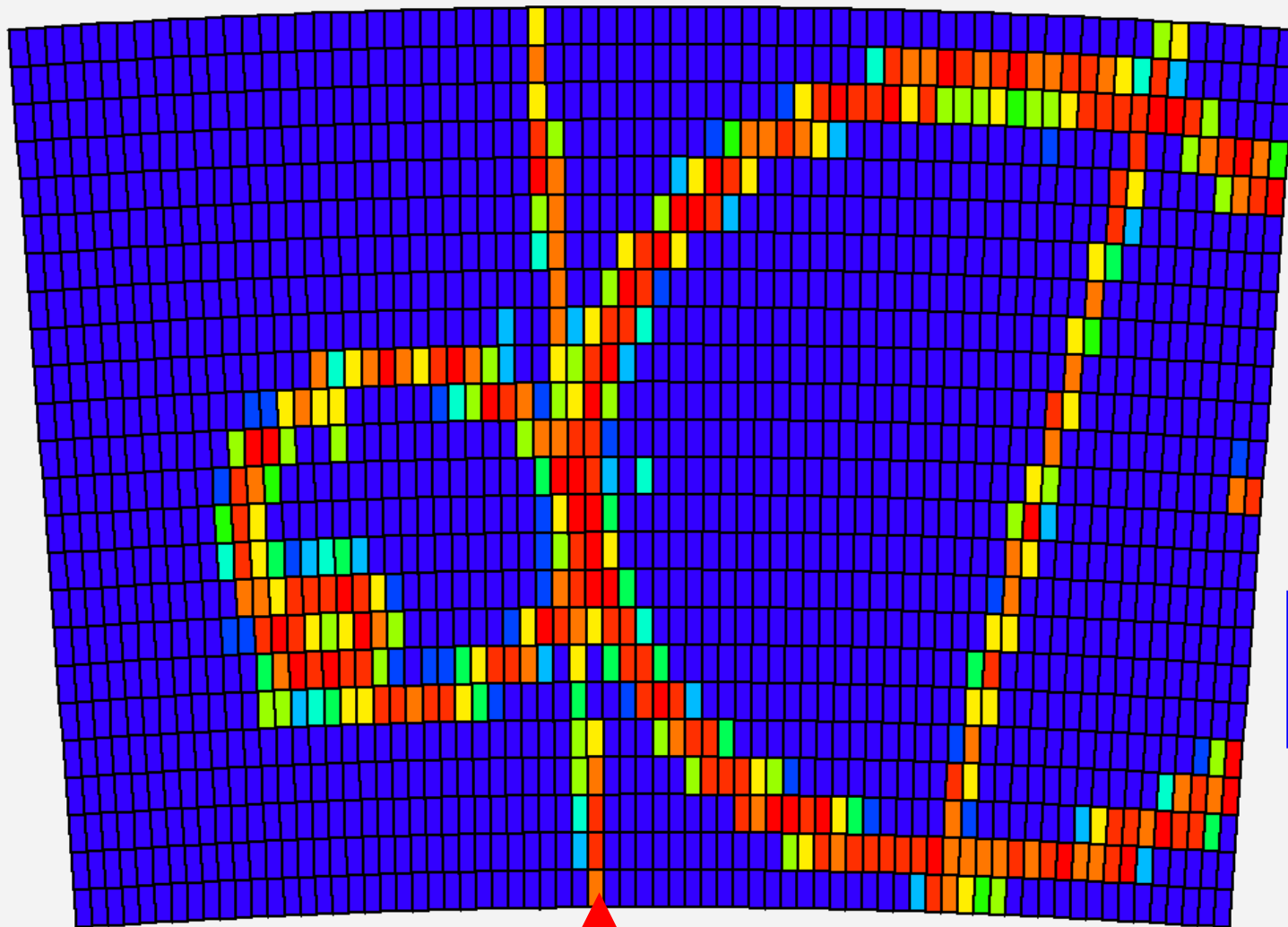


Now also Si_3N_4 protection layers ($7 \mu\text{m}_2$)

Pad readout vs. Pixel readout

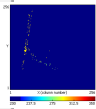
- Pad size $\sim 1 \times 5 \text{ mm}^2$ or $\sim 3 \times 7 \text{ mm}^2$
 - Timepix pixel size $55 \times 55 (\mu\text{m})^2$
 - Pad TPC $\sim 10^6$ pads; several 10^9 3D-voxels
 - CMOS pixel readout $\sim 2 \cdot 10^9$ 'pads' (but 'only' $\sim 4 \cdot 10^4$ chips); $\sim 10^{12}$ 3D voxels
- # pads/pixels might be problem for software,
but occupancy rather low

72x24 pads of $\sim 3 \times 7 \text{ mm}^2$

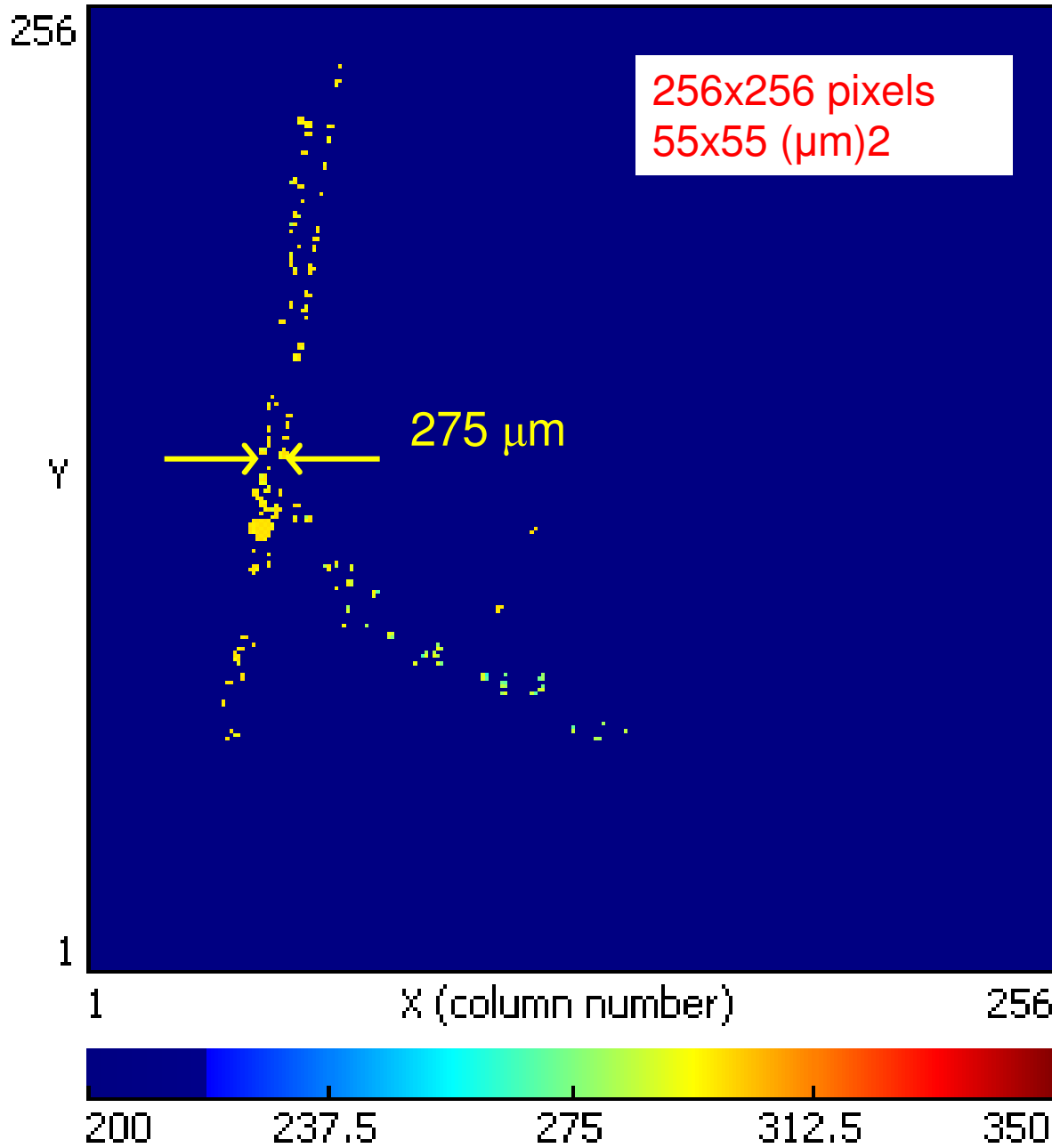


$B = 1 \text{ T}$

TimePix chip
 $14 \times 14 \text{ mm}^2$



5 GeV e^- beam



Two-track separation:

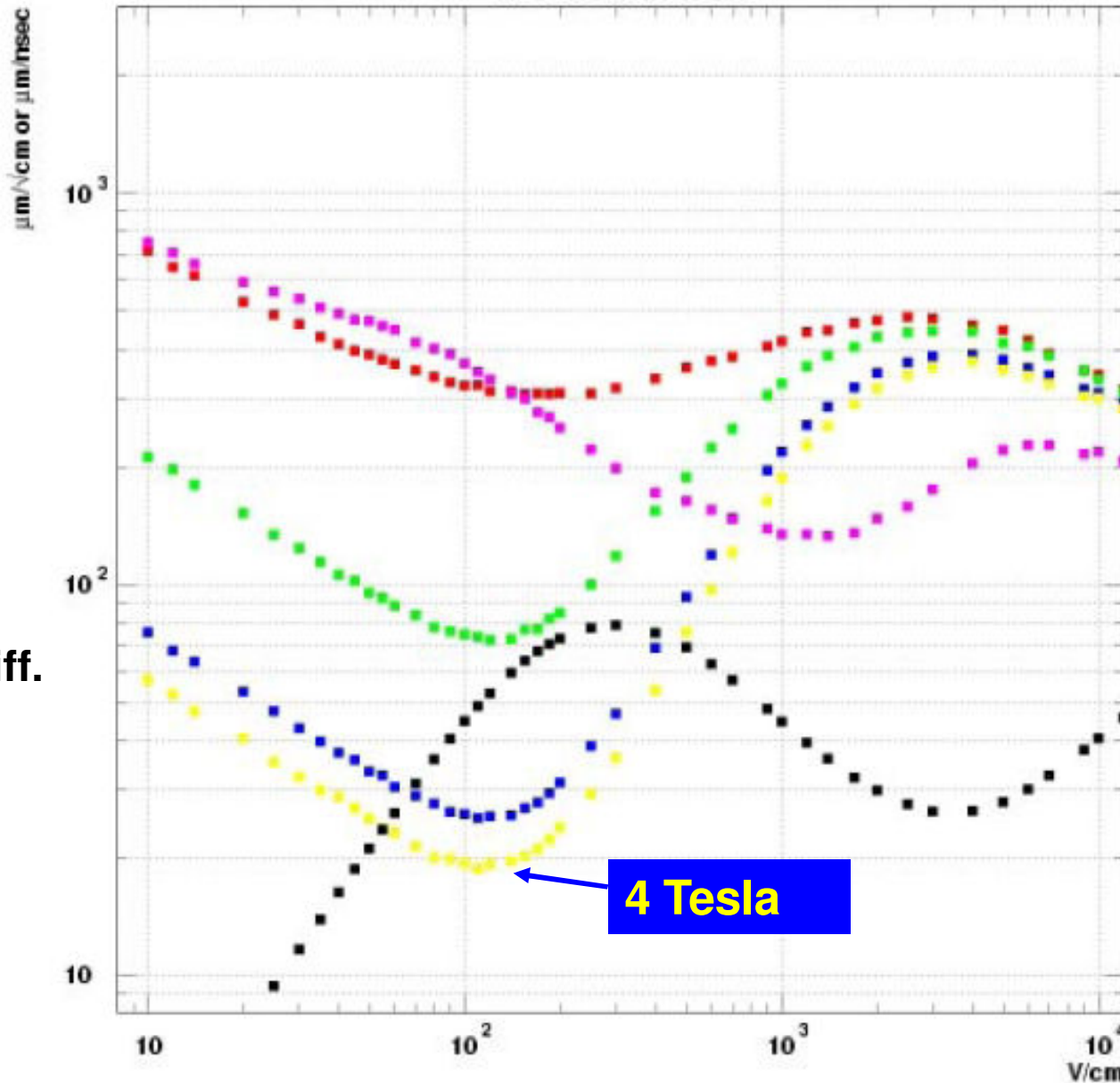
- Will be diffusion limited
- In this example:
5 pixels = 275 μm

Diffusion at 4T in
Ar/CF₄/iC₄H₁₀ is
 $\sim 20\sqrt{200} = 300 \mu\text{m}$

Longitudinal Diffusion
Drift Velocity

Transverse Diffusion 0T
Transverse Diffusion 1T
Transverse Diffusion 3T
Transverse Diffusion 4T

Ar-CF4-iC4H10_95-3-2



Long. Diff.

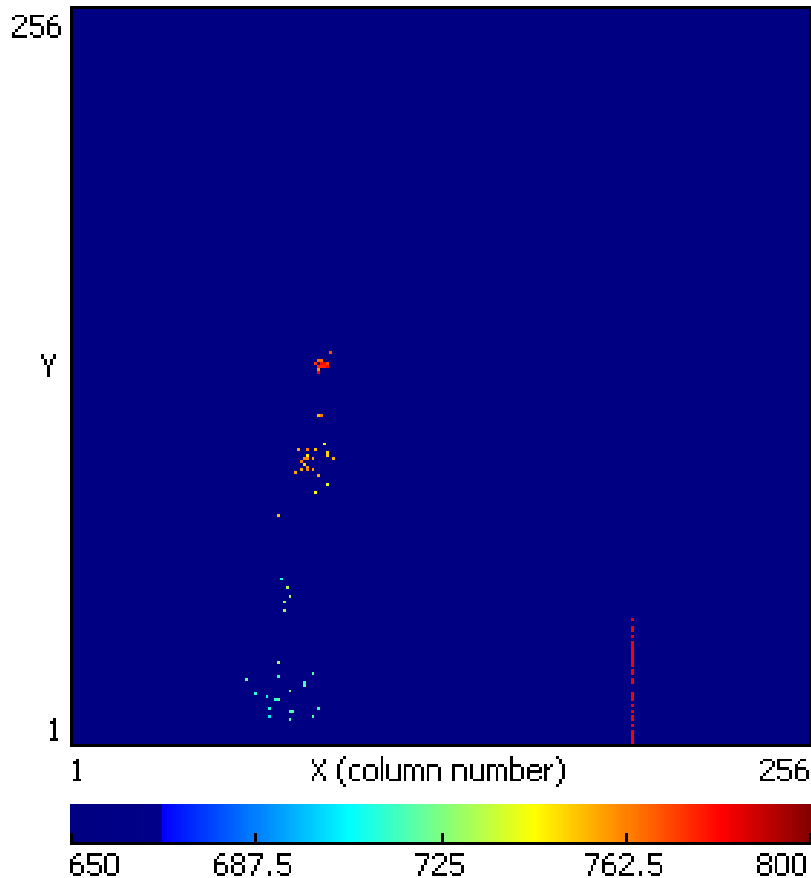
Transv. Diff.

Drift vel.

4 Tesla

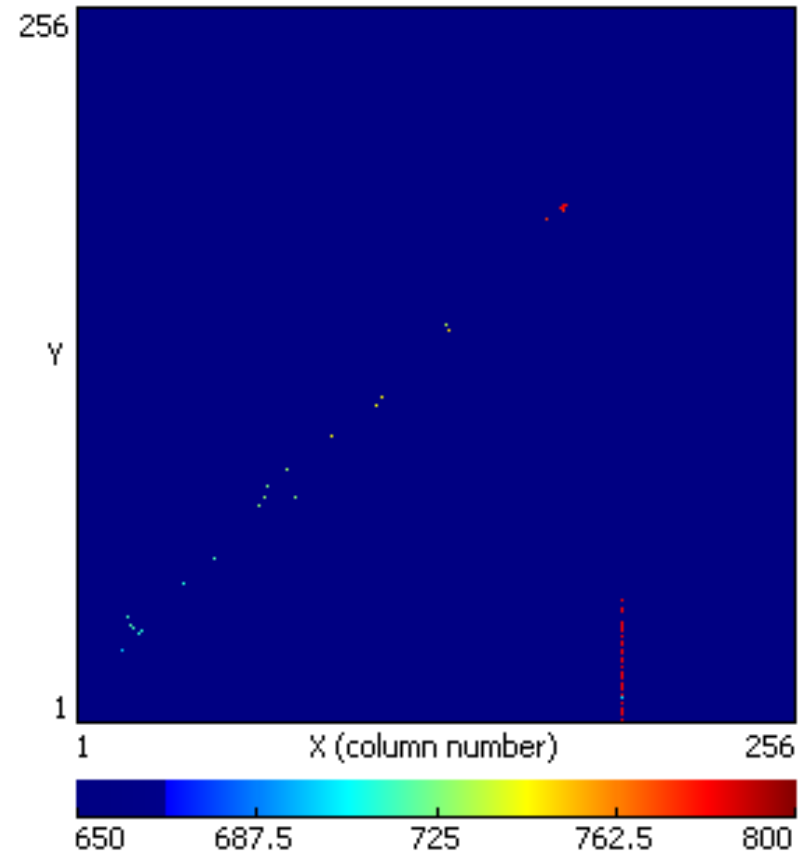
Cosmic tracks traversing ~ 30 mm drift space
Ingrid and Ar-CF₄-iC₄H₁₀ (95/3/2%)

0 T



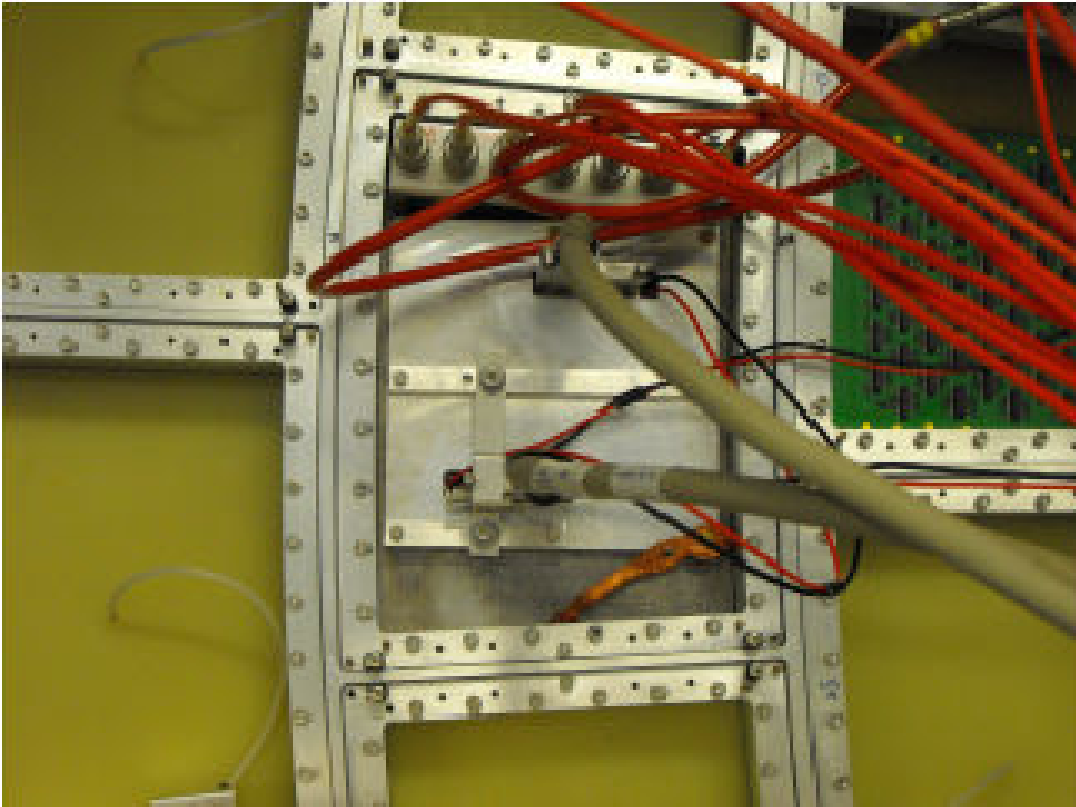
“large” diffusion

1 T

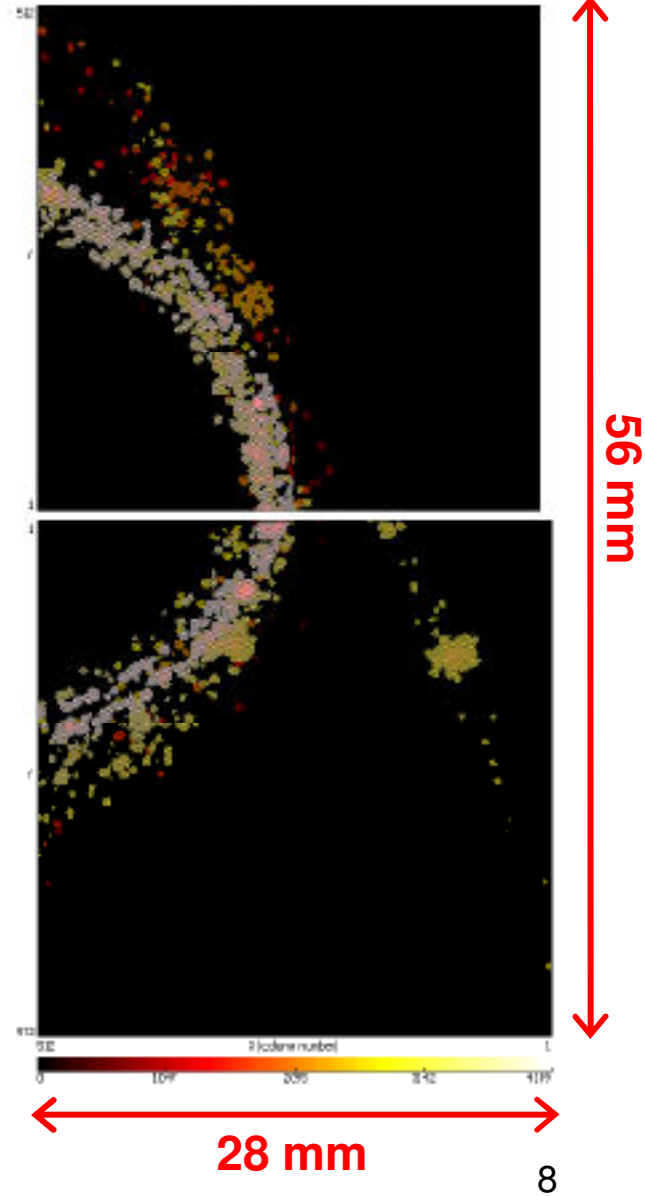


“little” diffusion

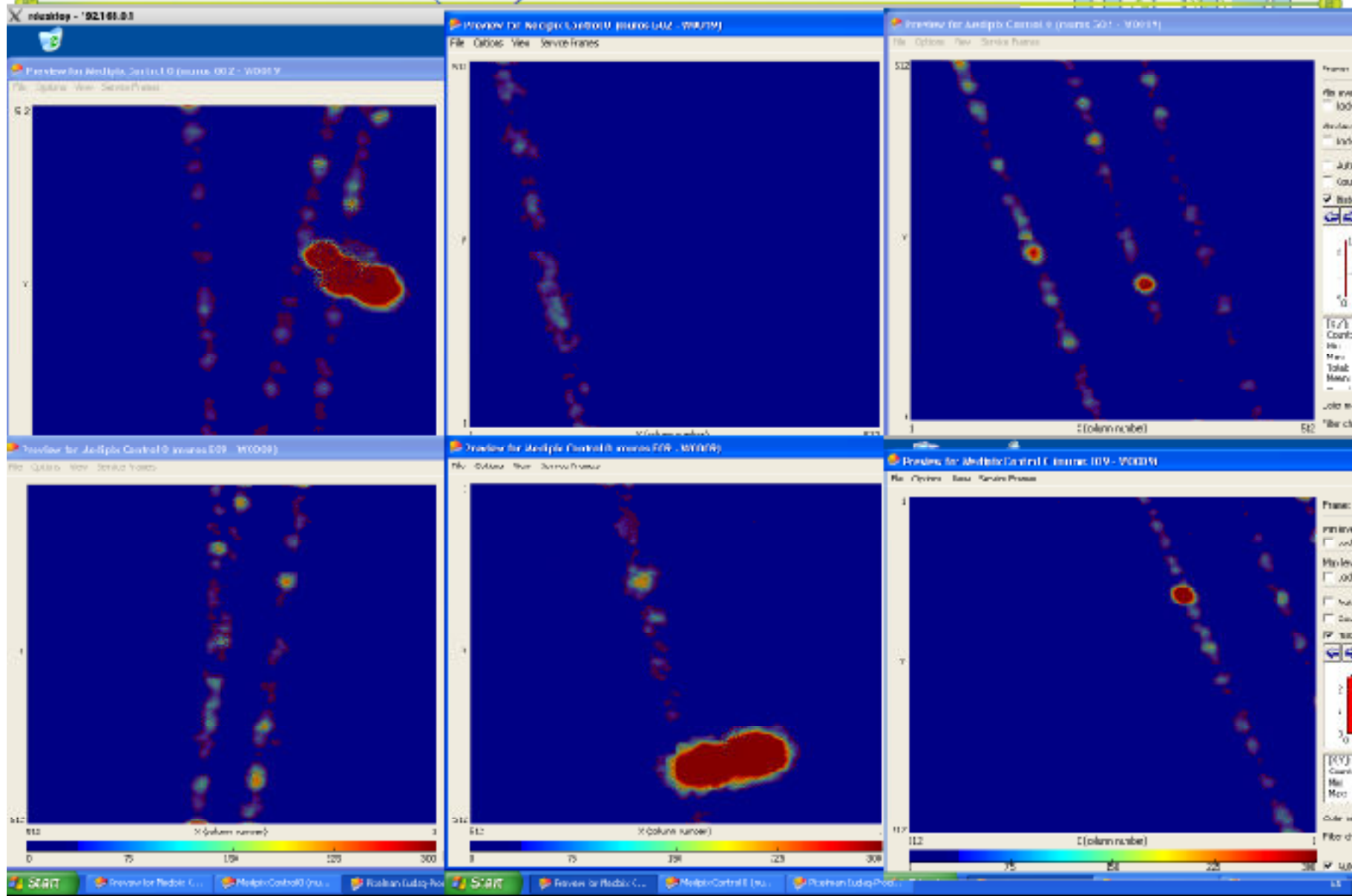
Triple-GEM module with readout by 8 Timepix chips: 16 cm² active area, 0.5M channels



Bonn/Freiburg



Some Pictures (III)

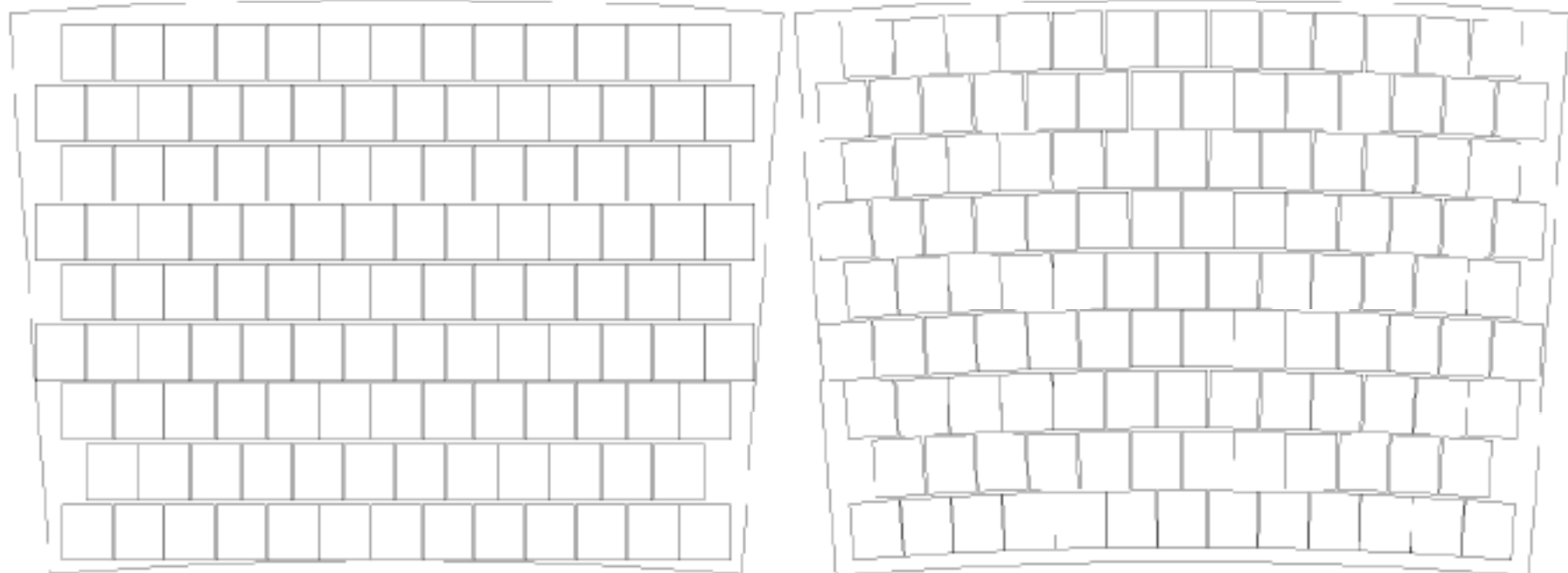


'Long-term' plans (end 2010)



LP1 module covered completely with Timepix modules

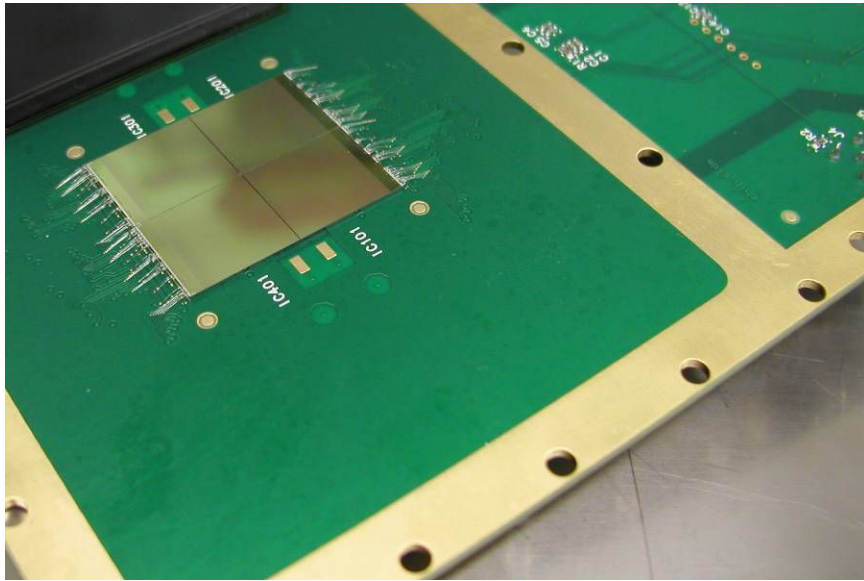
First ideas: 119 Timepix chips (more than 1 wafer, $\approx 7.8 \cdot 10^6$ channels)



Gas amplification: triple GEM, possibly also InGrids

Readout electronics: 'Scalable Readout System' developed
at CERN in the framework of RD-51

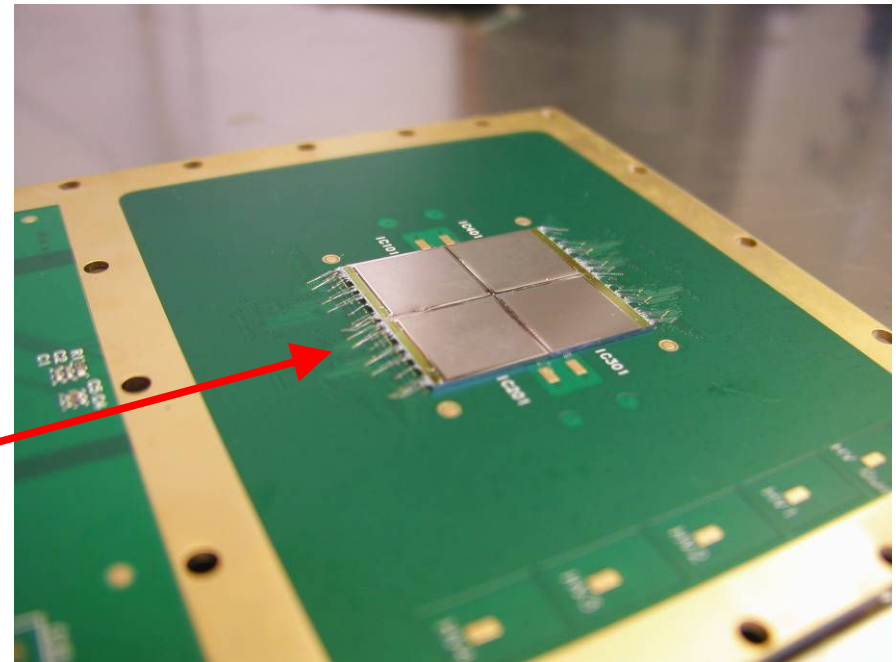
NIKHEF: emphasis on Ingrids



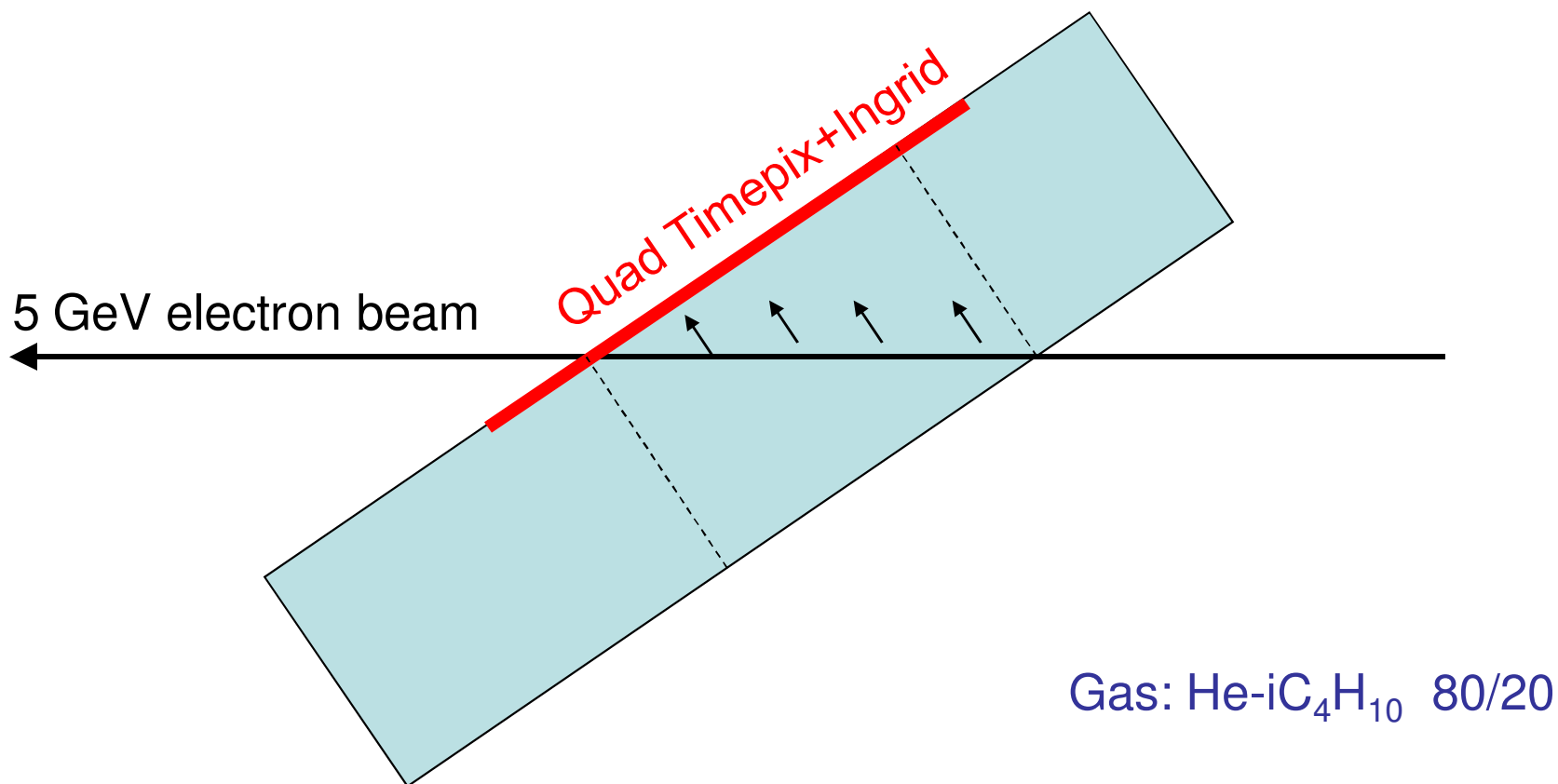
- within Relaxd project: 4x4 Medipix chips in compact mounting
- Will evolve in 8x8 Timepix chips for EUDET

- QUAD chips board tested OK in 2008
- Equiped with Ingrids in June '09
- Works with source and cosmics at NIKHEF in Nov'09 – Feb'10

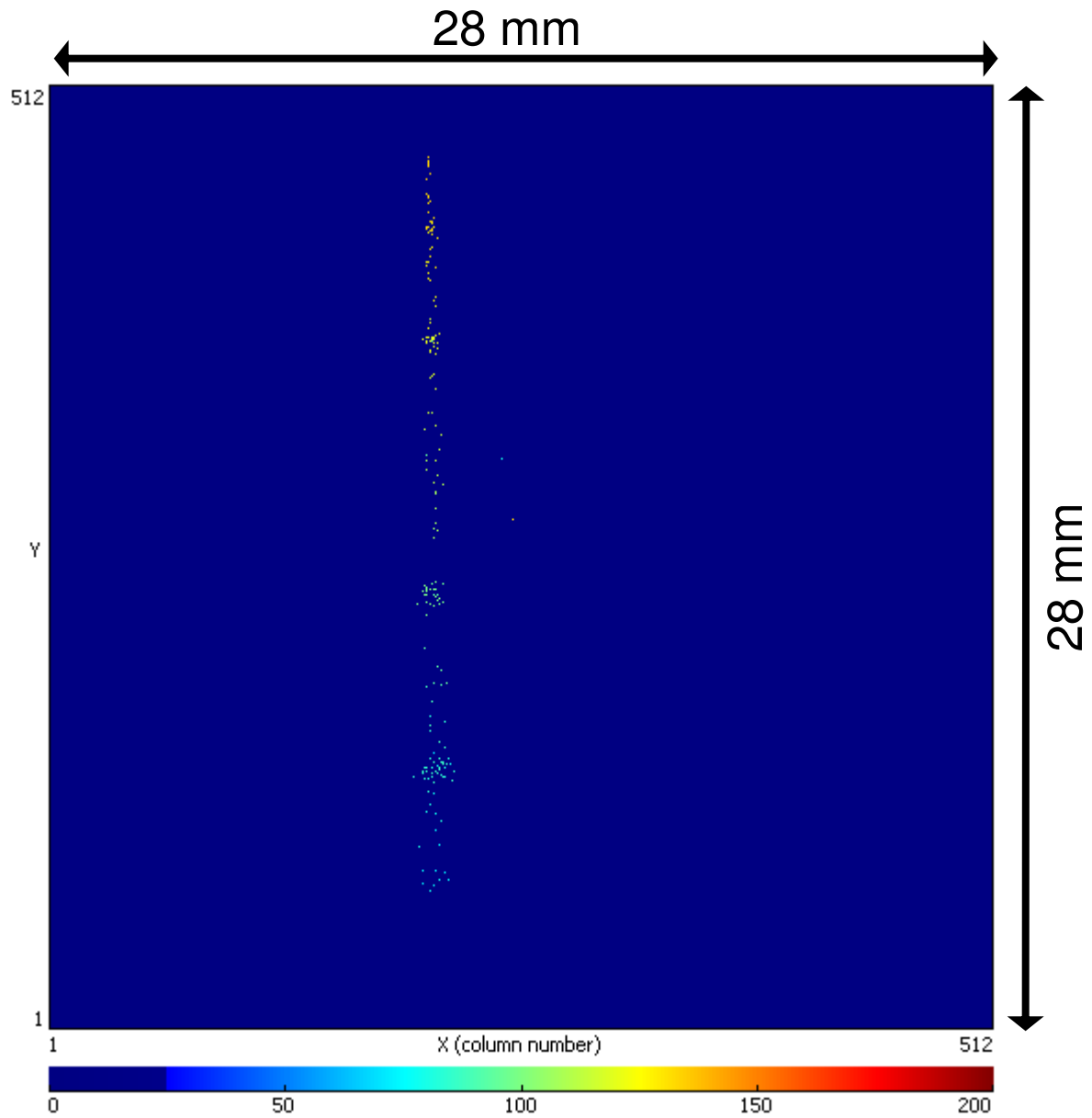
- Readout does NOT work at DESY (testbeam) in Dec'09 and Mar'10, except for 3 days in March'10



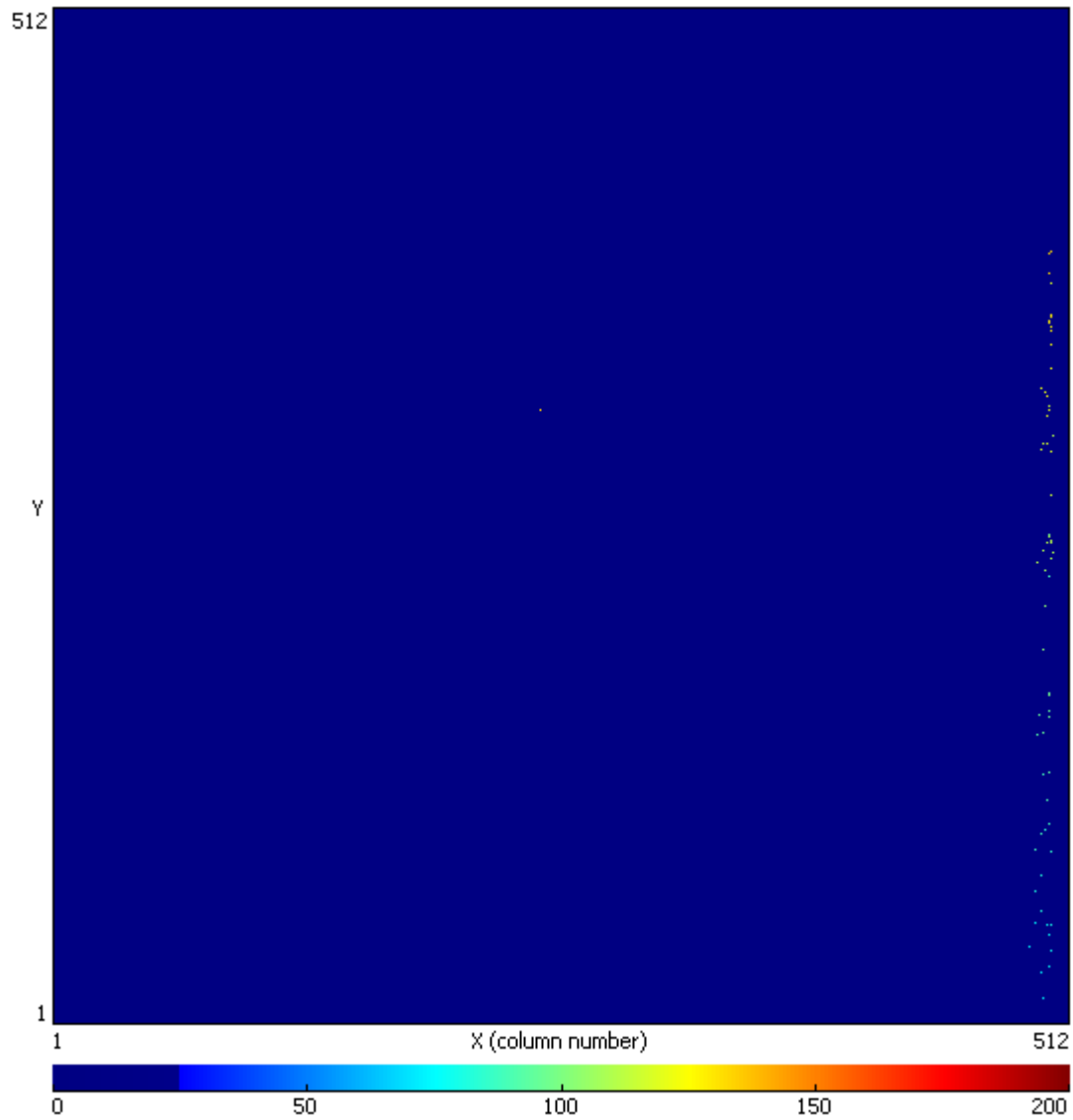
Few tracks from ~3-day test at DESY with quad-Ingrid detector



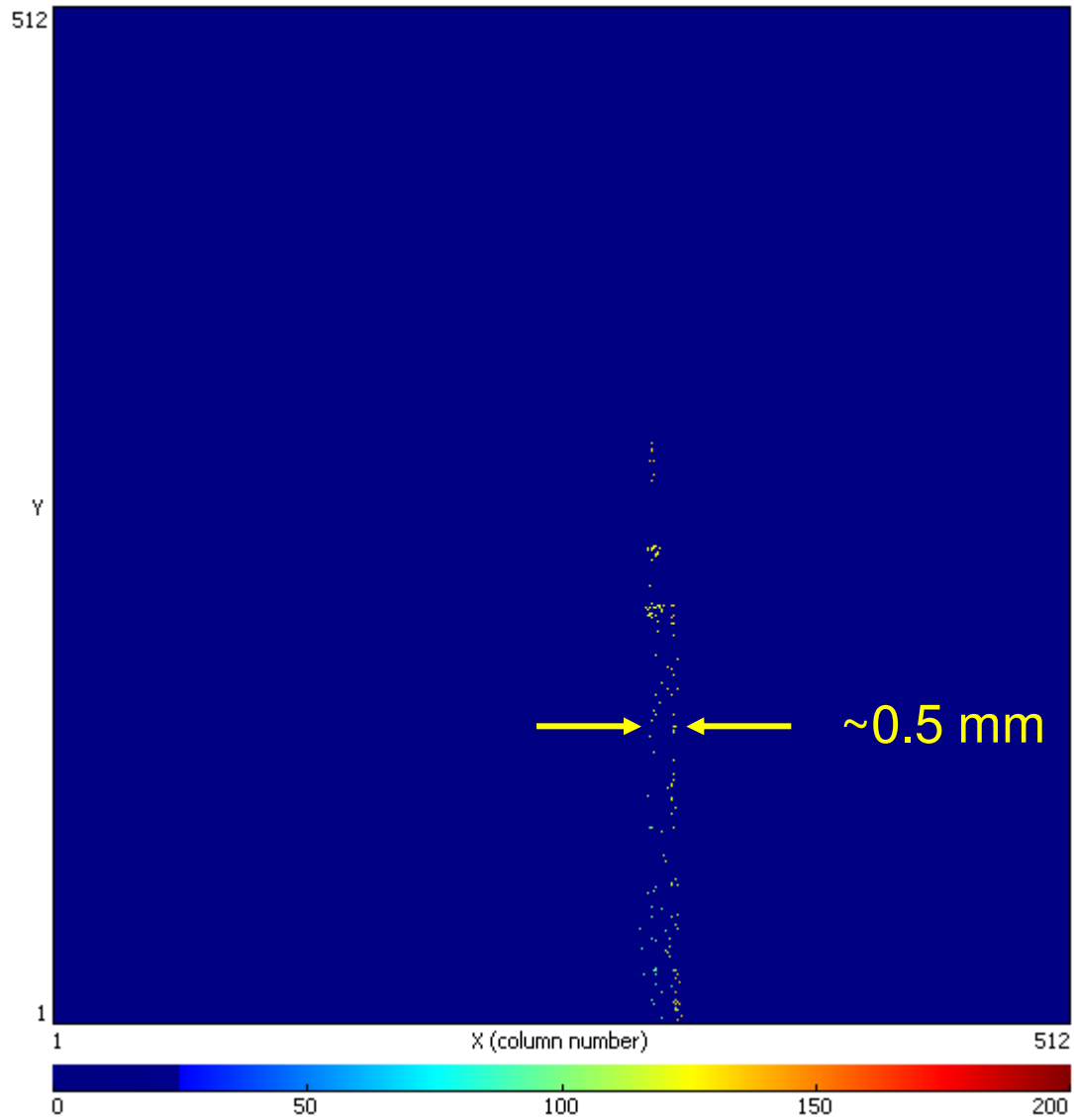
A normal track



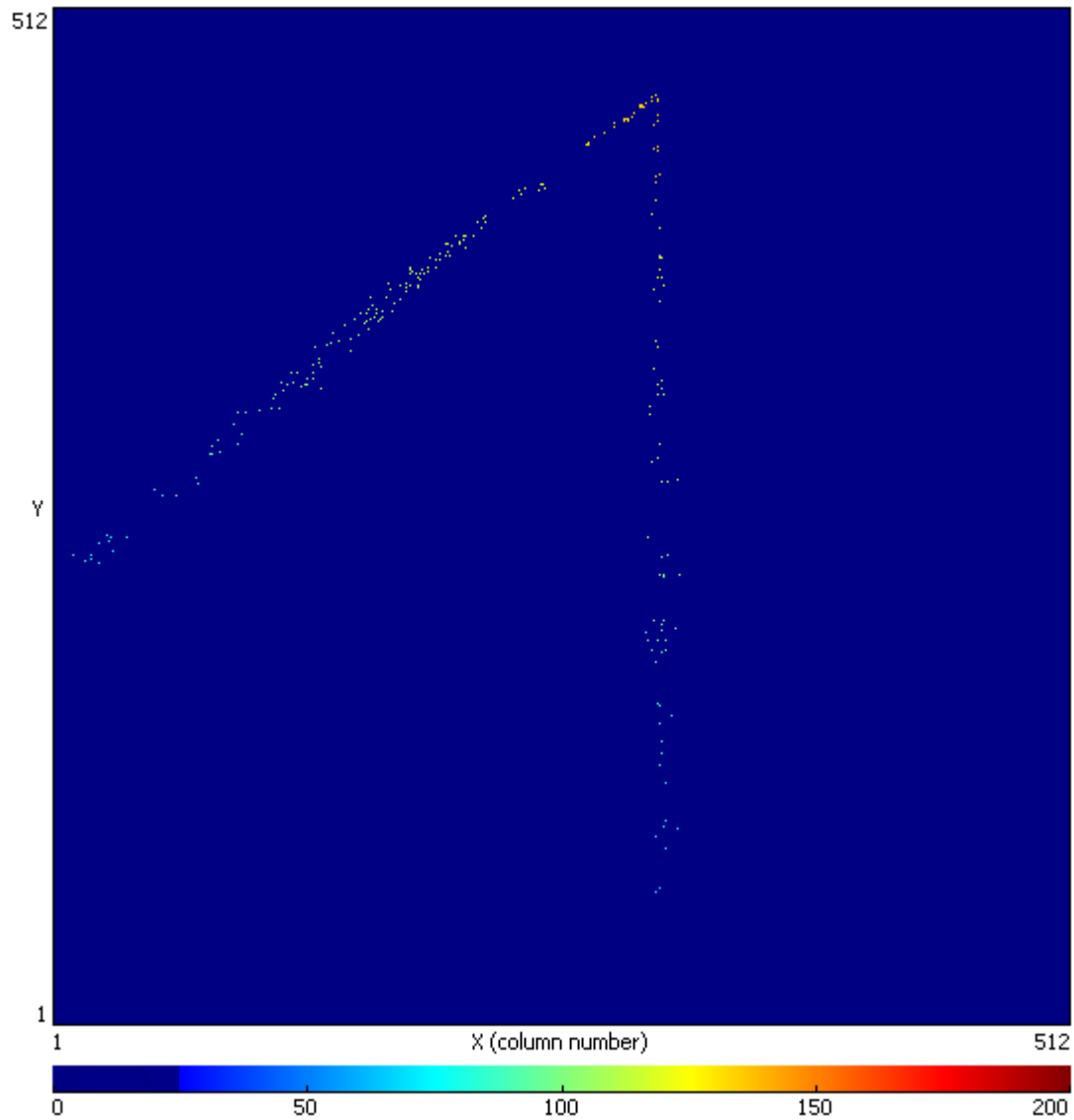
Track very close to border; there is 0.5mm 'dyke'



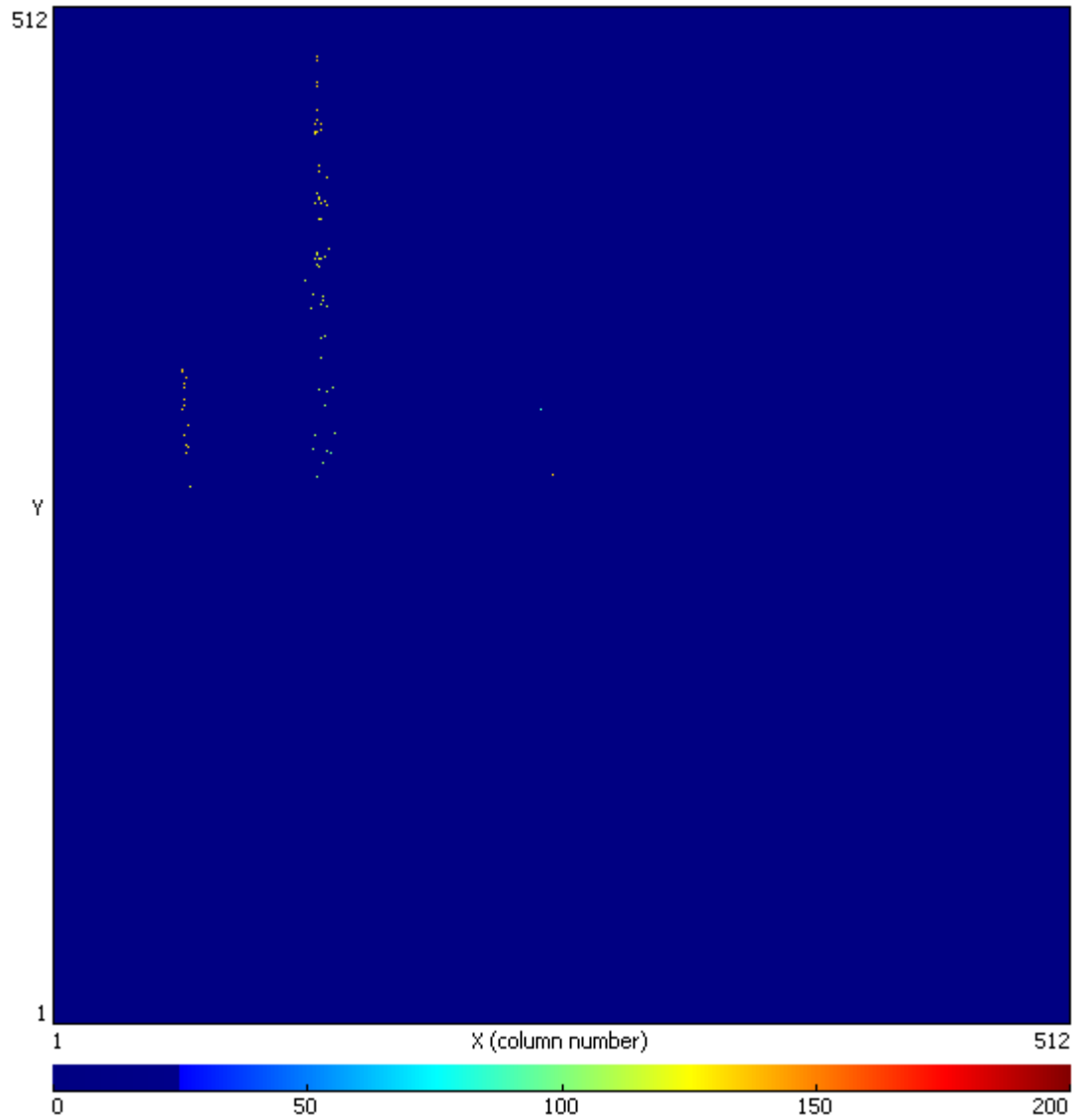
Two tracks about 0.5 mm apart in x



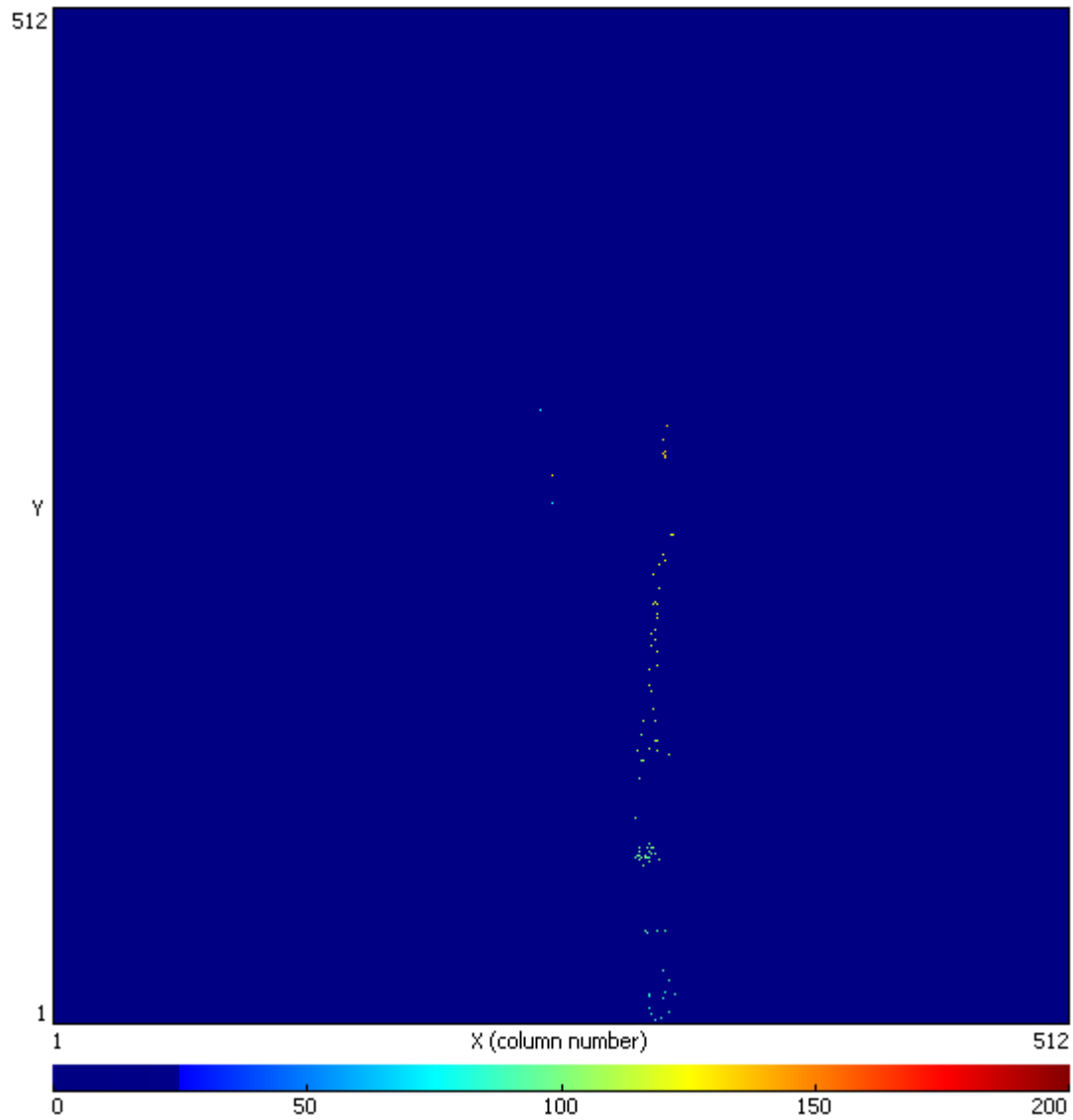
Track backscattering from chip (=anode)



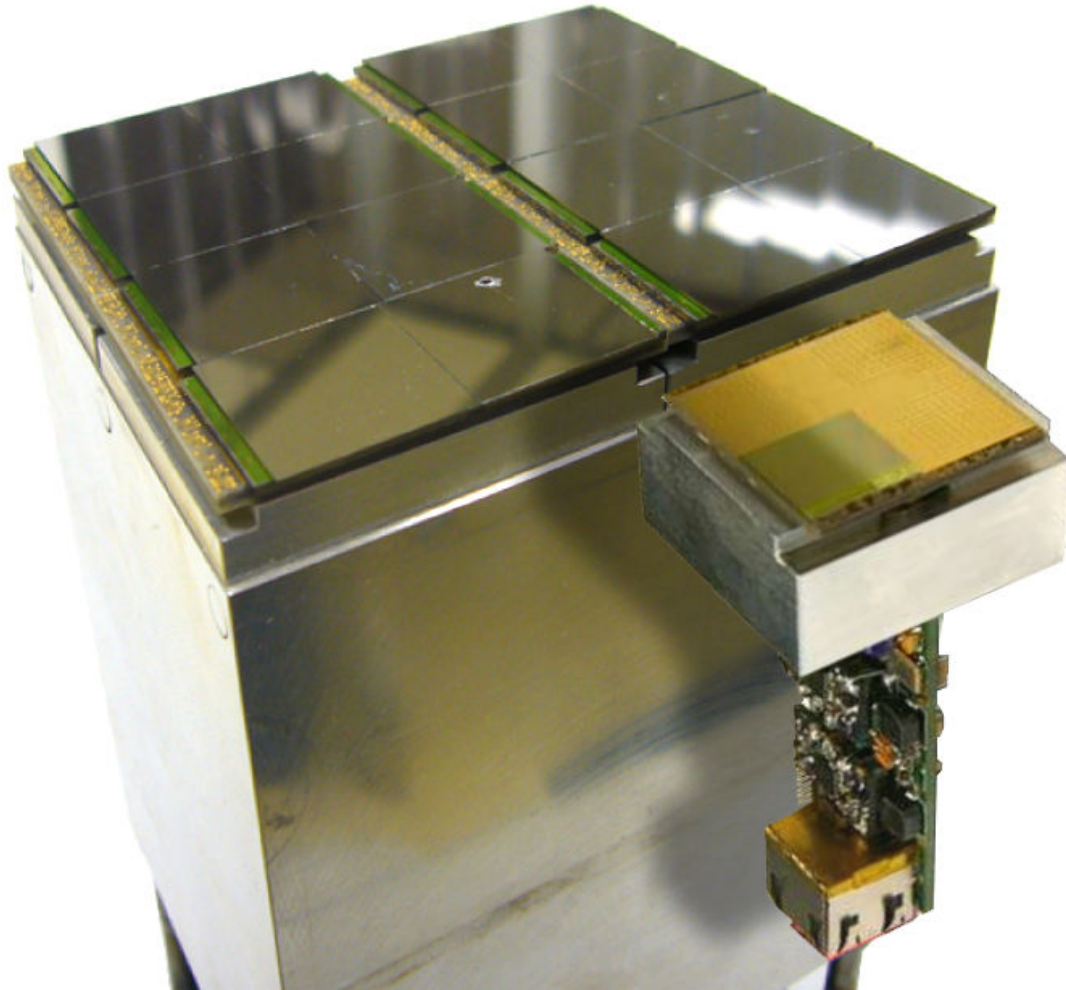
Two tracks; last day lower-left Ingrid lost HV connection



Track distorted by HV disconnected from lower-left Ingrid



NIKHEF

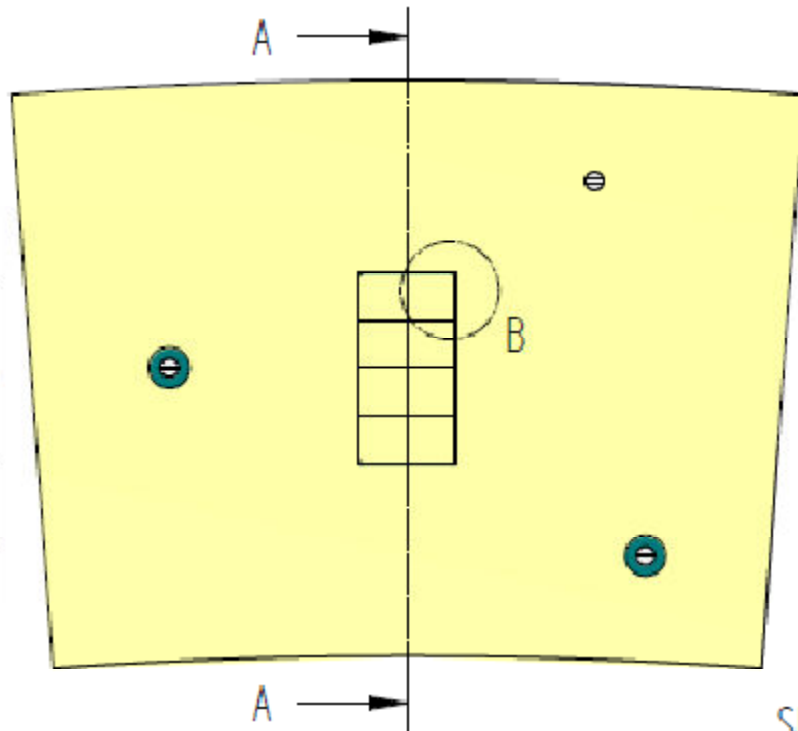


- within Relaxd project:
4x4 Medipix chips in
compact mounting
- Will evolve in 8x8
Timepix chips for
EUDET/LCTPC

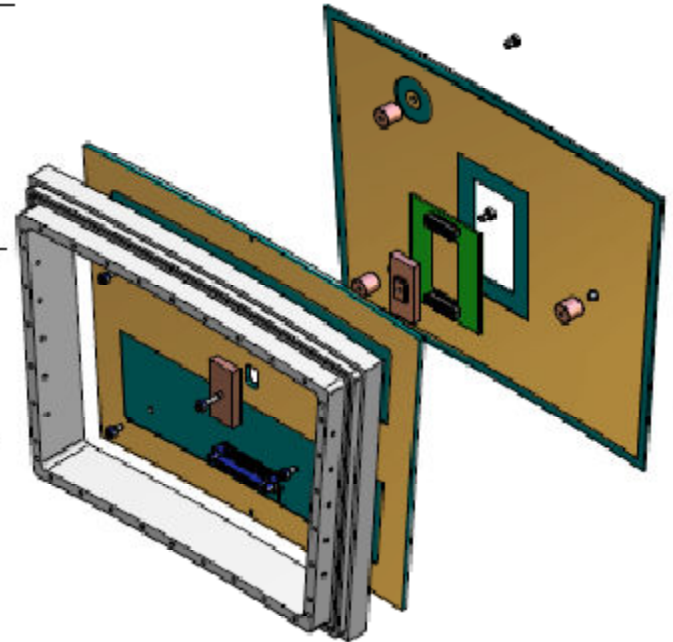
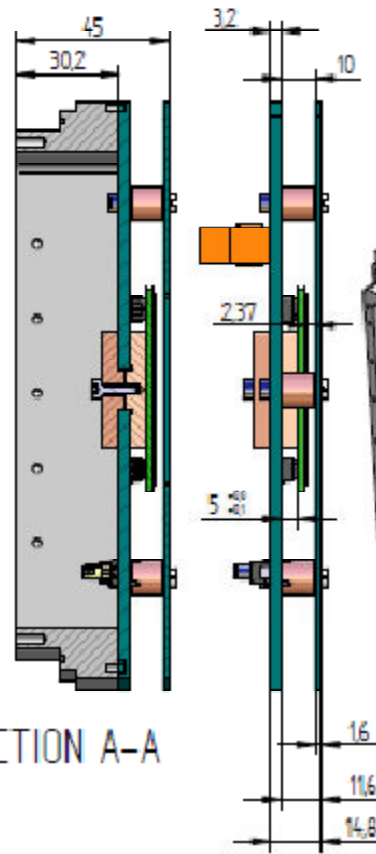
Pixel readout activities at Saclay

- Production of LP module with 8 Timepix+Ingrid chips (Saclay+Nikhef)
- Module (mother) board + 'mezzanine' board carrying chips produced by Saclay
- Timepix+Ingrid chips produced by Nikhef/Univ. Twente
- Readout working for 8 'naked' Timepix chips
- Mounting of 8 Timepix+Ingrid chips soon

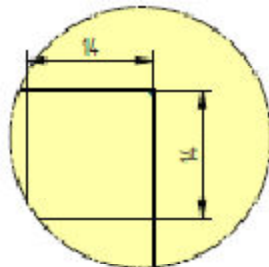
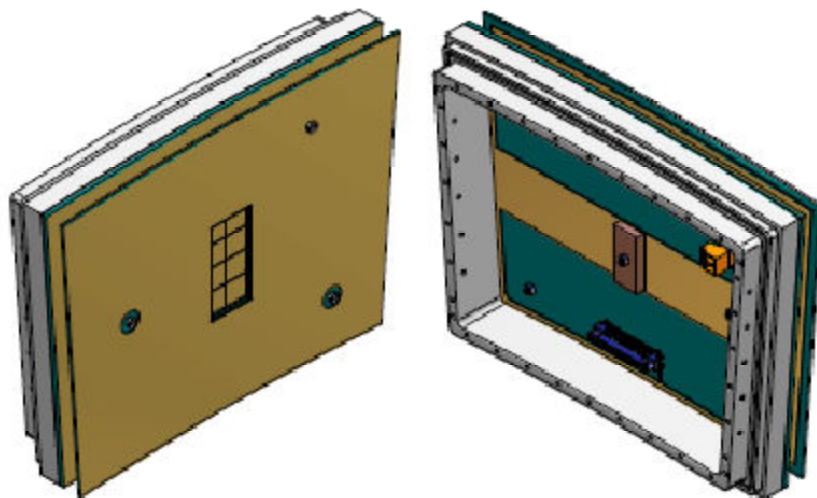
2x4 TimePix/InGrid matrix module for the LPTPC



SECTION A-A



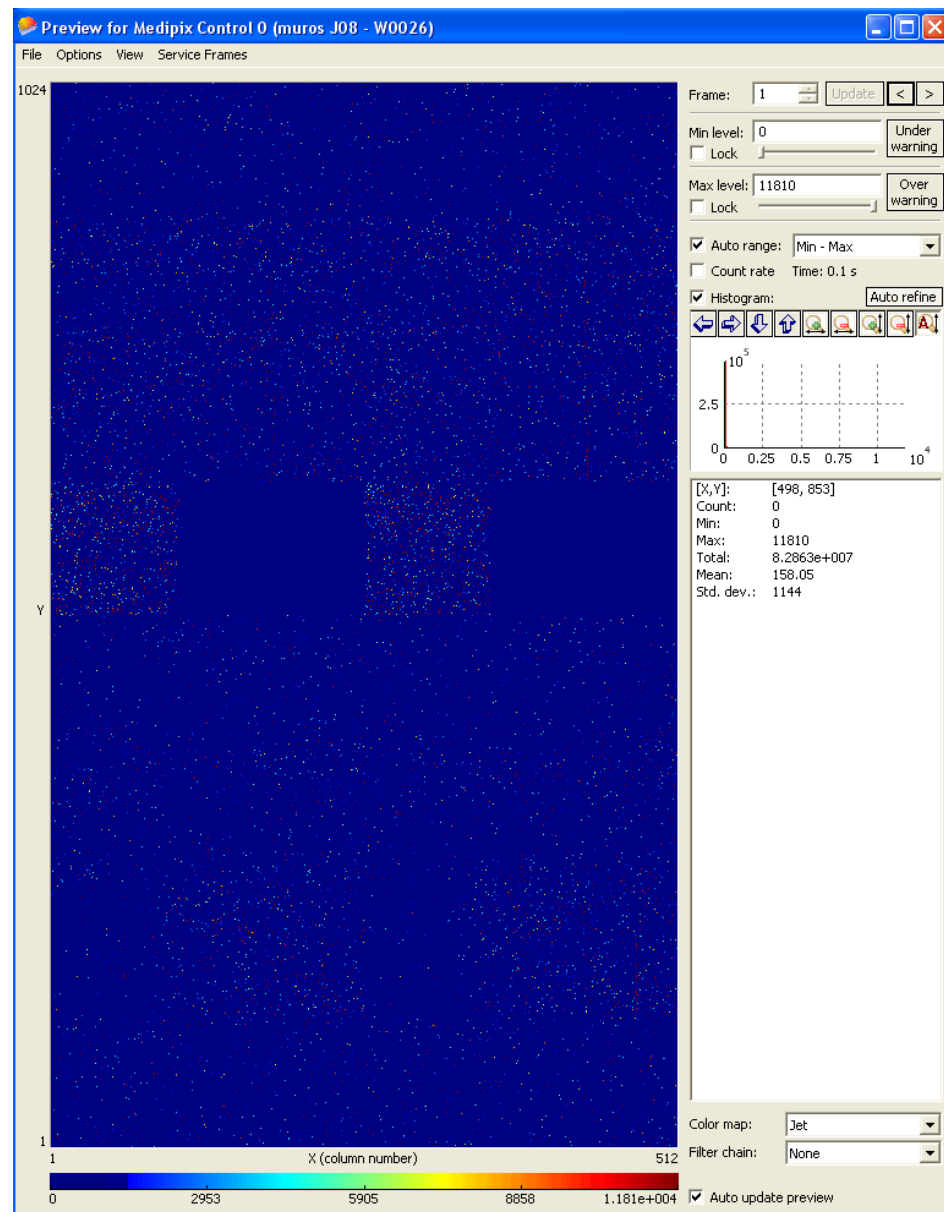
- Mother card
- Mezzanine card
- Guard ring card
- Heat dissipation block



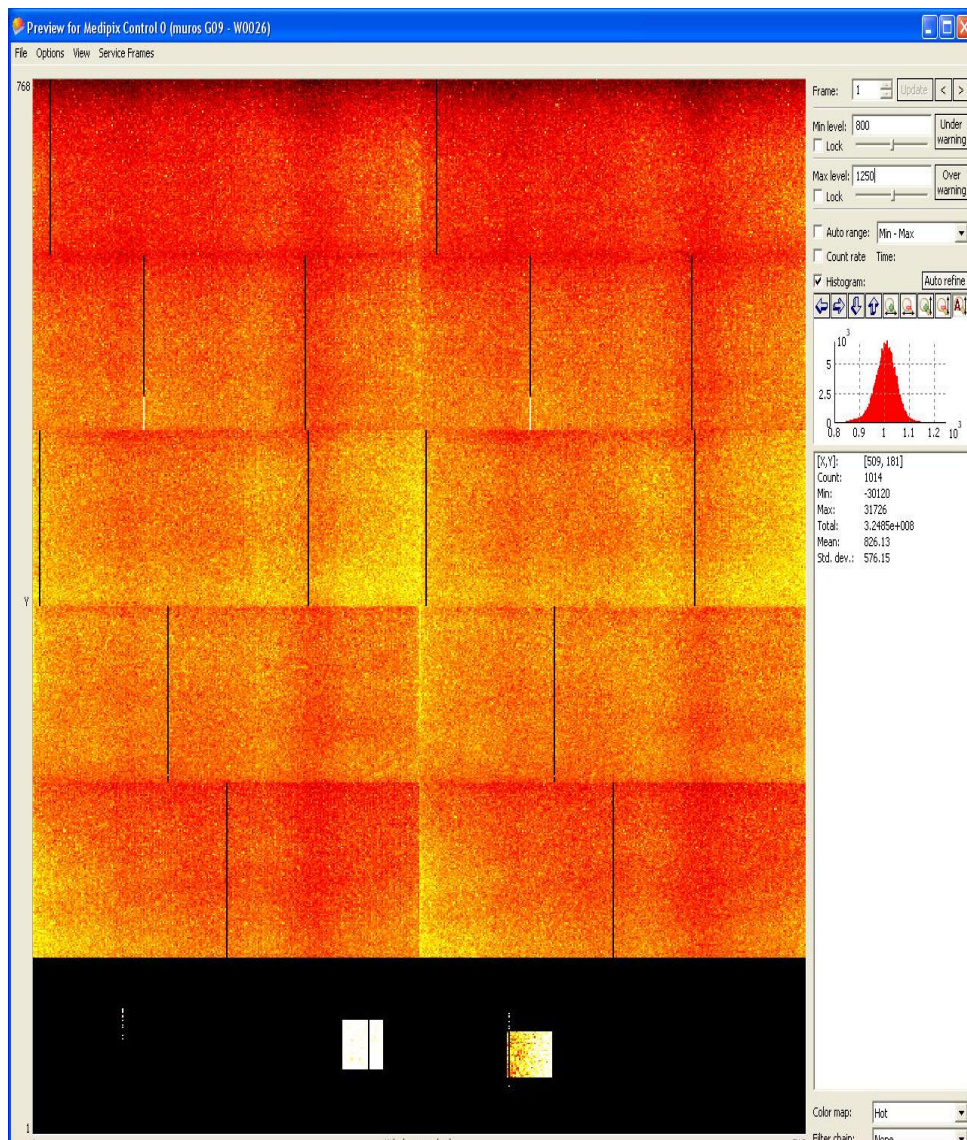
DETAIL B

Modèle:	FFM	Épave:		Évaluation:	FFM	DCP:	10-10	Date:	12/01/2004	Créé par:	PKL&OT
Éch:	1	Dét:		Version:	1.00	Modèle de:					
Titre: Ensemble PCB TimePixPanel_V3											
Solid Edge											
C.E.A. / SACLAY / IPRU / SECV											

- 8 naked TimePix chips have been bonded on the octopuce card by Joop in Nikhef last month.
- For the first time, 8 chips have been recognized by Pixelman
- The mezzanine card works electrically using power regulators
- During operation, the total power consumption is 20 watts
- Pixelman display issue found and has to be fixed



- The chip bypass has been tested
- The equalization was done and the test pulsers do the job
- Next month, 8 Ingrids could be mounted and tested in gas
- Next beam test in the Large Prototype of TPC in DESY before summer.
- To be continued...



Conclusions

- EUDET-SITPC final infrastructure available for 3-GEM + 8 Timepix chips – analysis beam data in progress
- LP module with 8 Timepix+Ingrid chips in preparation. Readout working with 8 ‘naked’ chips. Module mounting with Ingrids soon.
- Quad-Ingrid detector for standalone tests having readout problems at DESY (works at NIKHEF)
- Longer term: working on larger systems of 64 and 119 chips for Ingrids and GEMs.

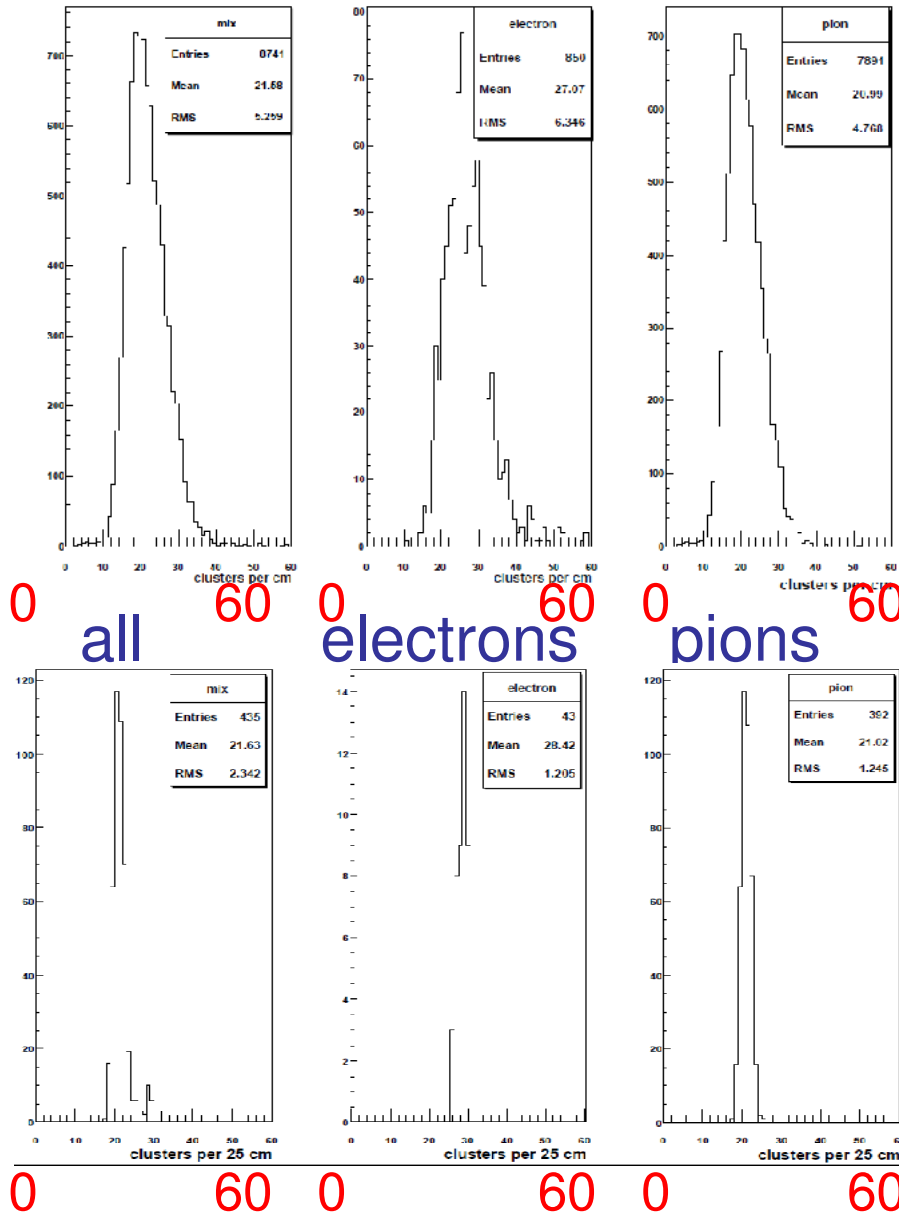
Backup

Performance goals and design parameters for a TPC with standard electronics at the ILC detector

Size	$\phi = 3.6\text{m}, L = 4.3\text{m}$ outside dimensions
Momentum resolution (3.5T)	$\delta(1/p_t) \sim 9 \times 10^{-5}/\text{GeV}/c$ TPC only ($\times 0.4$ if IP incl.)
Momentum resolution (3.5T)	$\delta(1/p_t) \sim 2 \times 10^{-5}/\text{GeV}/c$ (SET+TPC+SIT+VTX)
Solid angle coverage	Up to $\cos\theta \simeq 0.98$ (10 pad rows)
TPC material budget	$\sim 0.04X_0$ to outer fieldcage in r $\sim 0.15X_0$ for readout endcaps in z
Number of pads/timebuckets	$\sim 1 \times 10^6/1000$ per endcap
Pad size/no.padrows	$\sim 1\text{mm} \times 4\text{--}6\text{mm}/\sim 200$ (standard readout)
σ_{point} in $r\phi$	$< 100\mu\text{m}$ (average over $L_{\text{sensitive}}$, modulo track ϕ angle)
σ_{point} in rz	$\sim 0.5\text{ mm}$ (modulo track θ angle)
2-hit resolution in $r\phi$	$\sim 2\text{ mm}$ (modulo track angles)
2-hit resolution in rz	$\sim 6\text{ mm}$ (modulo track angles)
dE/dx resolution	$\sim 5\%$
Performance	$> 97\%$ efficiency for TPC only ($p_t > 1\text{GeV}/c$), and $> 99\%$ all tracking ($p_t > 1\text{GeV}/c$) [82]
Background robustness	Full efficiency with 1% occupancy, simulated for example in Fig. 4.3-4(right)
Background safety factor	Chamber will be prepared for $10 \times$ worse backgrounds at the linear collider start-up

with MPGD

Cluster counting distribution in He/iC4H10



• Using 1 cm tracklength

Electrons:

Avg=27.1/cm rms=6.3

Pions: 21.0/cm 4.8

• Using 25 cm tracklength

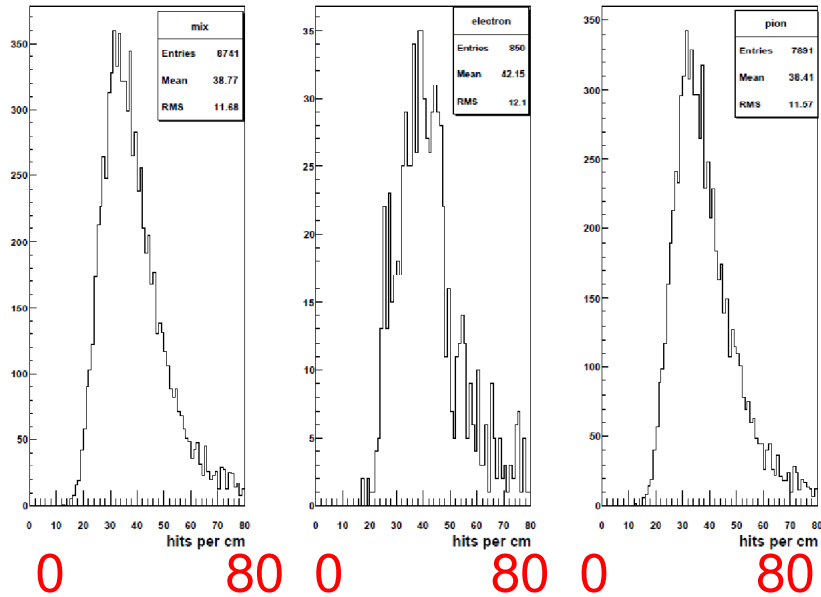
Electrons:

Avg=28.4/cm rms=1.2

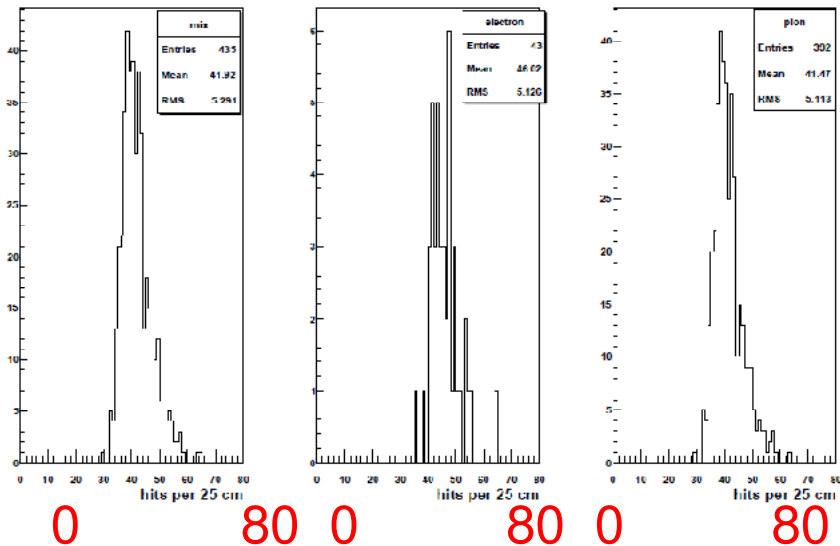
Pions: 21.0/cm 1.2

4.4 σ difference

Single hits counting distribution in He/iC4H10



all electrons pions



•Using 1 cm tracklength

Electrons:

Avg=42.2/cm rms=12.1

Pions: 38.4/cm 11.6

•Using 25 cm tracklength

Electrons:

Avg=46.0/cm rms=5.1

Pions: 41.5/cm 5.1

0.6 σ difference