Silicon Pixel Tracker (SPT) for CLIC

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- **SPT at CLIC - suggested architecture and track reconstruction procedure**
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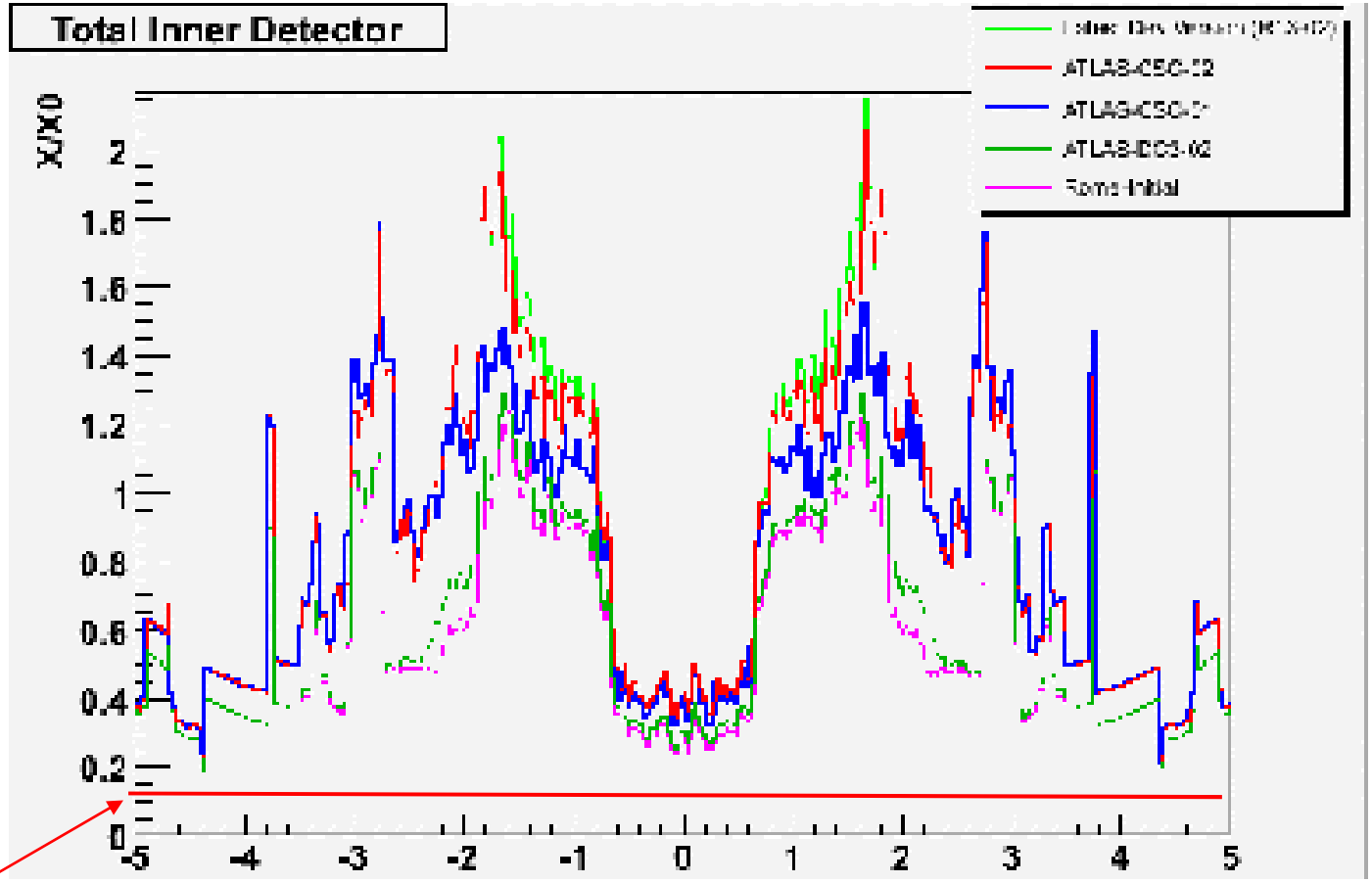
Goals and design principles

- For past two years, a few of us have started to consider a new approach to tracking at the LC (which is even better matched to CLIC than to ILC)
- Goal is excellent track reconstruction efficiency and precision, down to the minimum polar angle, with high transparency for photons
- Eliminate all material that isn't strictly necessary in the tracking volume
- Explore a monolithic pixel architecture (~50 μm pixels), since a pixel layer can be made thinner than a microstrip layer, and as regards track finding, one pixel layer is worth far more than two strip layers
- Integrate signals through the bunch train, EXCEPT for a timing layer (barrel plus endcaps) just in front of the ECAL, and a (short?) timing layer (barrel only) between vertex layers and tracker layers. Larger pixels than main tracker (~150 μm?), but best possible timing resolution.
- Track densities are sufficiently low that it will be possible to almost perfectly follow each on-time track through the tracking layers and through the vertex detector layers to the IP (or the decay point, if beyond the VXD inner layer)
- By reading out steadily between trains, we avoid the mechanical and thermal issues of pulsed power. In our case, peak power = average power, and power levels can be comfortably handled by a gentle flow of cooling gas (hence minimising the material budget)

- Apart from the judiciously located timing layers (~2% X_0 per layer?), the tracking system (closed barrel with endcaps) can achieve ~0.6% X_0 per layer. Ambitious!



10% X_0, a frequently-suggested goal for the LC tracking system. We hope for <1% (VXD) plus 2% (inner timing) plus 3% (main tracker) ie 6% total, disregarding outer timing double layer

- Some of these assertions are currently defended only at back-of-envelope level, but they are based largely on experience with, and recent developments in, monolithic pixel architectures

- Obvious concerns:
  - 30 Gpixels. 'No problem', given progress in astronomy etc
  - Excellent charge collection with large pixels, and need for excellent noise performance from large area devices, due to small signals from thin layers. 'No problem', with charge-coupled CMOS pixel technology
  - Quality of track reconstruction, given ~7000 out-of-time tracks per train. 'No problem', given well-defined starting point for each on-time track. Pixel systems are better at this than is often realised – the powerful combination of high precision space points and minimal material allows extremely efficient track linking, and suppression of fake tracks (very hand-waving at present; needs simulation)
  - General principle, established in ACCMOR and SLD vertex detectors – granularity can to a great extent compensate for coarser timing. Precision time stamping costs power, hence layer thickness, fine granularity does not.

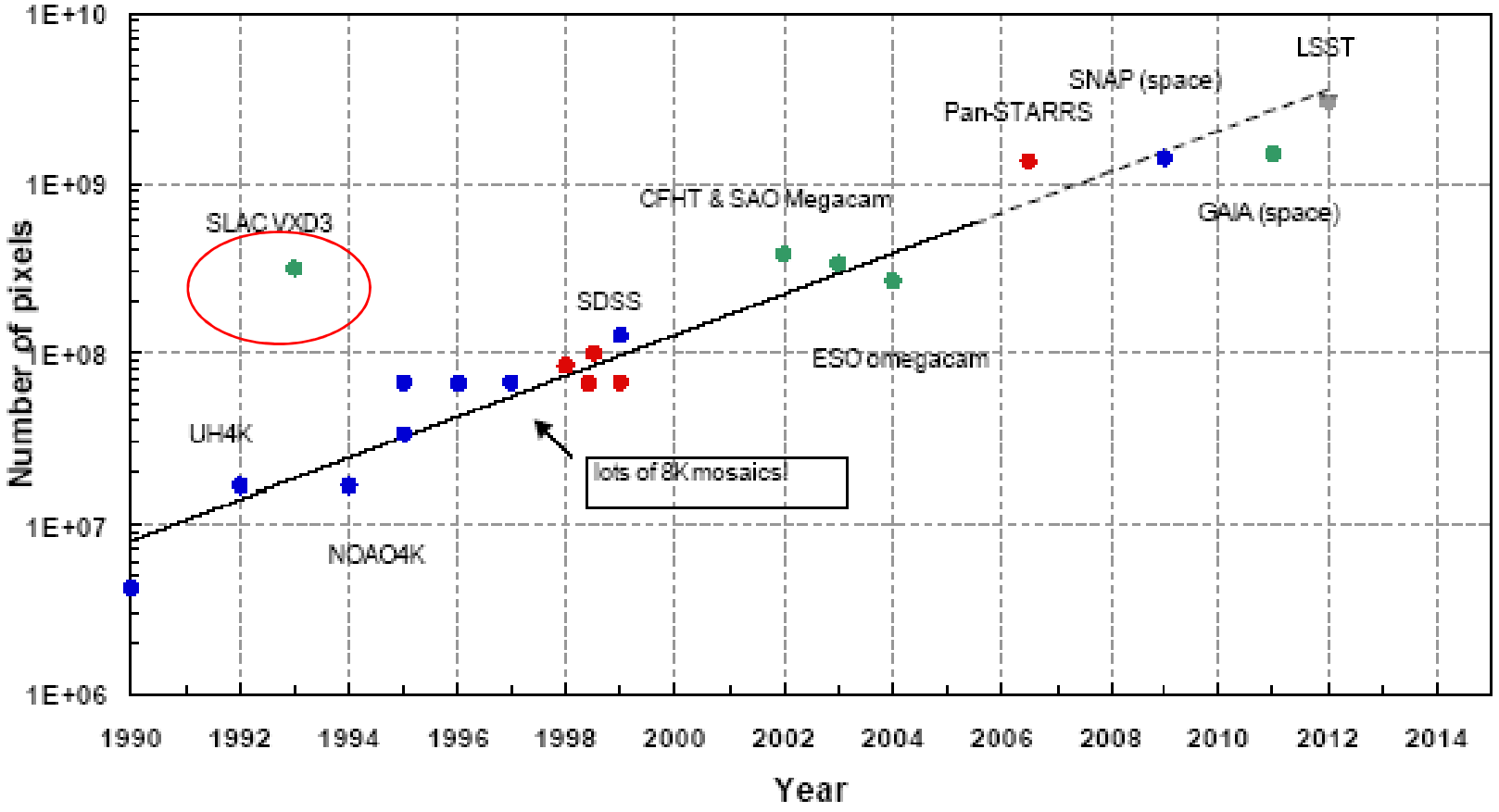
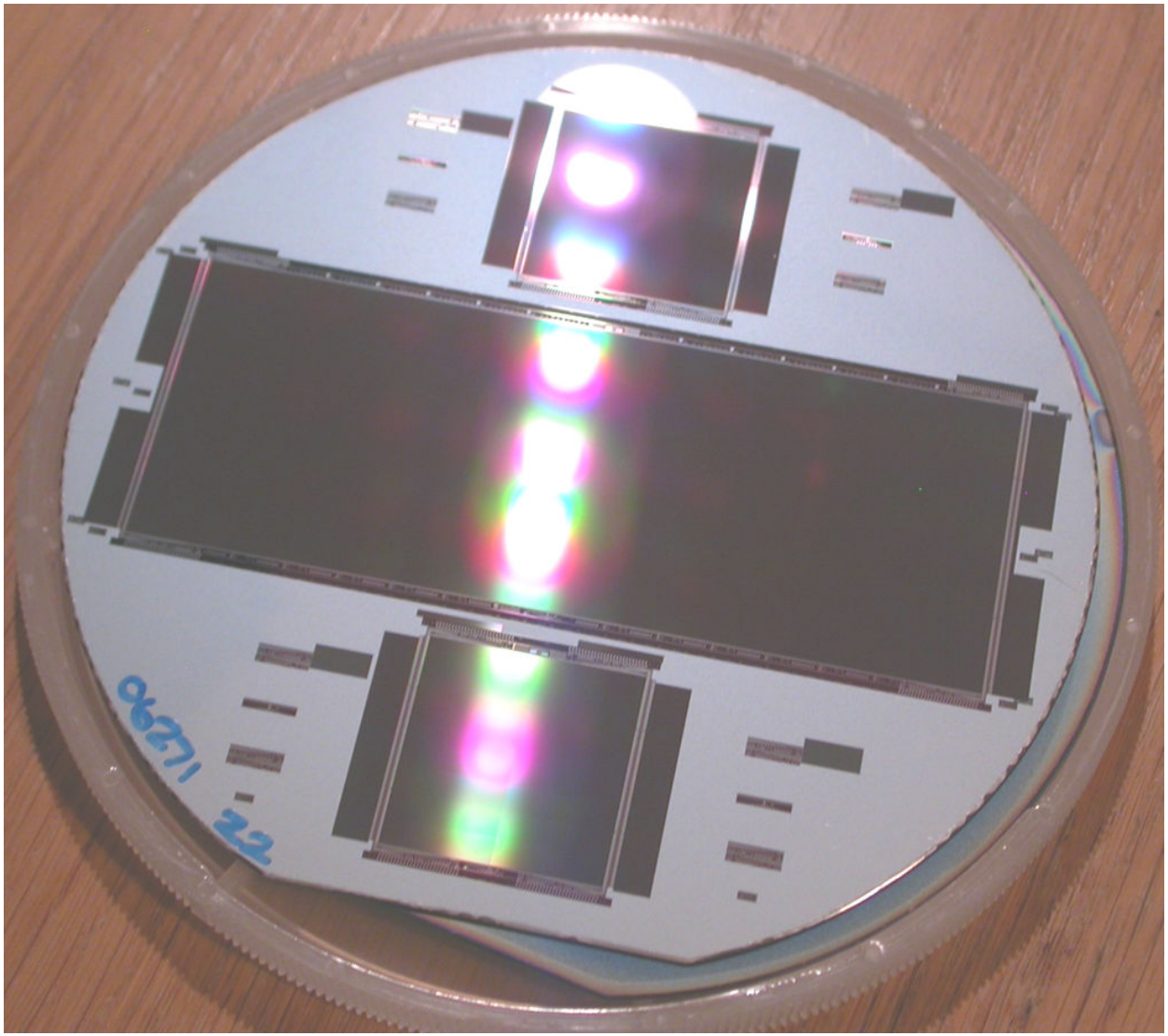


Illustration of focal plane sizes, from Luppino/Burke 'Moores' law

Focal plane size doubles every 2.5 years

From: Burke, Jorden, Vu, SDW Taormina 2005

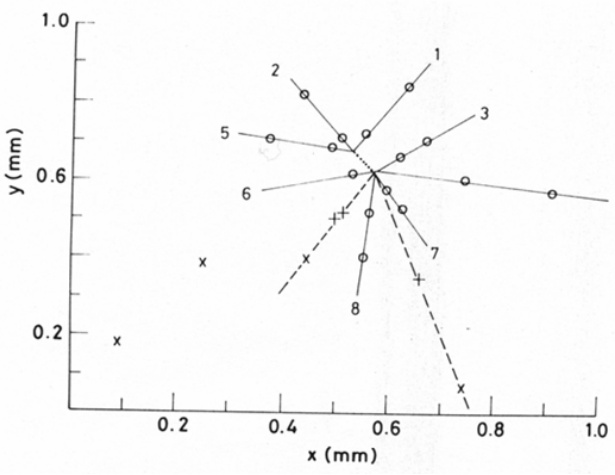


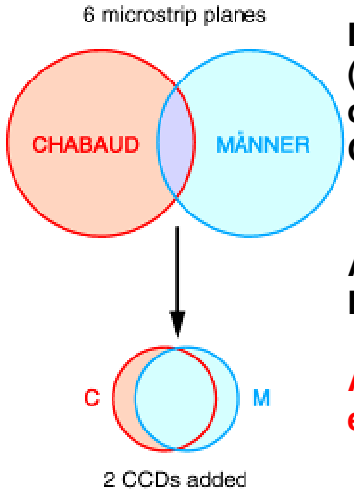
e2V technologies

6 inch wafer (CCDs)

(We are thinking of 8x8 cm^2 charge-coupled CMOS pixels, a **monolithic high-yielding process**)

Monolithic pixel detectors for tracking





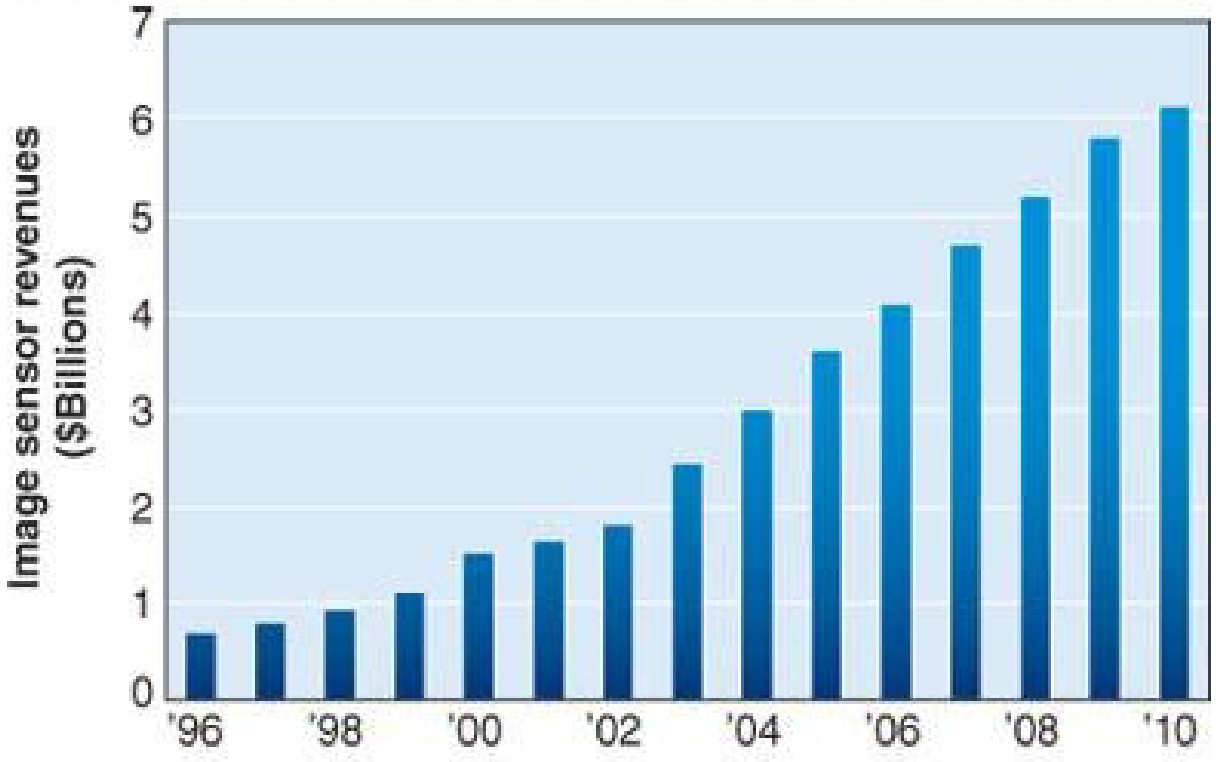
Note the scale (1 mm^2) Hit density on inner CCD ~ 80/ mm^2

ACCMOR 1984
Fred Wickens

A life-changing experience …

- The ACCMOR collaboration provided the first demonstration of the capabilities of pixel-based tracking detectors
- For LC vertexing, there is no longer any debate. Unanimity was achieved at LCWS 1993 in Hawaii. Prior to that, microstrips ('good enough for LEP') were pushed by some
- For LC tracking, studies began two years ago, but we have only scratched the surface, and not unreasonably the SPT is not yet in anybody's baseline. Progress on SPT reported at ILC workshops: Sendai, March 2008, Warsaw, June 2008 and Chicago, November 2008
- Meanwhile, for the rest of the world of digital cameras, scientific imaging, etc, the pace of progress is remarkable …

Nobel Prize for Physics, 2009



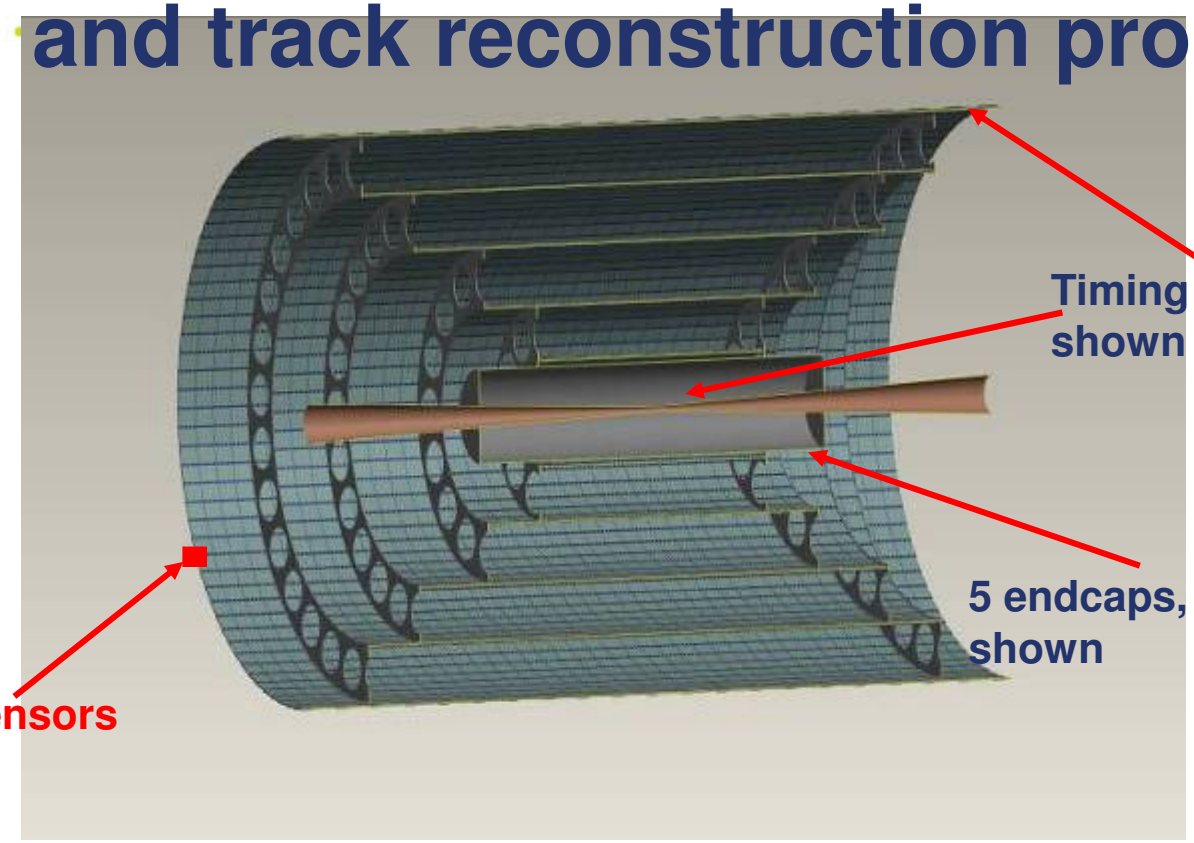
Fibre optics and the CCD: "Taken together, these technologies have had a greater impact on humanity than any others in the last half century" Fred Doyle, CEO of American Institute of Physics

"Optics technologies are exceptionally significant for scientific developments in today's world. We congratulate Kao, Boyle and Smith on this much-deserved recognition" Elizabeth Rogan, CEO of the Optical Society of America

Boyle and Smith having fun at Bell Lab, 1974

Boyle, 2009: At Bell Lab, there were no 'project proposals', no 'deliverables', no 'impact statements', just a bunch of bright people paid to work creatively together. So far, 10 Nobel Prizes have been awarded to Bell Lab, which was long ago shut down.

SPT at CLIC - suggested architecture and track reconstruction procedure



- SiC foam support ladders, linked mechanically to one another along their length
- 5 **closed cylinders** (incl endcaps) will have excellent mechanical stability
- ~0.6% X_0 per layer, 3.0% X_0 total, over full polar angle range, plus <1% X_0 from VXD system (goal)
- Additional timing layers, one (double) as an **envelope** for general track finding, and one (single or double?), **between VXD and tracker,** particularly to tag loopers with θ_p ~70-90 degrees and to establish a vital second point on each on-time track

Backgrounds in silicon tracker

- Thanks to Takashi Maruyama, Norm Graf, John Jaros and Marco Battaglia for help with this
- For ILC at 1 TeV, Takashi has calculated beamstrahlung-related and 2-photon backgrounds, both charged tracks and photon conversions
- 80% of hits are due to photons emitted from the BEAMCAL region, converting in the material of the tracker
- These photons are mostly of energy 0.1-1 MeV, with a peak at 0.51 MeV from positron annihilation in the BEAMCAL
- Using EGS, Takashi studied the conversion process in the detector, mostly Compton scattered electrons - tiny loopers which generate typically 1-10 hits in a tracker layer
- For CLIC at 3 TeV, 2-photon background dominates (Marco), ~7000 tracks per train. These will be easily absorbed by a fine-grained pixel tracker. Just need excellent rejection capability from the timing layers. Problem of hit ambiguity in tracking layers due to background appears to be at a low level, except for extremely low momentum tracks (<< 1 GeV/c) (to be simulated)

Possible track-finding strategy

- Start with timing layer 5 (double, to provide a reasonable initial vector) and extrapolate to tracker layer 5 and (if necessary) layer 4, with a loose IP constraint
- We can now extrapolate tracks of increasingly well-defined momentum to layer 3, 2, 1 with precision limited mainly by multiple scattering, and end up with well below one fake track per event (back of envelope, for ILC case)
- At a low level, the multiple-scattering-limited search ellipse from layer N to layer N-1 may find two hit candidates. Take the closest hit to the current helix, and possibly revise at end of the hit-assignment process, including the inner timing layer
- This procedure will surely deteriorate for low momentum tracks in the forward region. Could consider an intermediate time-stamping disk, or additional, hence more closely-spaced time-integrating disks. To decide, take account of the balance in material; one time-stamping disk is equivalent to three time-integrating disks, and has 9 times coarser granularity. [These figures are subject to revision and refinement, it's a question of optimisation that goes beyond back-of-envelope!]
- K-shorts and lambdas are accommodated, given the vector from the two external timing layers (Garfield approach) and loopers with θ_P close to 90 degrees are accommodated by using the inner timing layer

Monolithic pixels: historical/technical overview

Charge-coupled devices (CCDs)

devices up to wafer-scale, wide range of pixel sizes, low dark current* and excellent noise performance, slow readout

Wide range of scientific applications

CMOS active pixels (MAPS)

3T pixels restricted to small pixel sizes, relatively high dark current* and poor noise performance**, fast readout

Limited scientific applications

Charge-coupled CMOS pixels

wide range of pixel sizes, low dark current and excellent noise performance, fast readout

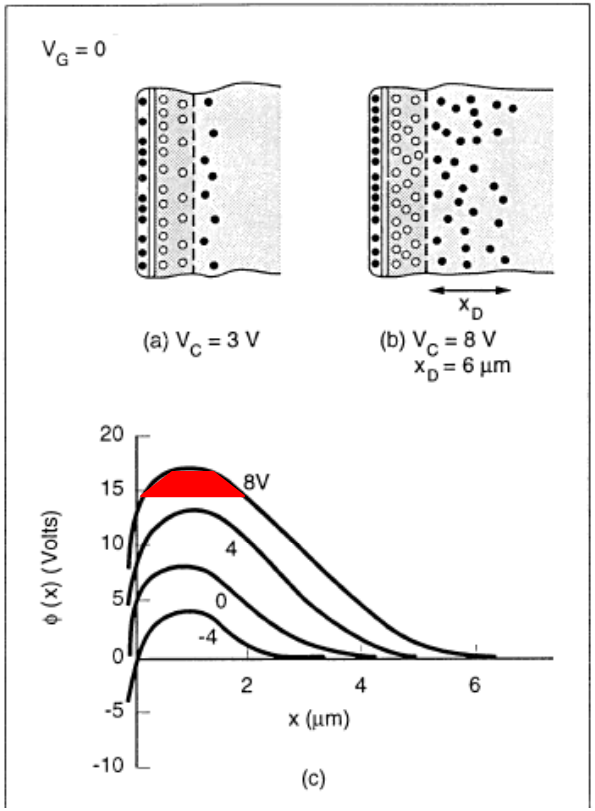
Potentially wide range of scientific applications

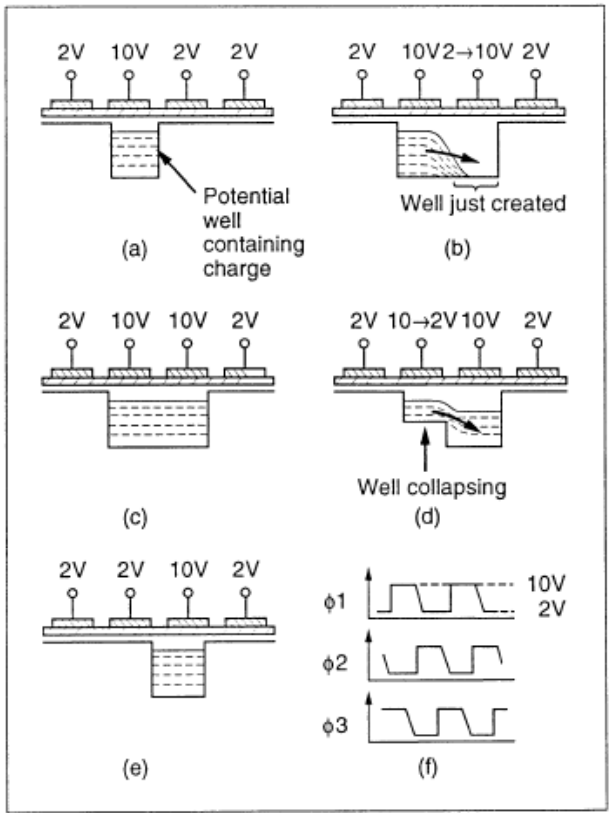
* 1-10 pA/cm^2 (CCD) cf 200-500 pA/cm^2 (3T CMOS)

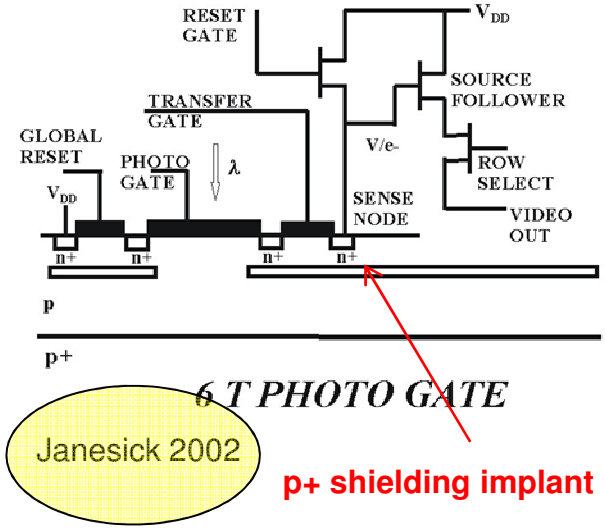
** frame-rate CDS, severe problems for large chips

Omitted: DEPFET, which is an MPI Halbleiterlabor in-house charge-coupled non-CMOS architecture with special properties and wide scientific applications

From CCDs to charge-coupled CMOS pixels



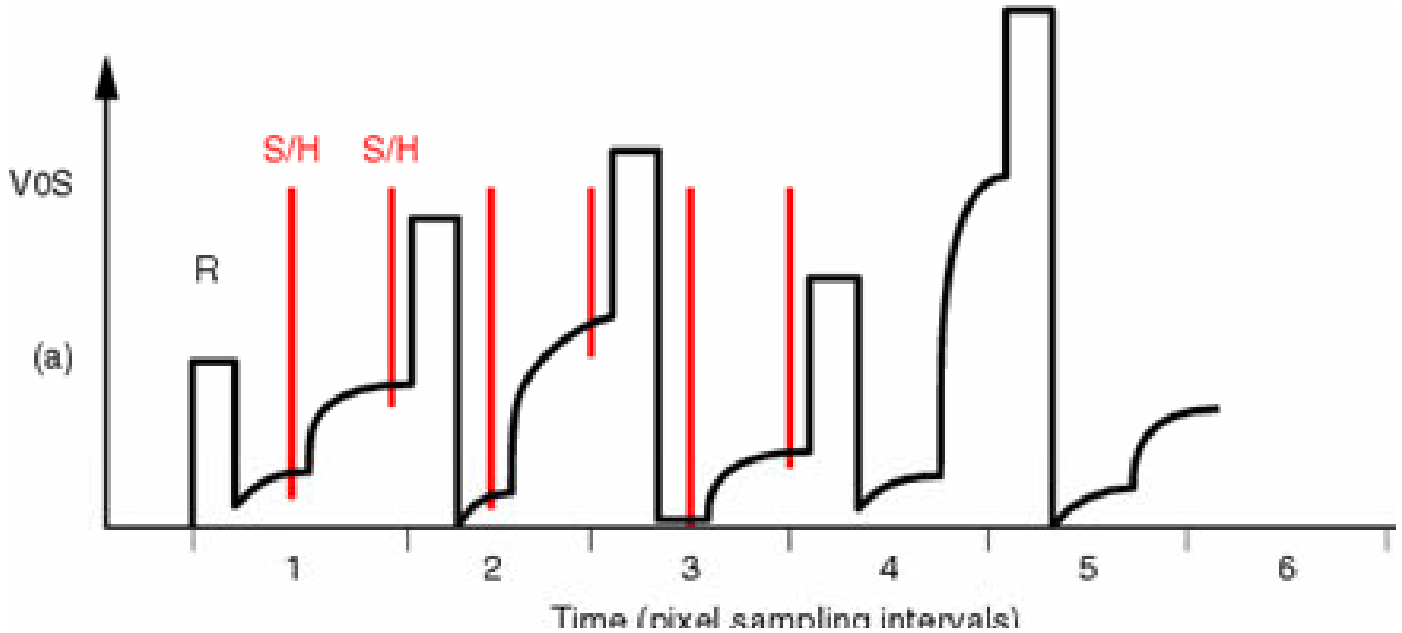




- **There are several variants, but in all cases, the key features are:**
  - **Collect signal charge on a fully-depletable structure (PG or PPD) having relatively large capacitance. Shield in-pixel electronics with a deep p-implant**
  - **Sense 'baseline' voltage on gate of submicron transistor having minimal capacitance**
  - **Transfer entire signal charge to this gate and sample again, *promptly***
  - **The voltage difference is CDS measurement of the signal**

Correlated double sampling (CDS)

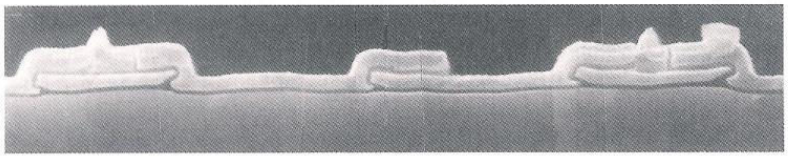
[which is possible only for charge-coupled pixels – beware of imitations such as 'frame-rate' CDS]



Baseline settles to a different level after each reset, due to *kTC* noise. Entire signal charge is transferred to the output node between the two CDS phases

This eliminates reset noise, fixed-pattern noise, noise from node dark-current, and suppresses pickup – low and high frequency. It enables astronomers to achieve few-electron noise performance with long exposure times, and particle physicists to make efficient trackers with large area devices having ~20 μm of active silicon

- Advantages are obvious, so why has the CMOS pixel community been stuck with 3T pixels for so long?

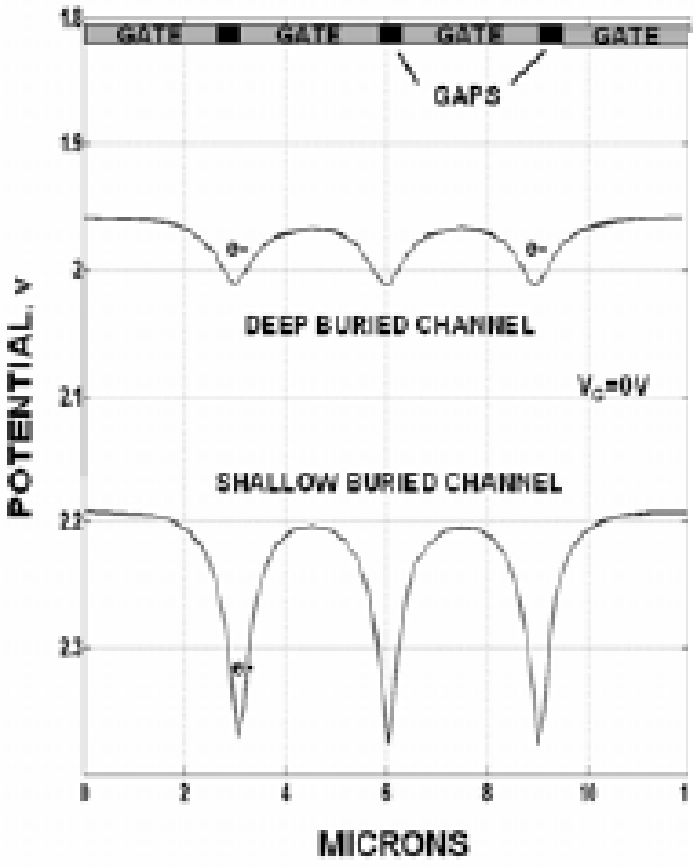


- D Burt, many years ago: 'The literature is littered with failed attempts …' Why was this difficult, and how has the problem been solved?

- Unlike with CCDs, every layer of a CMOS device needs to be precisely **planarised,** or the photolithography for the next layer will be out of focus

- For metal and polysilicon layers, planarisation
- is achieved by the technique of **damascening**

- With 0.18 μm CMOS, an intergate gap of 0.25 μm can be achieved with a single poly layer, and this is (just) adequate



- **Massive progress over past 3 years, described in papers by Jim Janesick et al,**

Proc SPIE 6276-7 (2006)

Proc SPIE 6690-2 (2007)

Proc SPIE 7439A-6 (2009) (in publication)

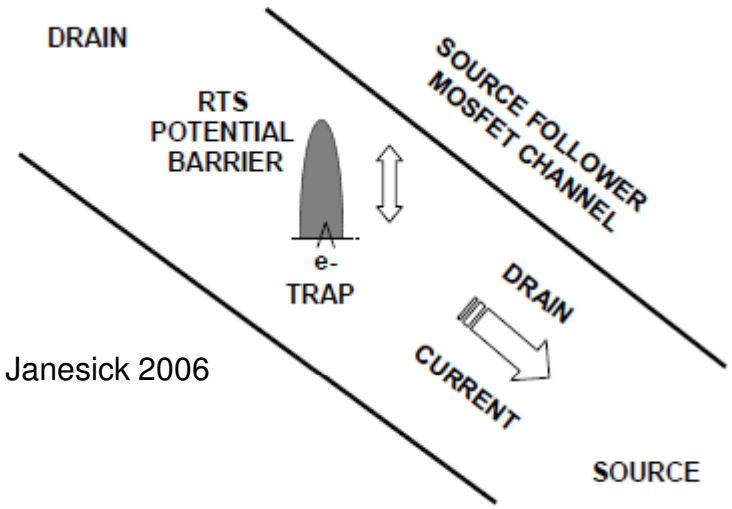
- **Simulations for BC charge-coupled CMOS (Janesick 2009)**
- **Similarly encouraging results even for gates as short as 1 μm (Konstantin Stefanov 2007)**
- **However, short-channel effects and fringing field effects are a big issue (George Seabroke 2009)**

- Charge-coupled CMOS pixels were first developed for commercial products - high quality cameras, circa 2000

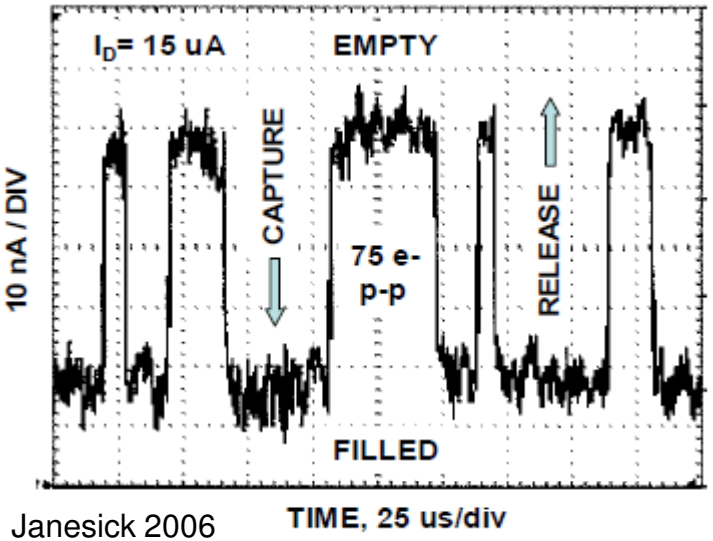
- For scientific applications, there are numerous developments under way:
  - Jim Janesick with Jazz Semiconductor
    (note his multi-project wafer Sandbox service)
  - Oxford/RAL with Jazz Semiconductor (ISIS) (surviving remnant of LCFI R&D)
  - James Beletic with Teledyne Imaging Sensors
  - Oregon/Yale with Sarnoff (chronopixels)
  - e2V with Tower Semiconductor
  - Spider Collaboration with 'Foundry A' (Fortis)
  - Andor/Fairchild/PCO (sCMOS) – Press release 15 June, they list 23 scientific application areas, devices to be marketed from next year
  - And probably many others …

- Numerous design variants, 4TPPD, 5TPPD, 4TPG, 6TPG etc. However, the key in all cases has been to develop a working charge-transfer capability within the CMOS process

RTS noise



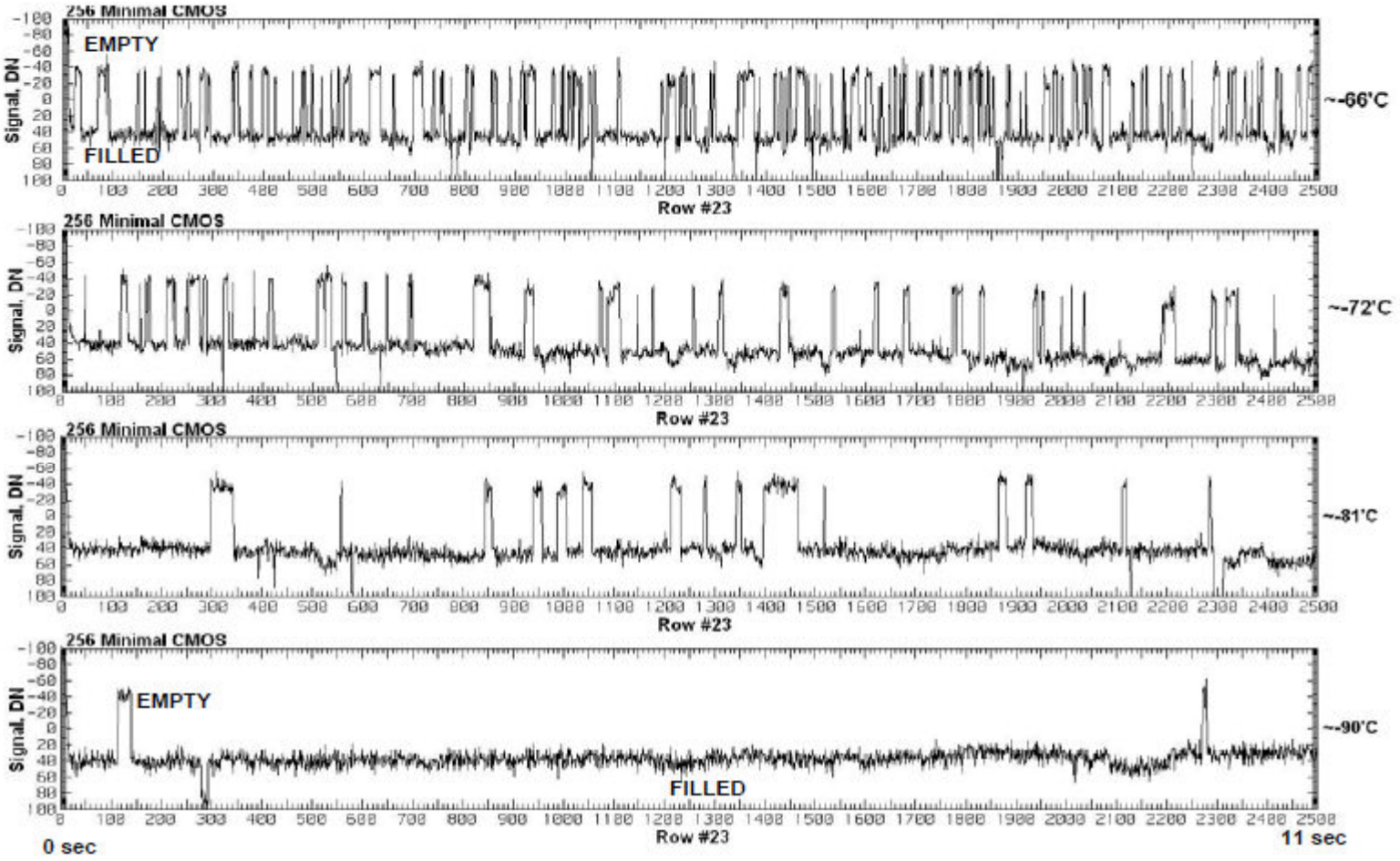
Janesick 2006



Janesick 2006

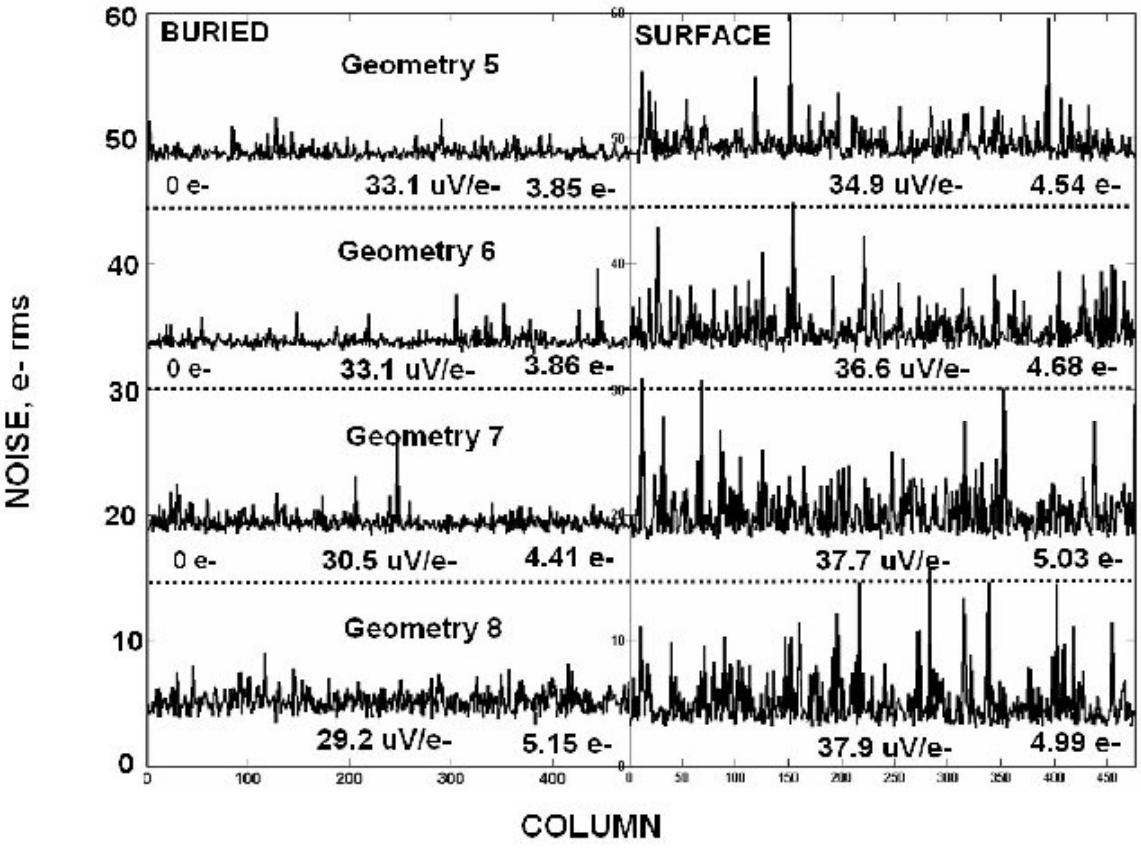
Note: These fluctuations amount to only 0.3% of the drain current

- **This is the dominant residual noise source in charge-coupled CMOS pixels**
- **As with CCDs, transistor noise can be much reduced by using a buried-channel MOSFET for the source follower (but not completely eliminated, due to the presence of bulk traps)**

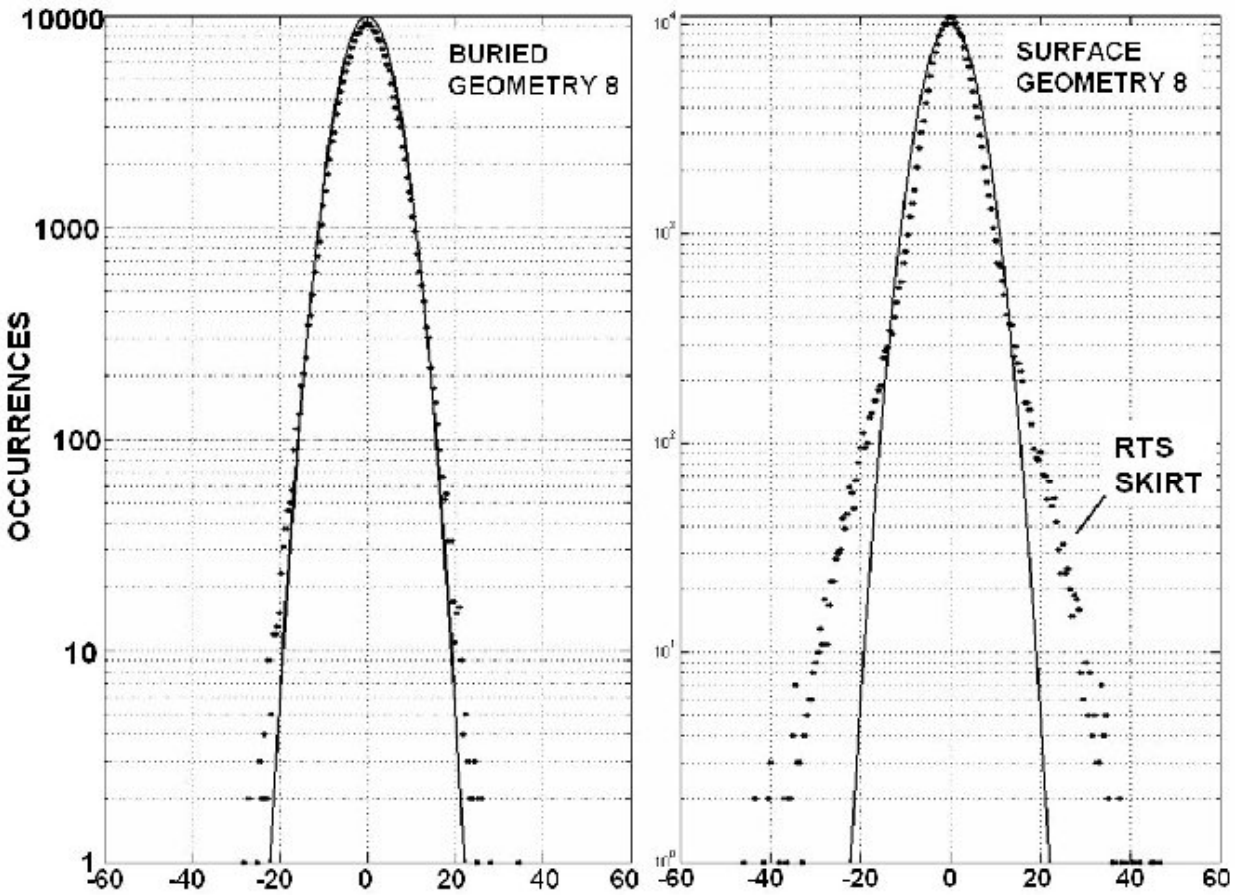


Janesick 2006

Despite this behaviour, there is *nothing* (as regards noise performance) to be gained by cooling!

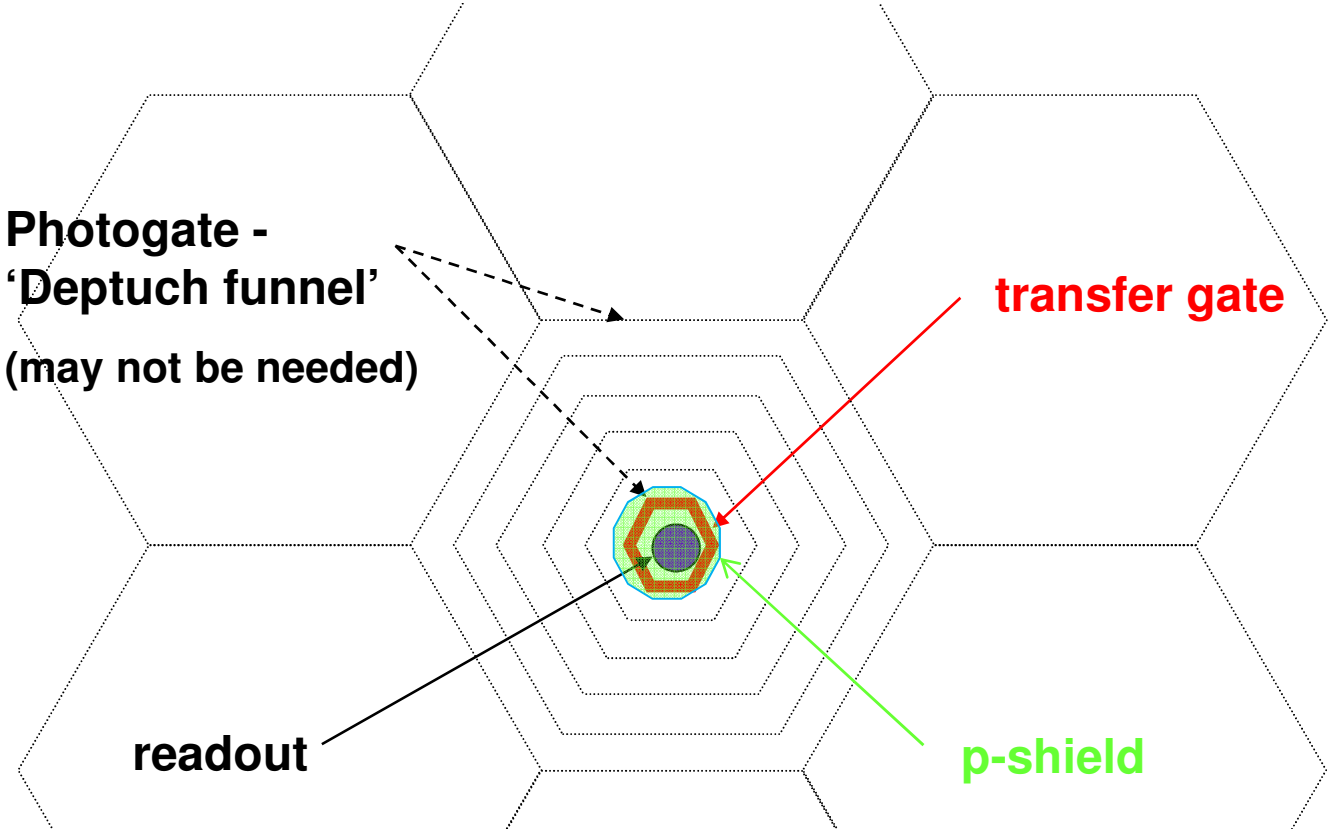


Janesick latest, week of 5 October, 2009



Janesick latest, week of 5 October, 2009

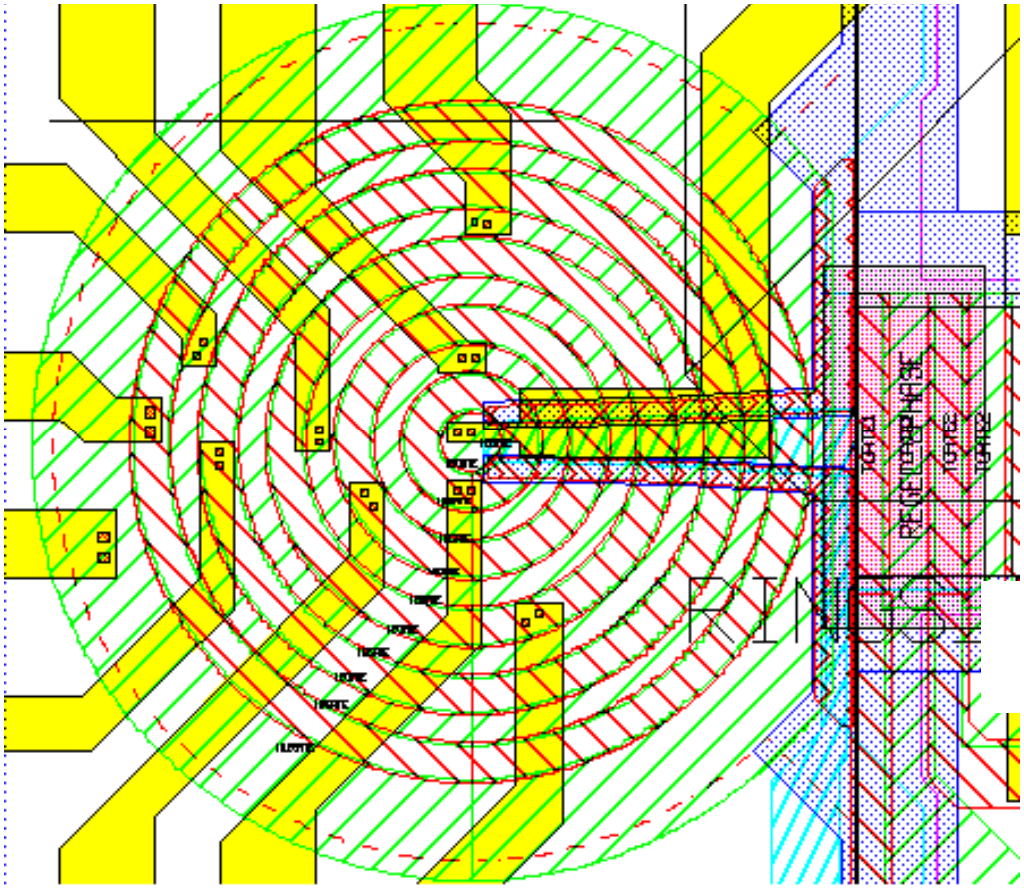
Silicon Pixel Tracker for CLIC
A possible architecture



SPT pixels (~50 μm diameter):

- **PG preferred over PPD for such large pixels, in which is embedded the ring-shaped transfer gate and 3 tiny transistors, below the p-shield**
- **'Deptuch funnel' – need only ~50 mV per stage (and couldn't be much higher, if one uses a 0.18 μm process, limited to 5 V) [dual gate thickness, 12 nm and 5 V; 4.1 nm and 1.8 V]. Needed only if an unstructured PG has excessive potential variation.**

- It turns out that both funnel and register have been fabricated by e2V for confocal microscopy: 100% efficient for single photoelectrons – noiseless, by using LLL (L3) linear register



Diameter of outer active ring ~ 100 μm

[David Burt, e2V technologies]

Conclusions and Outlook

- For visible light and x-ray imaging in astronomy, monolithic silicon pixel detectors took over from photographic film in the 1990s
- Their development for particle physics has been slow, but with some exceptions (eg LHC GPDs), these detectors are likely to evolve as the technology of choice for vertexing and tracking in particle physics (my opinion)
- It still wasn't accepted for vertexing at SLC as late as 1982; remember the baseline just 8 yrs before startup (next slide). Similar story for the linear collider - until 1993. 'What was good enough for LEP will be good enough for ILC.'
- Even in 2009, monolithic pixels aren't widely studied for tracking at ILC or CLIC, due largely to entrenched opinions. They aren't in the baseline for either of the validated concepts.
- We are fortunate to have strong interest and encouragement from the SiLC collaboration – Marcel Vos already made a valuable simulation of our first concept, reported at the LC workshop, in Sendai, March 2008
- SPT could be an attractive option for both CLIC and ILC
- Main tracker (30 Gpixels) will be in line with state-of-art for charge-coupled CMOS systems by 2020
- Timing layers (probably three, details tbd), depend on inexpensive bump-bonding or vertical integration for large chips. OK on this timescale?
- 'The better is the enemy of the good.' Yes, if it's really going to be good enough. Also, time is on the side of the better, in this case.

SLC Experiments Workshop 1982, just 8 years before start of SLC

Who knows what the future holds? Beware of premature technology choices for ILC!

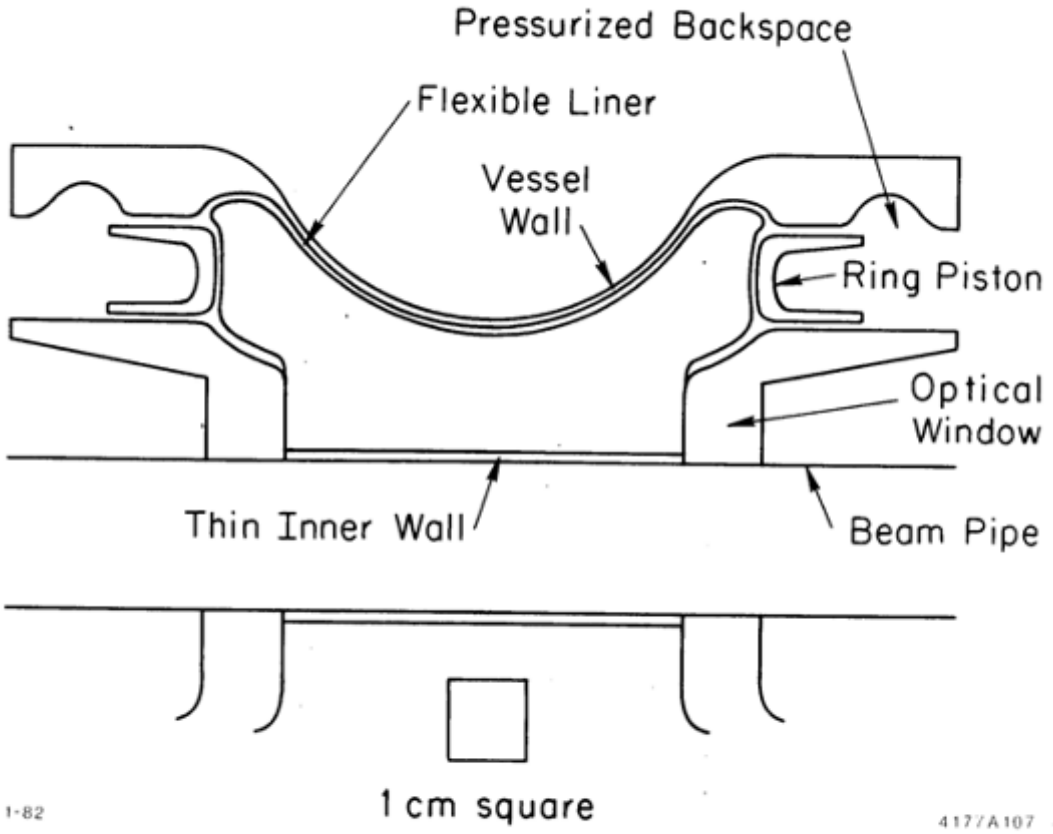
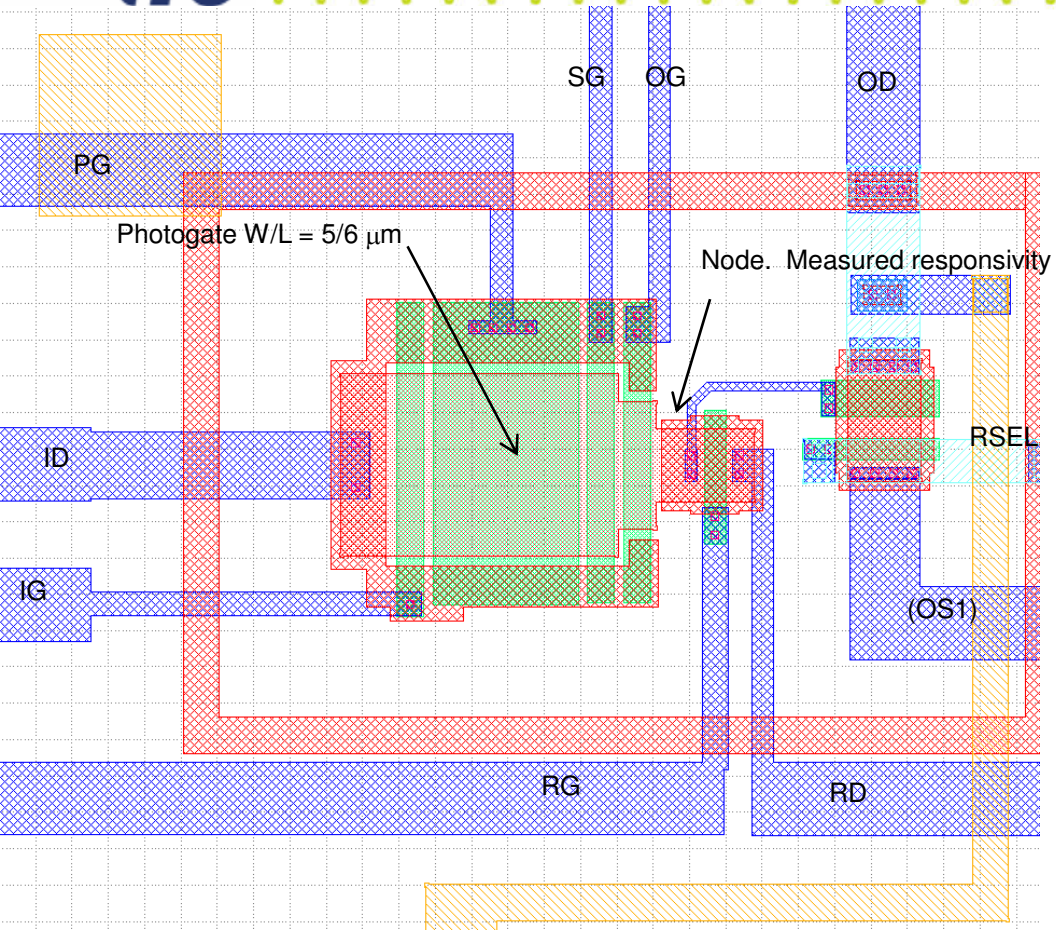


Fig. 7. Conceptual design of a propane bubble chamber vertex detector.

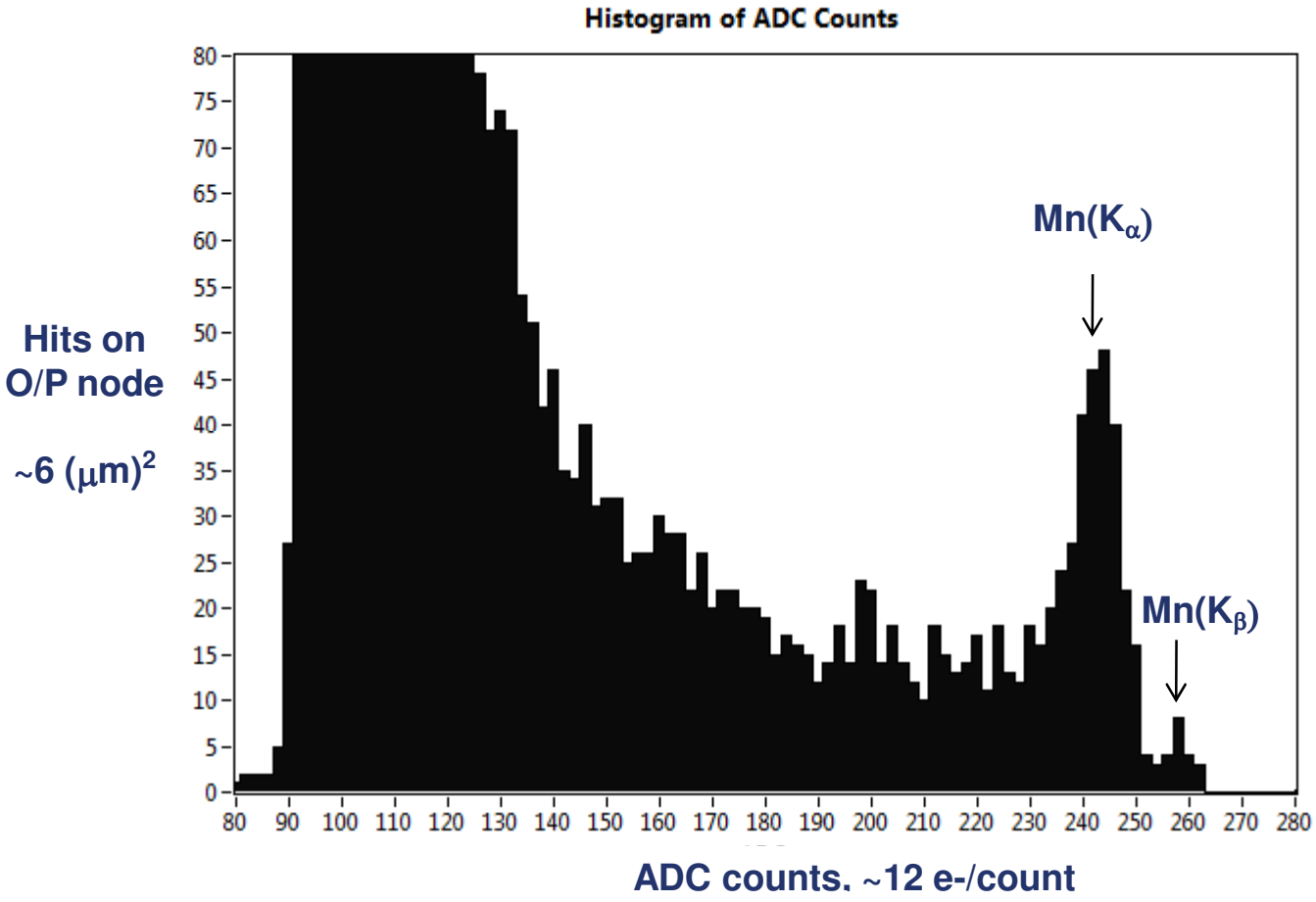
backup

ISIS-2 buried channel test structure



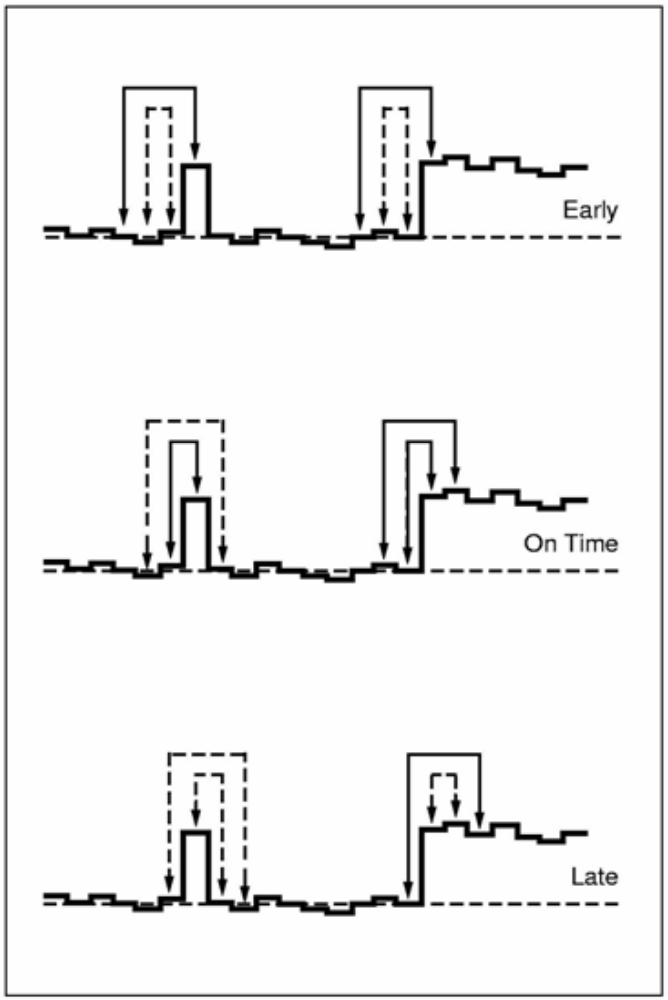
- **Short-channel and fringing field effects are large. Former have been simulated, latter still under way …**
- **Combining results with this BC structure, and Janesick's 130-element SC register, we can see that the ILC technical requirements are already in hand**
- **The most urgent need now is to develop the ISIS for near-term SR applications**

^{55}Fe Signal - Gary Zhang – 4 June 2009

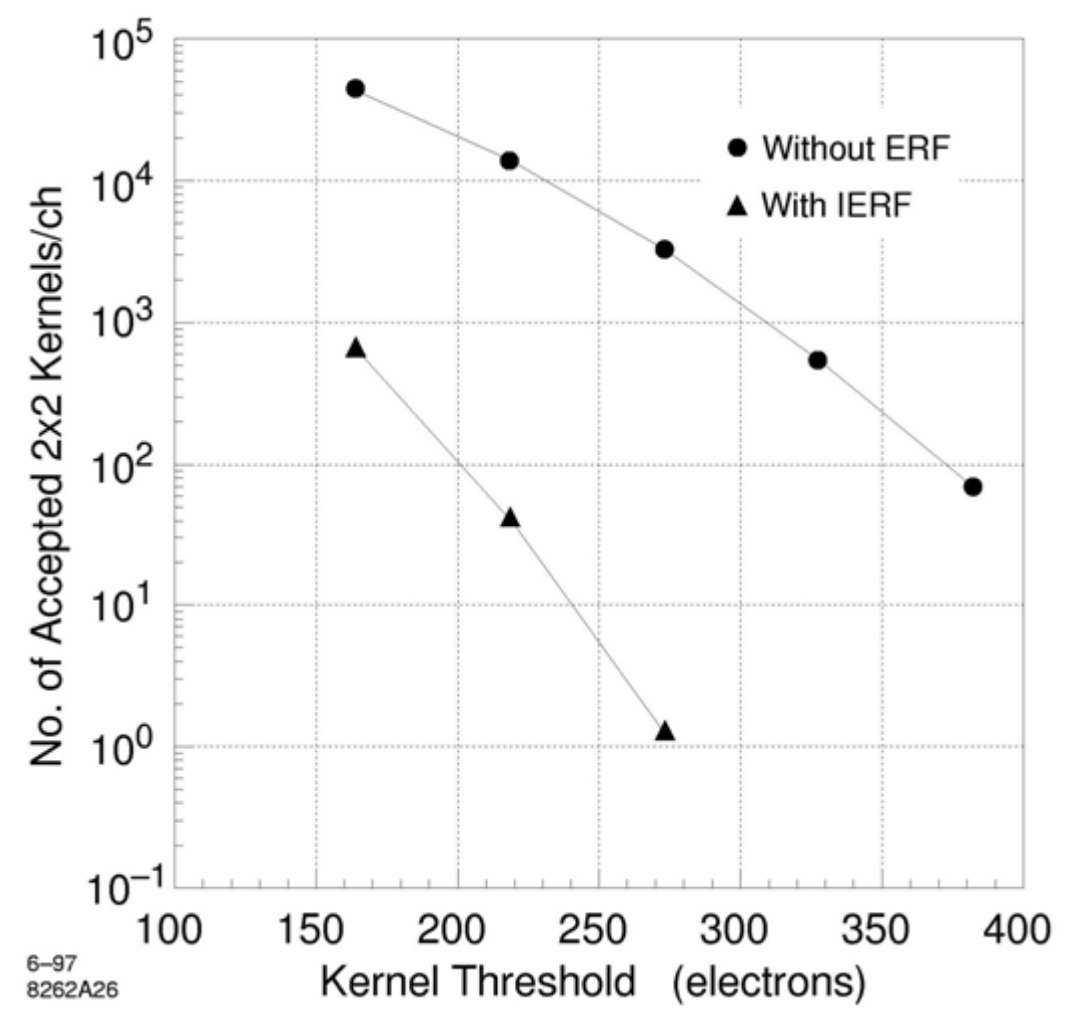


- Shaping time matched to 7 MHz readout
- in 30 years working with fast readout CCDs, we never resolved these peaks
- Promises micron precision in centroid finding for MIPs with approximately normal incidence

Extended Row Filter (ERF) suppresses residual noise and pickup:



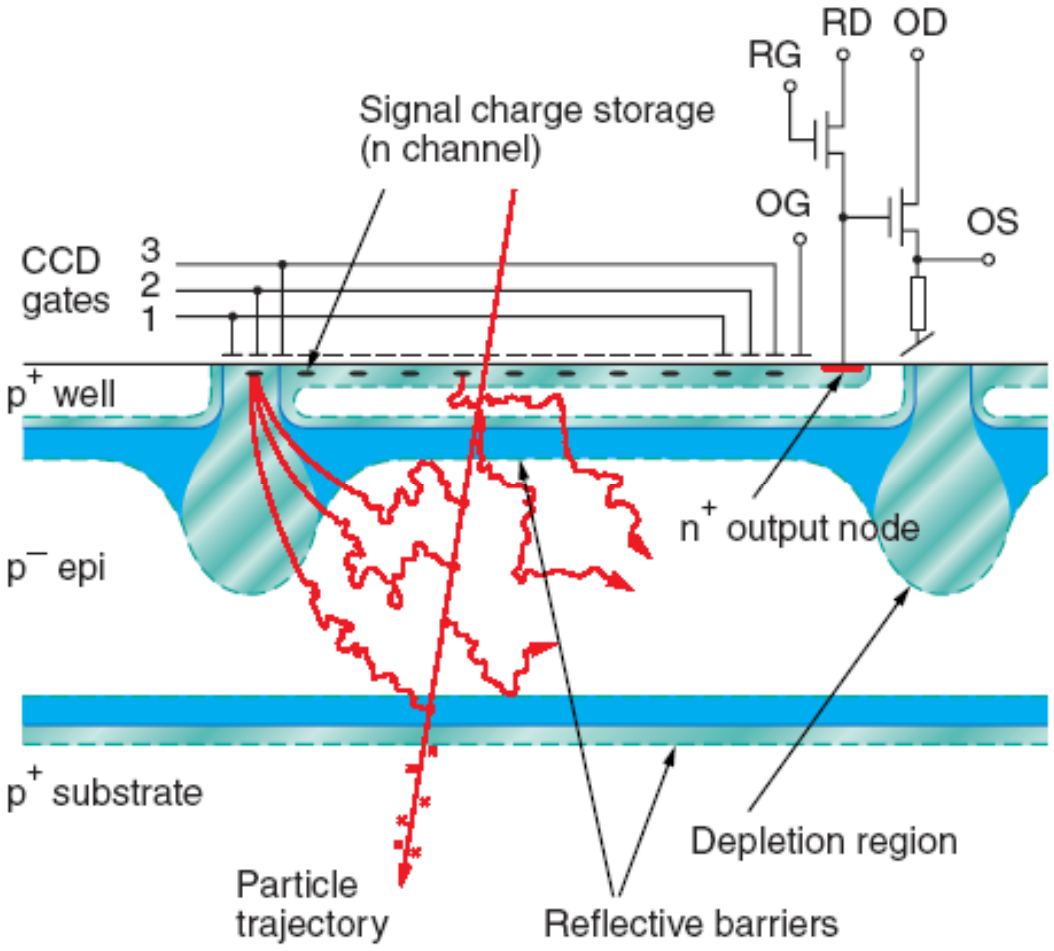
SLD



Without ERF, rate of trigger pixels would have deluged the DAQ system

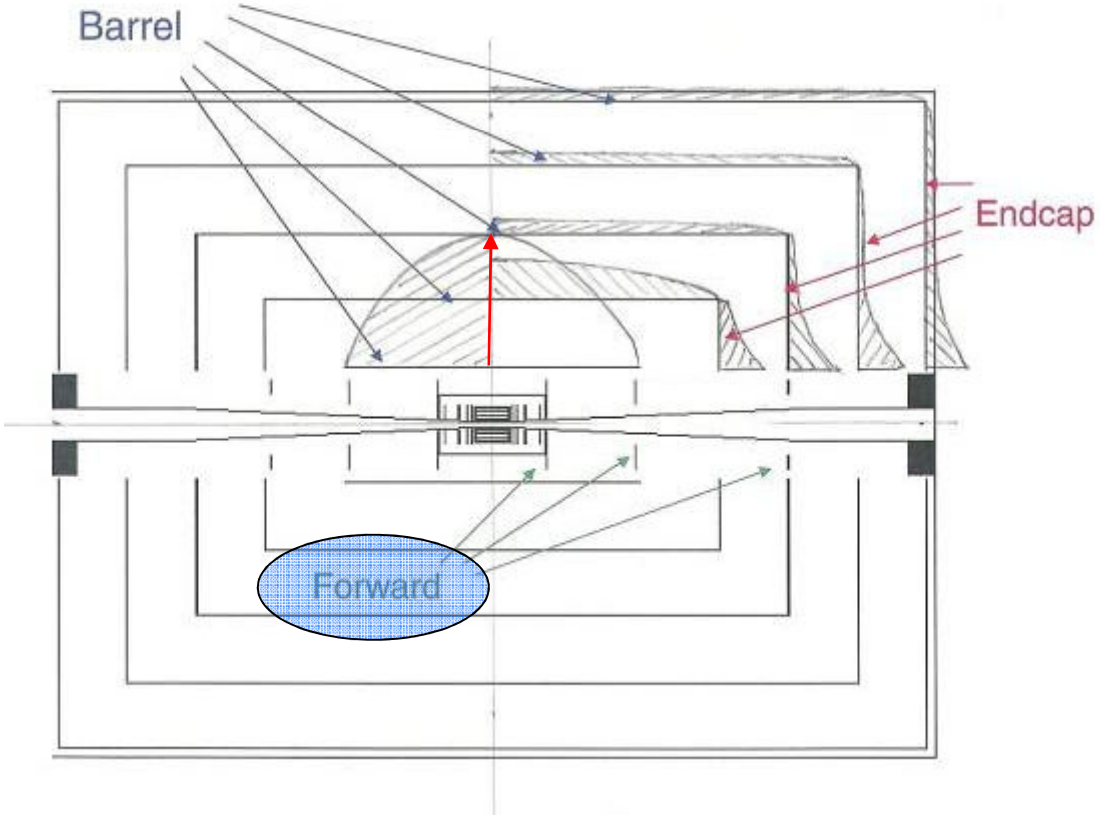
Read out at 5 MHz, during ‘quiet’ inter-bunch periods of 8 ms duration

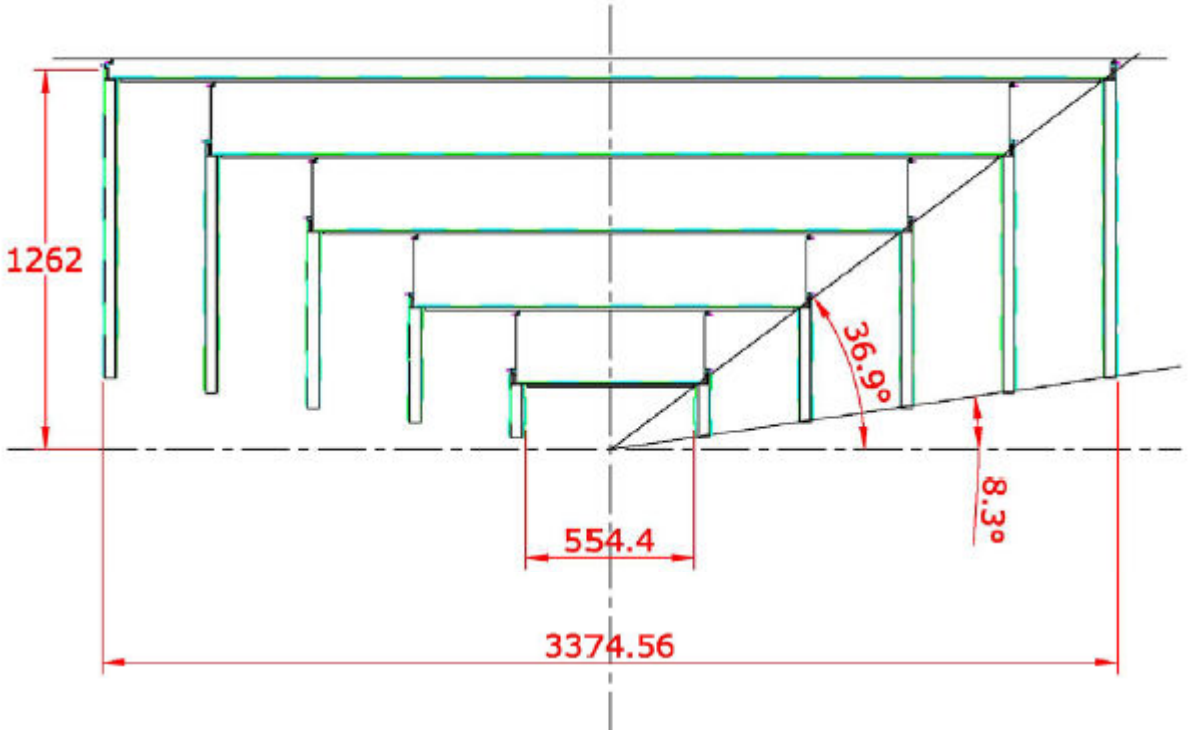
Origin of the pickup spikes? We have no idea, but not surprising given the electronic activity, reading out other detectors, etc



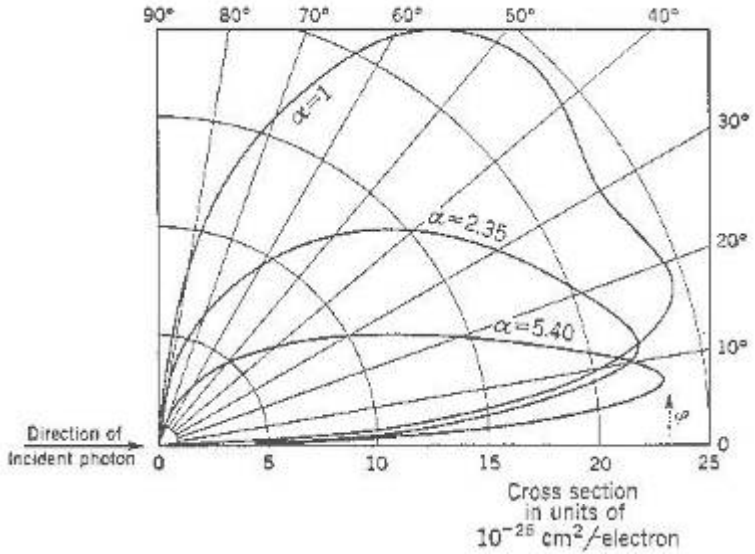
- charge collection to photogate from ~20 μm silicon, mainly by diffusion, as in a conventional CCD
- no problems from Lorentz angle
- signal charge shifted into storage register every 50μs, to provide required time slicing
- string of signal charges is stored during bunch train in a buried channel, avoiding charge-voltage conversion
- totally noise-free storage of signal charge, ready for readout in 200 ms of calm conditions between trains
- 'The literature is littered with failed attempts …'

- Total hit density ranges from 2.5/cm^2/train (layer 1 barrel) to 1/10 of that (layer 5 barrel) – occupancies in SPT are everywhere < 10^{-4}
- For the forward disks, densities exceed 600/cm^2/train, so pixels with short sensitive windows will be needed. Fortunately, area to be covered is small



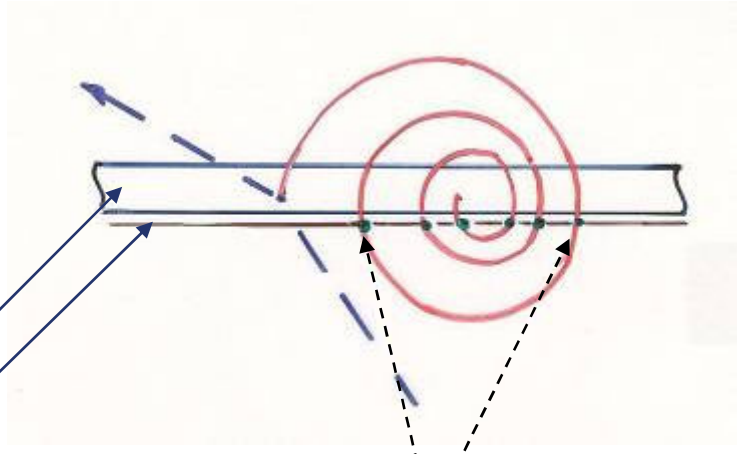


- Barrel and Forward trackers, total area = 70.3 m^2
- With 50 μm × 50 μm pixels – 28.1 Gpix system
- If each chip is 8 cm × 8 cm (2.6 Mpix): 11,000 sensors is total



Evans, p 691: photon energies 0.51, 1.2 and 2.76 MeV; electron angular distns

barrel ladder, rϕ view

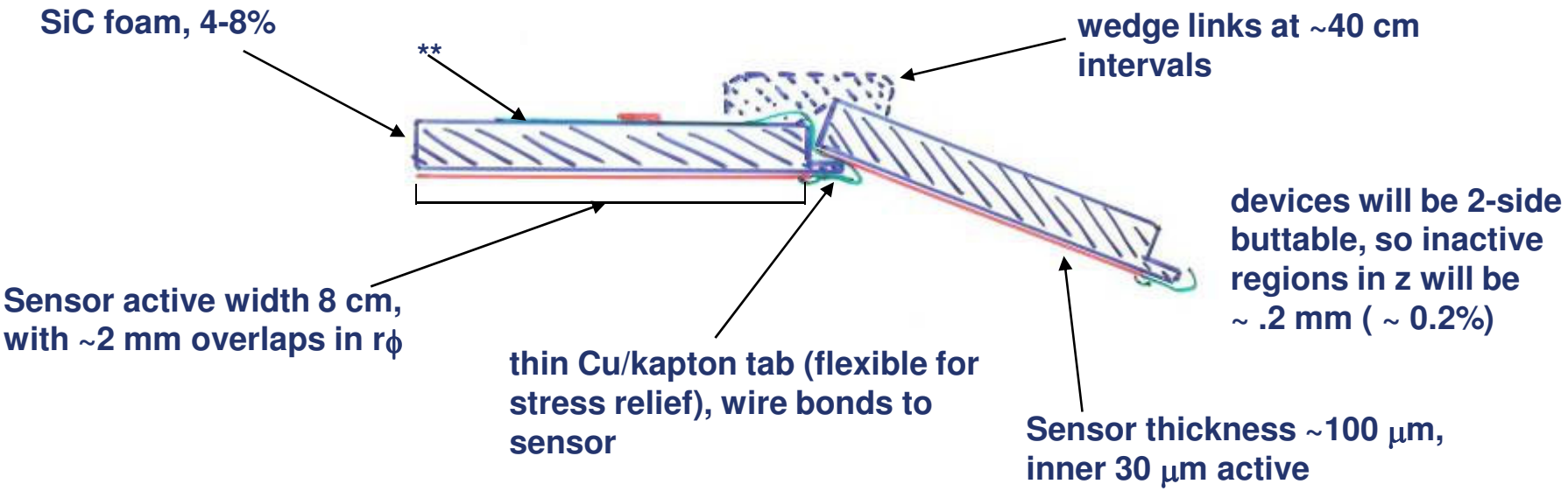


~0.5% X_0 support foam and Cu-kapton

~0.1% X_0 silicon, 30 μm active on inner surface

6 hits, stepped in z, each hit indistinguishable from min-I

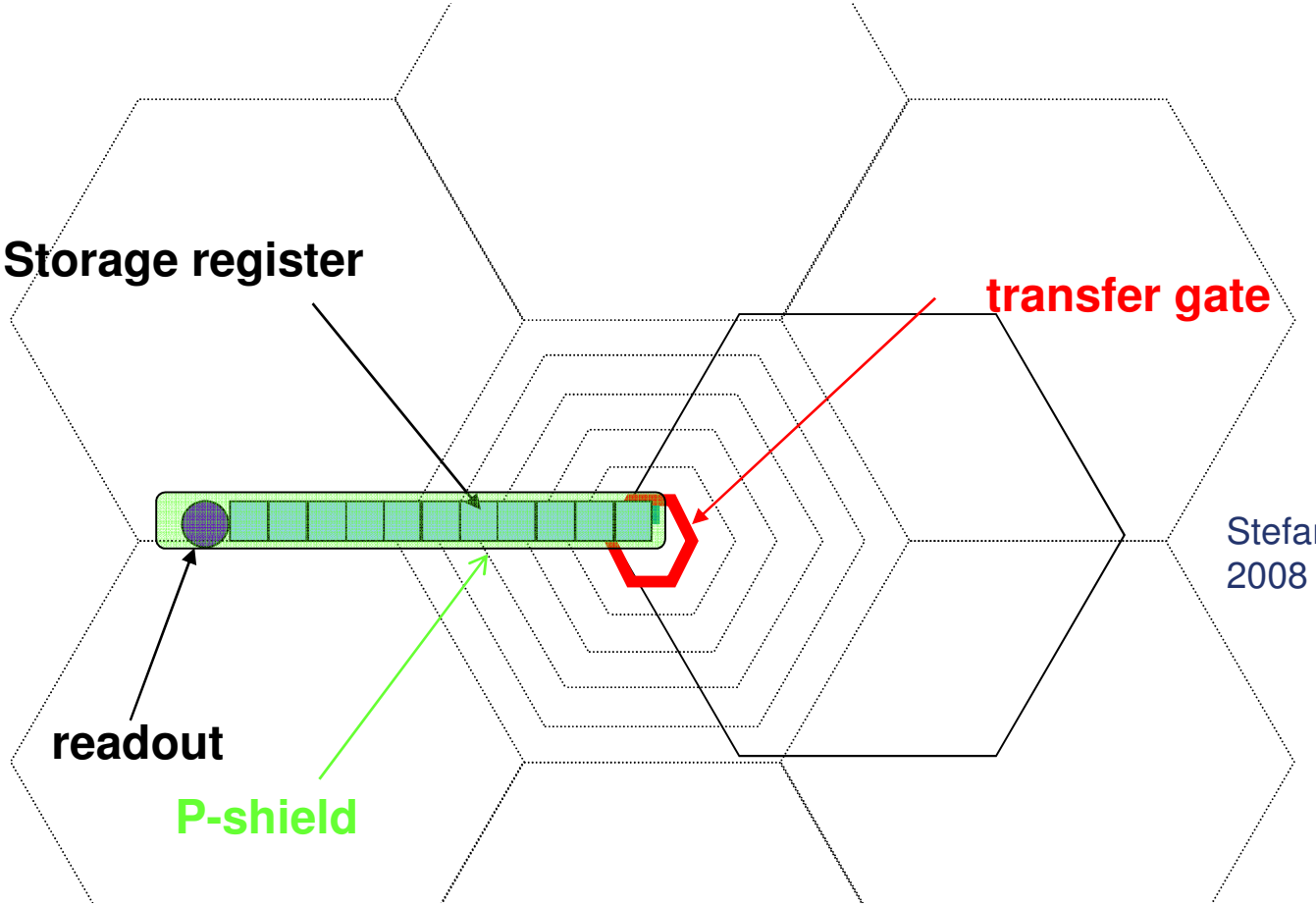
End view of 2 barrel ladders ('spiral' geometry)



** single layer Cu/kapton stripline runs length of ladder, double layer in region of tabs (~5 mm wide) which contact each sensor. Single Cu/kapton stripline runs round the end of each barrel, servicing all ladders of that barrel

Bottom line: potential material budget ~0.6% X_0 per layer, but much design and R&D needed to establish mechanical stability, including shape stability wrt push-pull operations (taking advantage of stress-free 3-point kinematic mount)

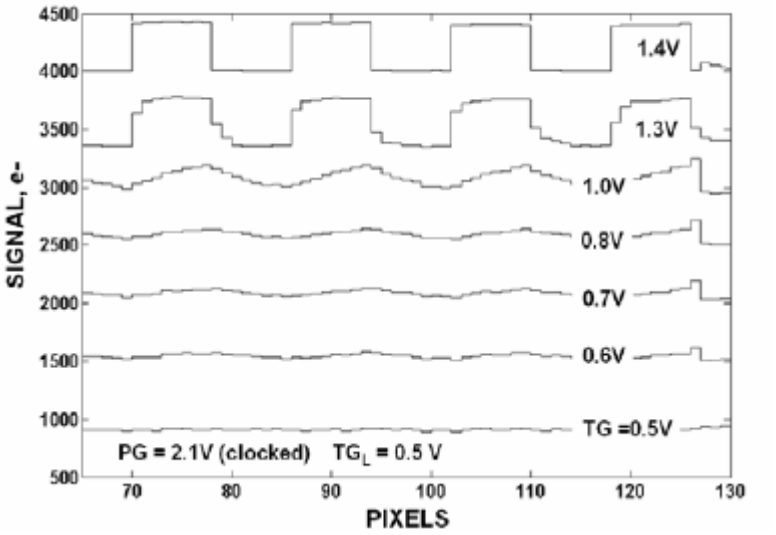
Silicon Pixel Tracker for ILC (not CLIC) forward region

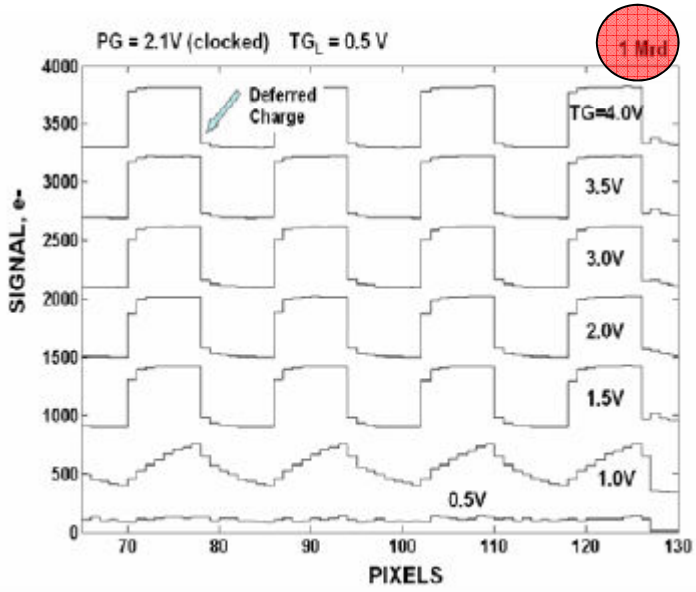


Stefanov, Sendai LC wkshop, 2008

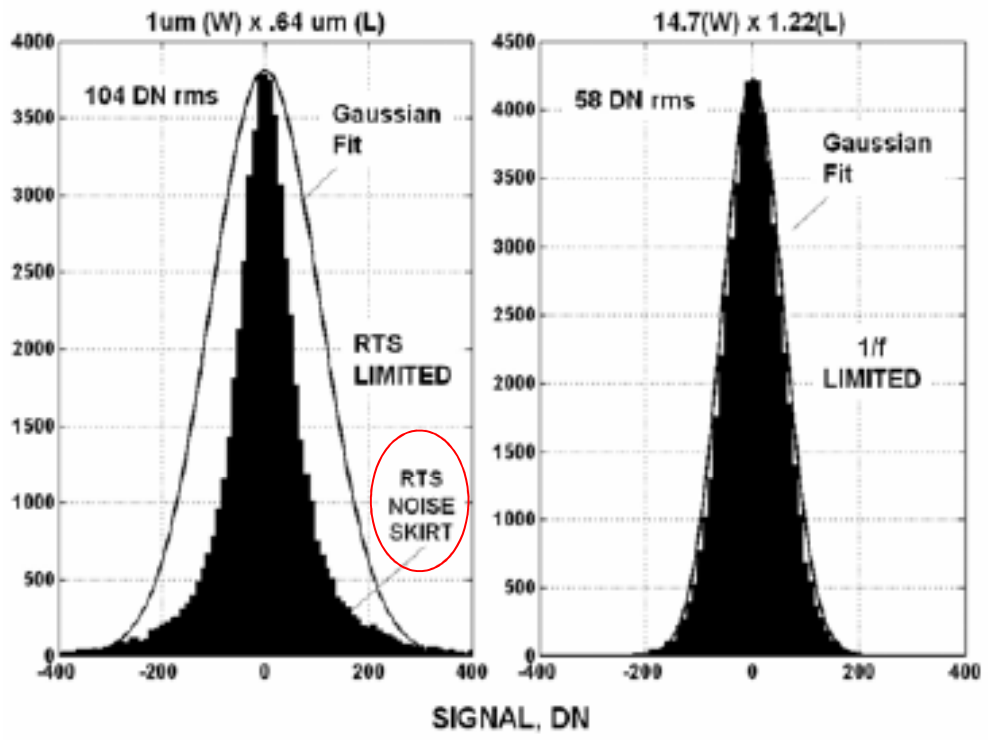
- **This ISIS structure (initiated for ILC vertexing) is also of interest as a fast-frame burst camera for X-ray imaging at 4th generation light sources (LCLS and XFEL)**
- **For the x-ray application, fully deplete (currently 30 kΩ-cm epi is available), and back-illuminate: soft X-rays: direct conversion**
  hard X-rays: via columnar CsI

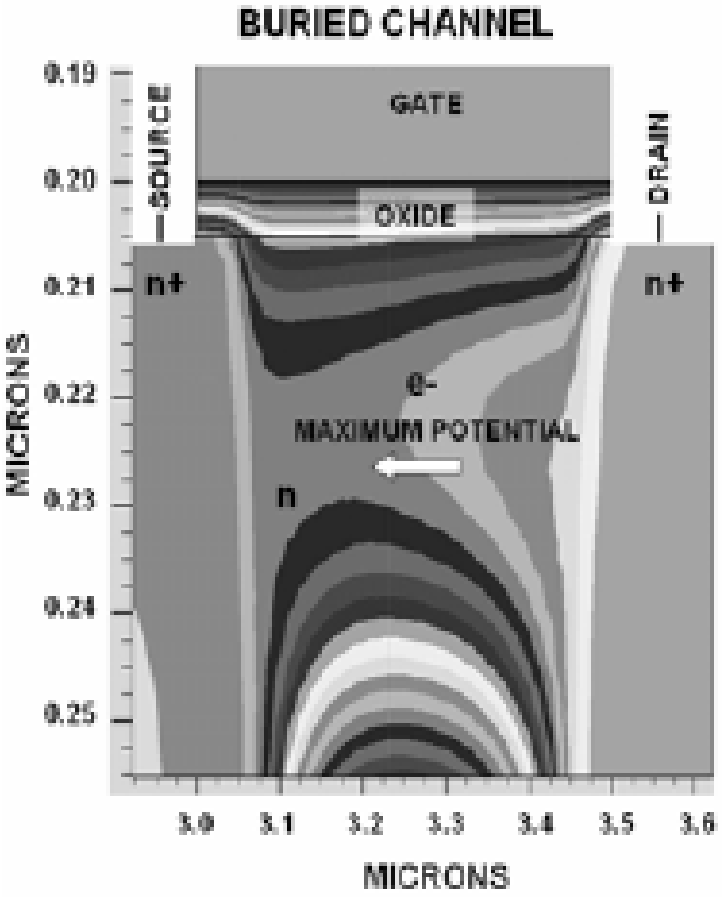
- Due to the small pixel sizes, even surface channel devices perform well
- Usable up to 1 Mrad ionising radiation (need 2.6 V higher TG amplitude), and this is only the beginning

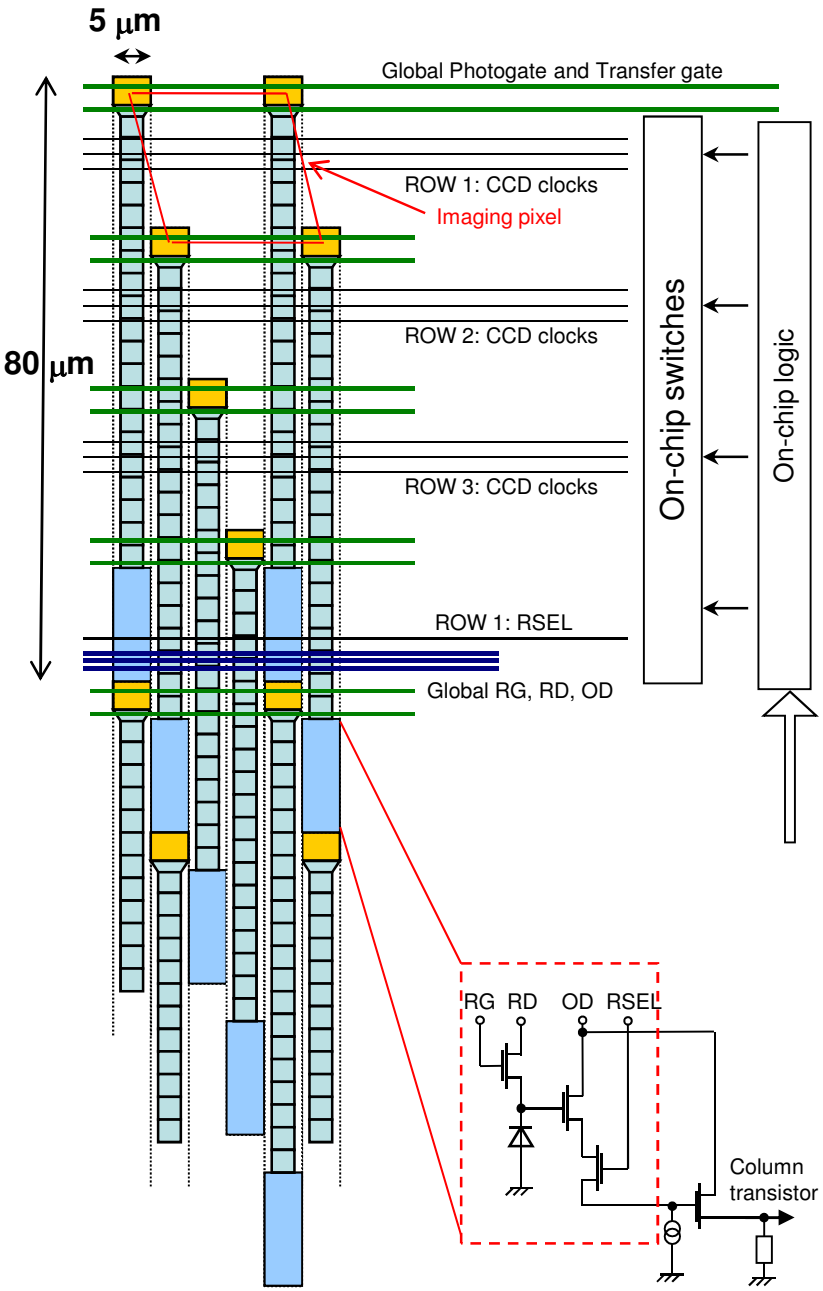




Janesick 2009

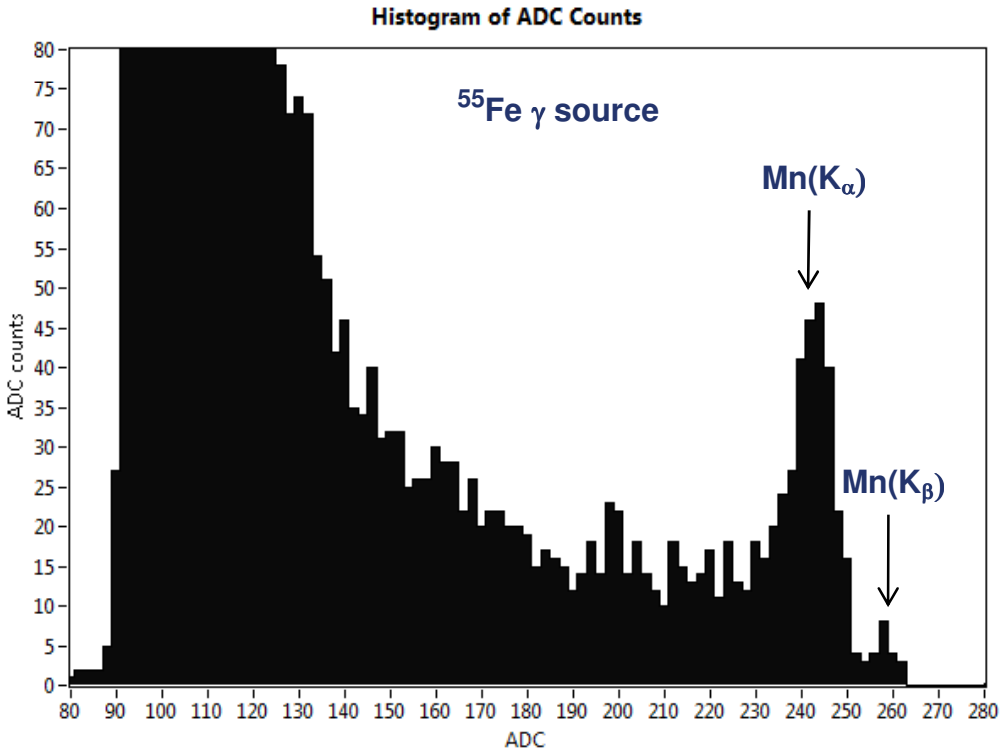

1um (W) x .64 um (L)
104 DN rms
Gaussian Fit
RTS LIMITED
RTS NOISE SKIRT
14.7(W) x 1.22(L)
58 DN rms
Gaussian Fit
1/f LIMITED
SIGNAL, DN


BURIED CHANNEL
SOURCE
GATE
DRAIN
OXIDE
n+
n+
e-
MAXIMUM POTENTIAL
n
MICRONS
MICRONS



- **For ILC vertexing, photogate area is reduced to a minimum, to achieve approximately 20 μm square imaging pixels, much smaller than needed for tracking**

- **We are already close to this with our ISIS-2 prototypes – we have 10x80 μm storage pixels**



ISIS: Imaging Sensor with In-situ Storage

- Pioneered by W F Kosonocky et al IEEE SSCC 1996, Digest of Technical Papers, p 182
- Current status: T Goji Etoh et al, IEEE ED 50 (2003) 144
- Frame-burst camera operating up to 1 Mfps, seen here cruising along at a mere 100 kfps – dart bursting a balloon
- Evolution from 4500 fps sensor developed in 1991, which became the de facto standard high speed camera (Kodak HS4540 and Photron FASTCAM)
- International ISIS collaboration now considering evolution to 10^7 – 10^8 fps version!