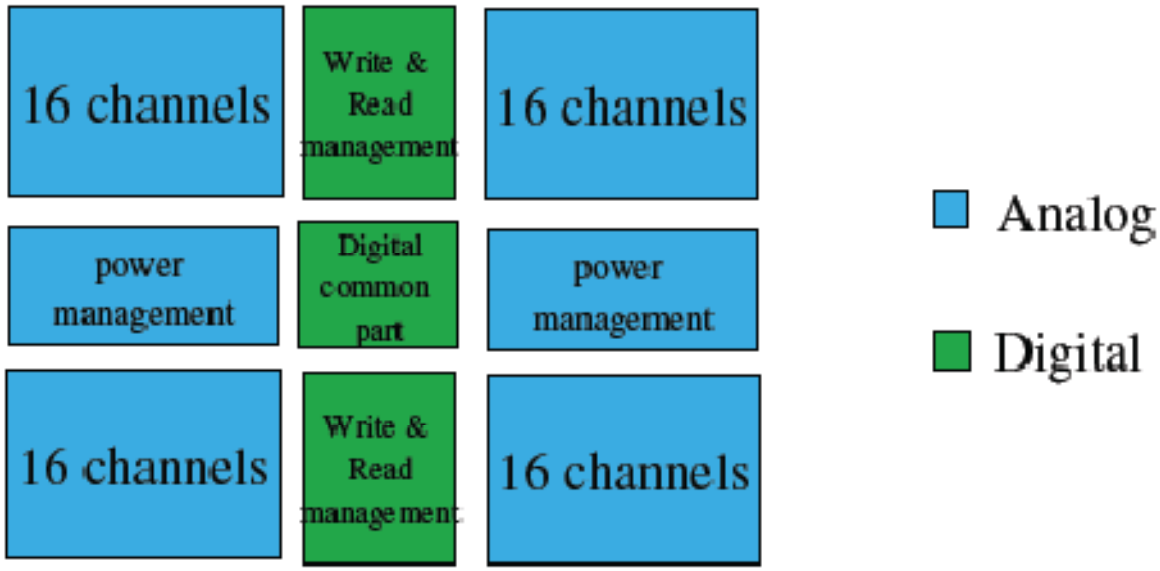
Brief summary of the present SiTR_130-128 version

T.H. Hung, L. Vaubien, A.S.N

SiTR_130-128 new design: status

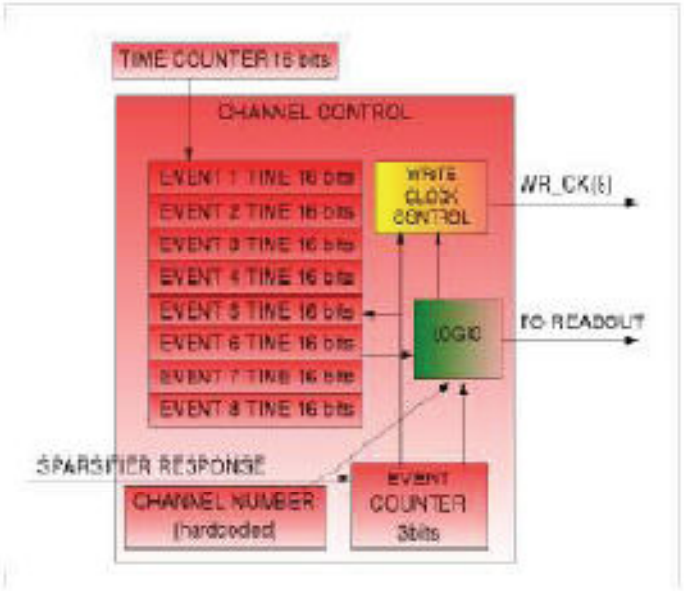
It was decided to implement a new architecture for the chip based on a more modular design and trying to include 128 channels in a single chip, size 5x10mm2.
This new architecture implies an elementary module organized as shown here below and gathering 64 channels. The chip contains 64x2 channels organized this way.



The read & write management follows the same features as the ones defined in The previous design; namely:

Write & Read management block contains:

- Channel control:



Maximum 4 events per channel to memorize.

With "logic" block consisting essentially in a finite states machine.

Generates signals to control conversion, calibration ...

The readout control as well:

- Readout control:

One register per channel with parallel writing and serial readout.

Digital common part generates and manages signals common to the channels.

The analog part is almost finalized except from parasitic analysis for ADC's.

Digital part is coded, simulated before synthesis and synthesized.
Simulation after synthesis and formal verification have to be done.
Then we plan to perform mixed signal simulation before placing and routing the digital part.

We intend to organize as soon as possible a discussion with our colleagues from B.U. on a number of still opened issues