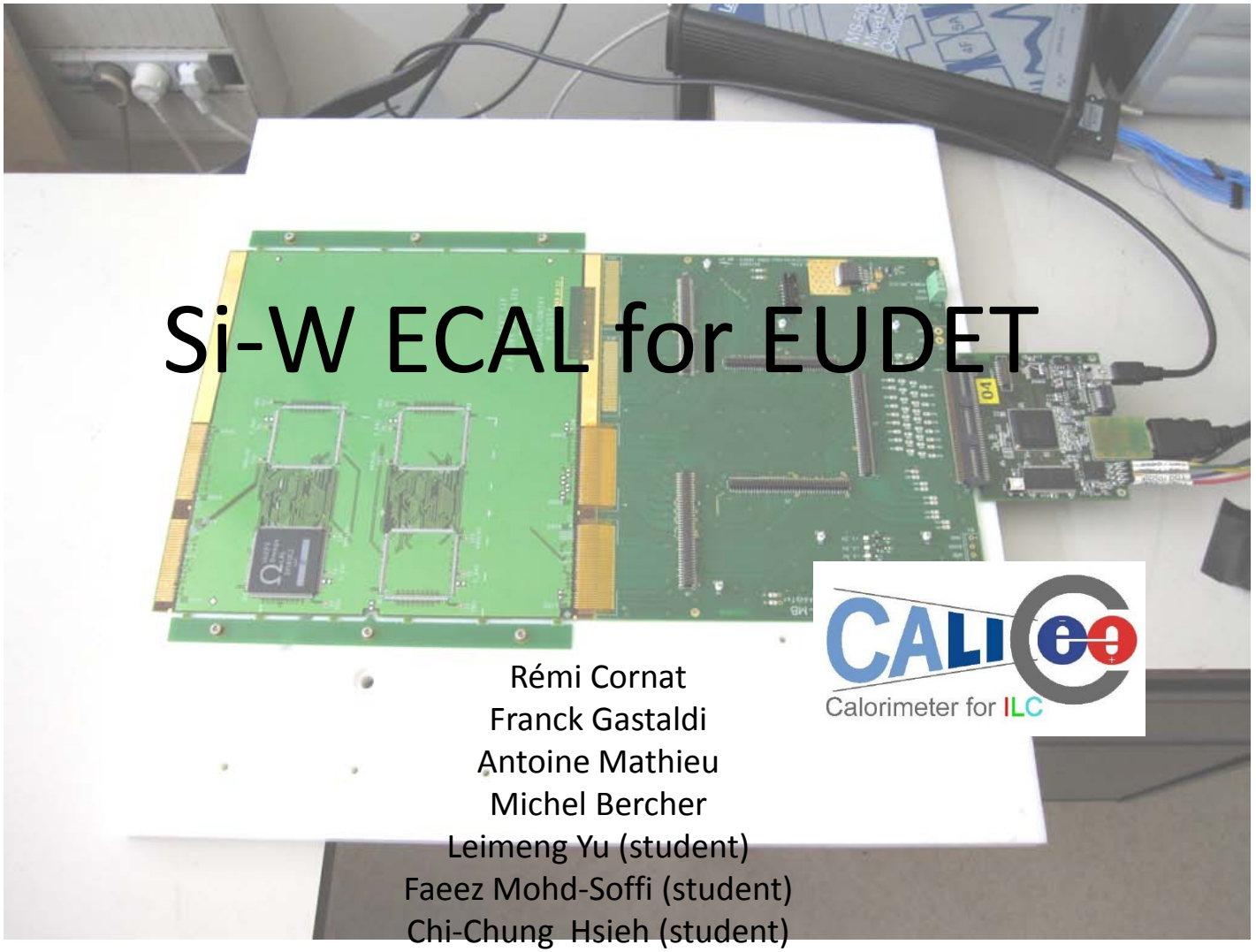

# Si-W ECAL for EUDET

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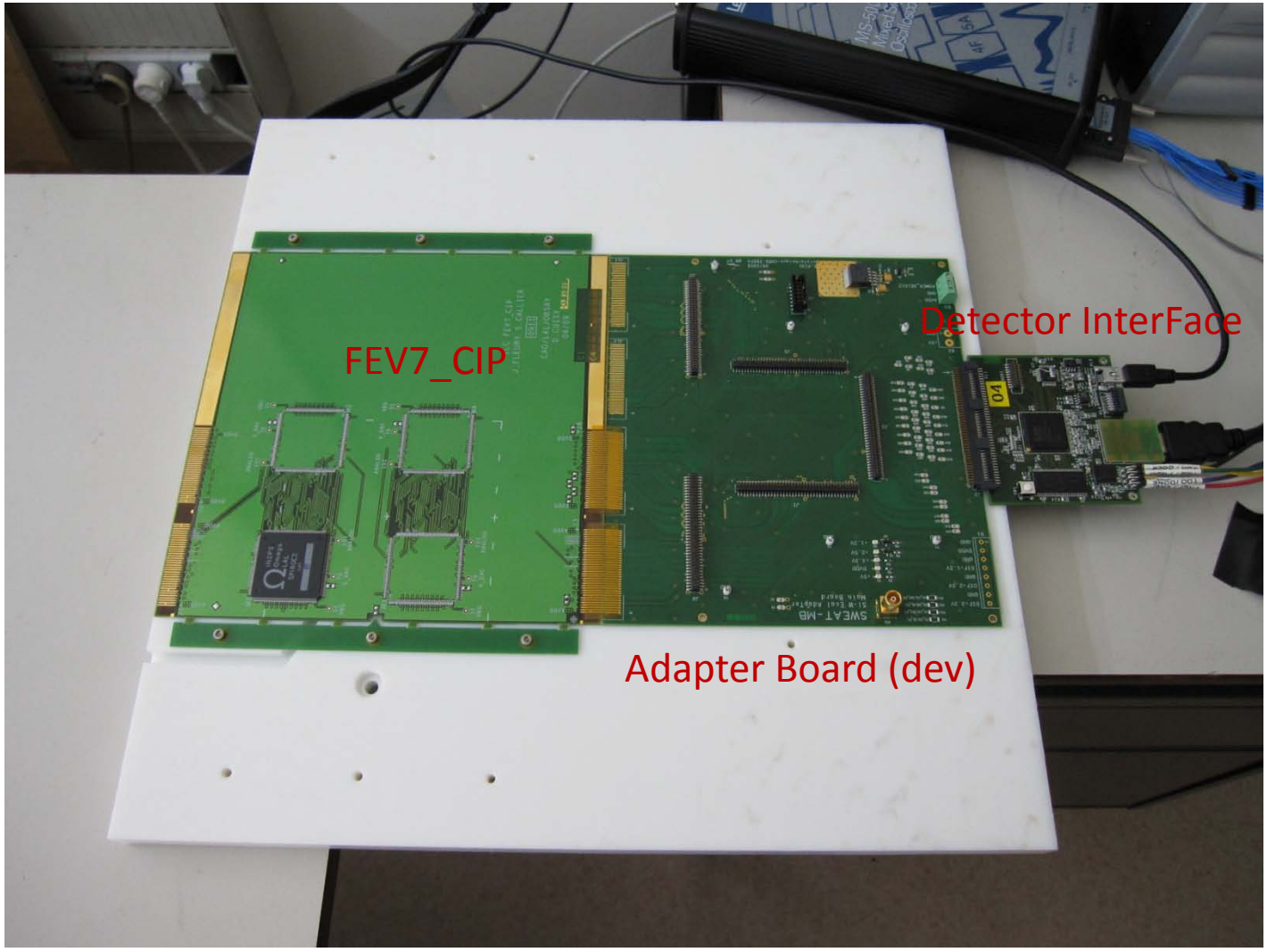
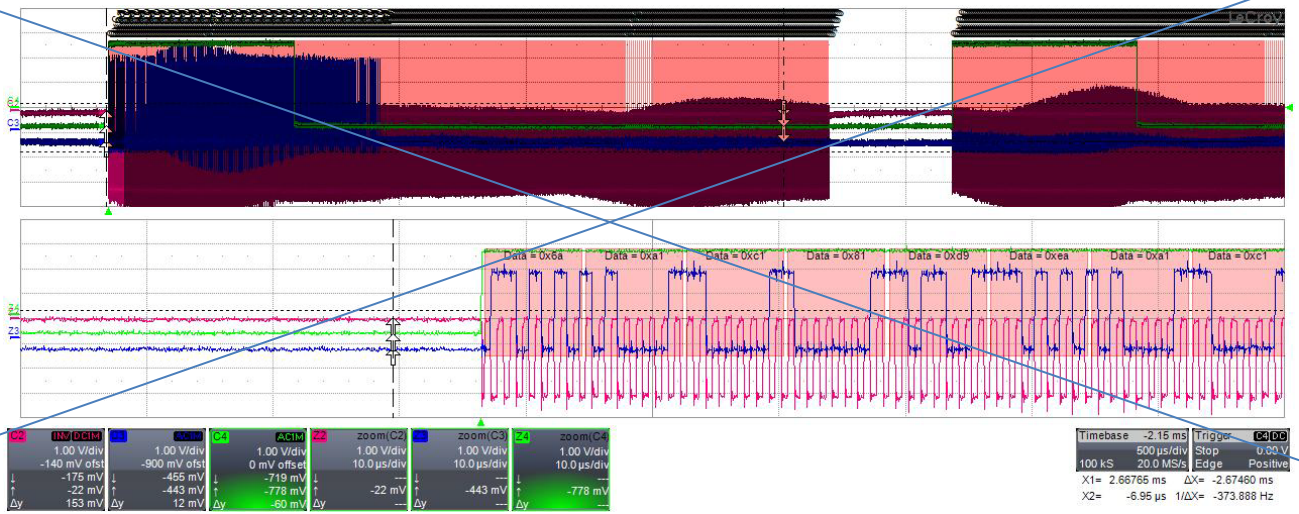
# First SLAB prototype assembled (03/07/09)

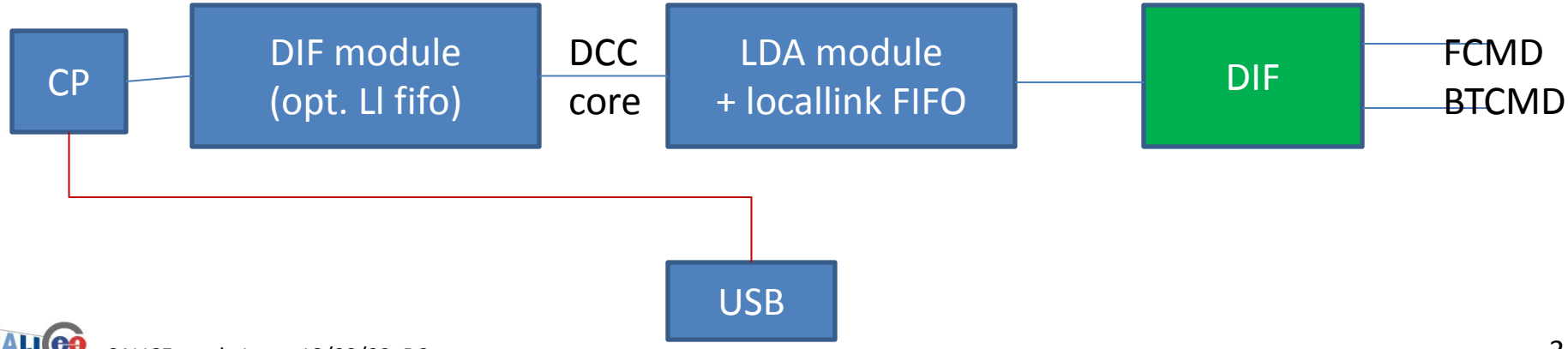


# HW tests

- Slow control the ROCs (without ROCs)



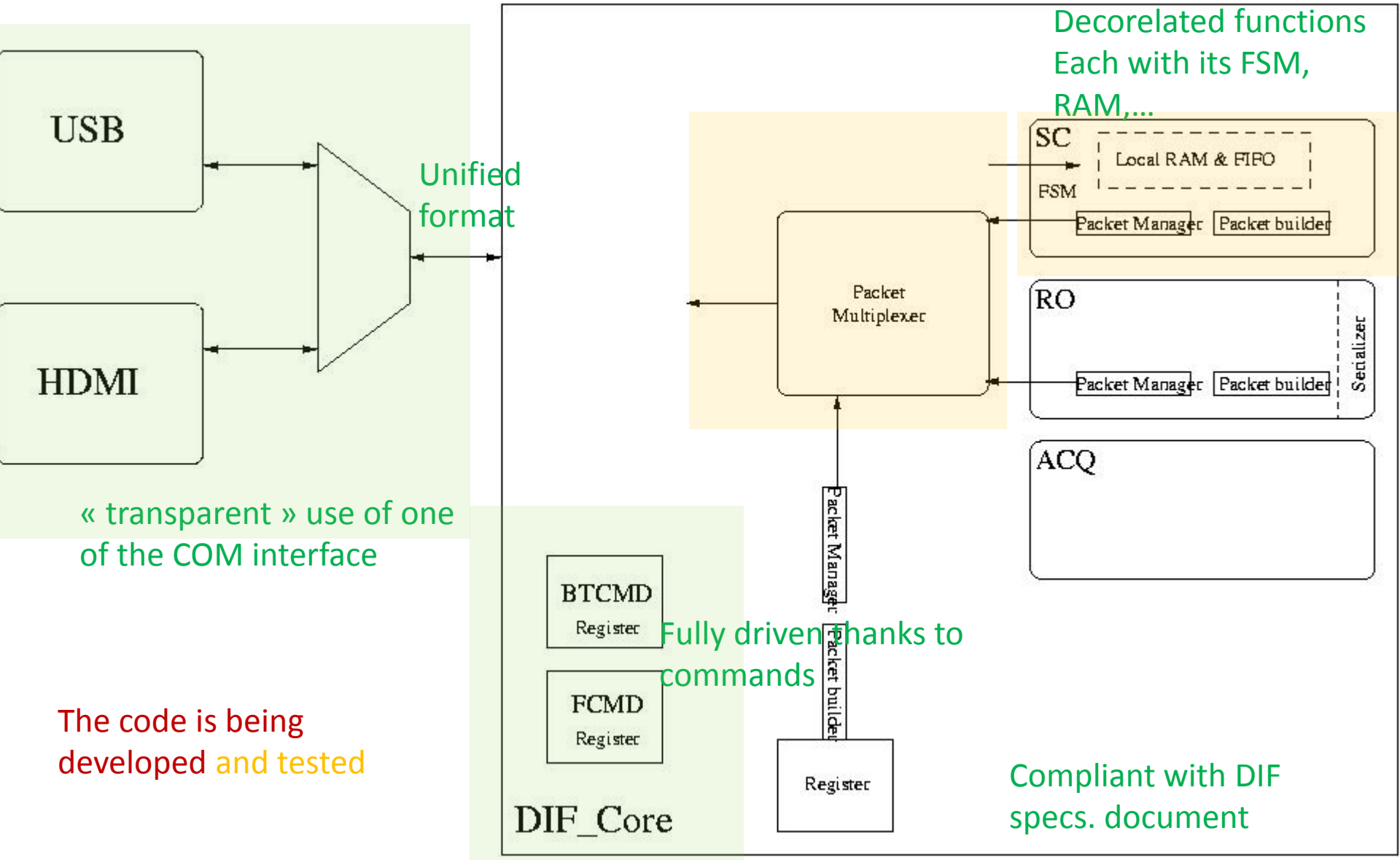

- CMD generation through HDMI



# CMD generation through HDMI

- Two cascaded DCC
  - USB – DIF-LDA-DIF-LDA-DIF
- Fast commands
- Block transfer commands (few tested)
- Unfortunatemy we changed test room
  - Only fast commands are working now

# DIF : basic version




« transparent » use of one of the COM interface

Fully driven thanks to commands

The code is being developed and tested

Compliant with DIF specs. document

# Dev. environment

- File lists
- LDA emulator
  - Bypass port (sim only)
  - USB
  - LDA module (to be updated soon)
    - Already exist for the DCC dev.
- Cadence NC (IUS)
- Modelsim
- Synplify + ISE

# HDL

```
type slabsc_t is record
  srout_int     :  std_logic;
  srin_int      :  std_logic;
  clk_int       :  std_logic;
  resetn_int    :  std_logic;
  load_int      :  std_logic;
end record;
```

- Use of RECORD types
  - Bundle of signals
  - Ports of same direction
  - Very readable code
  - Hierarchy automatically updated
  - Easy modifications
- Agreement ?

# I/O bloc

# Data flow ?

- I/O bloc
- Downstream
  - RX port
  - PKT decoder (header decoder)
  - Data flow directed to
    - FCMD
    - CMD
    - DATA
  - DATA : adresses for final receiver ?
- Upstream
  - Data generation in functions
  - Packet formatter
  - Packet queue
  - Packet mux
  - Send queue
  - TX port

# Questions

- I/O port select
  - USB poweren
  - Activity
- Standard internal interfaces
- RST
- Main FSM : state transition conditions
- CMD acknoledge
- DIF registers ?
- Use of the SC ram
- …