AHCAL Electronics.

Status Commissioning

Mathias Reinecke
for the AHCAL developers
HCAL main meeting
Hamburg, Dec. 10th, 2009

HELMHOLTZ GEMEINSCHAFT

CALICE Calorimeter for ILC

EUDET

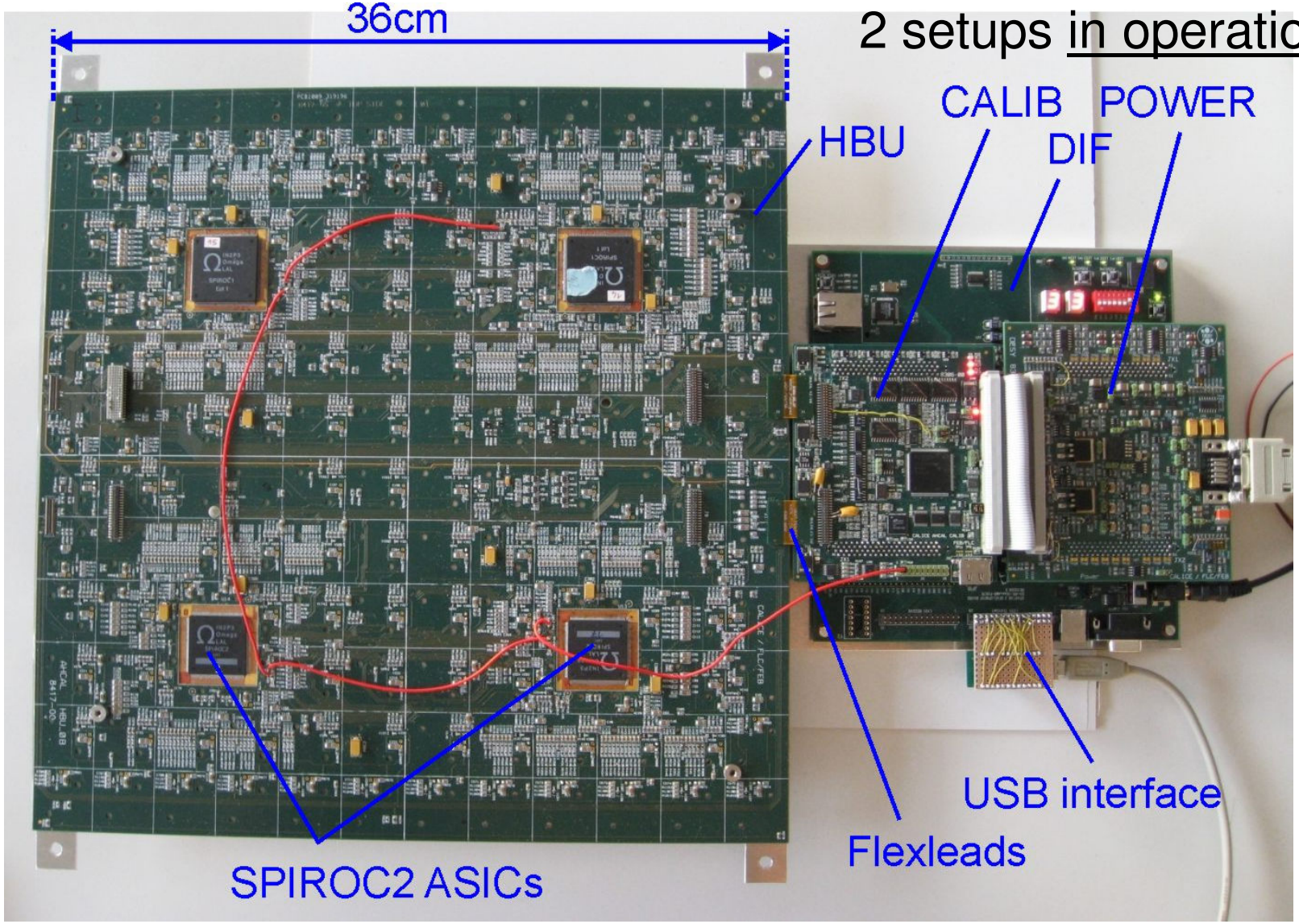
DESY

Outline

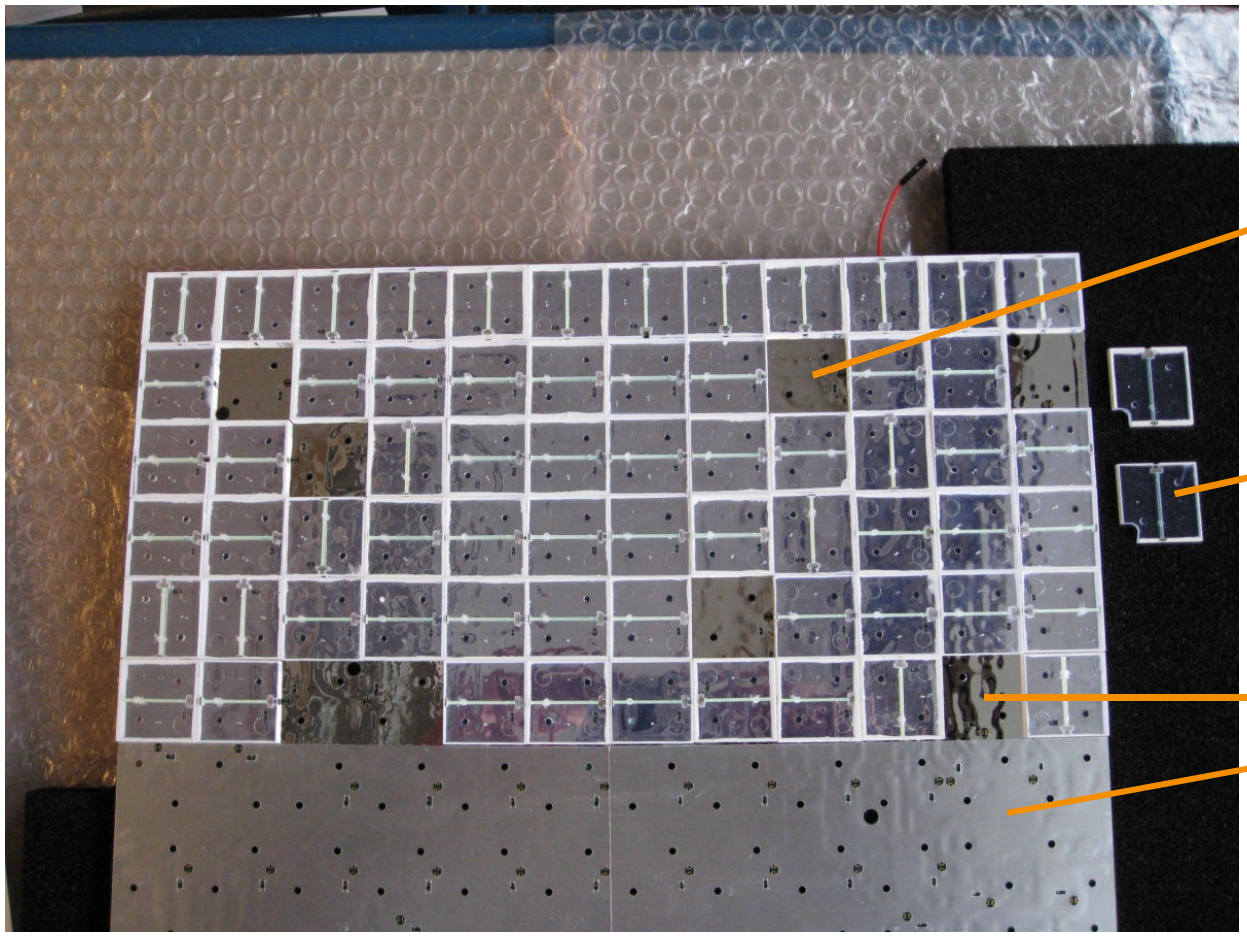
- System Commissioning
  - Labview DAQ operation
  - First Results
- Testbeam Preparation
- The Next Generation
- Conclusions and Outlook

DESY

HCAL Base Unit (HBU) and system setup



Tile Assembly – HBUII SPIROC2 area

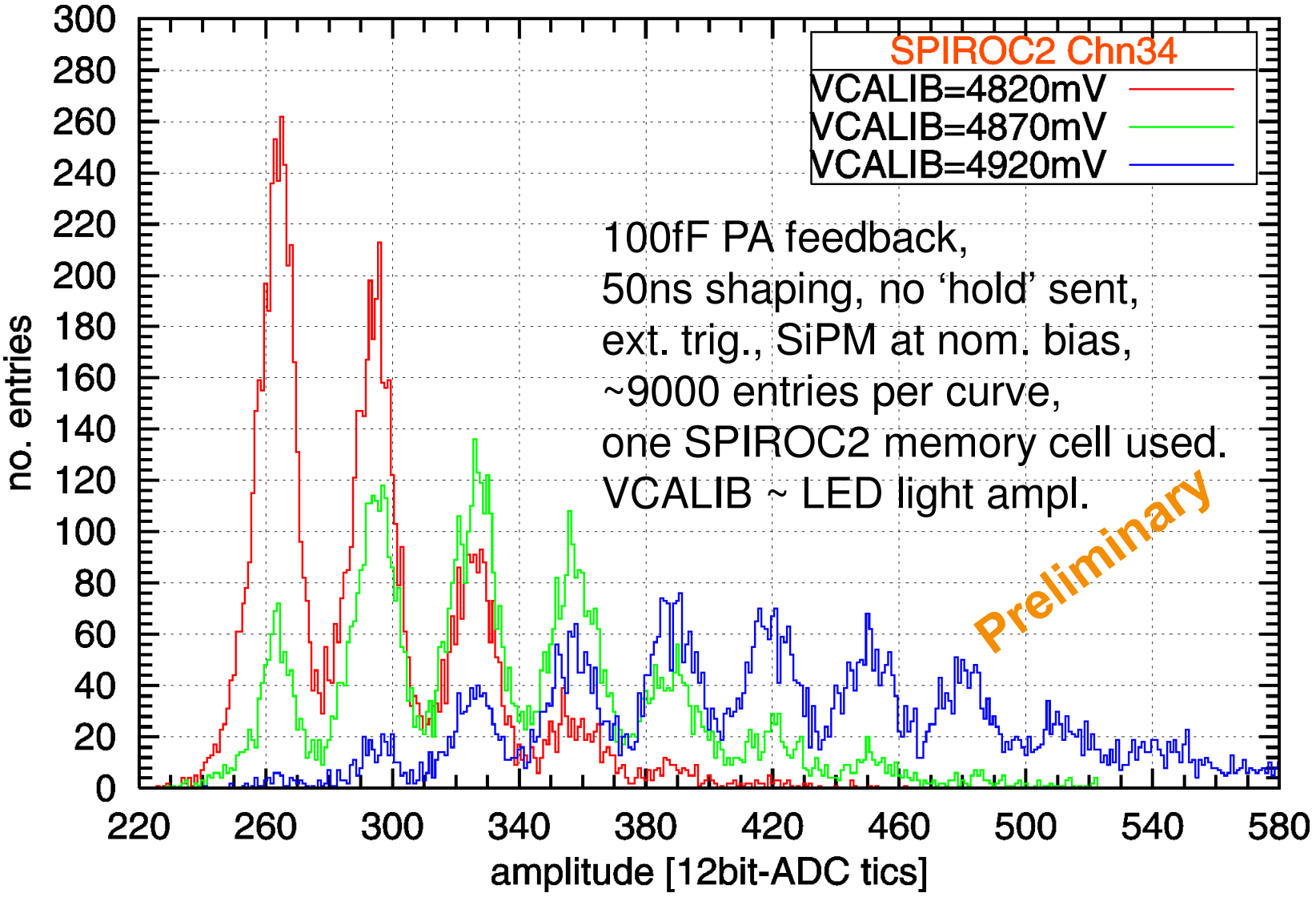


Some positions cannot be assembled (tiles do not fit in)

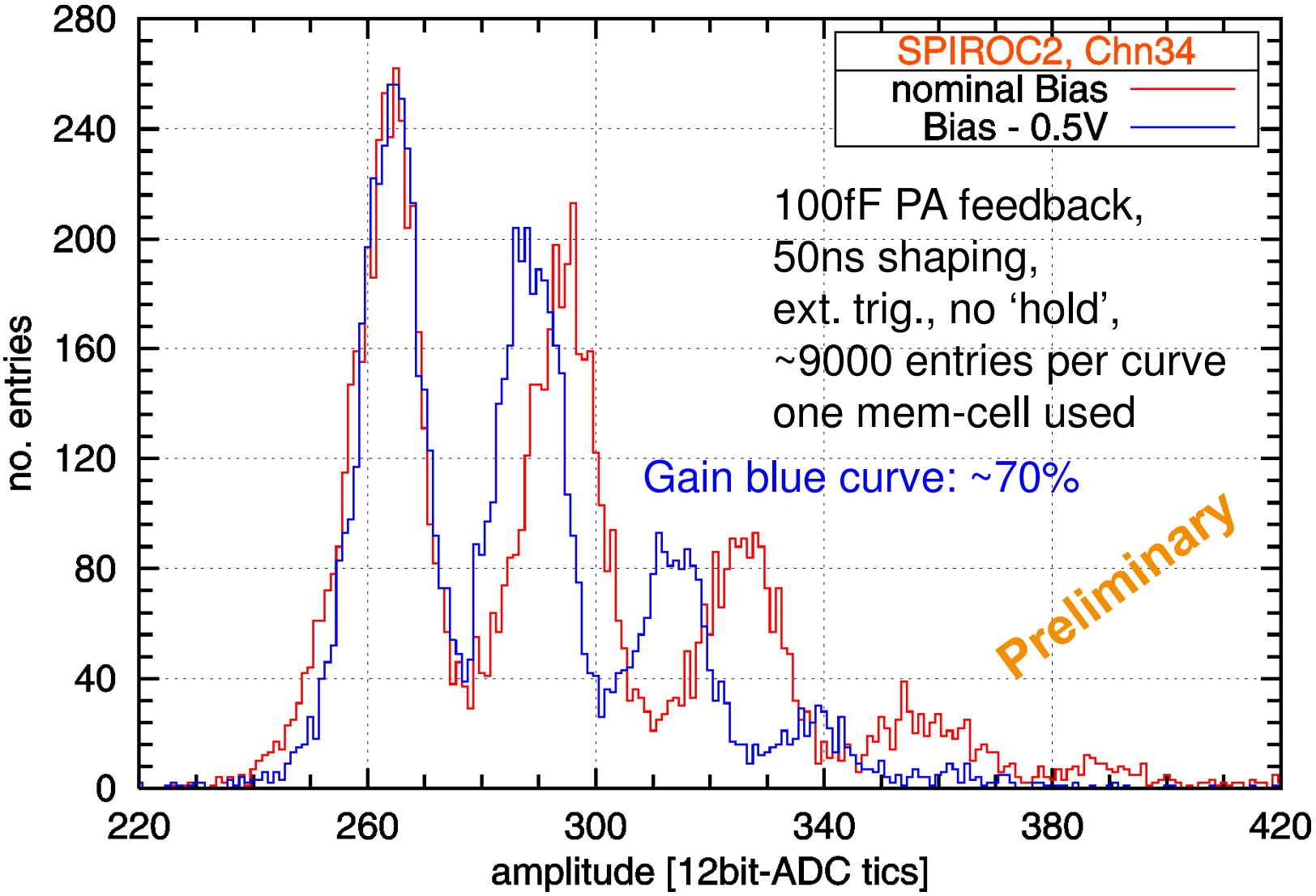
“mechanics tiles” (cassette construction)

Reflector foil:
without cover (blank)
still with cover

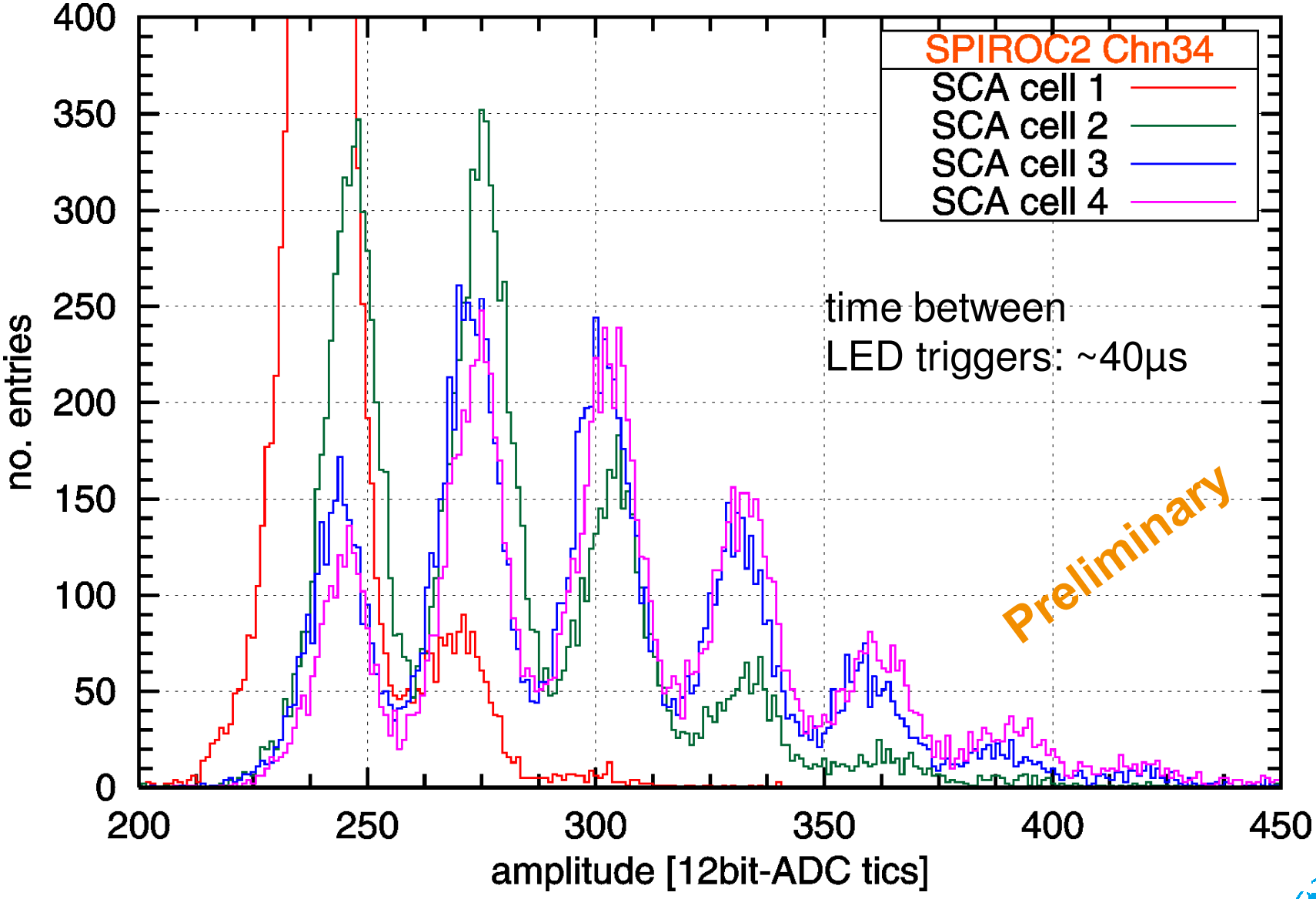
Single-Photon Peaks I



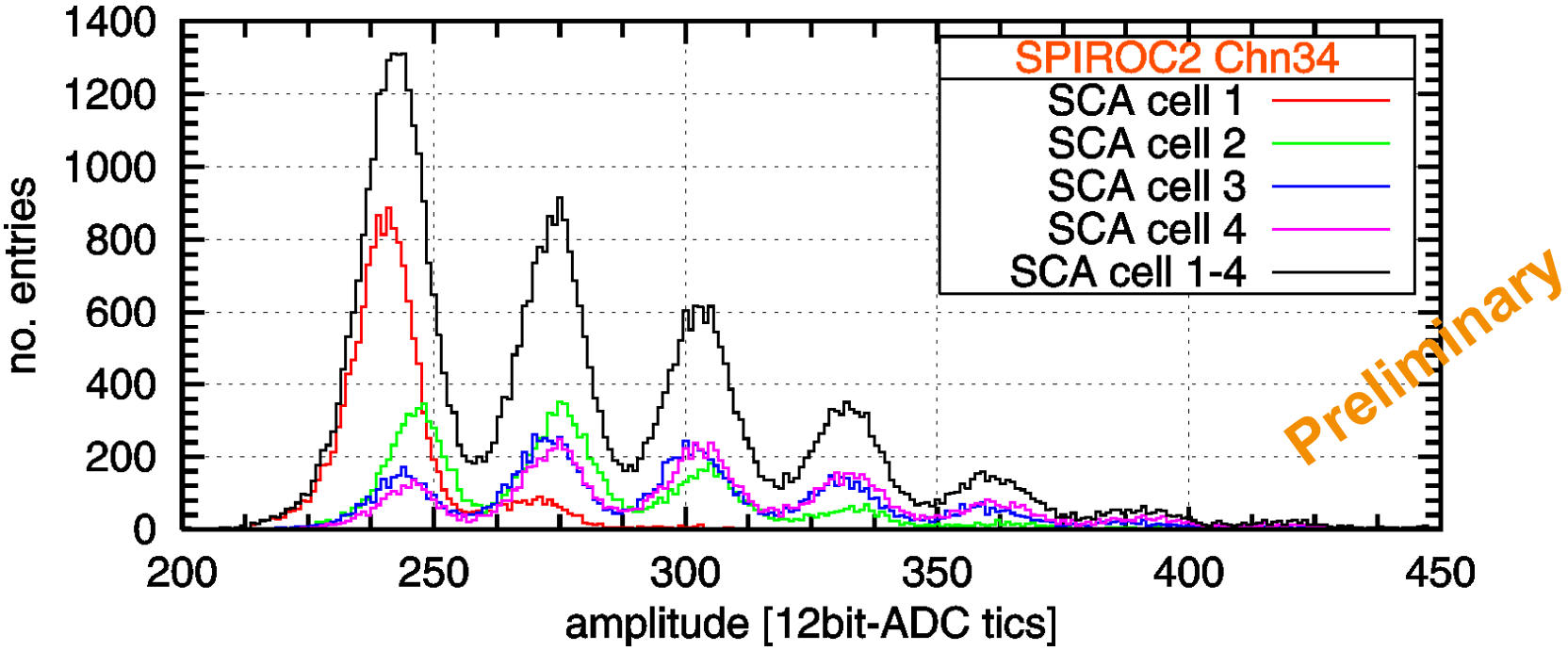
Single-Photon Peaks II (reduced SiPM bias)



Single-Photon Peaks III (SPIROC2 SCA test)



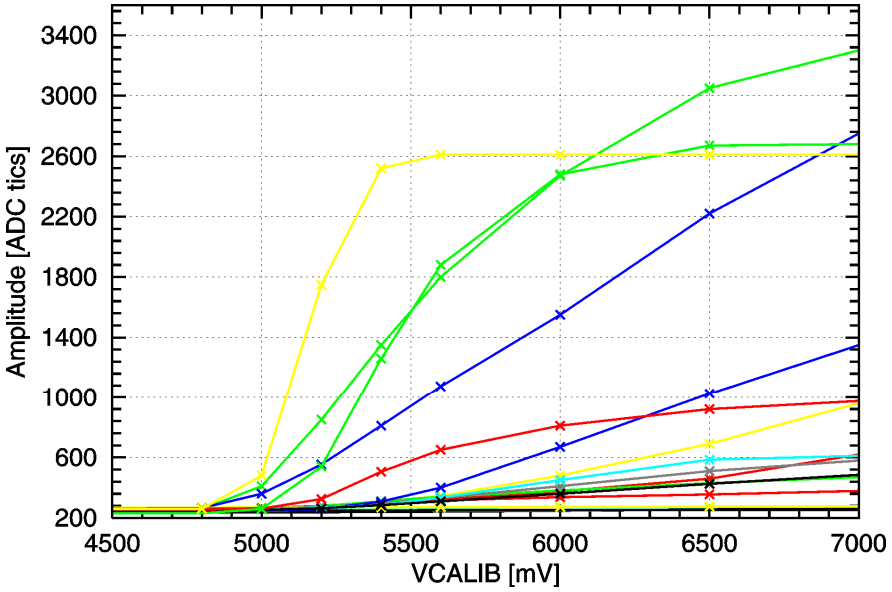
Single-Photon Peaks III (SPIROC2 SCA test)



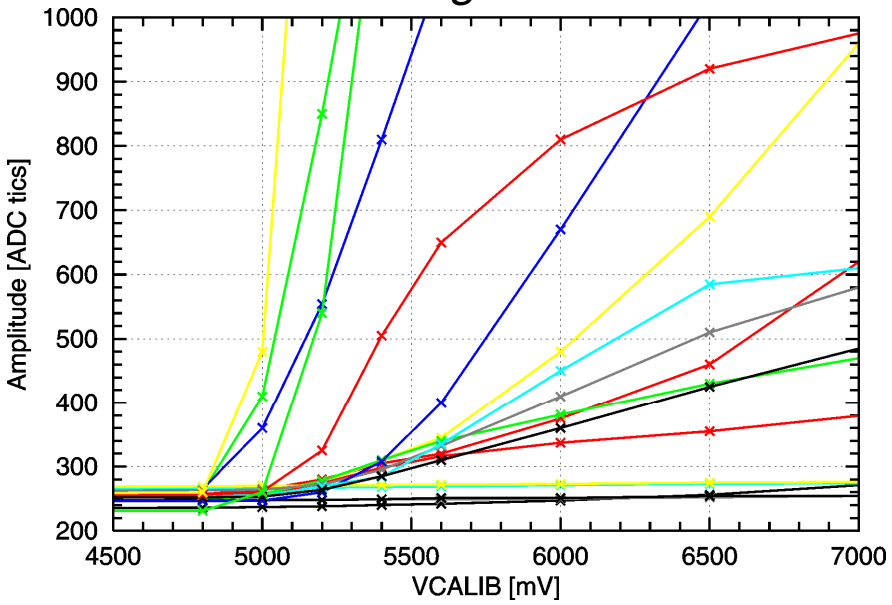
- Different light amplitudes due to integrated LED system, but reason unknown (no level shifts of GND or VCALIB observed).
- Offset may be due to SCA cells, or due to GND level shifts.
- Without correction, sum of SCA cell results (black curve) should not be used.

integrated LED system – dynamic range

SPIROC2: 400fF PA feedback, 50ns shaping, results for 18 assembled channels shown



Zoom of Fig. on the left



- LED comp-to-comp spread is large => preselection necessary.
- Dynamic range: Change LED capacitor? VCALIB max = 10V.

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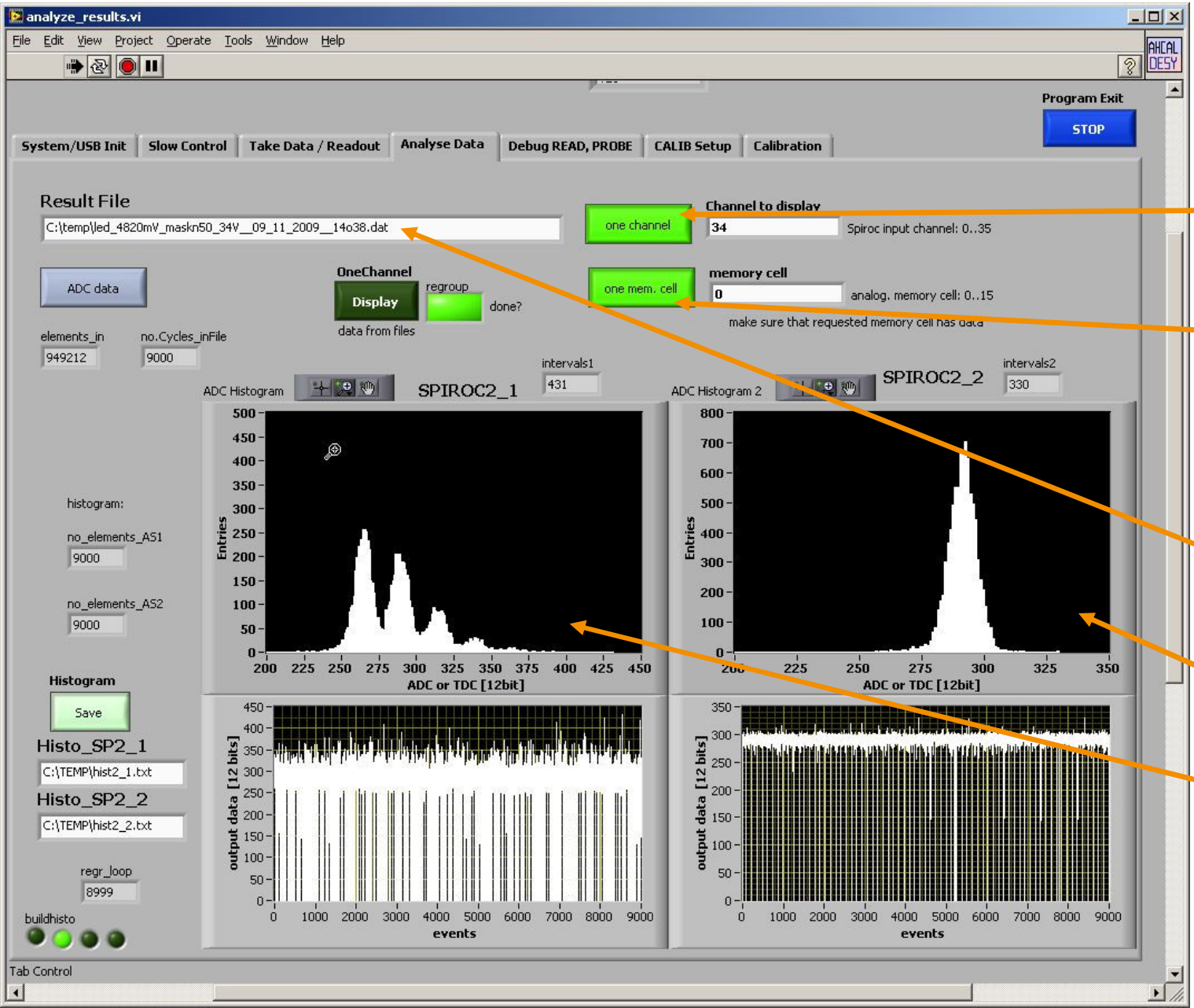
Testbench Labviews – Histogram Building



Choose:

Channel
0..35 or all

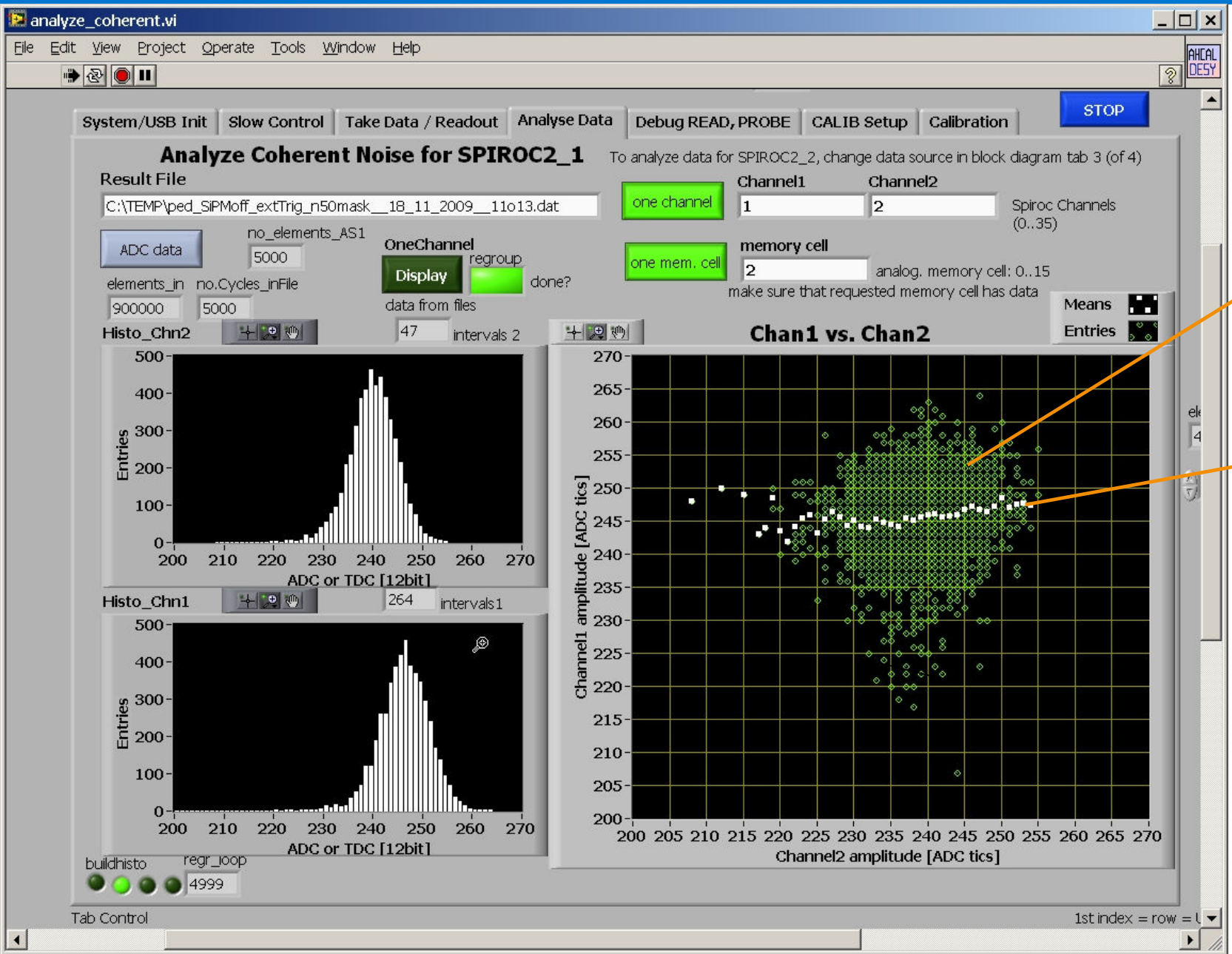
Memory cell
0..15 or all

Result file

SPIROC2_2

SPIROC2_1

Testbench Labviews – Coherent Noise Analysis



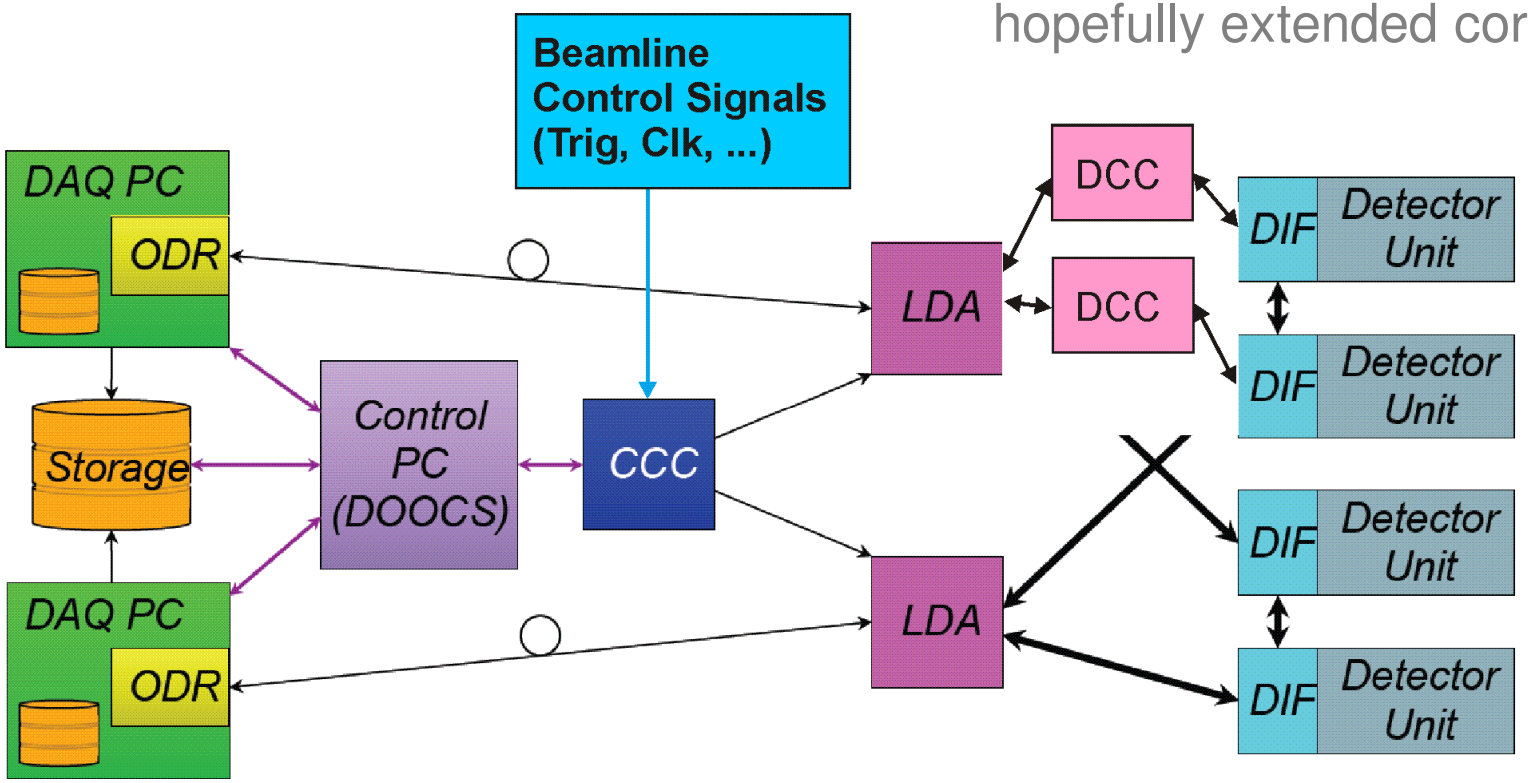
no coh. noise: circular shape

mean values (white points)

now: rip off block capacit.

Testbeam Synchronization (CALICE DAQ setup)

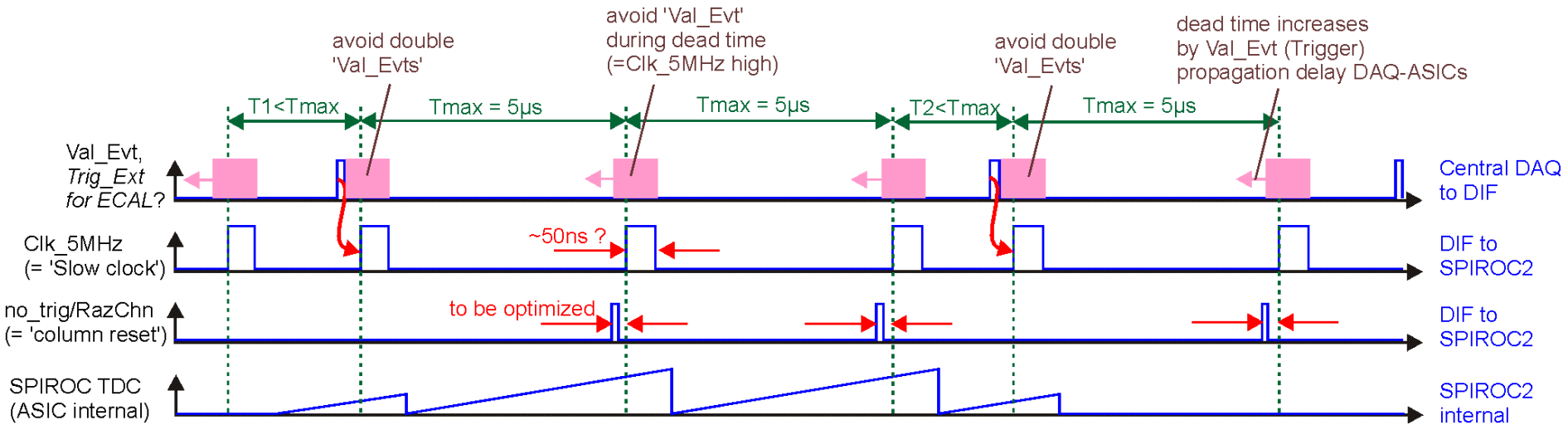
Concept: M. Wing et al.,
hopefully extended correctly



- All timing critical signals are distributed from central DAQ (via CCC).
- All detector units (+DIFs) run synchronously.

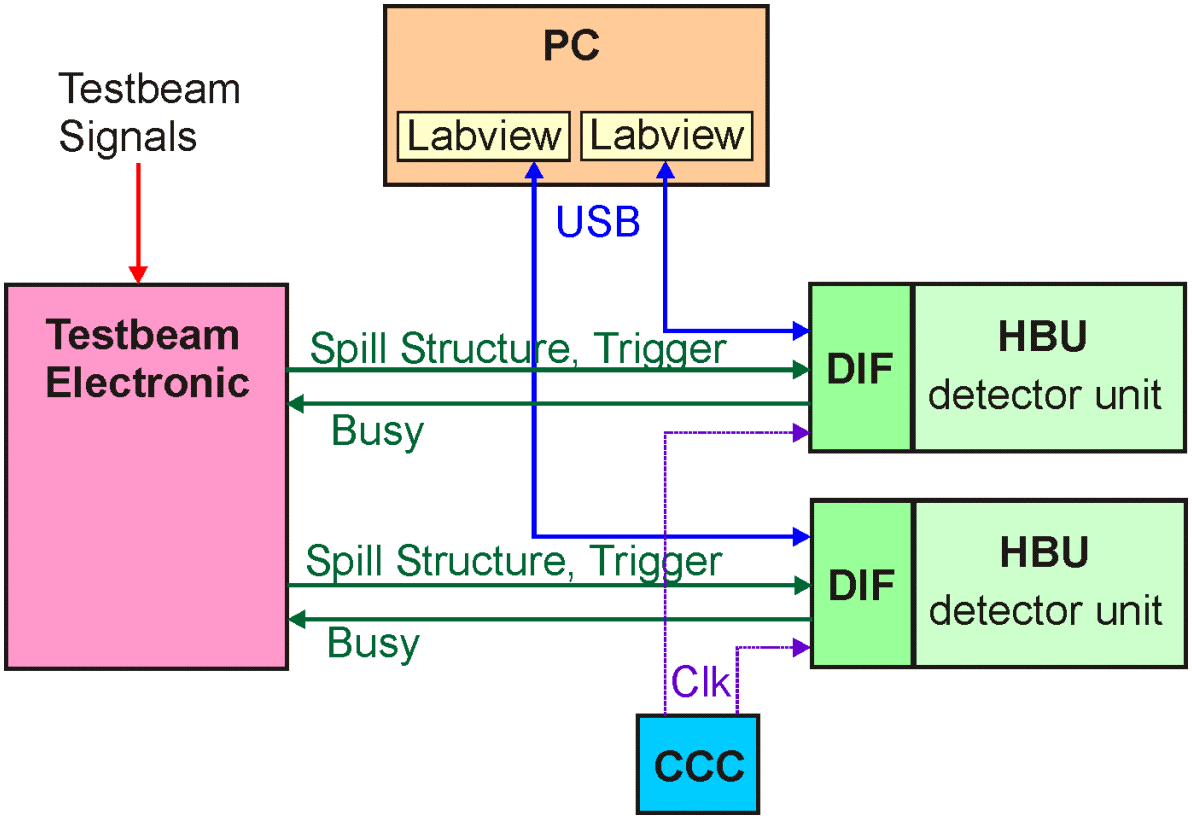
Testbeam Data Taking: Internal Trigger

AHCAL timing scheme for common CALICE testbeam



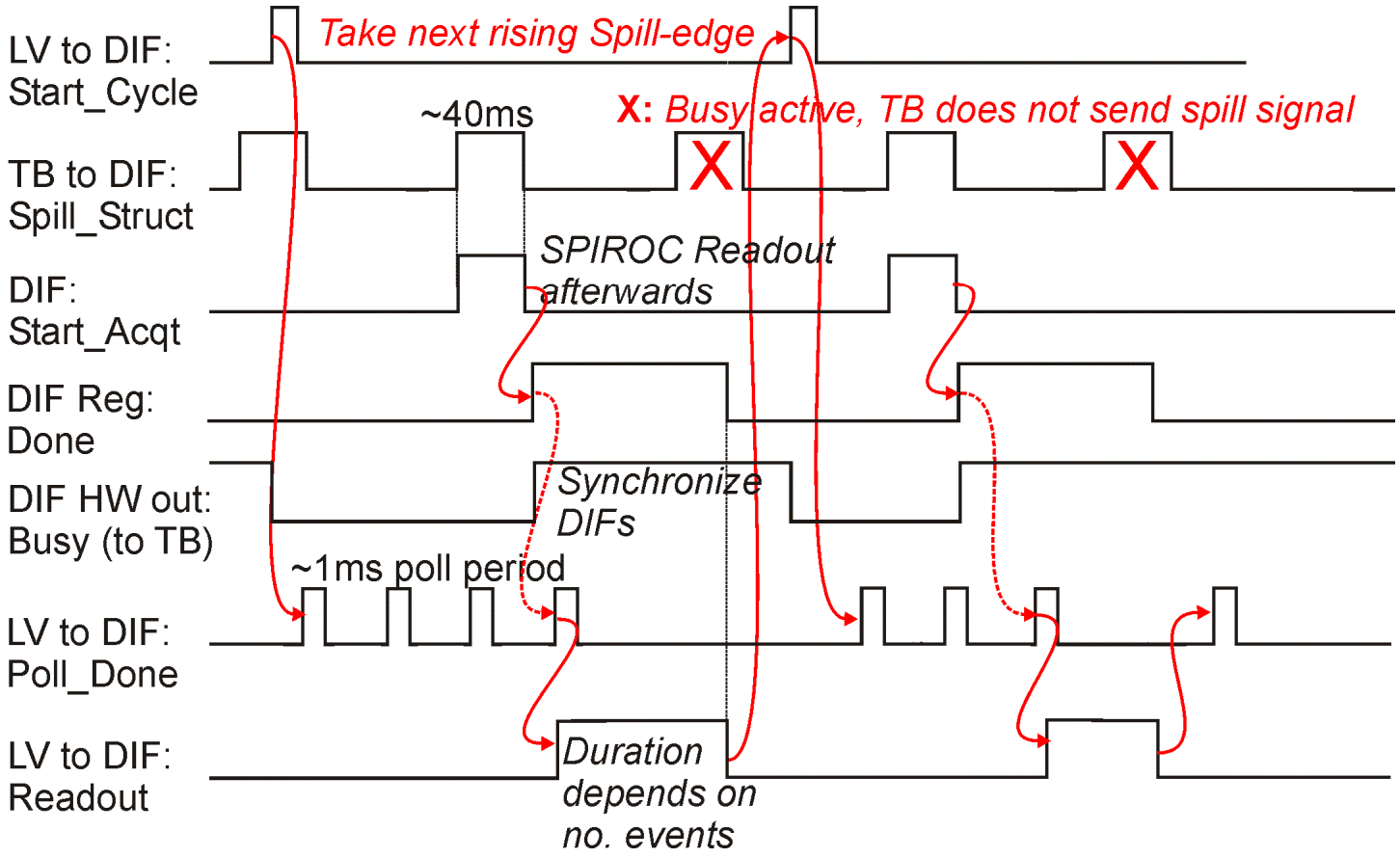
- Internal Trigger with “Validate_Event”. **Pink boxes: deadtime!**
- Do we need “Internal trigger mode” without Val_Evt in TB (full clock rate)?
- CALICE DAQ: Synchronize Val_Evt on global clock (multi-DIF synchron.).

DESY Testbeam Synchronization (Labview setup)



- Synchronization done by temporary hardware signals to/from DIF.
- First: Only one DIF/HBU used. With two HBUs the CCC is needed.
- Readout Speed limited due to USB/Serial Interface.

DESY Testbeam Synchronization (Labview setup)

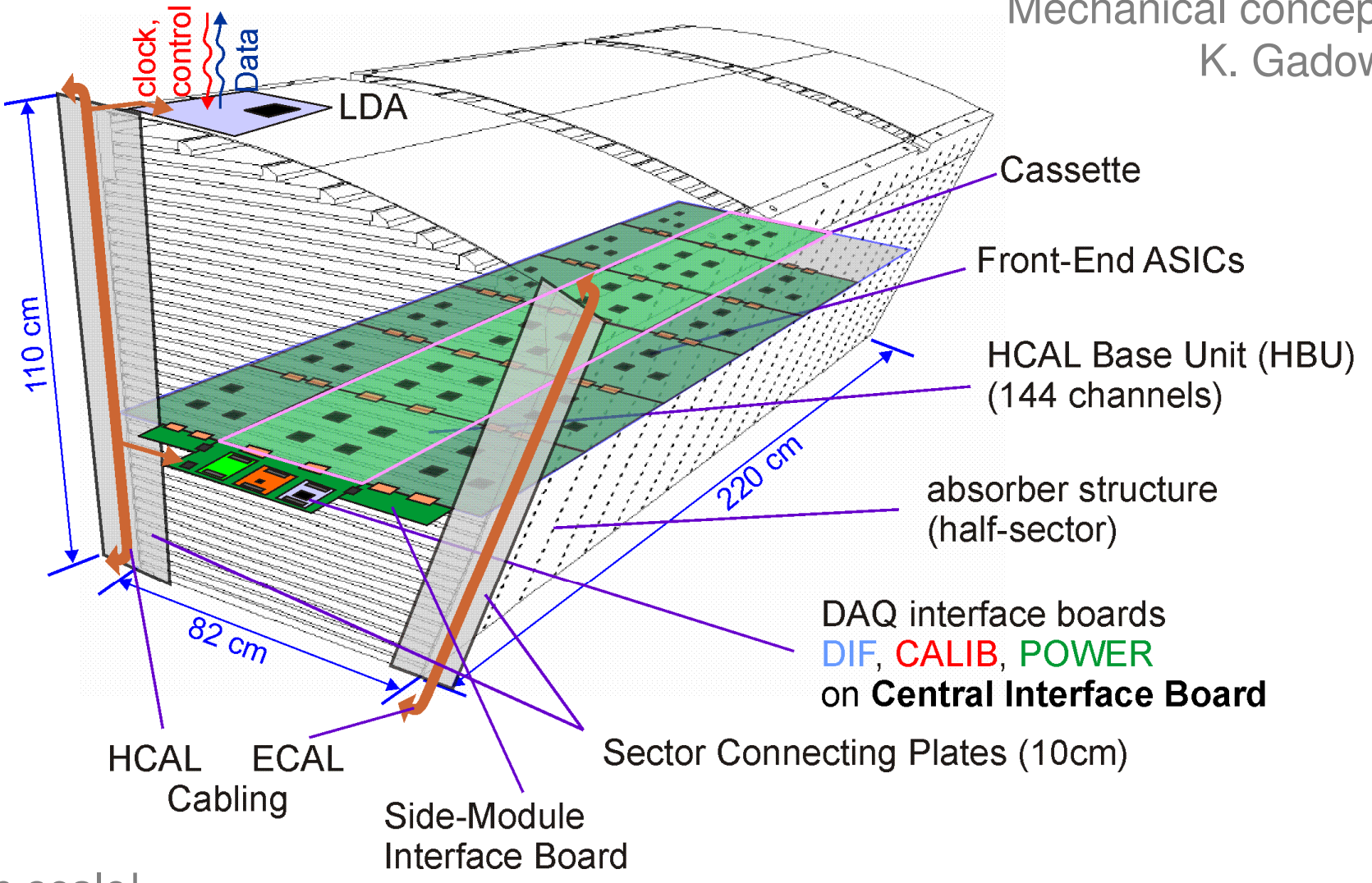


LV: Labview
TB: Testbeam Electronics
HW: Hardware

- Due to shutdown of DESYII: HBU testbeam tests end of Feb 2010.
- External and Internal trigger will be tested.

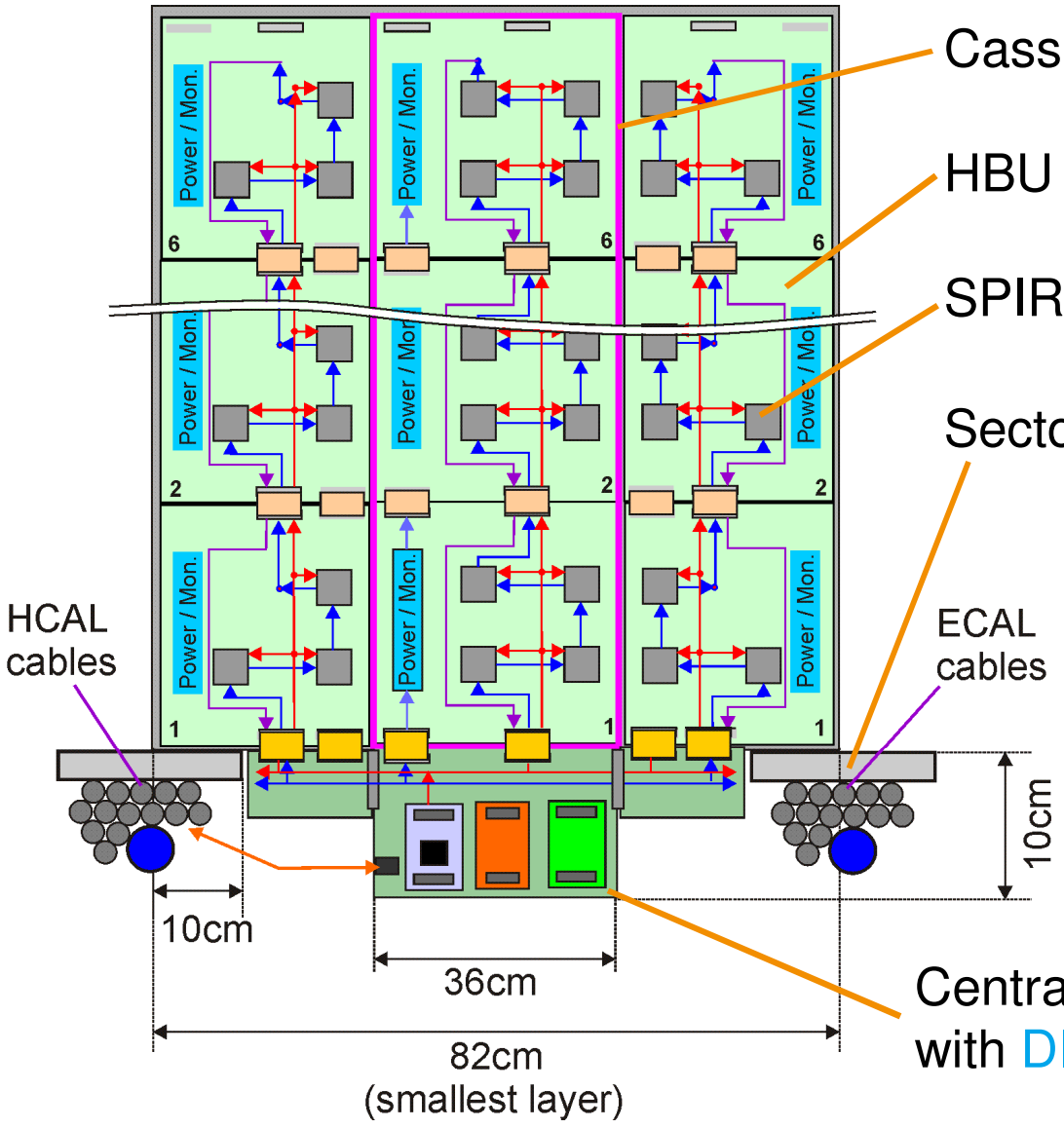
The Next Generation ('final' ILC setup concept)

Mechanical concept:
K. Gadow



Not in scale!

The Next Generation



Cassette (=slab)

HBU

SPIROC

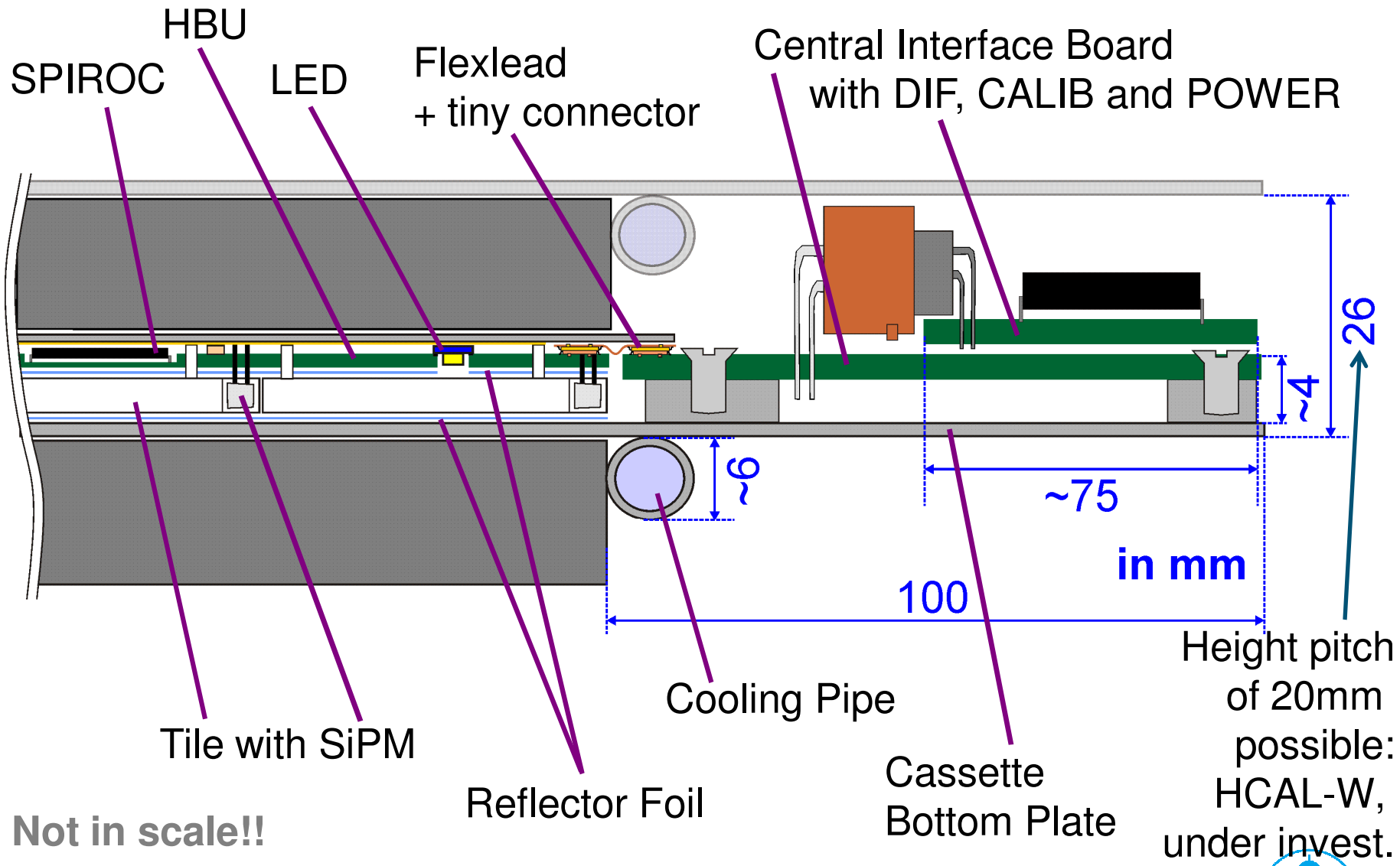
Sector Connecting Plate

Not in scale!!

Central Interface Board with DIF, CALIB and POWER

DESY

The Next Generation



Conclusions and Outlook

- AHCAL prototype in full operation! 2 setups realized!
- CALICE DAQ (hardware, DIF firmware) still has to be implemented.
  - we expect a first system Feb/March 2010. Till then: Labview operation.
- SPIROC2a submission Jan2010. Changes under discussion.
- DESY electron-testbeam preparation ongoing.
- Redesigns of AHCAL modules are prepared now.
- Fibre based calibration system in operation as well! (see Ivo's talk)

- A lot of system's and SPIROC analogue and digital tests ahead.
  - all shown analysis have not been completed.
  - status only demonstrates readiness of the system and system's tools.

DESY