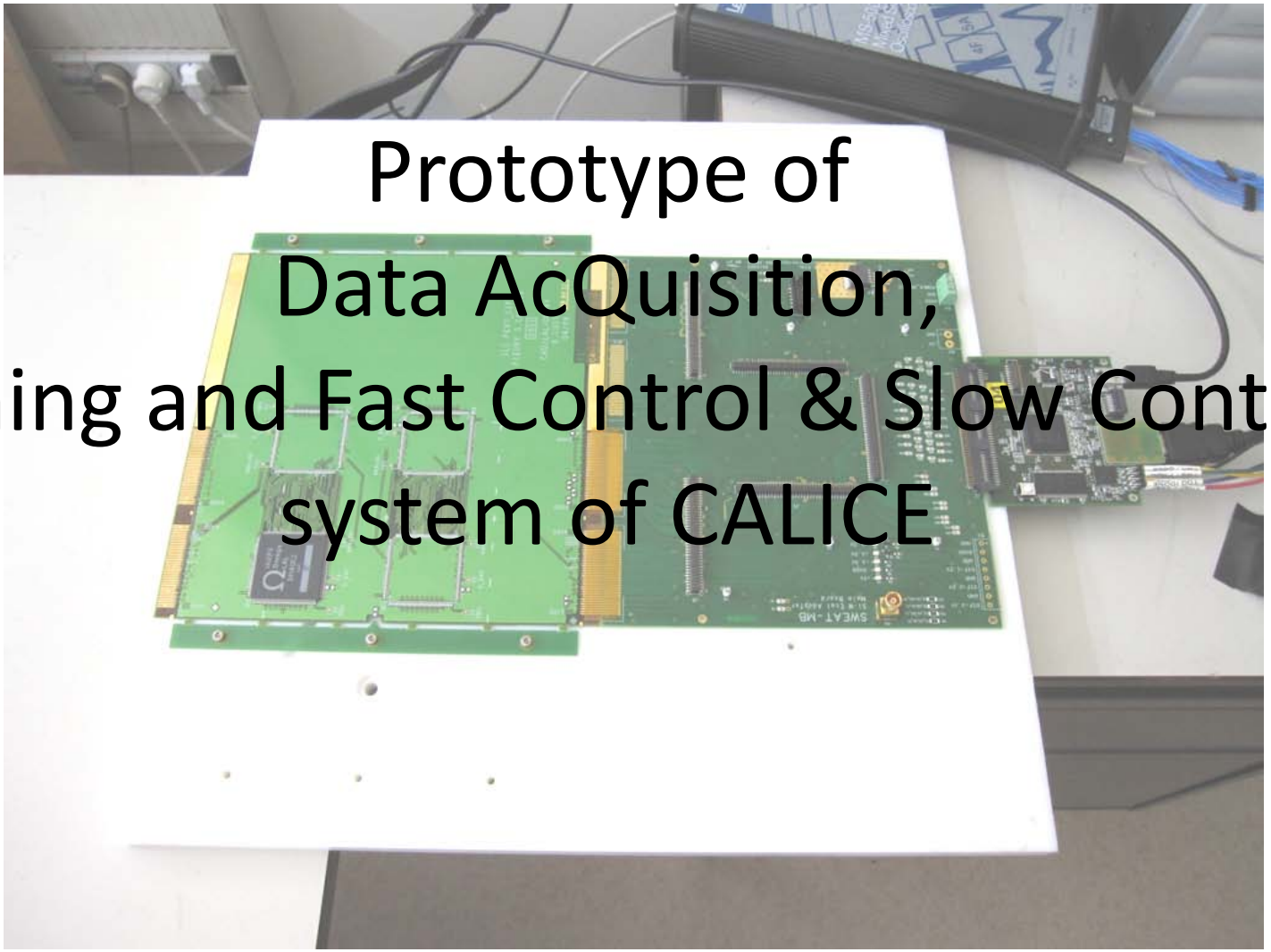


Prototype of Data AcQuisition, Timing and Fast Control & Slow Control system of CALICE

Acquisition and control system

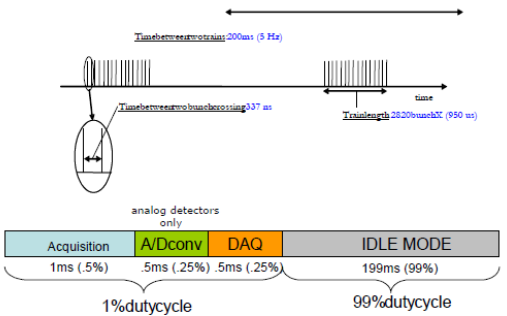
- Scalable
  - Tree architecture
  - Successive concentration of data
- Standard
  - Rely on standard protocols, data coding
    - Ethernet, optical links,
    - Serial 8b10B
  - Cables and connectors
    - Hdmi
    - CAT5, RJ45
    - Optical
  - Front end interface unified among the detectors (CALICE standard)
- Compact
  - Serial links used everywhere
  - “one cable for everything” : DAQ, TFC, SC
  - Front end components
- Flexible
  - (re)programmable parts (fpga)
  - Routing, switching, buffering of data packets
- but some limitations
  - Low speed access to a chain of 10-100 very front end chips (1k-10k channels) : 1-5 Mbit/s (daisy chain and reduced number of connections for compacity, length of PCB traces, low power consumption)
  - Therefore assume : auto trigger, zero suppression at VFE level
  - TFC interleaved with SC, DAQ using 8b/10n protocol : limited timing precision (>10 ns)
  - Events build at VFE level, inter-bunch train read out : limited buffering capacity (10-100 evt)

Low occupancy of the detectors is assumed (<0.5%/cell/bunch)

Common interface to VFE chips

ECAL
DHCAL
AHCAL
…

- TFC (clk, ext-trig, …) : parallel bus, lvds
- SC : shift register + parallel bus (upgrade to industry standard protocol foreseen)
- DAQ : open collector data bus + daisy chain (token)
- Parallel bus can serve a partition of 10-100 chips
  - Up to 2m long : frequency limitation
  - 1-4 partition per detector unit/detector interface
  - This number can be set according to the detector region
- Daisy chain is secured
  - Redundant connections
  - Bypass traces : in case of failure the detector unit is not fully lost
- Optimization for ILC beam structure



Detector InterFace (DIF) board

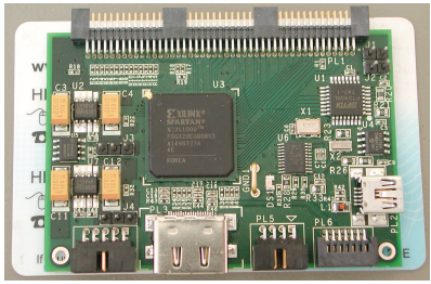
- Can use the same hardware for every detector
  - Same connectors & interfaces
  - Compact : credit card and below
- Customizable anyway
  - Size
  - Test beam/calibration features (add exttrig, clk, RAM, …)
  - Debug (test of single detector module)
- Functionalities are simple
  - VFE chip management (power pulsing, SC, DAQ)
  - Local storage of SC data
  - Protocol conversion (8b/10b to VFE)
  - Based on low cost fpga
- DIF task force (4 persons)
  - Specifications
  - Common firmware

Actually 3 different DIFs
in use : ECAL, DHACAL,AHCAL

UNIVERSITY OF CAMBRIDGE · MANCHESTER 1824 · Royal Holloway University of London · UCL

ECAL DIF

- The ECAL DIF has been developed by the Cambridge group; HCAL DIFs developed by other groups, but all within the DIF task force.
- Produced a prototype board which worked well, in use at LLR.
- For production, have reduced number of components, whilst maintaining functionality.
- 10 new DIFs have been produced and being used in system tests at UCL and also at LLR.



Prototype of the complete system

- Studied and done by UK group (see next slides)
- Prototypes based on generic commercial mainboards
  - Not the final shape
  - Functionalities are there, to be used with next detector prototypes (Q3'10)
- Complies with actual VFE chips prototypes
  - Not final interfaces
- Allow test beam operations
  - External trigger is distributed (isochronous distribution tree)
  - Memory full feedback from chip
  - Compliance with other beam structure & occupancy
- Debug features
  - User test connector
  - USB access on most boards

DAQ system hardware status

Matthew Wing (UCL)
for DAQ groups: Cambridge, Manchester, RHUL and UCL

ECAL / Electronics / DAQ Meeting, LLR, 14–15 January 2010

DAQ system overview

(**Detector Unit** : ASICs)

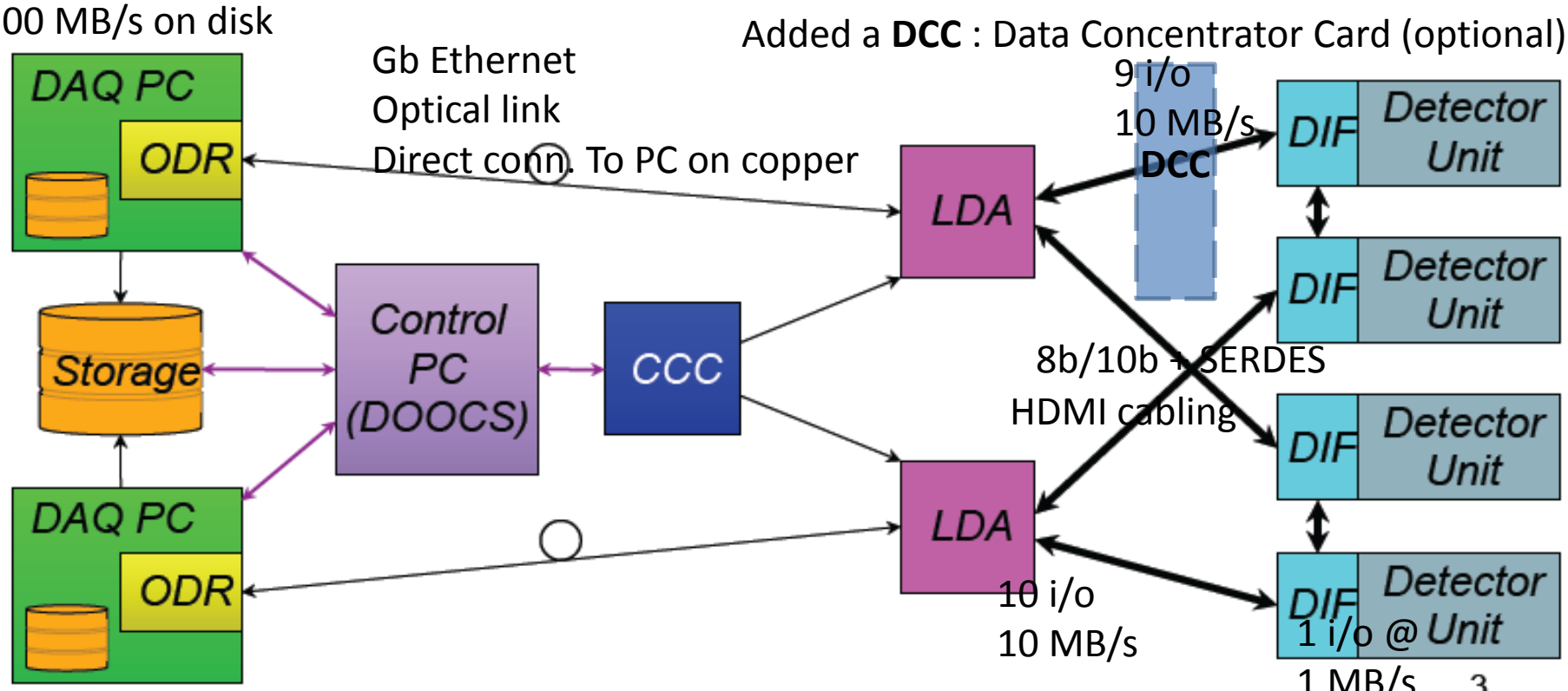
DIF : Detector InterFace connects generic DAQ and services

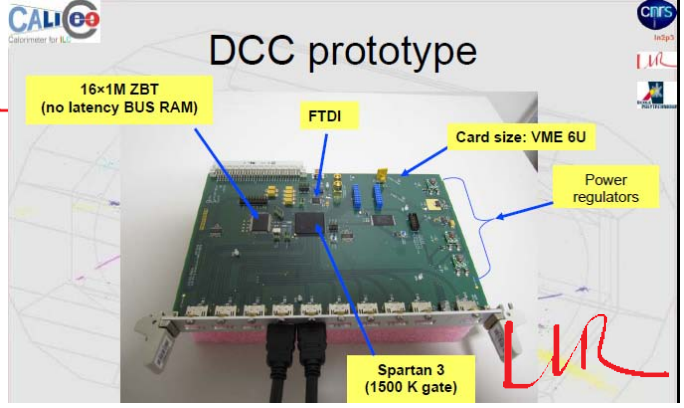
LDA : Link/Data Aggregator fans out/in DIFs and drives links to ODR

ODR : Off-Detector Receiver is PC interface

CCC : Clock and Control Card fans out to ODRs (or LDAs)

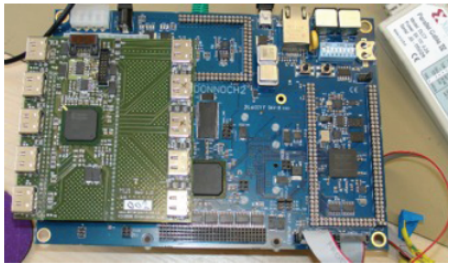
Control PC : Using DOOCS





LDA

- The LDA (from Enterpoint) consists of :
  - Mulldonoch2 baseboard;
  - add-on HDMI board to connect to 10 DIFs;
  - an add-on ethernet board to connect to an ODR.
- Firmware development :
  - DIF <=> LDA link running;
  - new code soon to be posted to svn;
  - same format as ODR in svn repository.



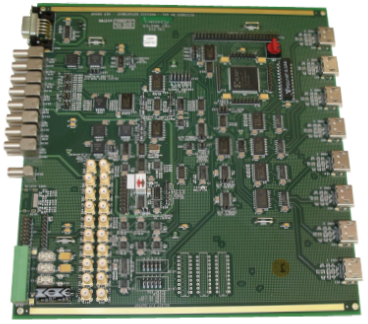
DCC and LDA are essentially similar to an ethernet switch but using a low level protocol

They both fan-out/in fast isochronous signals on a dedicated path and commands on the 8b/10b serial link

LDA has a fast link : Gb ethernet to the upper level = ODR, and can connect to 10 DIFs or DCC with the 8b/10b serial link
DCC can connect to 1 LDA and 9 DIFs using the 8b/10b serial link, data from DIF are buffered and sent to the LDA

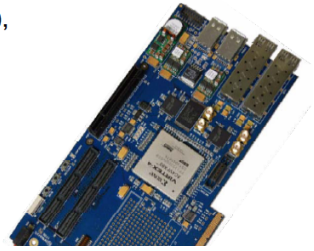
CCC

- Overall status unchanged for a while.
- Fans out clocks, fast commands and control signals.
- Fans in busy.
- Full complement of 10 boards with power supplies tested.
- One in LLR and one in LAPP.
- CCC link to LDA still needs to be done :
  - Board designed and firmware developed for testing;
  - Soon to produce enough boards for all LDAs.



ODR

- Receive data on 4x fibre (RX),
- Write to disk FAST (>150MB)
- Send data up fibre (TX)
- Controlled from Linux driver
- DOOCs Interface



Documentation / repository

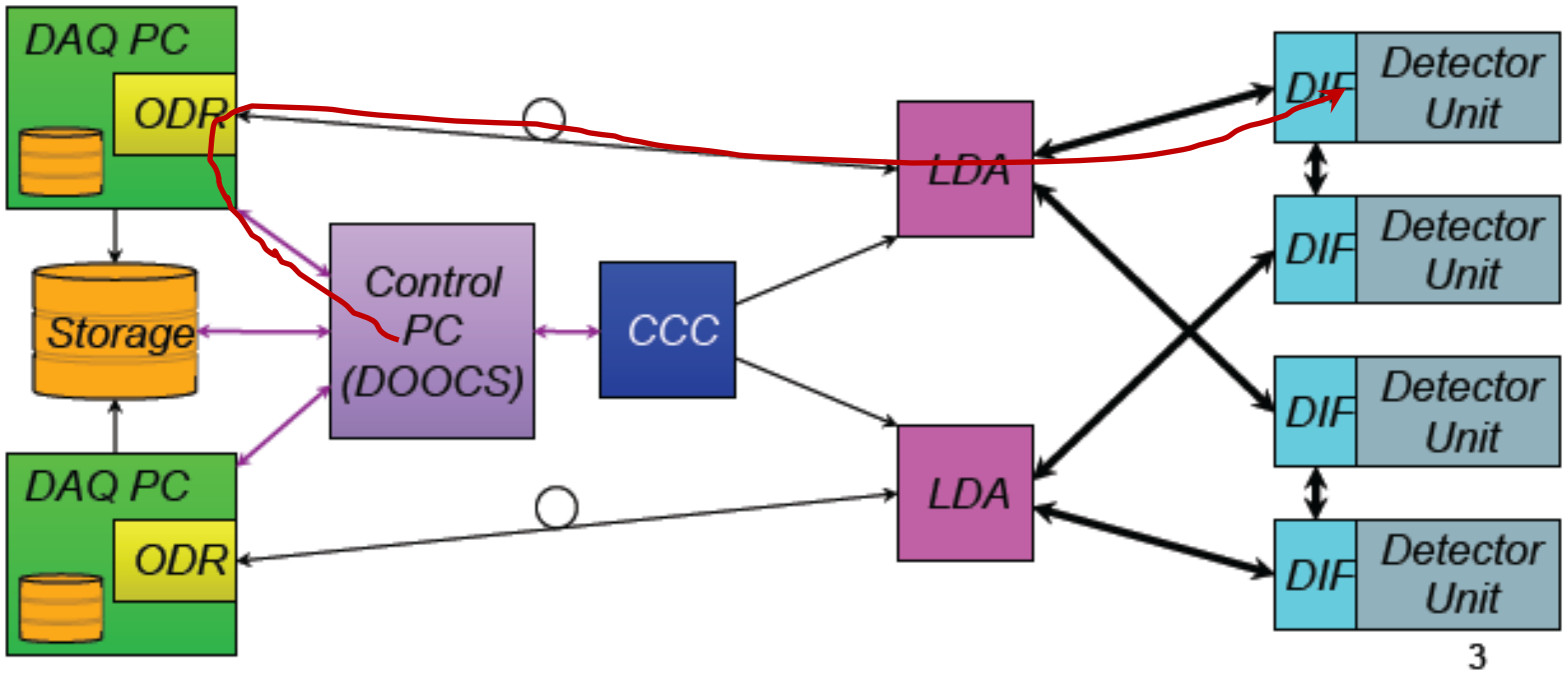
- All components *should* have extensive documentation on twiki : it is being updated and as components are basically done, can soon be finalised.
- Twiki main :

  https://twiki.cern.ch/twiki/bin/view/CALICE/CALICEDAQ
- Also list of hardware availability /status started.

  https://twiki.cern.ch/twiki/bin/view/CALICE/HardwareList

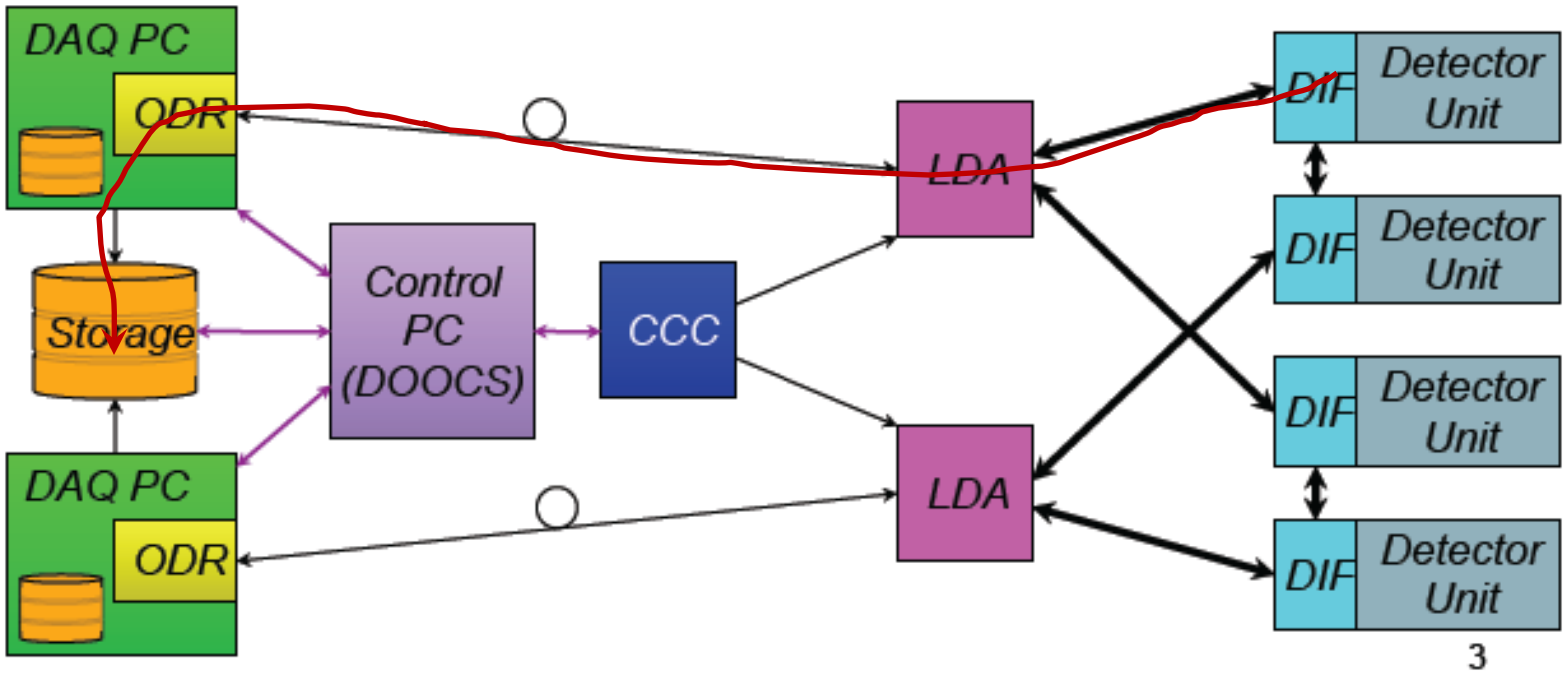
Slow Control / Commands

- Detector (DIF & VFE) configuration
- Simple orders (not timmed, broadcast possible)



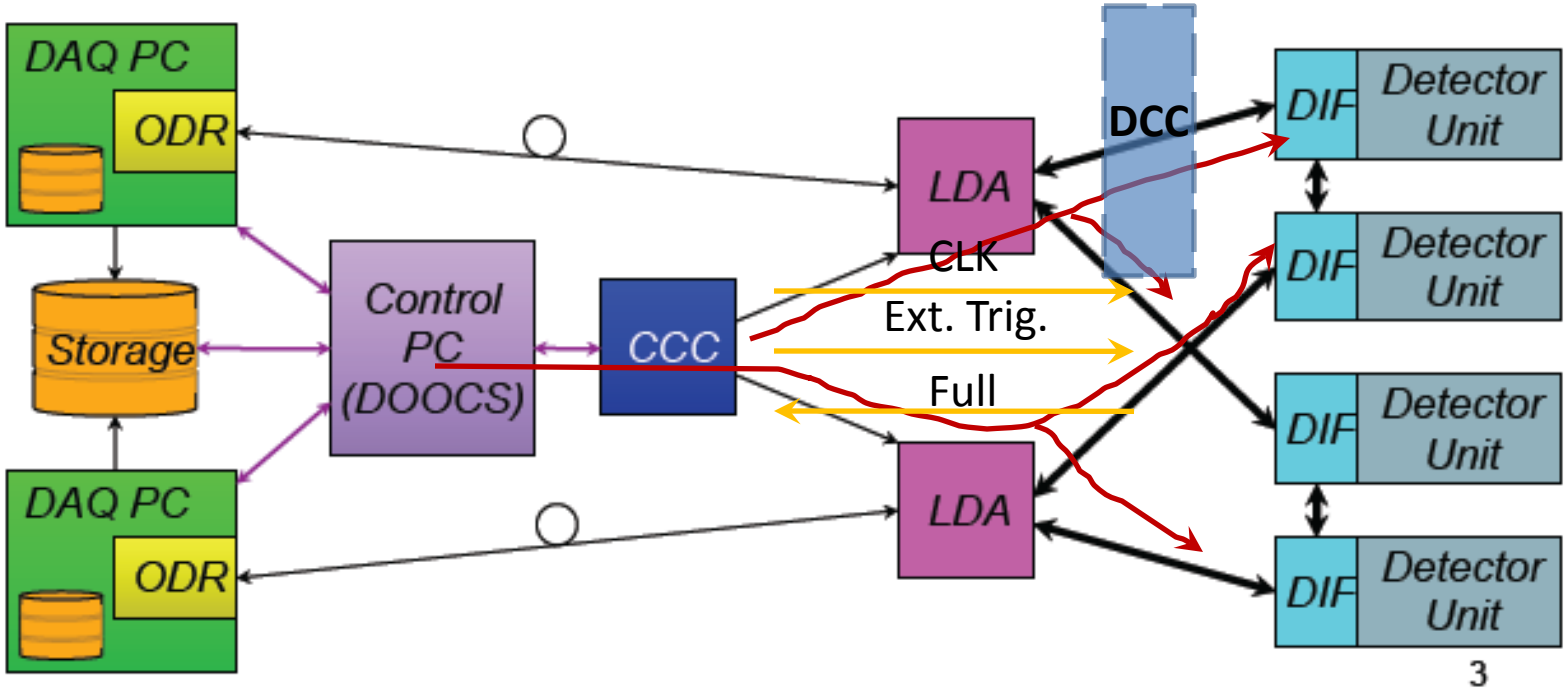
DAQ

- Detector Read Out
- Command triggered



TFC

- Clock distribution (+ ext trig, + ram full)
  - Uses discrete components, know delay, low jitter (<200 ps)
  - A clock is also encoded in the data link
- Machine interface (trains, BX)
- Fast Commands (isochronous) : reset, arm chips
  - Mixed with SC/DAQ on same link
  - Use low level protocol controls



2 aims = 2 modes ?

- Calibration / Noise / Test beam

The aim of the calibration mode is data taking in order to perform the calibration of the detector and physics studies about properties and performance of the detector. The detector and the electronic systems are configured to ensure the highest rate for the data tacking.

- EUDET/ILD

The demonstrator mode is intended to run the detector as close as possible to ILC functioning in order to perform engineering studies on power pulsing, power supply, thermal dissipation. It is under the scope of the EUDET contract for which technical solutions must be tested and engineering feasibility must be proven.

Calib/Noise/Test beam mode

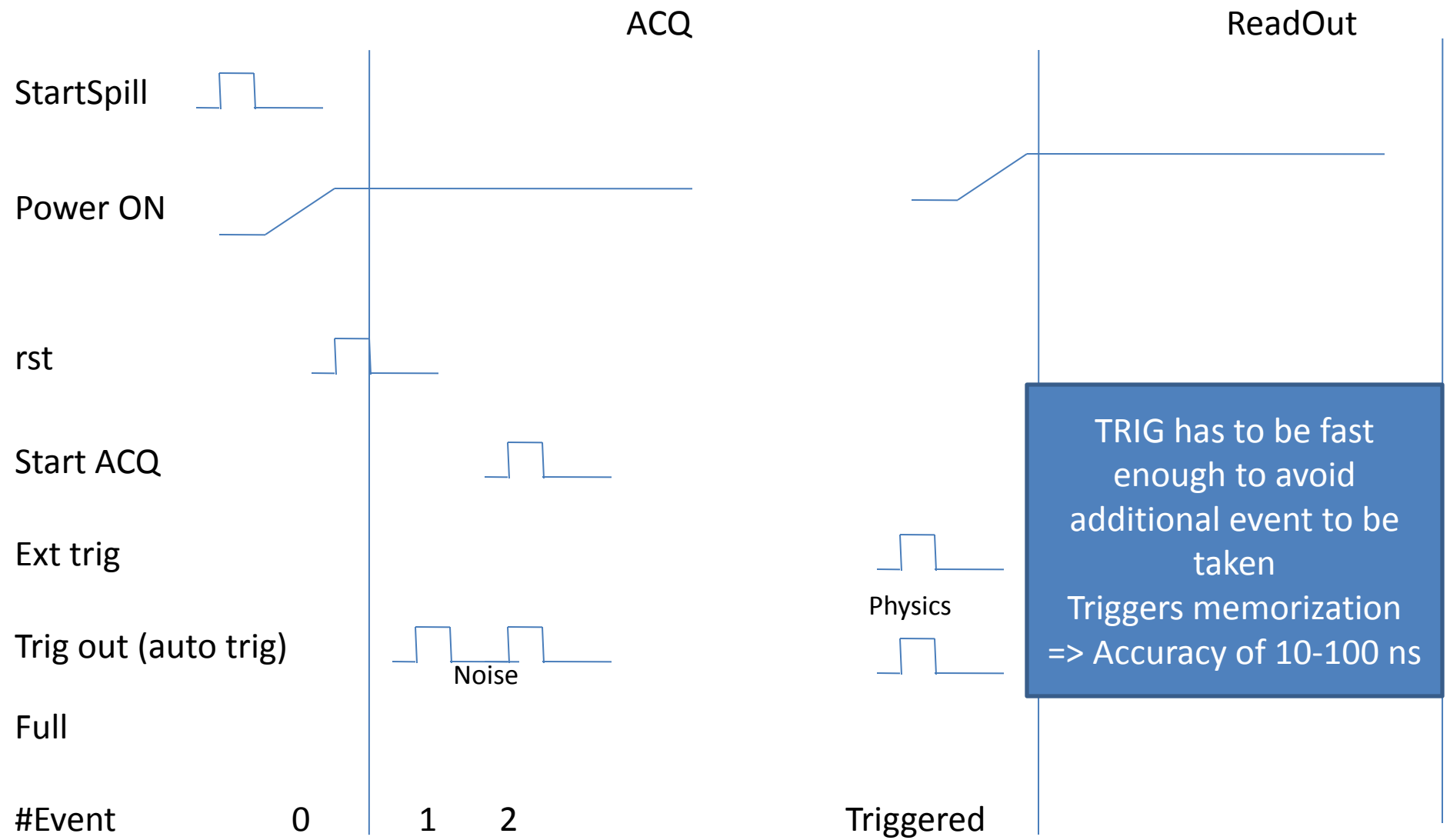
- Beam structure different as for ILC
  - Detector and DAQ not optimized
- Structure inside the SPILL

"The structure we see is that the beam particles are not spread completely randomly in time, but are bunched at the O(10-100us) level." (FNAL=11 us)

- Few particles within the micro-spill
- SINGLE event option = Study of Noise = acquire all the channel over the detector
- BURST option = physics, zero suppression and trigger (internal or external), more than one event acquired

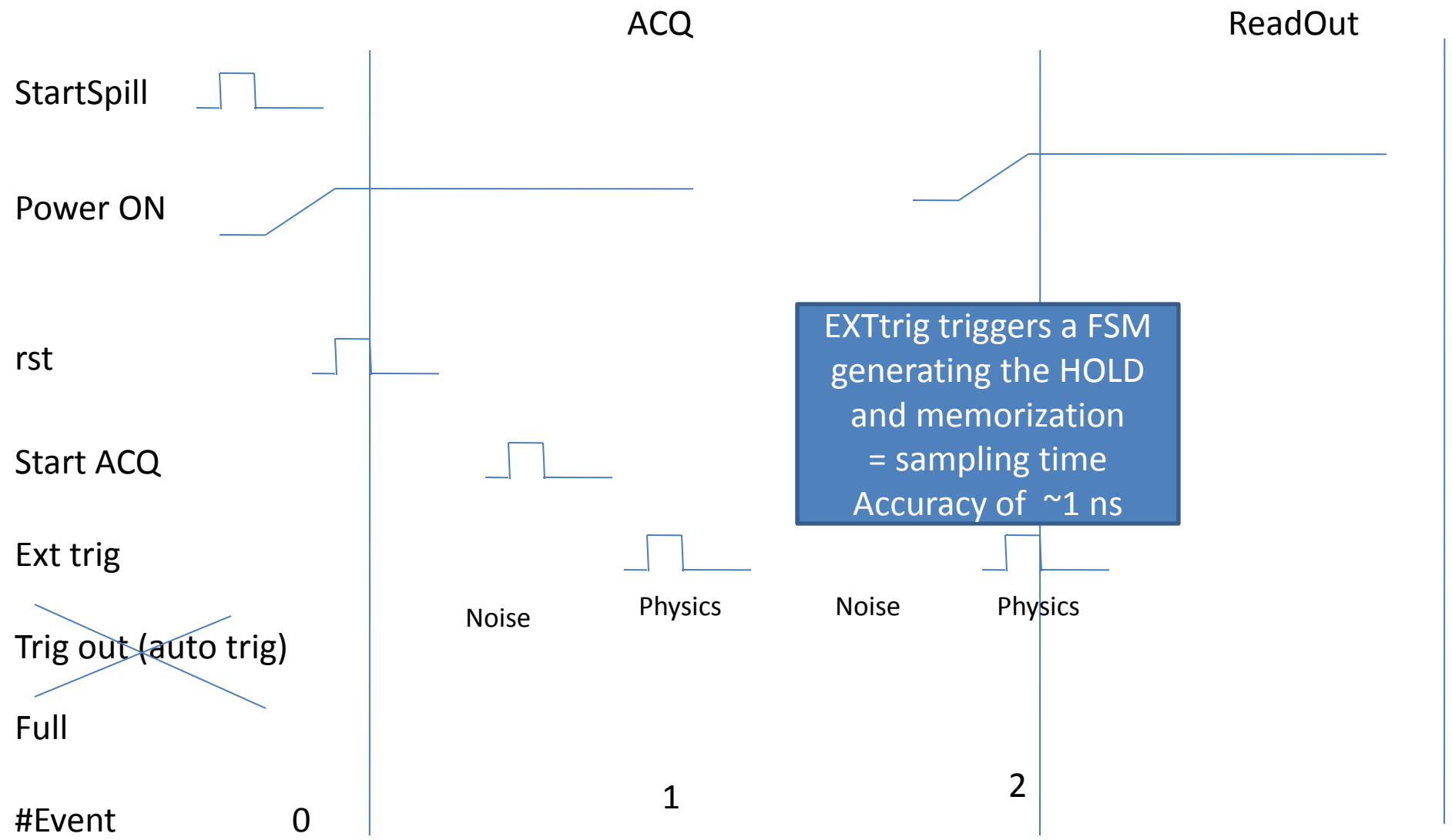
single event

The last event is triggered then read out



Triggered burst or single event for Noise

Event are acquired thanks to an external trigger

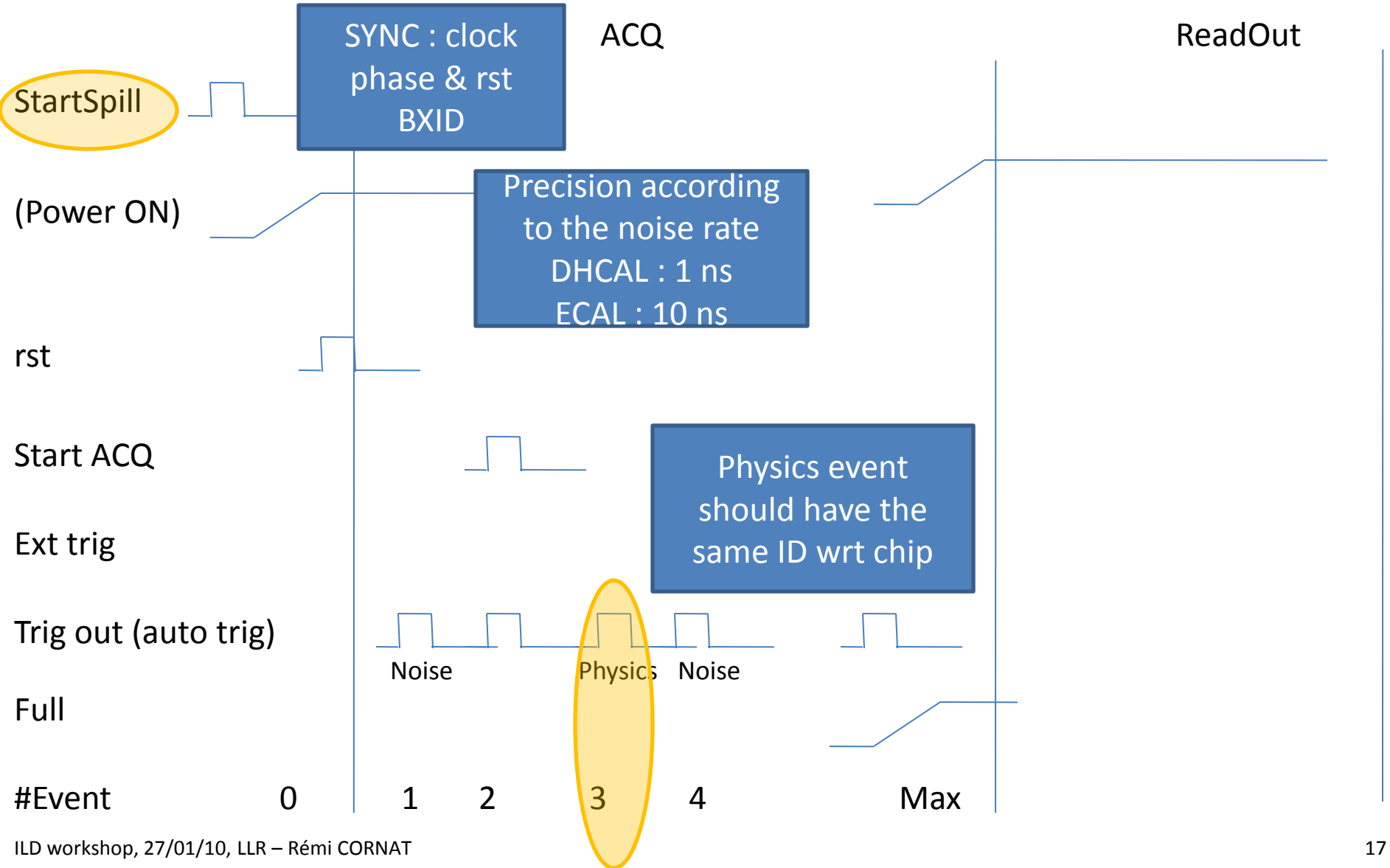


Demonstrator mode

- Would need beam structure like ILD
- If not:
  - Can be emulated setting the trigger threshold high in ROCs (avoid noise)
  - Stop acquisition from time to time to reach a duty cycle of about 1%
- Use of power pulsing possible (w.r.t. beam spills)
  - Particular configuration for the electronics
- Electronics is optimized for that mode
  - Size of internal buffers (small)
  - Data rate (small at VEF output)

Internally triggered burst

Stops when chip is full (local or global)
or when a command is issued



Outcome

- Prototype of a flexible DAQ
  - For calorimeter system
  - Designed with ILC/ILD in mind
  - Compatible for Test Beam
- Firmware is being developed
- System tests are ongoing
- First operation foreseen on June
- Could be extended to other detectors
  - DIF is detector specific
  - Specifications and study to be performed