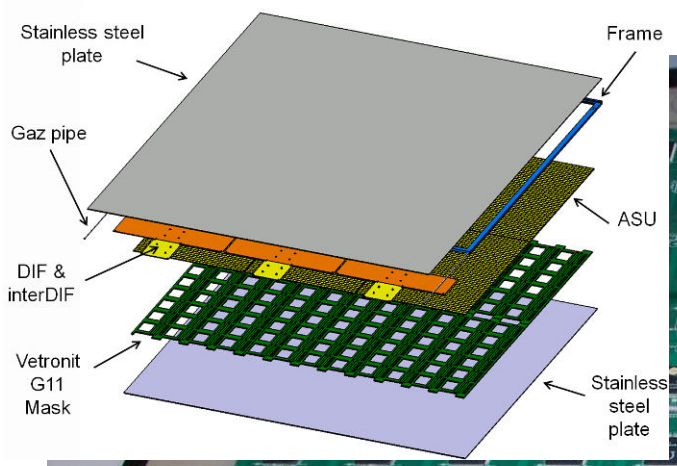
HARDROC2: Before production

http://omega.in2p3.fr/

Nathalie Seguin-Moreau

Orsay MicroElectronic Group Associated

TOWARDS A TECHNOLOGICAL PROTOTYPE

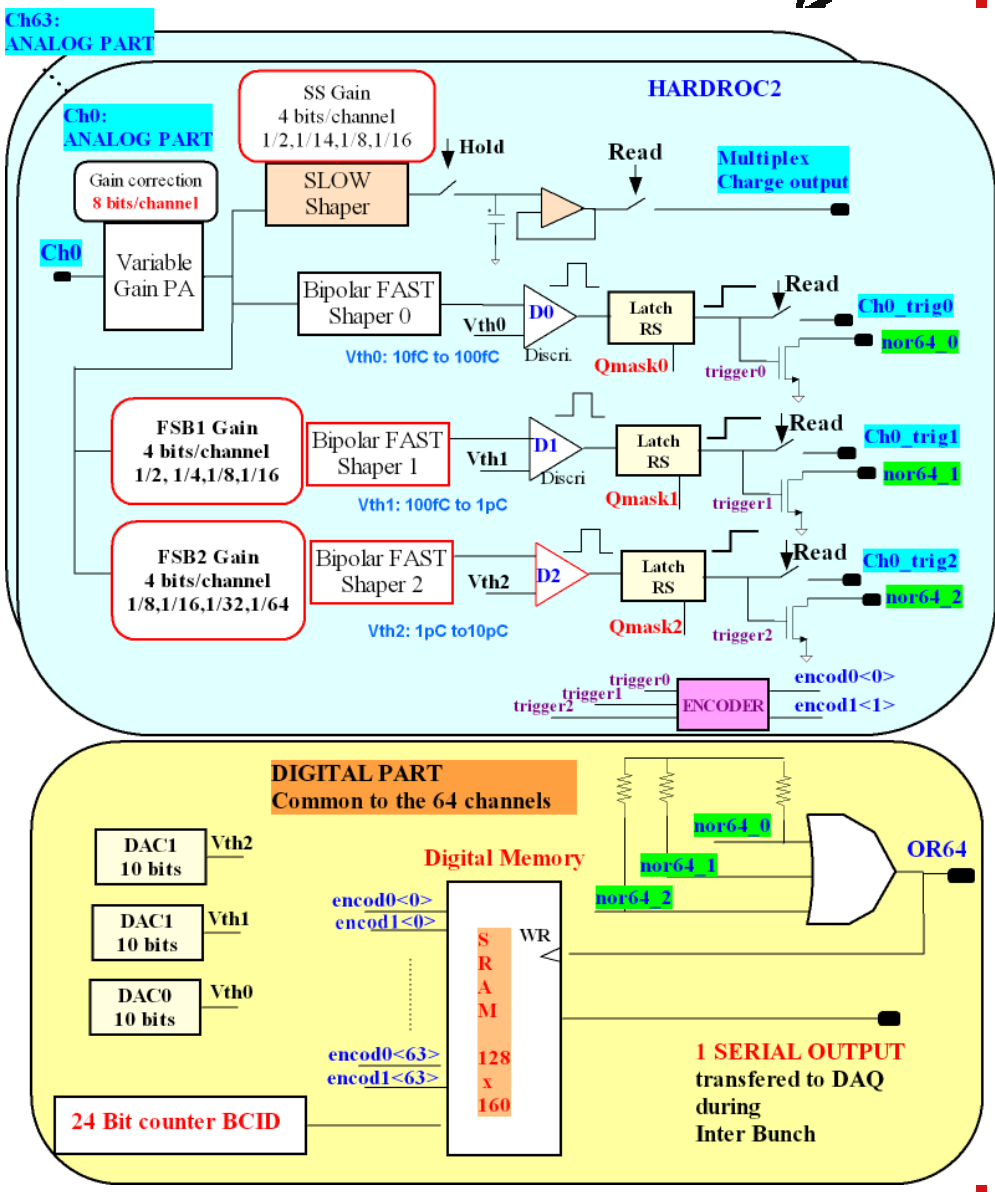


1m^2 scalable detector equipped and tested with cosmics and in testbeam in summer and automn 2009. 144 chips/m^2

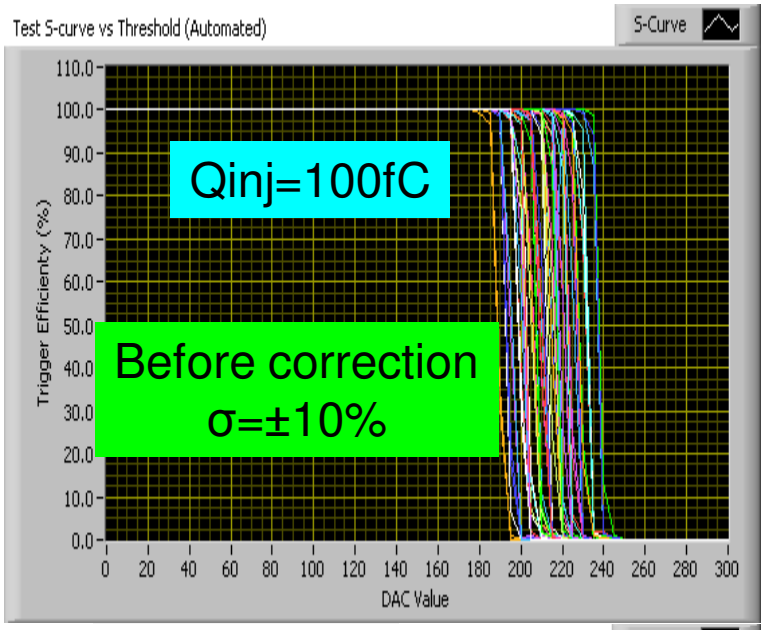
About 6000 chips necessary to equip 40 plans of 1 m^3

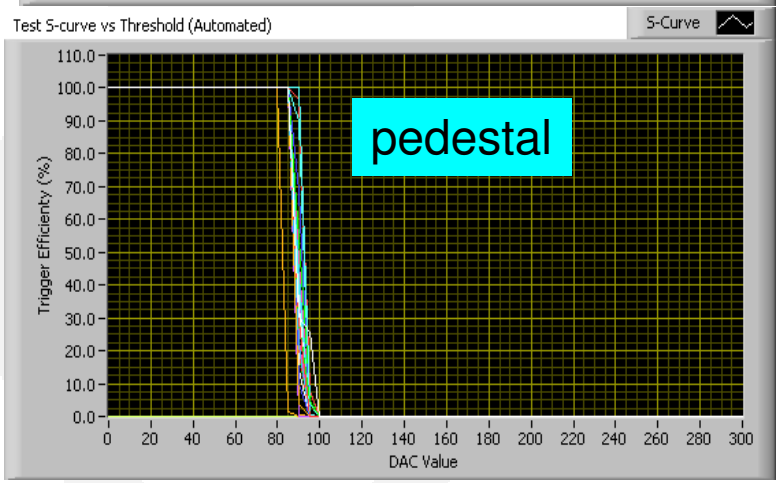
HARDROC: HAdronic Rpc Digital ReadOut Chip

- 240 chips HARDROC1 produced in june 2007 to equip 4-chip and 24-chip RPC and Micromegas detectors
  - Package PQFP240
  - Not completely power-pulsed
- 400 chips HARDROC2 produced in june 2008 to equip 24-chip RPC and Micromegas PCBs for square meter
  - 3 thresholds (0.1-1-10 pC)
  - Power pulsed to 5-8 µW/ch
  - Package TQFP160
  - **Difficult SC loading: SOLVED in HARDROC2B**
- 200 HARDROC2b (medical application) in plastic package received beginning of jan 2010

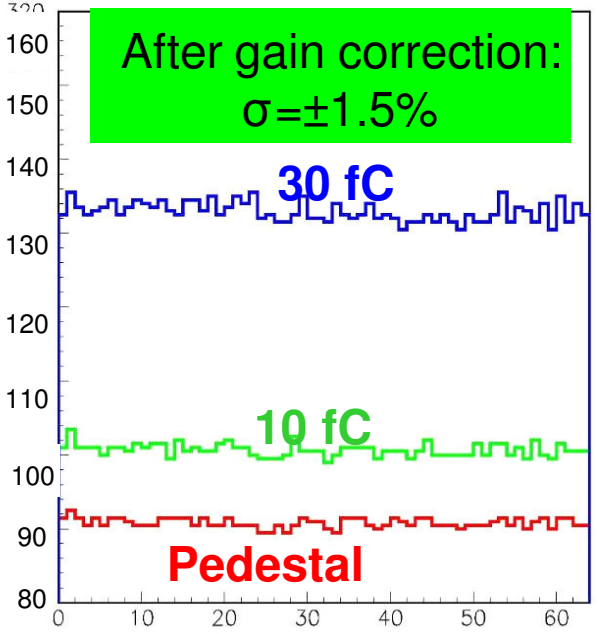


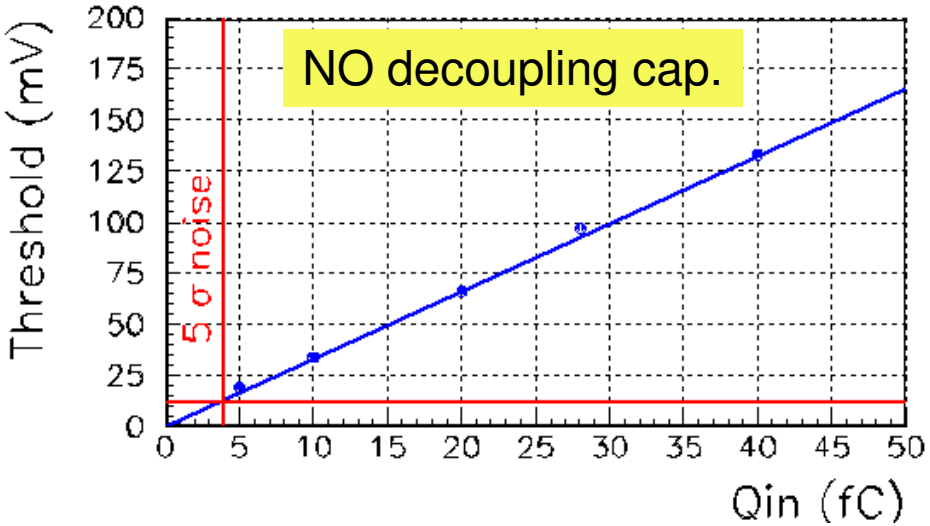
Trigger efficiency measurements (HR2)





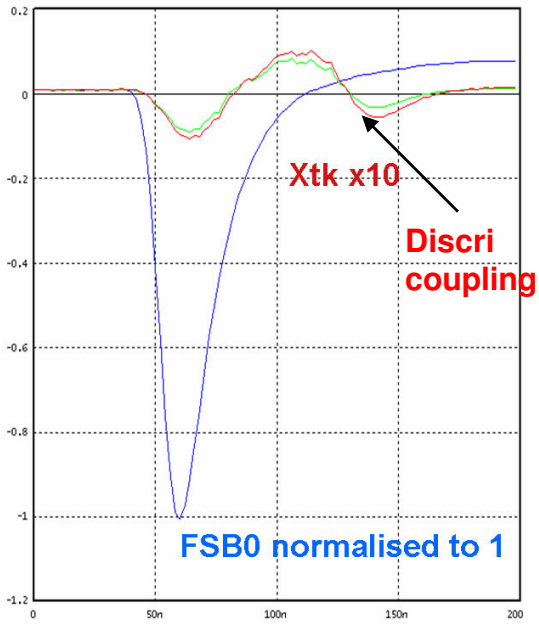
FSB0, 100K, 100fF, G=144

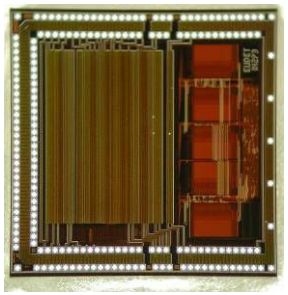


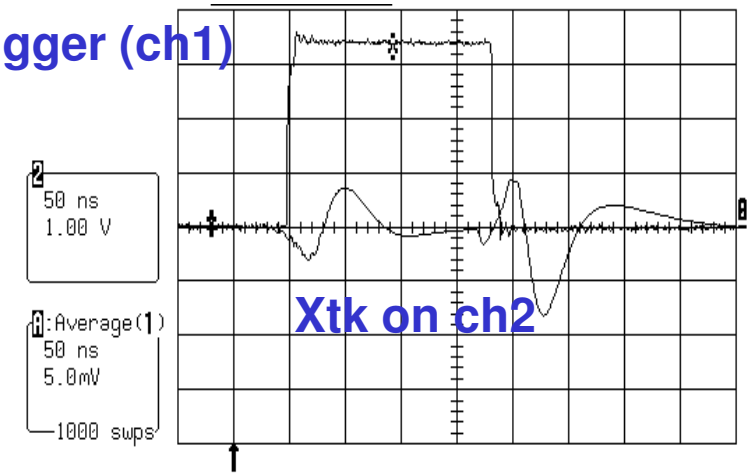


Analog and Digital crosstalk (HR2)

- No decoupling capacitors (on bias and reference voltages)
- Crosstalk ~1%
  - Well differentiated, capacitive like
  - Dominated by the input
  - No long distance crosstalk
- Coupling of discriminator to inputs through ground or substrate
  - Trigger on CH1 and look at analog signal on CH2
  - 8 mV coupling = 3 fC
- Can limit the minimum threshold (not in this case as similar to noise)
- Needs careful chip layout

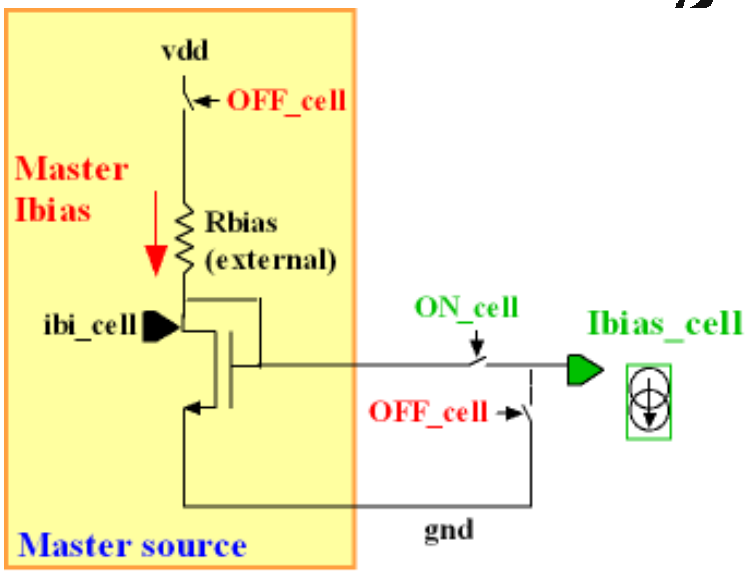






POWER CONSUMPTION

HR2	ON
Vdd_pa	5.5mA
Vdd_fsbx3	12.3 mA
Vdd_d0,1,2	7.3 mA
Vddd	0.67 mA
vddd2	0.4mA (=0 if 40MHz OFF)
Vdd_dac	0.84 mA
Vdd_bandgap	1.2 mA
Total (noPP)	29 mA
Total with 0.5% PP	145 µA



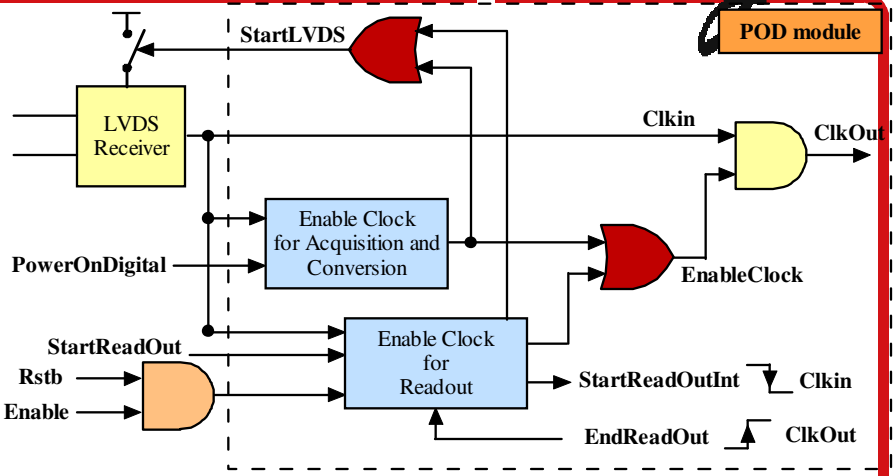
HR2:

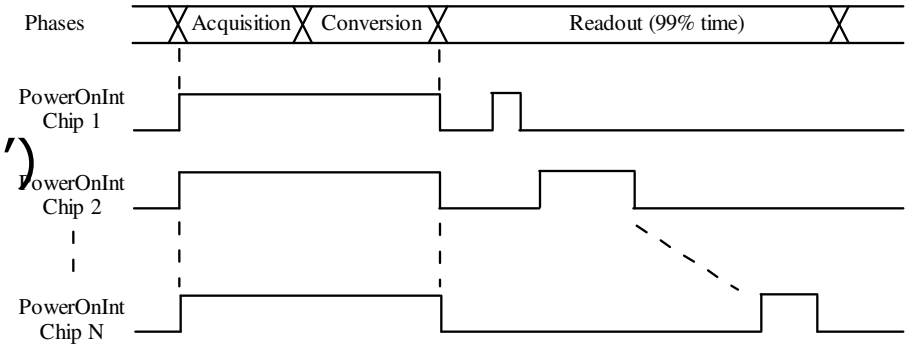
Pwr_on_a alone	14.9mA
Pwr_on_dac	1.025mA
Pwr_on_d	0.93mA
ALL ON (default config)	17 mA
ALL OFF	**<4µA**

- **OFF= Ibias _cell switched off during interbunch**
- **HR1:a few forgotten switches (Bandgap, some reference voltages not power pulsed)**
- HR2: switches added:
  - **ALL OFF => 0**
  - **5.5 µW/ch with 0.5% duty cycle**

Power On Digital:

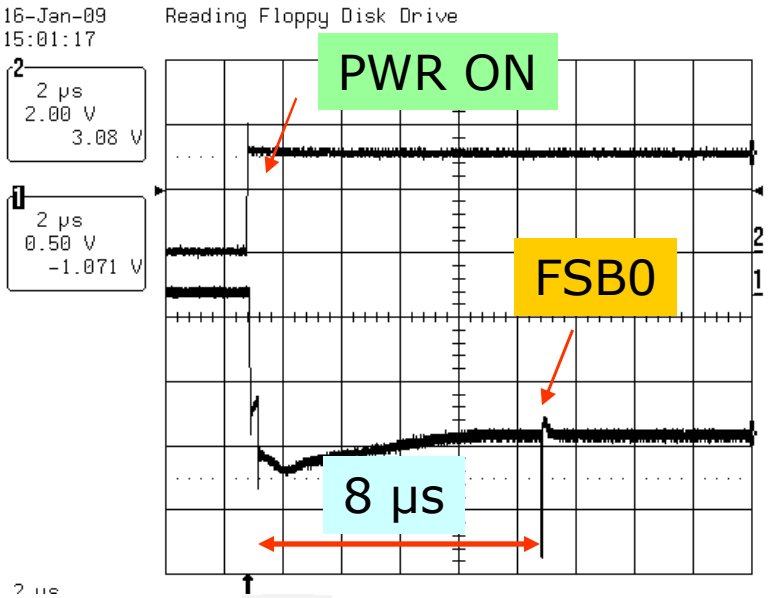
- PowerON start/stop clocks and LVDS receiver bias current to meet power budget.
- LVDS receivers for RazChn/NoTrig and ValEvt ON during PowerOnAnalog (during bunch crossing)
- Clock is started asynchronously, enabled and stopped synchronously (at '0')
- 2 operation modes :
  - Acquisition, Conversion ➔ common to all managed by DAQ
  - Readout ➔ daisy chained managed by StartReadOut and EndReadOut





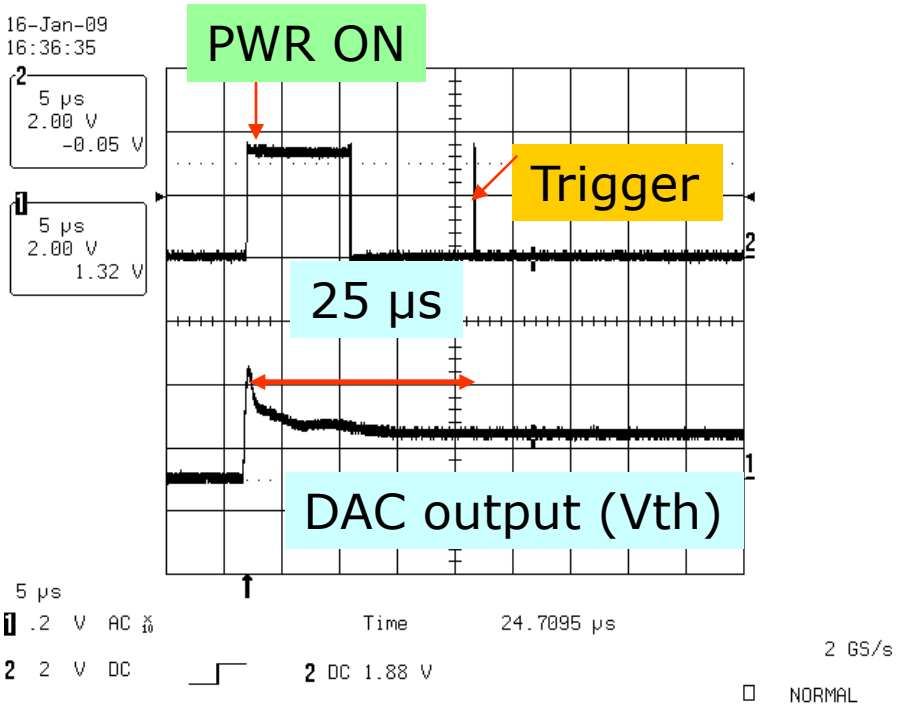
• POD successfully tested on testbench

Power pulsing: « Awake » time

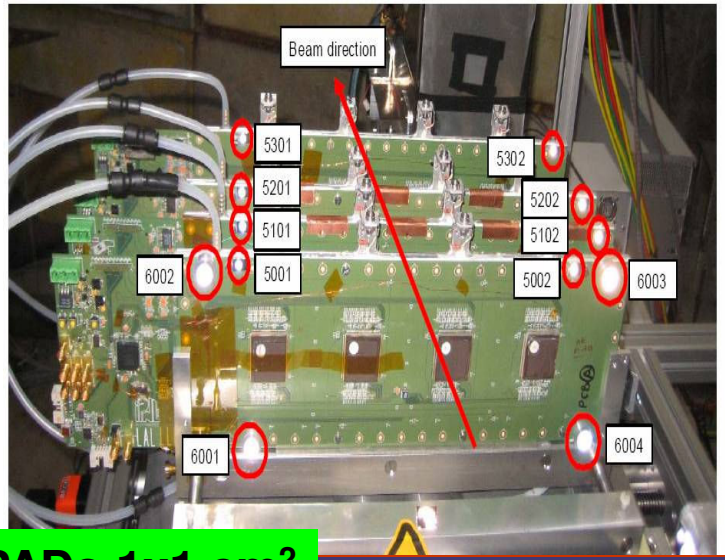


- **All decoupling capacitors removed**
- **PWR ON: ILC like (1ms,199ms)**
- **PP of the analog part:**
  - **Input signal synchronised on PWR ON**
  - **=> Awake time= 8 µs**

- **Power pulsing of the DAC:**
  - **25 µs (slew rate limited)**

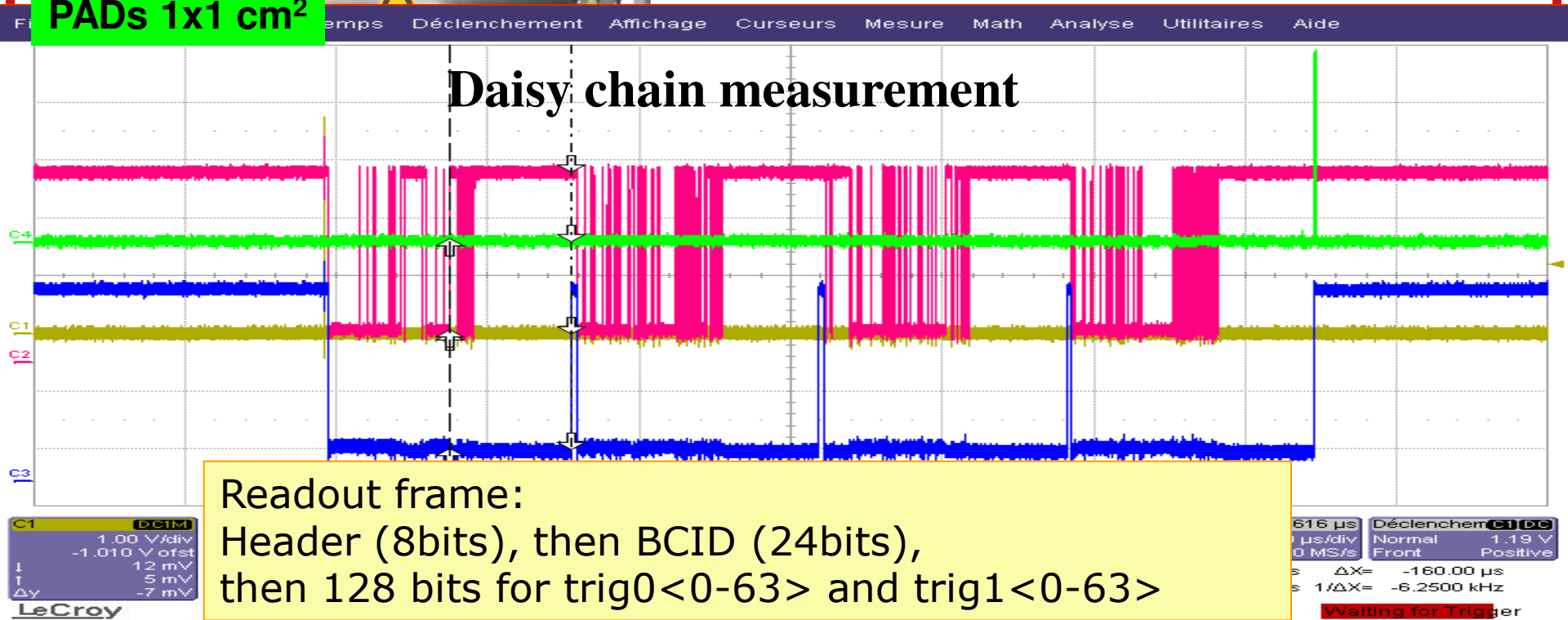


PCB board associated to both RPC and µMegas detectors



Semi-digital electronics readout system validated in beam conditions (daisy chain,stability, efficiency, no external componant)

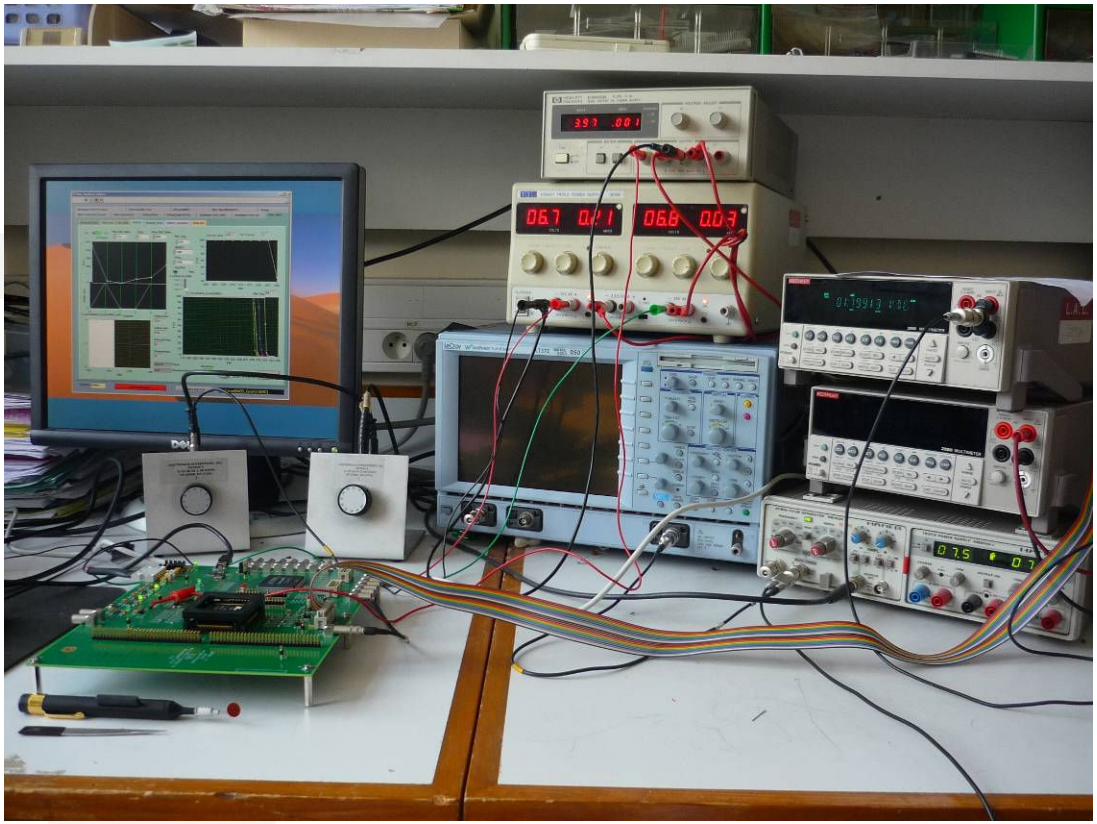
PADs 1x1 cm²



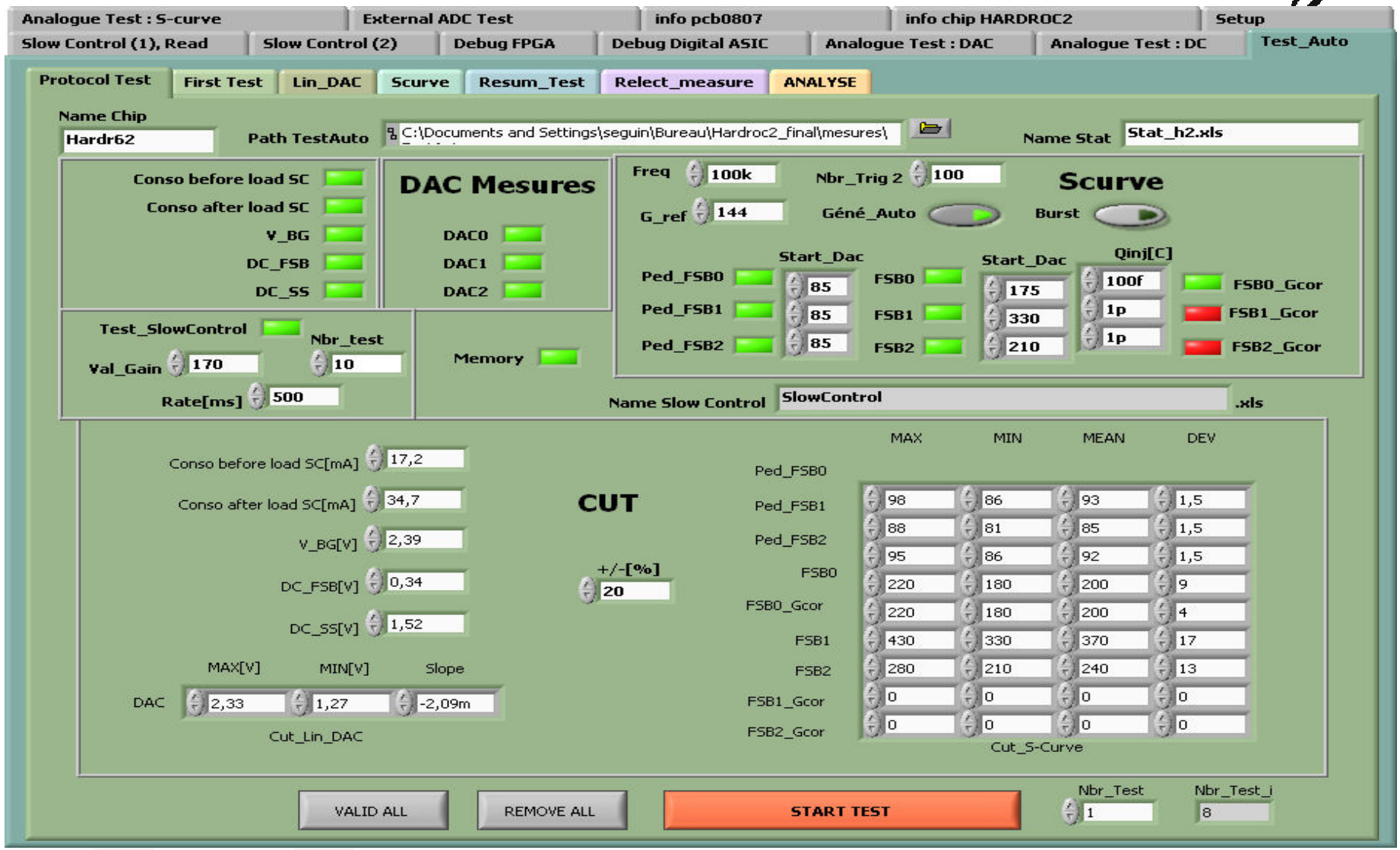
Readout frame:
Header (8bits), then BCID (24bits),
then 128 bits for trig0<0-63> and trig1<0-63>

HARDROC2: test of 400 chips

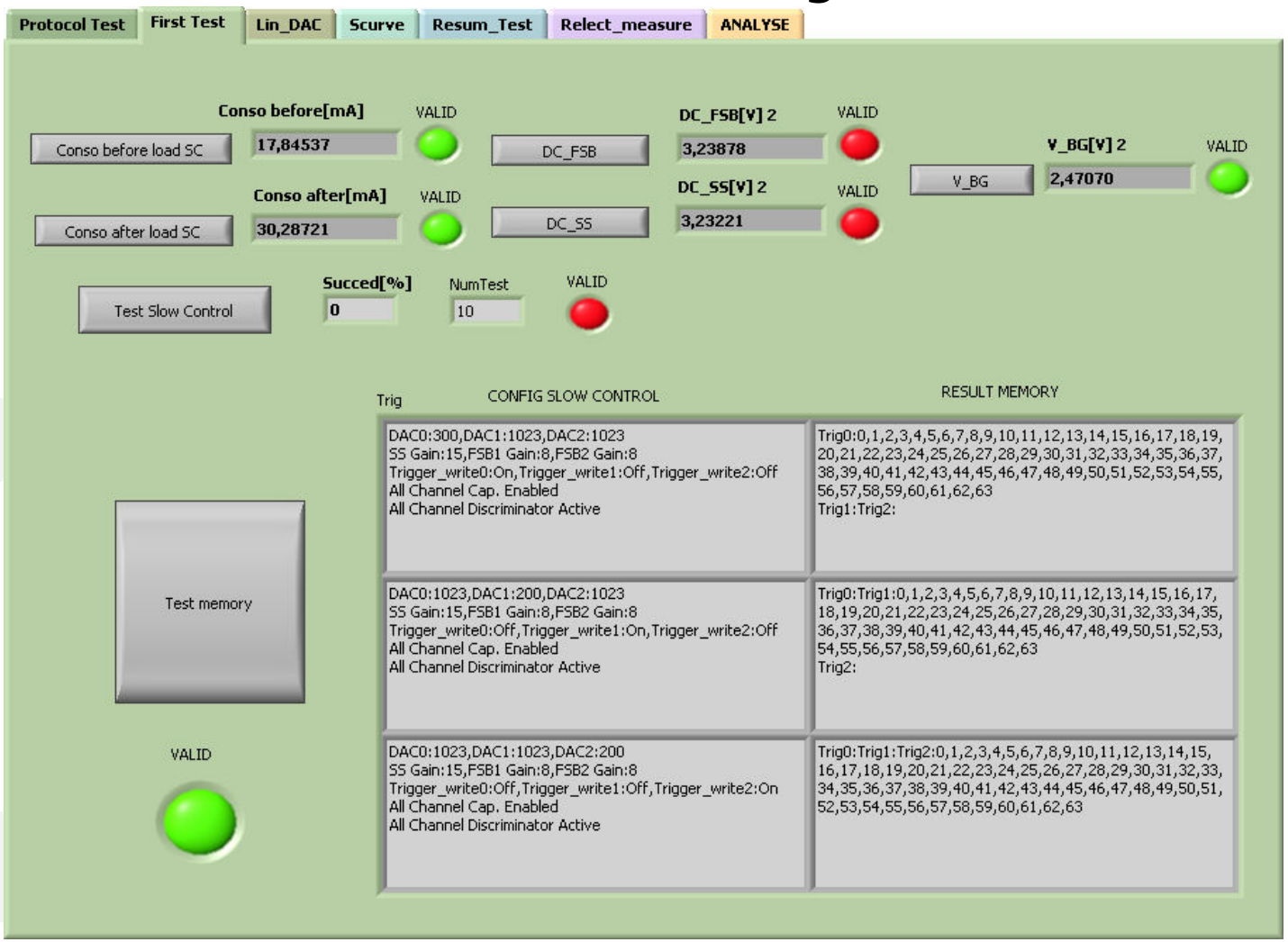
- 400 HR2 to equip 1m2 RPC and µmegas detectors
- ≈300 chips tested this summer in ORSAY and in Lyon
- Good exercise before tests of productions (5000 chips)



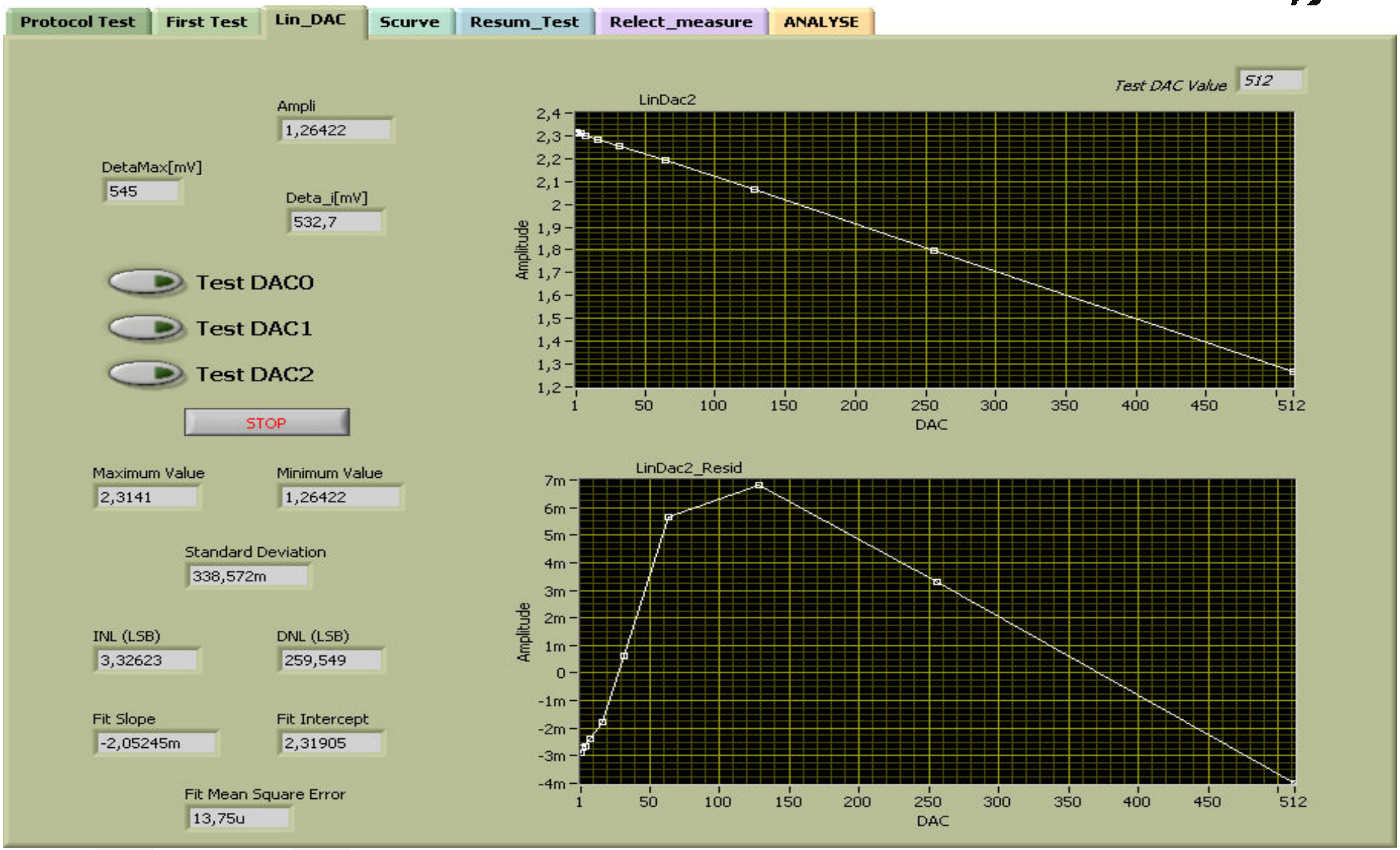
LABVIEW SETUP @Rodolphe Della Negra (IPNL)



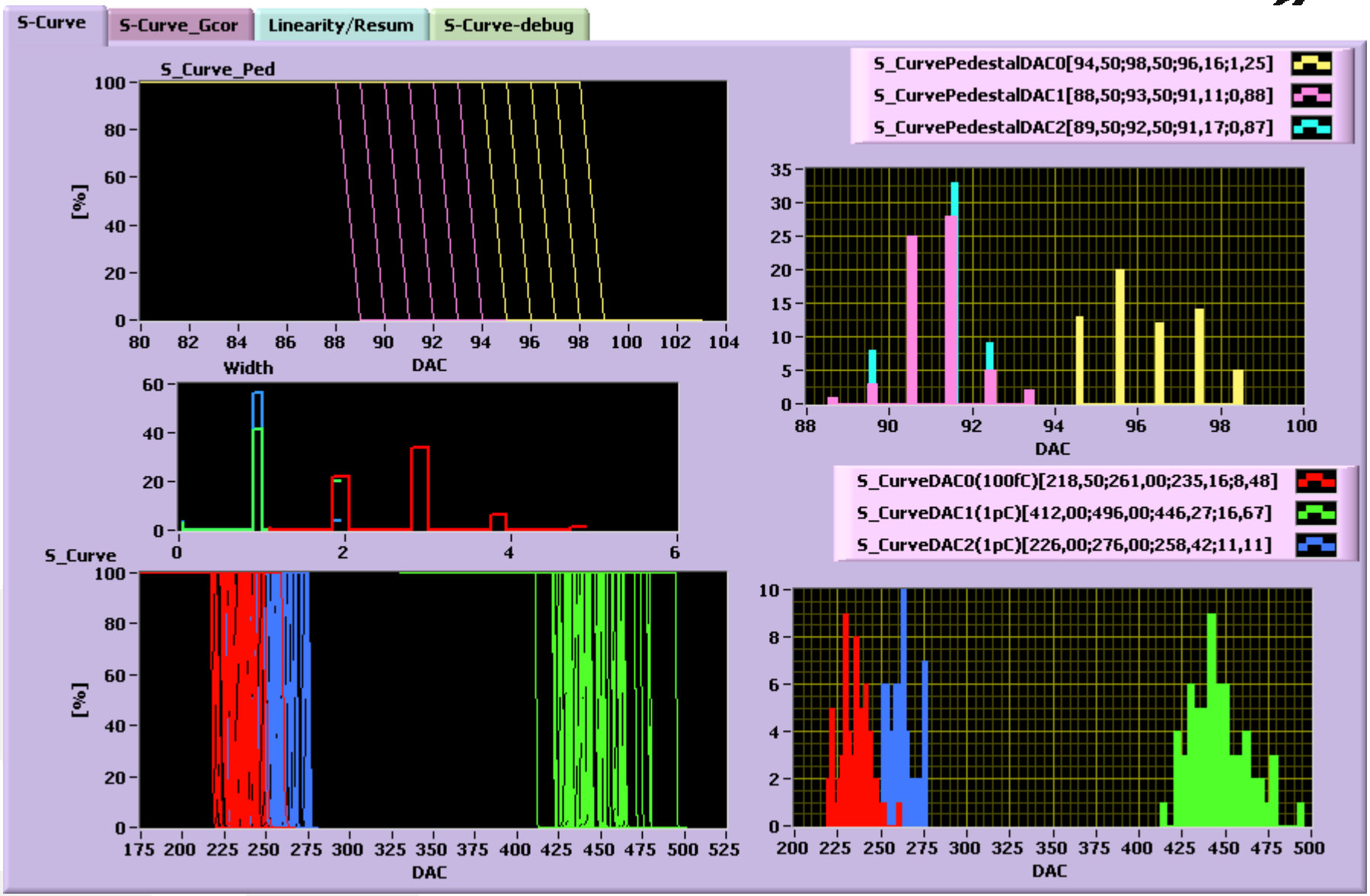
- DC levels, power consumption, VBG, memory test, SC test with a « difficult config »



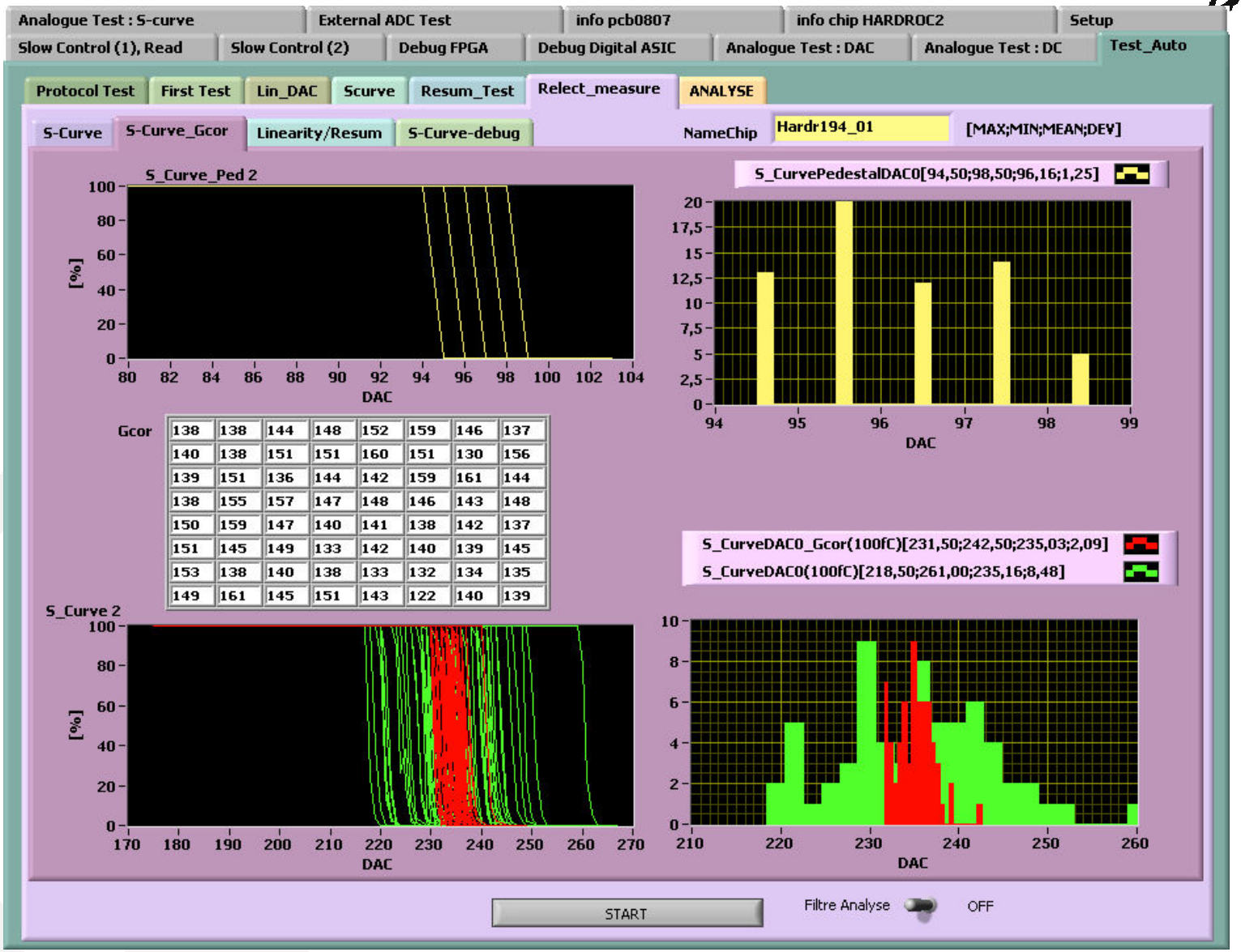
3 DACs linearity



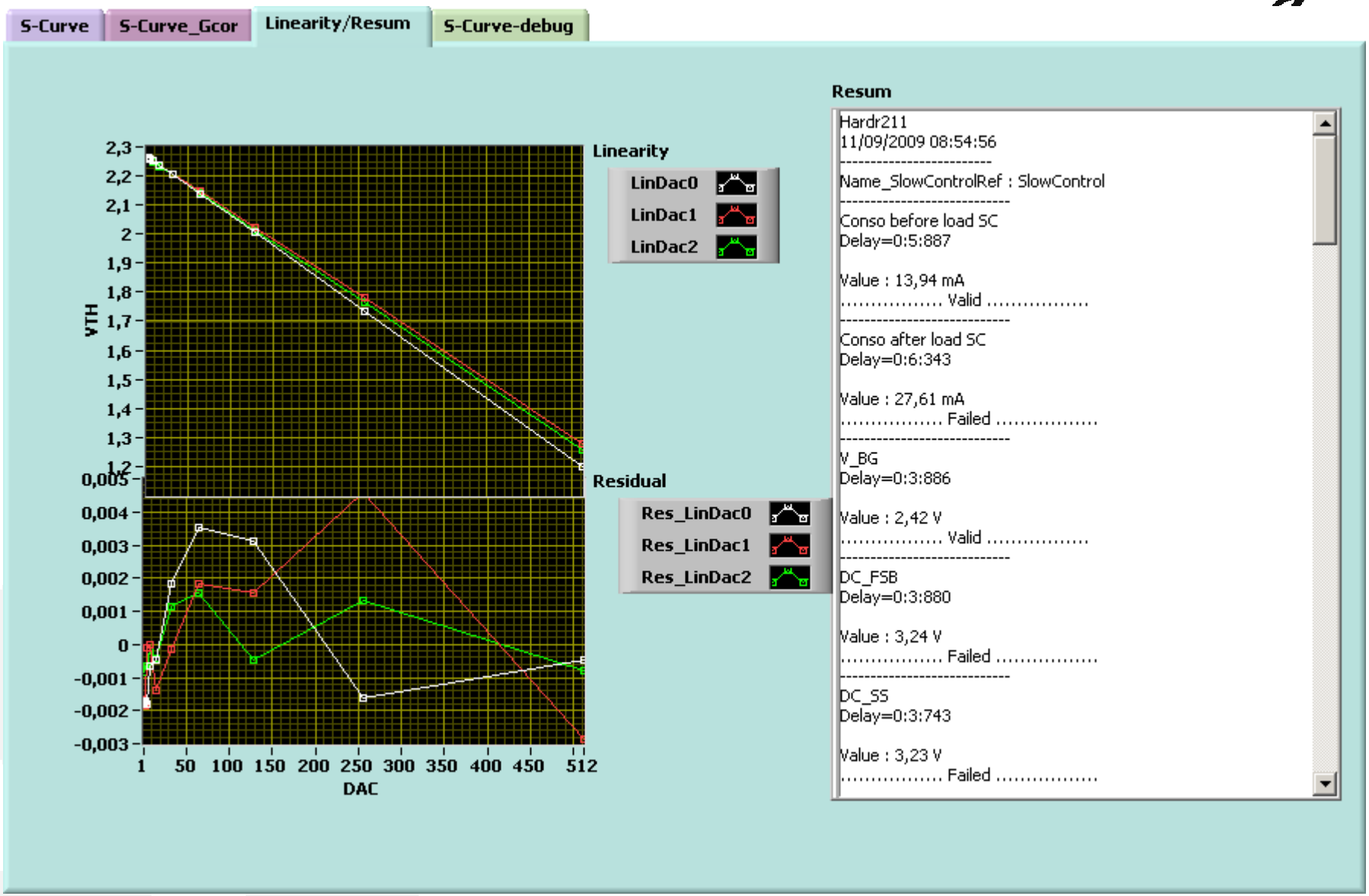
SCurves measurements: pedestal, 100fC, 1pC



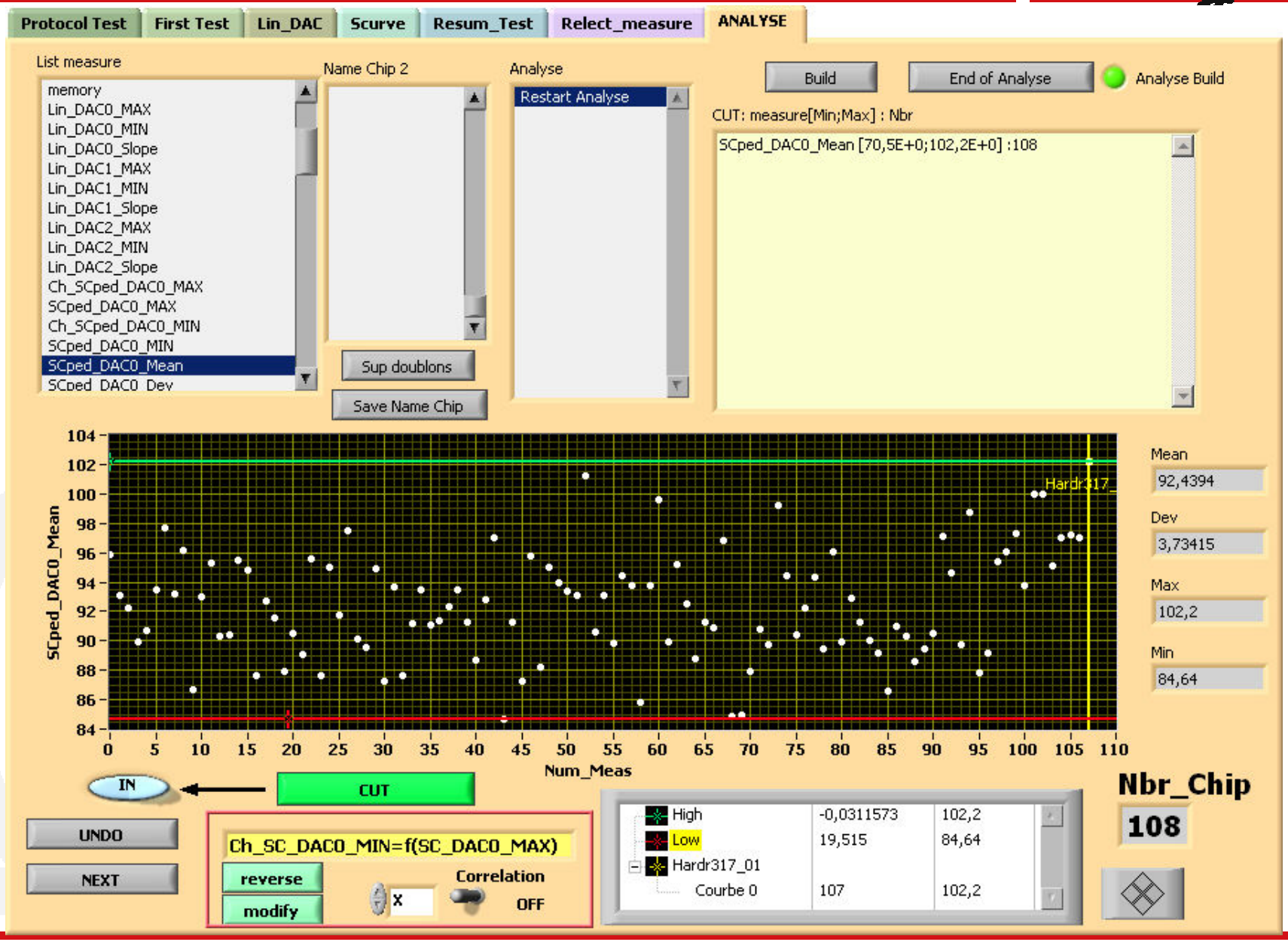
FSB0 Gain Correction



Read back of the measurements



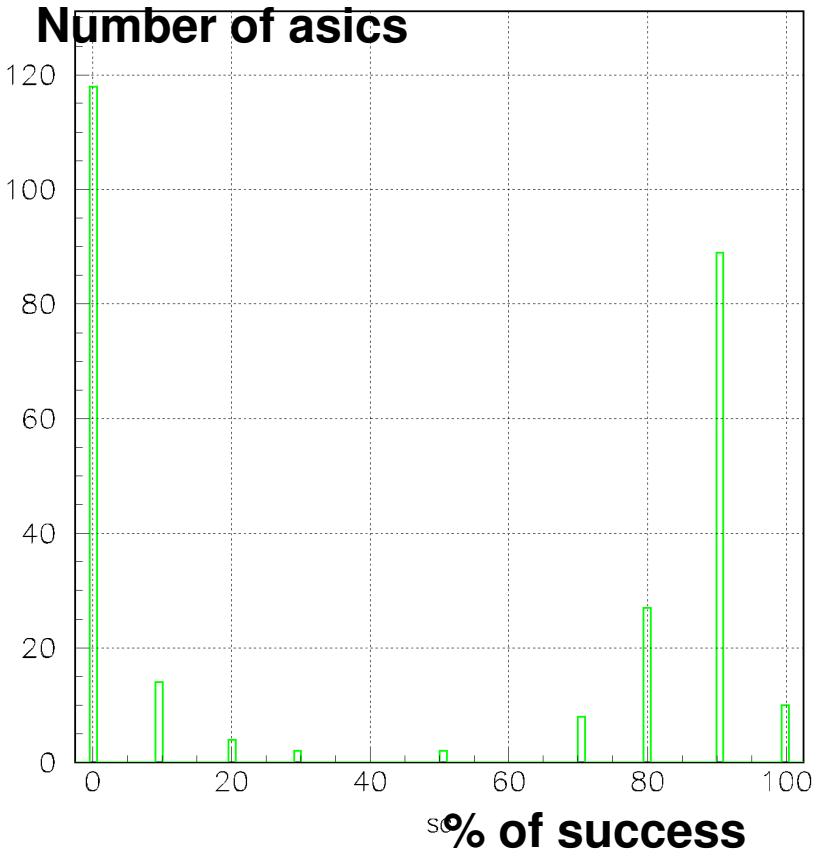
DATA ANALYSIS



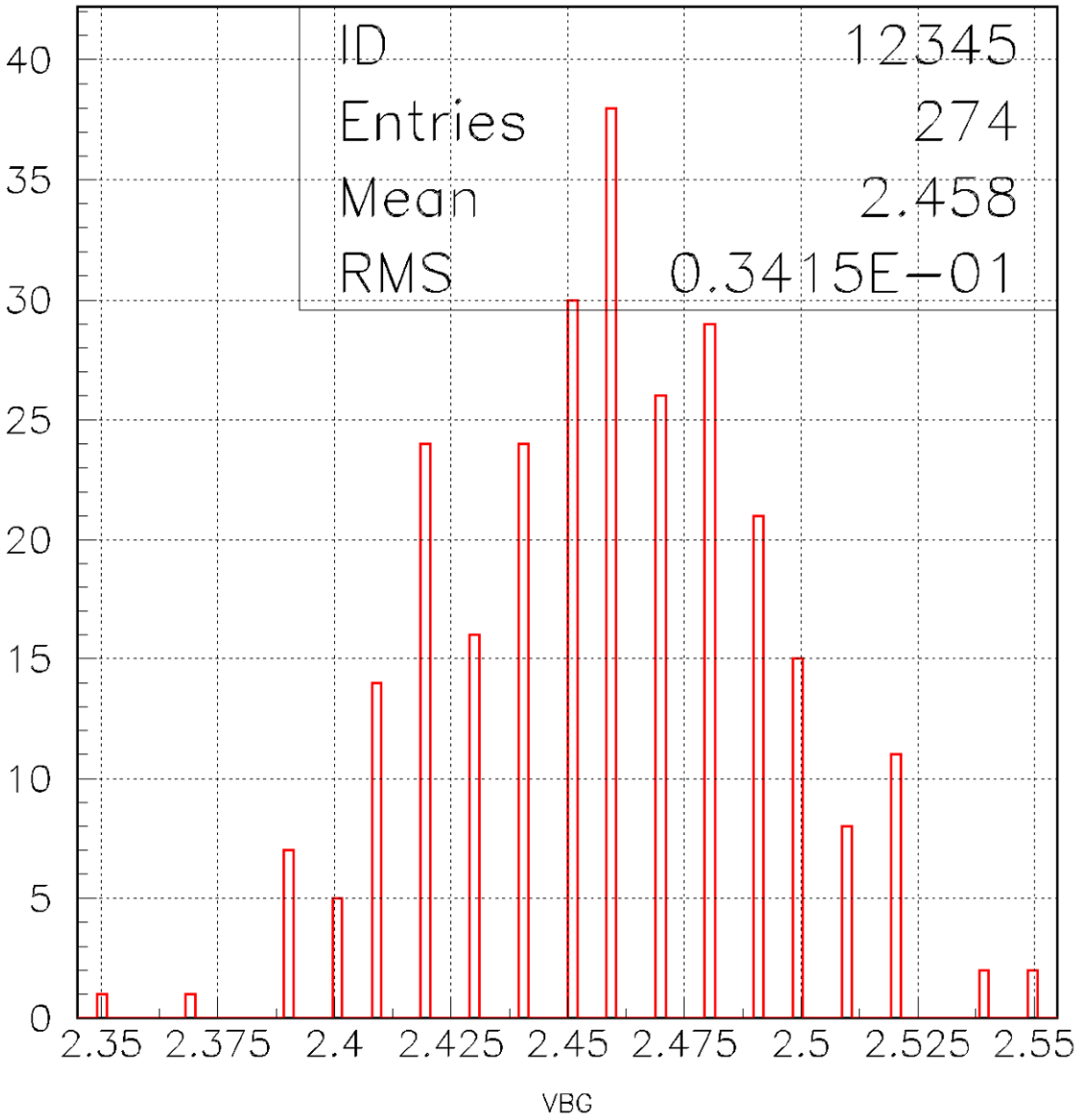
Results of the SC test performed on 274 HR2

- Some gain configurations are sometimes difficult to load in hardroc2
  - Due to long connections between flip flops inside the chip: can be corrected with additional buffers on clk and data signals
  - **necessity to increase digital vdd to 4V**.

- But still, ≈50% of the chips exhibit pb with the loading of « difficult » SC config.
  - Gain=170 = 10101010 loaded 10 times, calculation of the ratio of success.
  - **Anyway 90% of the chips OK for the other tests performed with various SC configs have to be loaded**

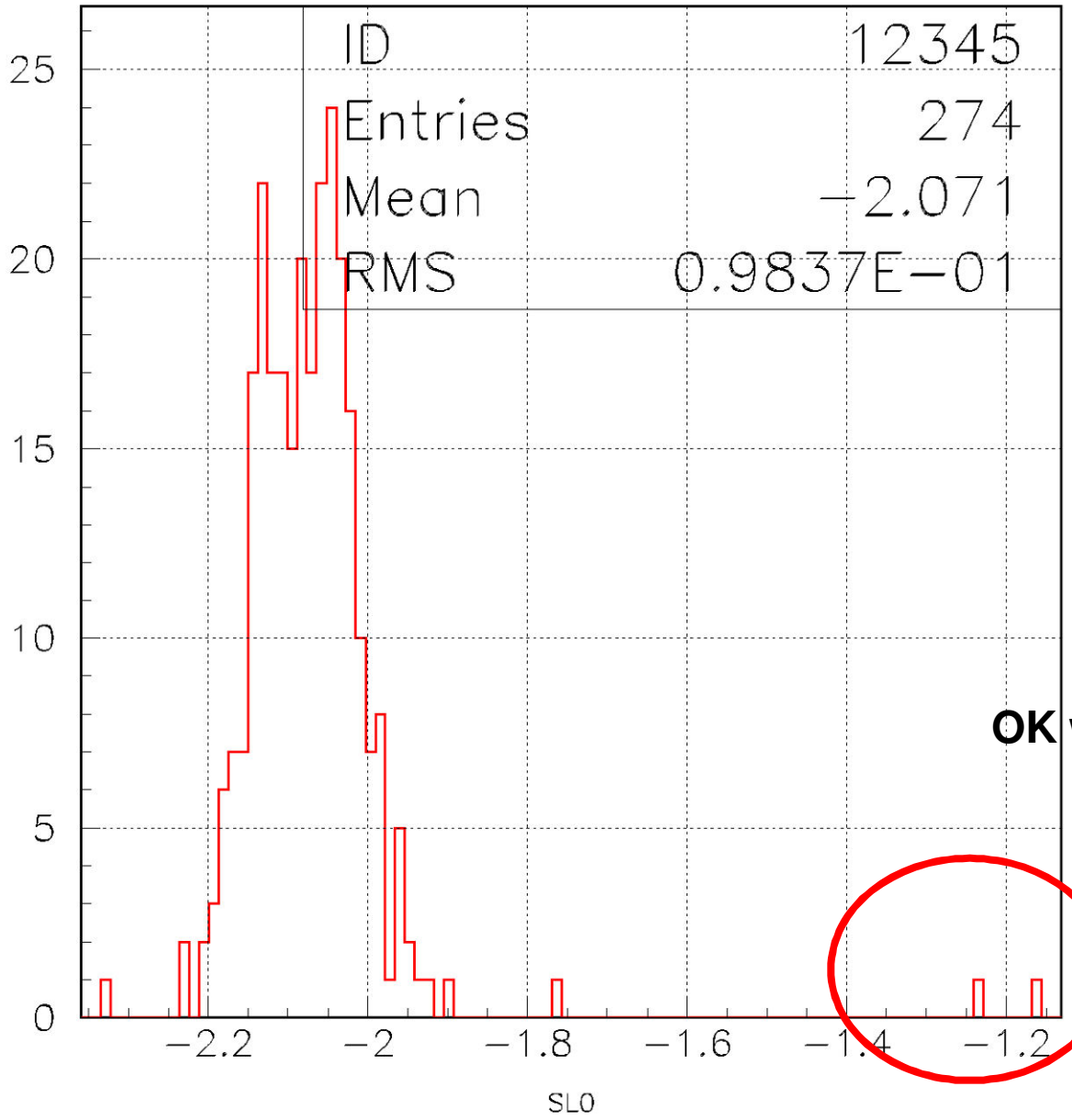


VBG



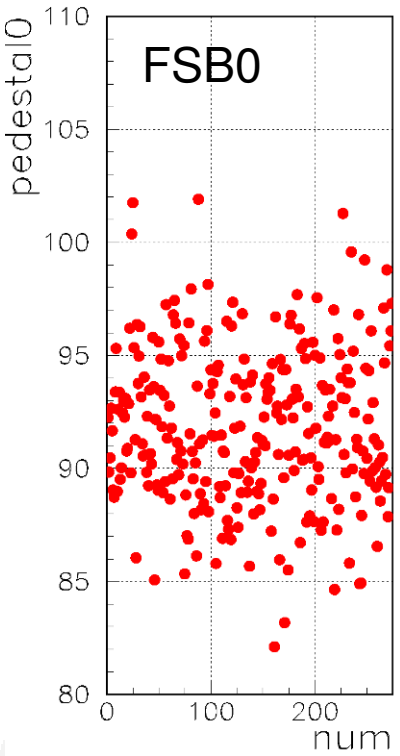
Rms=34 mV
Offset to be improved

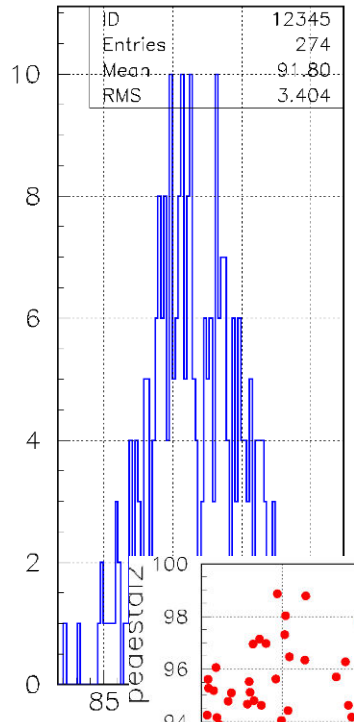
DAC0 slope

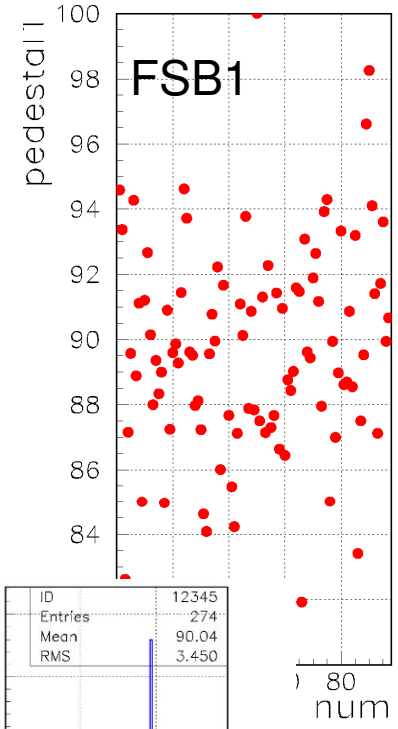


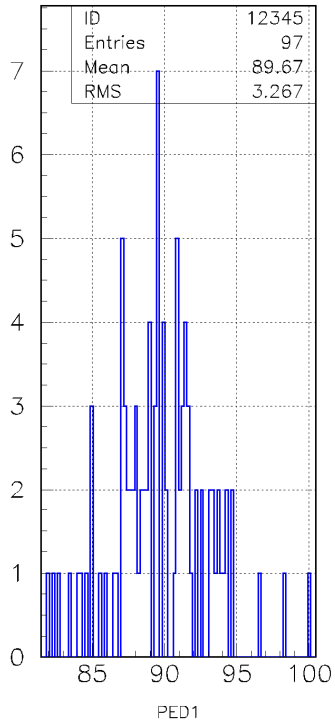
OK when redone

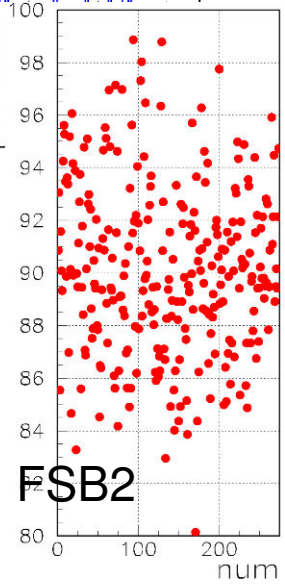
FSB0,1,2 PEDESTALS dispersion between chips

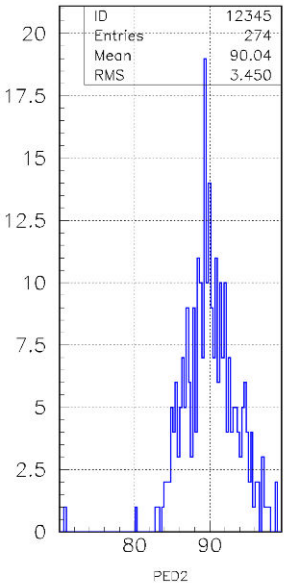








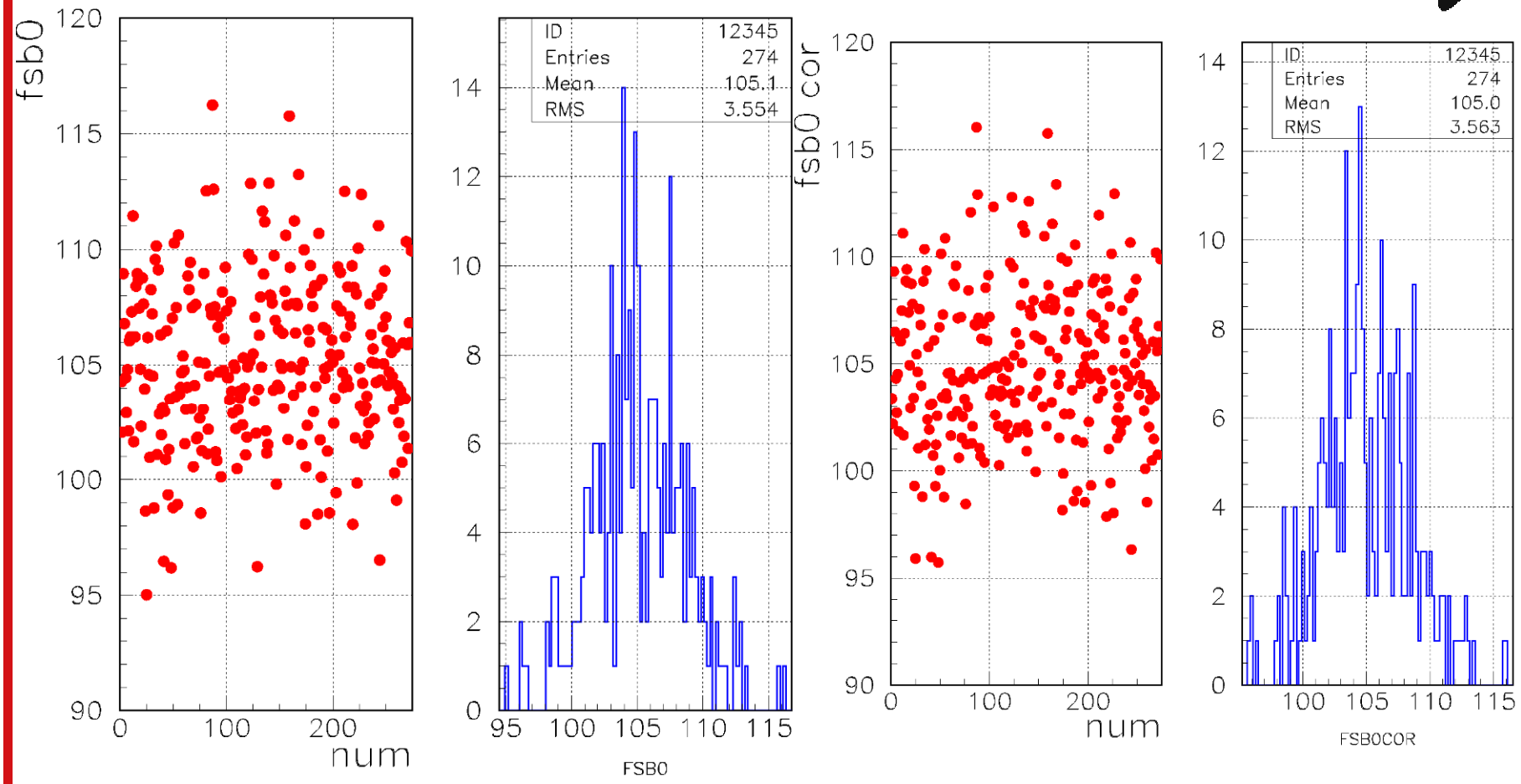




Mean=90, rms=3

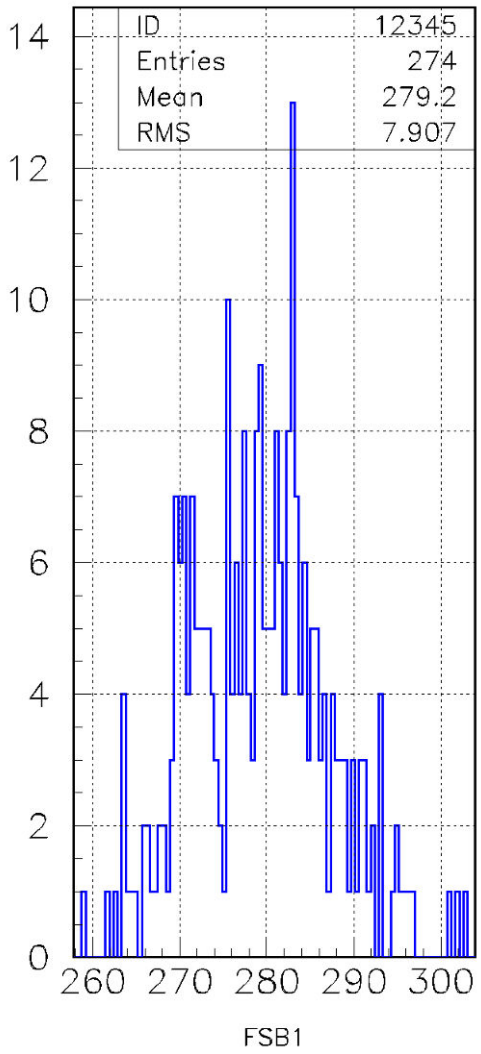
FSB2

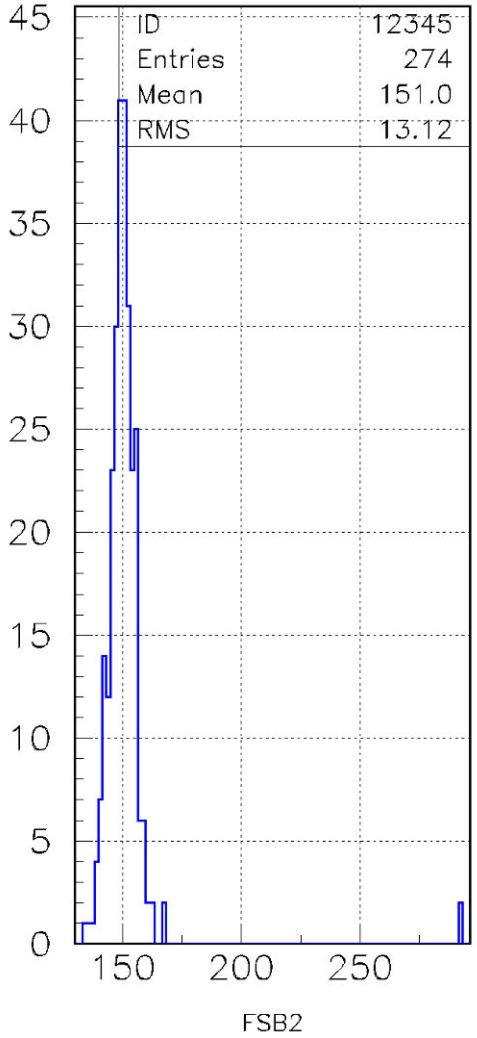
FSB0: before and after gain cor



pedestal substracted

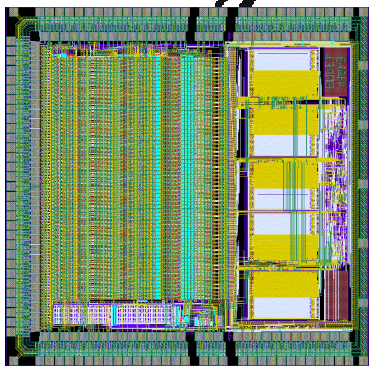
FSB1 and 2 (pedestal subtracted)



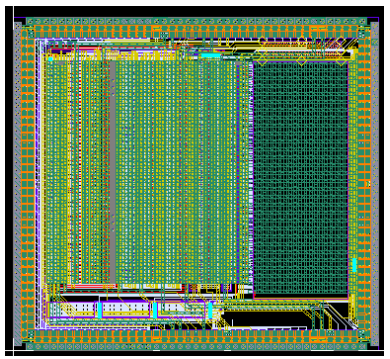


HaRDROC status

- 240 chips HARDROC1 produced in june 2007 to equip 4-chip and 24-chip RPC and Micromegas detectors
  - Package PQFP240
  - Not completely power-pulsed



- 400 chips HARDROC2 produced in june 2008 to equip 24-chip RPC and Micromegas PCBs for square meter
  - 3 thresholds (0.1-1-10 pC)
  - Power pulsed to 5-8 µW/ch
  - Package TQFP160
  - **Difficult SC loading: SOLVED in HARDROC2B**



- 200 HARDROC2b (medical application) in plastic package received beginning of jan 2010.

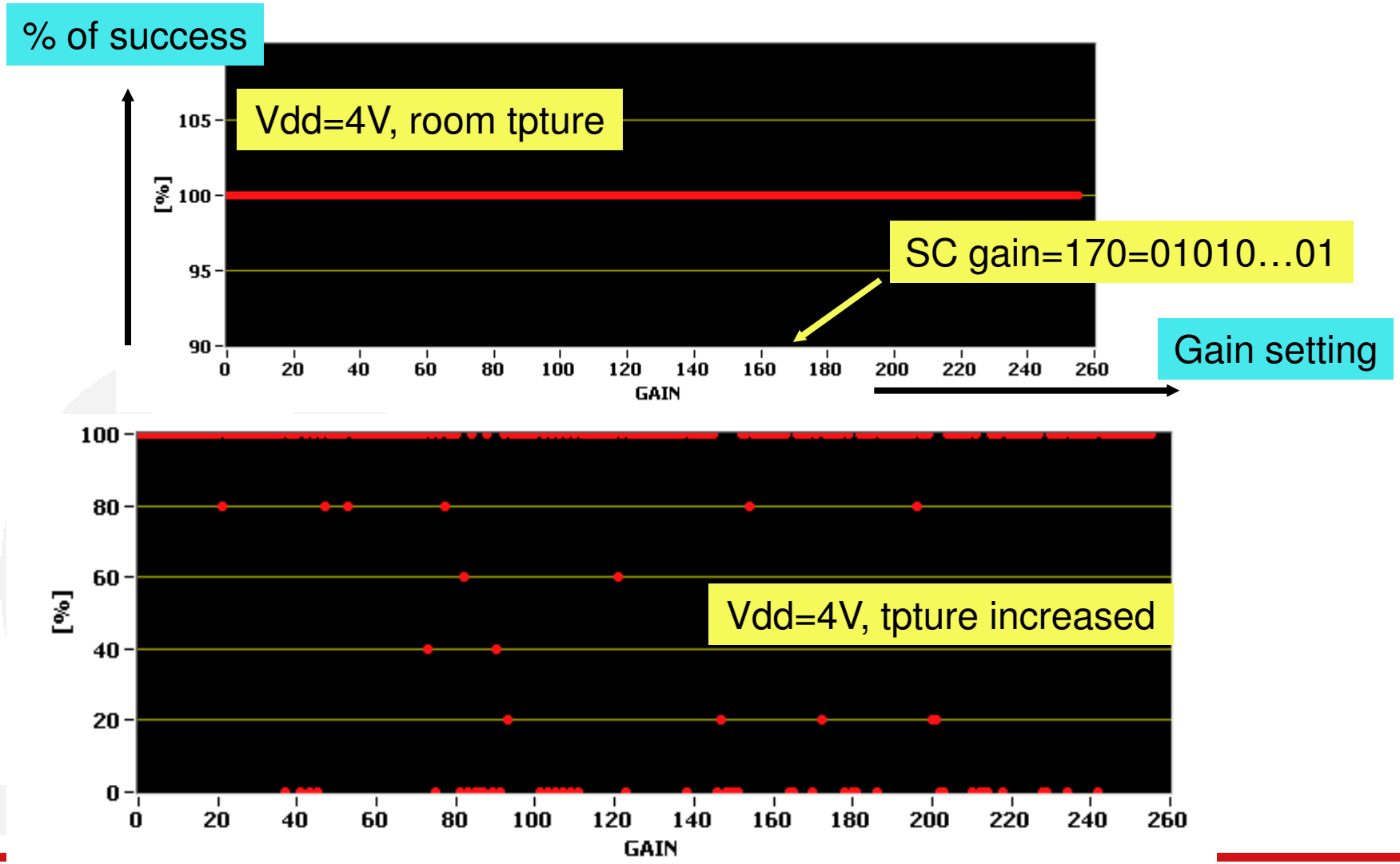
TQFP: t=1.4 mm

HARDROC2B

- Hardroc2b submitted mid June for a medical application, minor modifications
  - Pinout UNCHANGED
  - Bandgap: offset minimised
  - Read/SC selection bug corrected
  - **SC control register: buffers added on the Clk**
- 200 HR2b in plastic package received at the beginning of january 2010
- On going test in Lyon

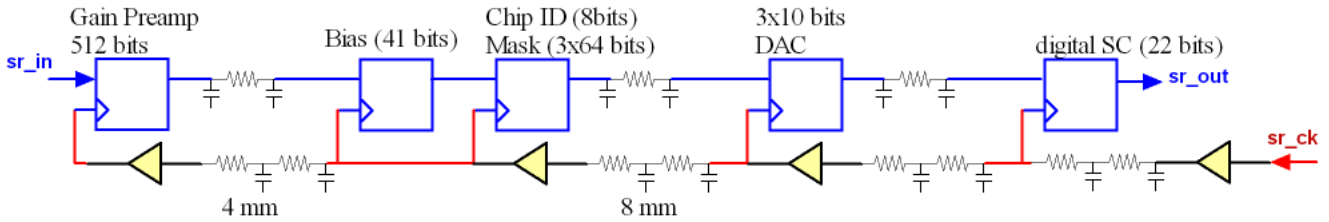
SC pb with HARDROC2

- Test of the SC: 64x8 Gain bits, Gain set from 0 to 255, SC config sent 10 times =>Loading success

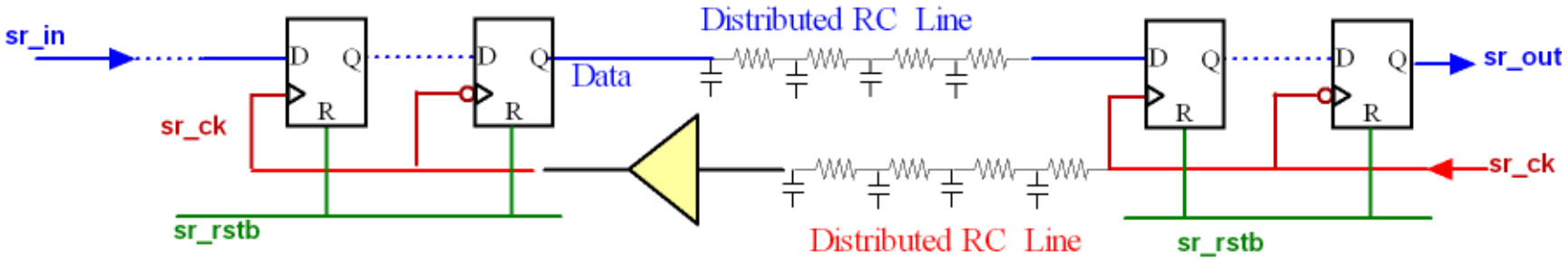


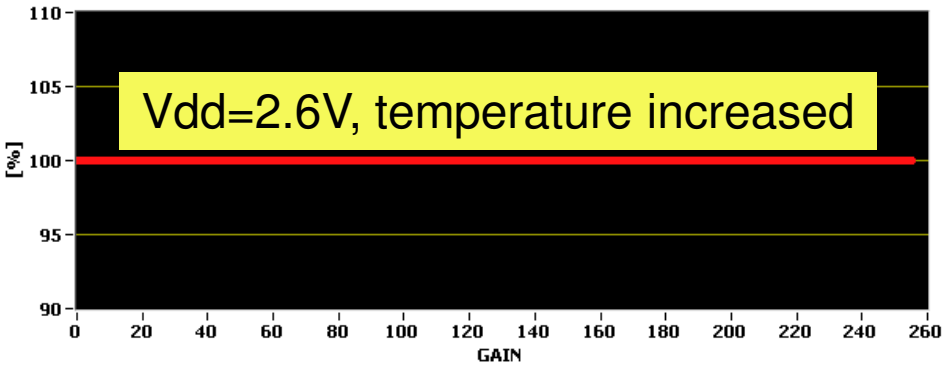
SC with HARDROC2b:

- Buffers added on the Clk only



64 x 8 bits= 512 SC parameters for Gain correction

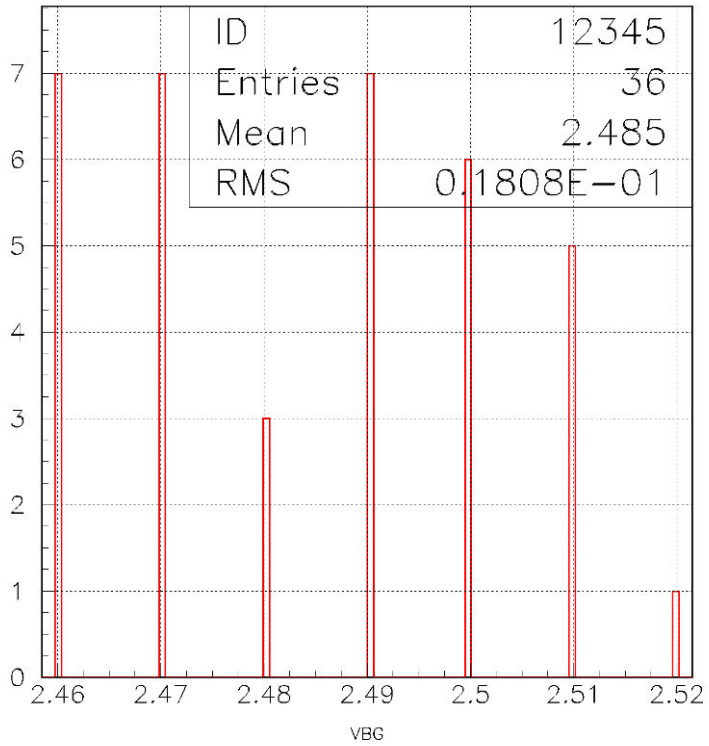




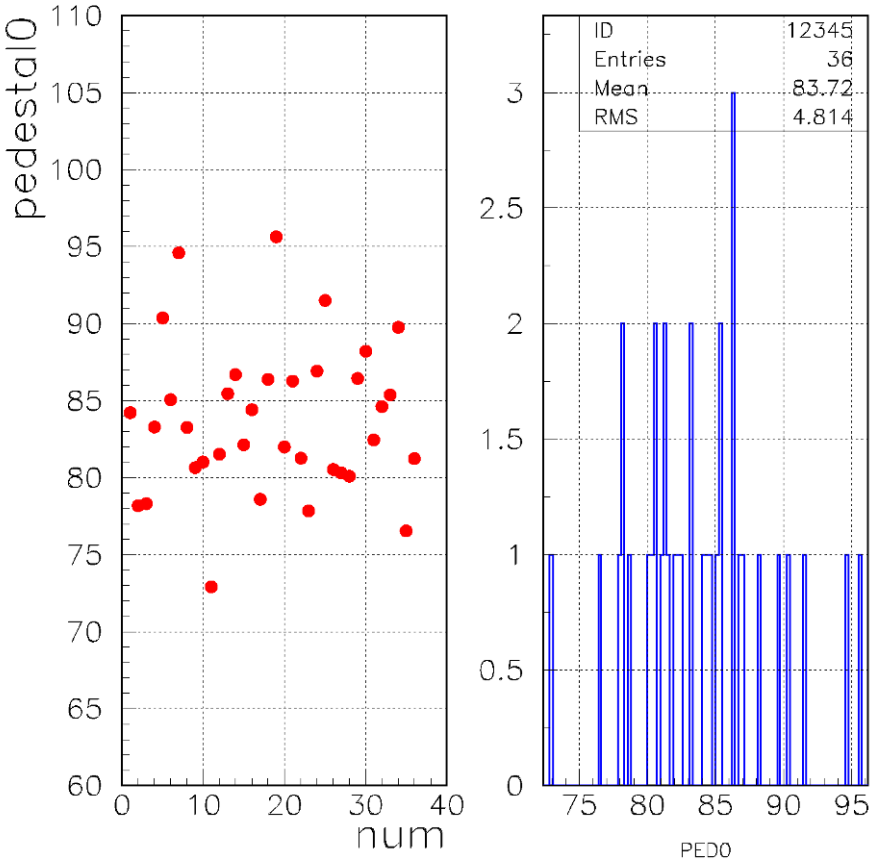
- 36 HR2b measured in Lyon: 100% success when sending the difficult SC config=10101…10, 100 times

HR2b measurements (1):

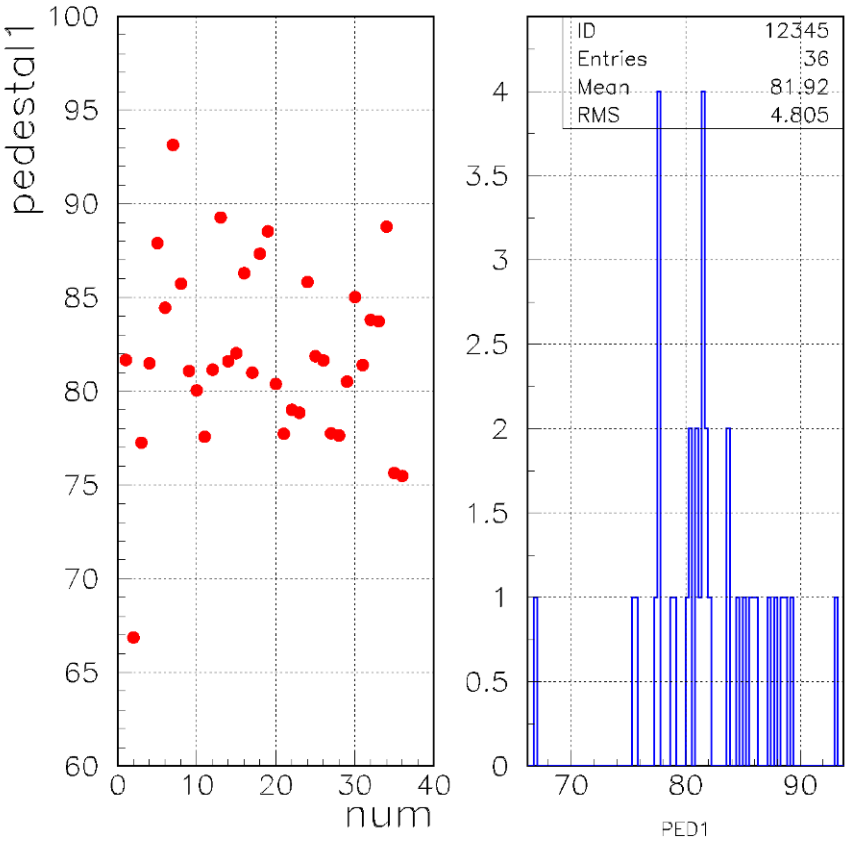
- Vbg measurement: rms=18mV instead of 34 mV in HR2

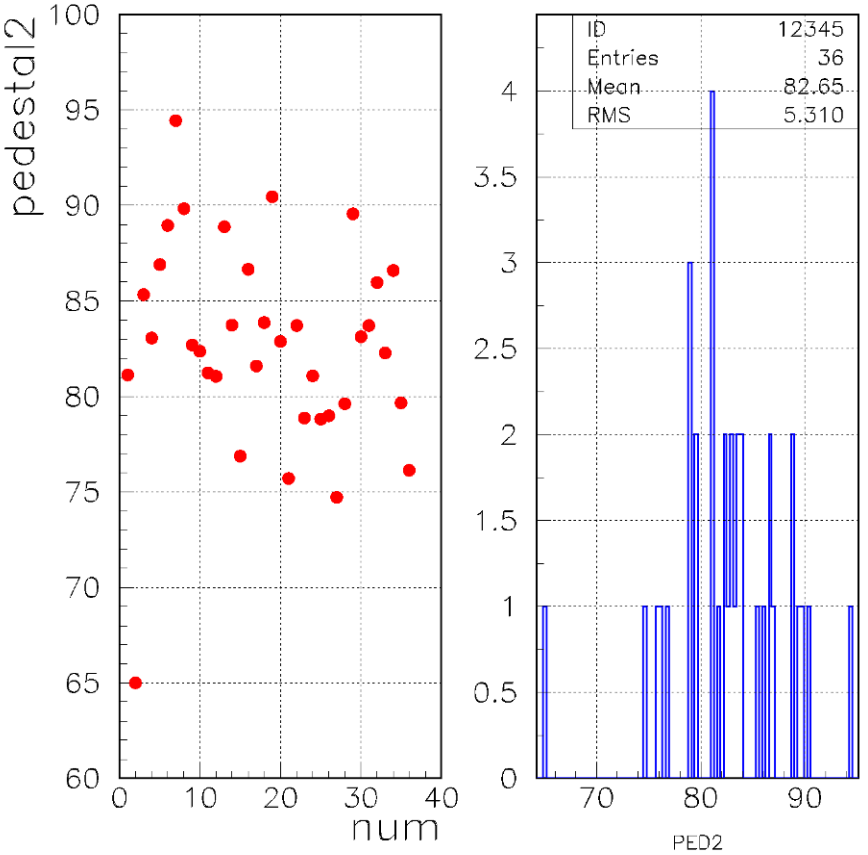


- Pedestal of FSB0



HR2b measurements (2):



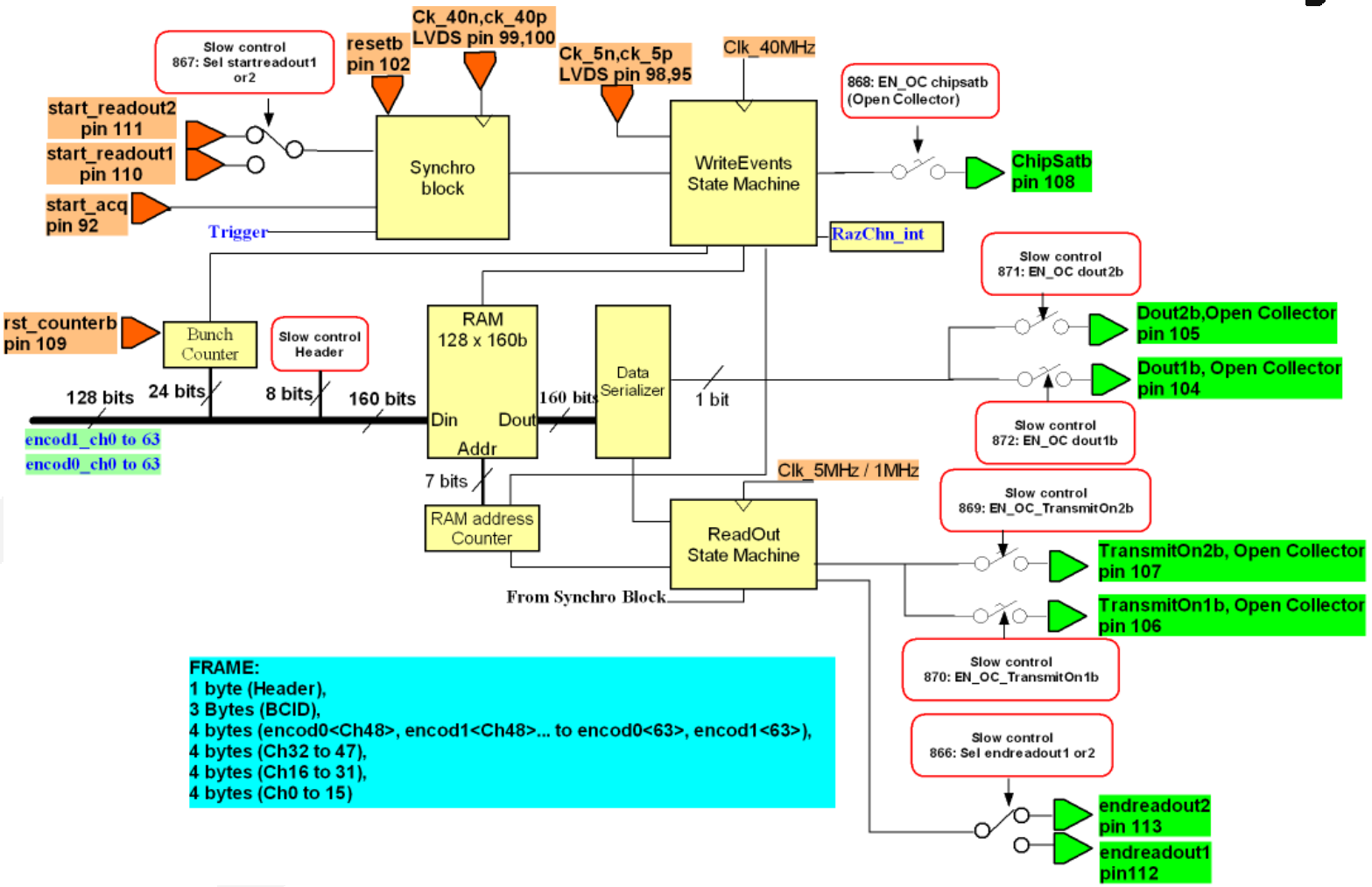


Summary

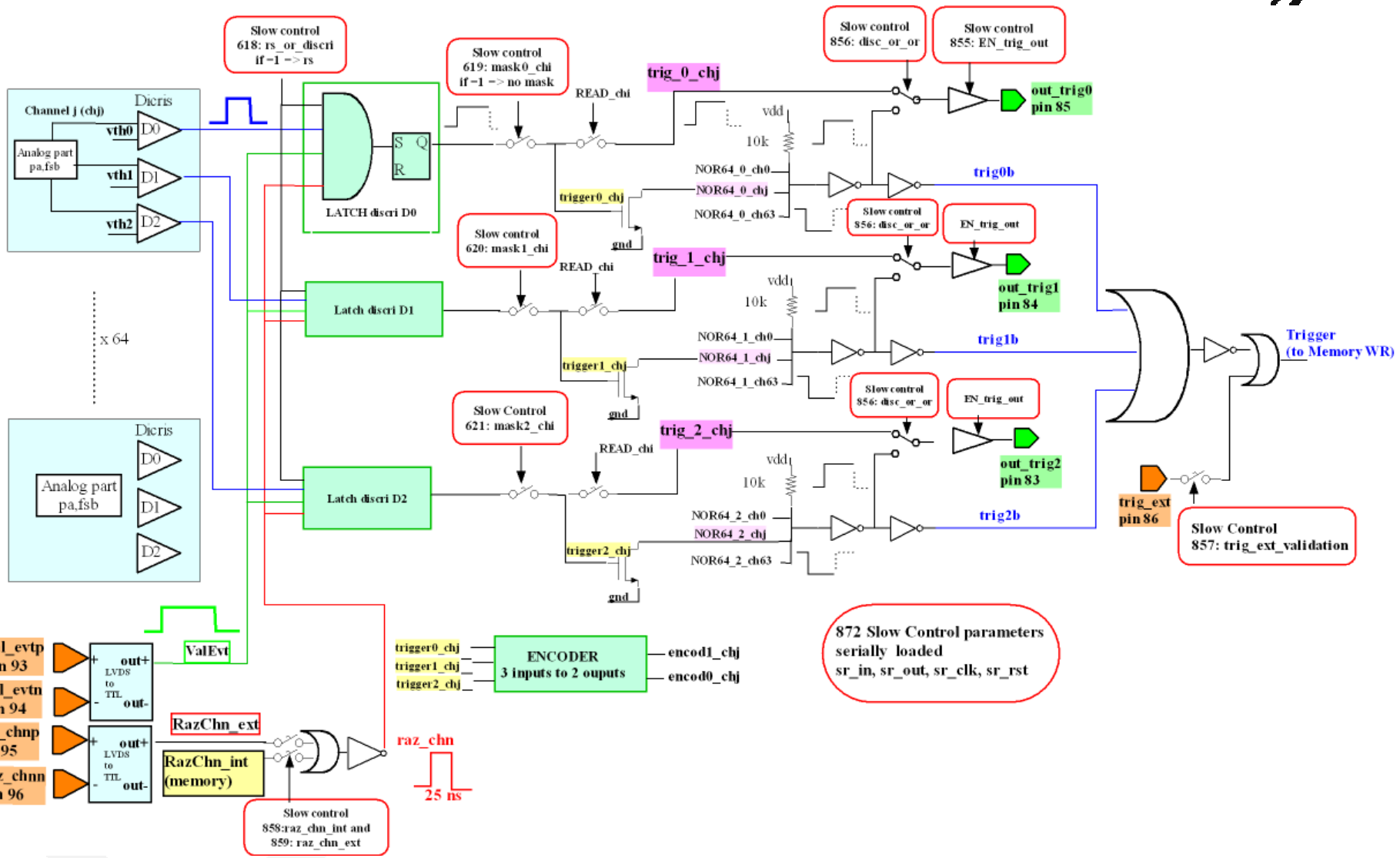
- Analog and digital performance of HR2 validated on test bench and testbeam
- SC pb solved in HARDROC2B
- On going test of the 200 HR2b: in Lyon
- => HARDROC for prod= HARDROC2B
- Test setup with a robot to test 10000 chips (IPN Lyon)

ANNEX

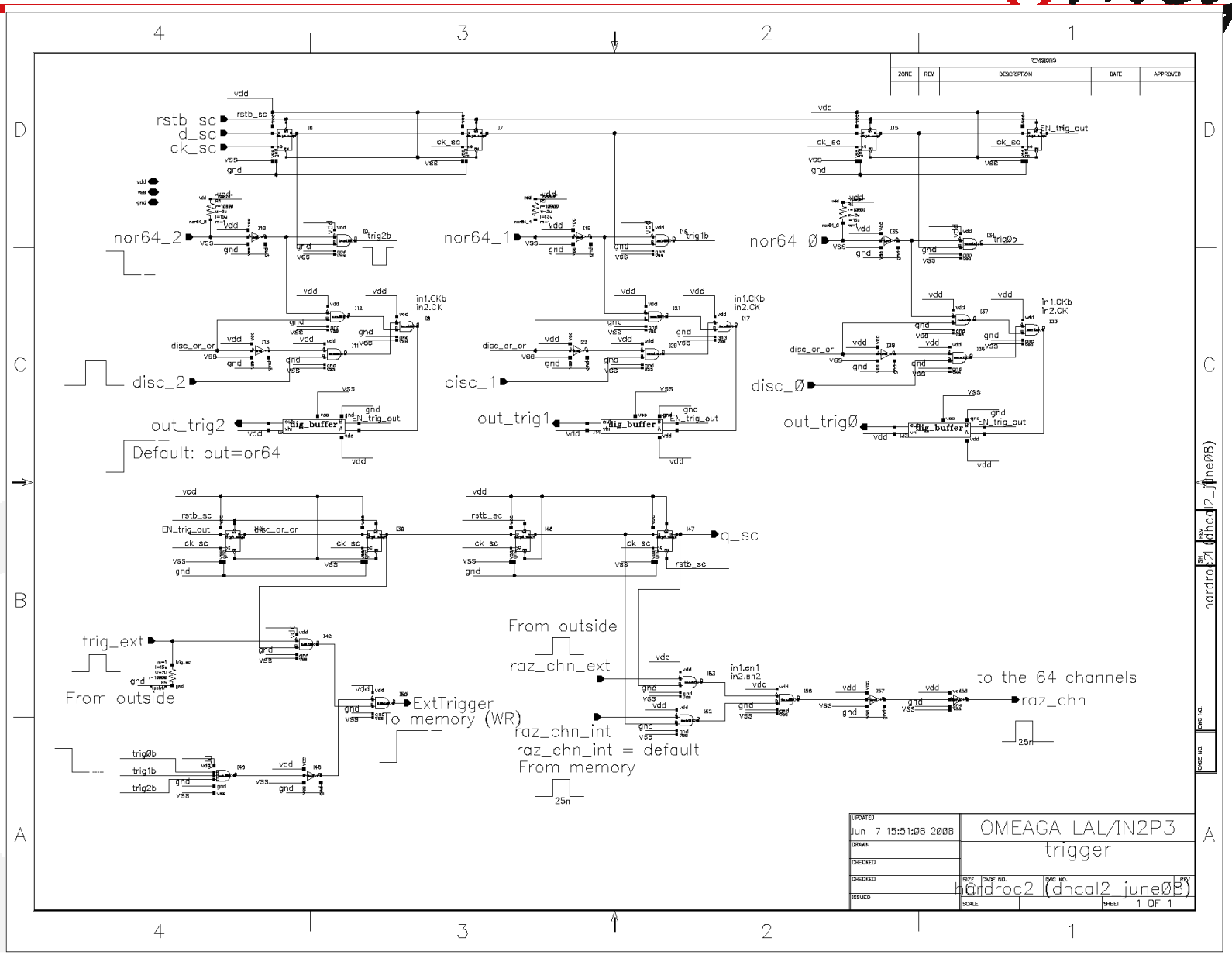
Digital part



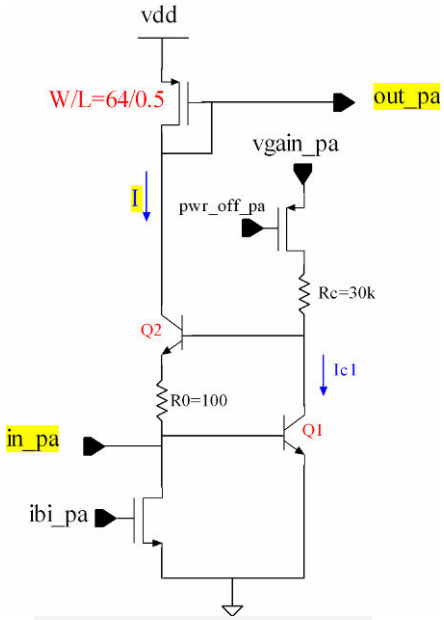
Analog to Digital schematics

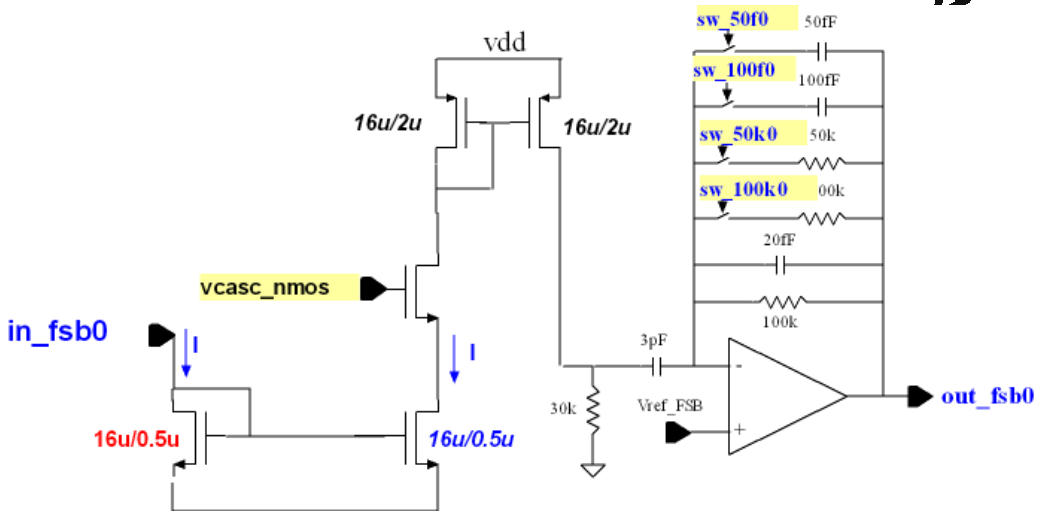


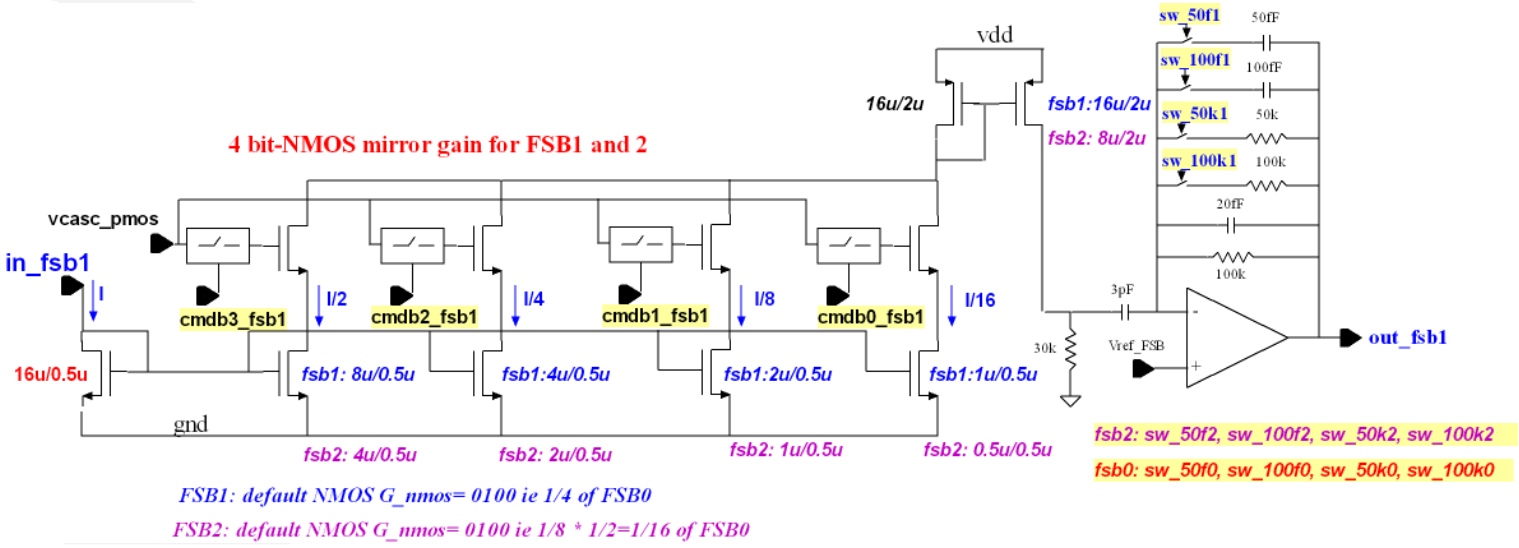
TRIGGER and RazChn



PA+FSB schematics

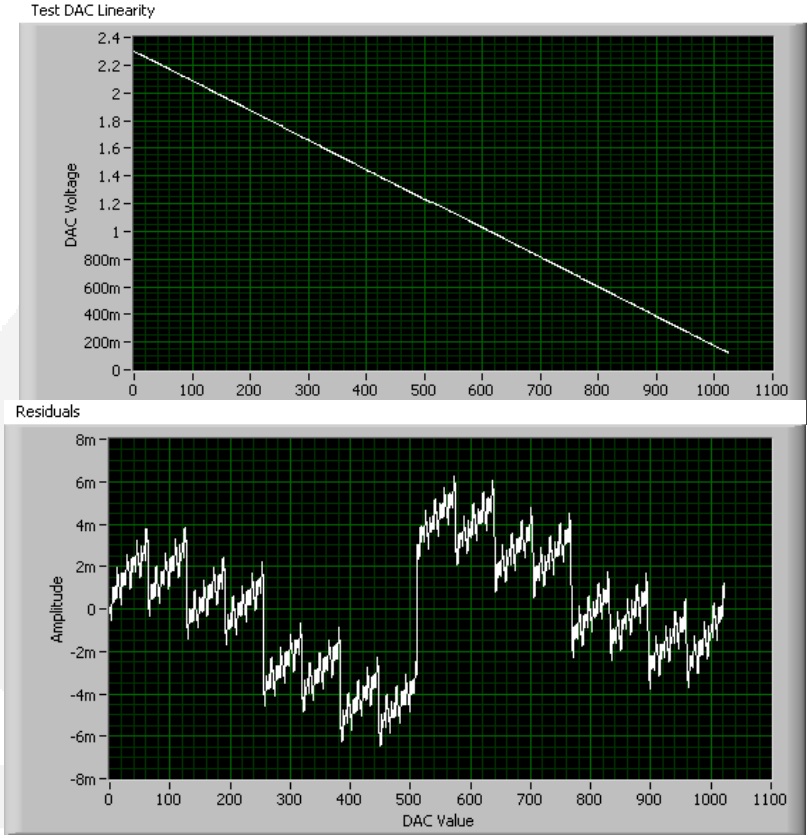


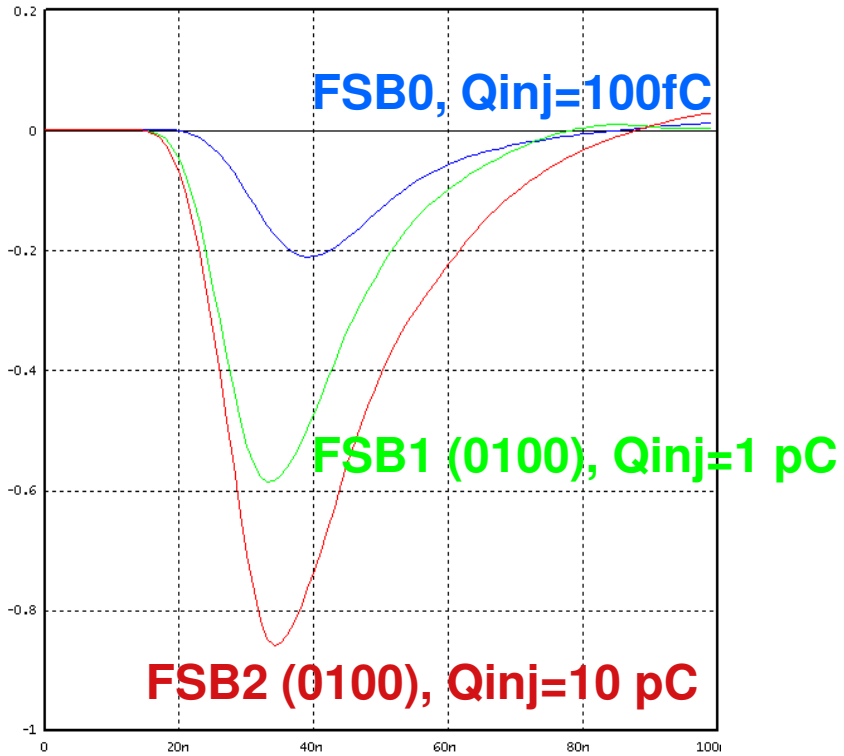




Trigger path : fast shaper and DAC

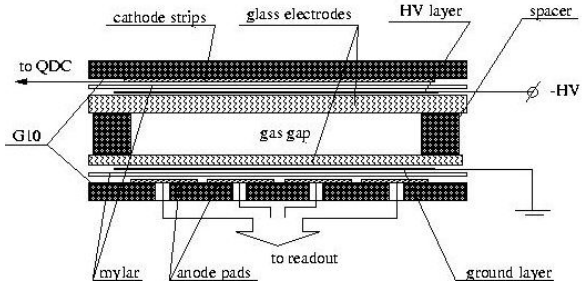
- Charge injected in one channel: 100fC
  - **Fsb0: Typically 2mV/fC** (variable by a factor 10)
- Scurves performed by varying the DAC value (Threshold)
  - 3 integrated DACs to deliver threshold voltages
  - Residuals within ±5 mV / 2.2V dynamic range. INL= 0.2% (2LSB)
  - **2.1 mV/DAC Unit ie 1 fC/DAC Unit (fsb0)**

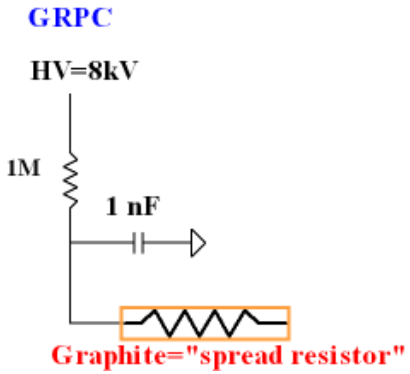




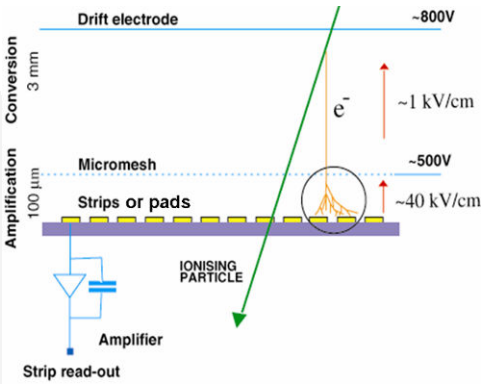
HV sparks (ESD)

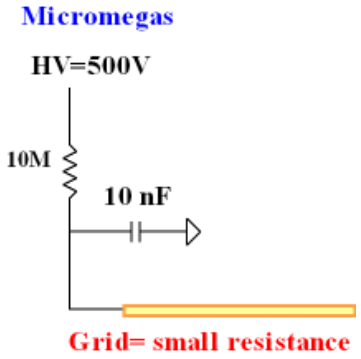
- **GRPC**: HV=8 kV, PADs= a few pF
  - High spread resistor= isolates FE inputs





- **Micromegas**: HV=400V, Pads= a few pF
  - Small spread resistor= NO ISOLATION of the FE inputs

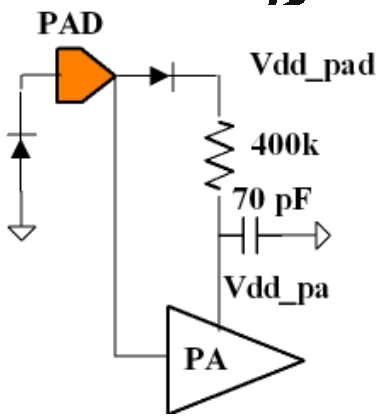




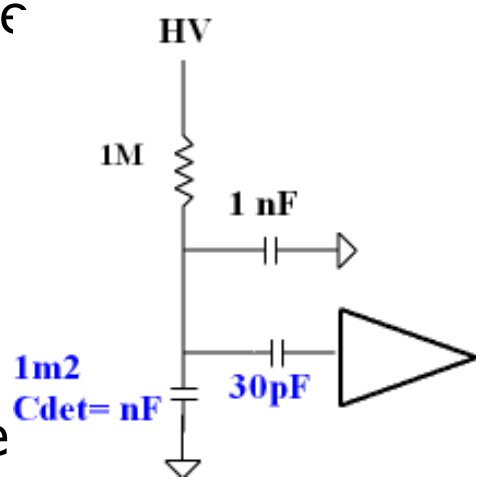
- **1m²** => C_{HV}~ **1nF**

HV sparks (ESD)

- ASIC inputs:
  - protection PADs (AMS library): robustness up to 2kV HBM (100pF)

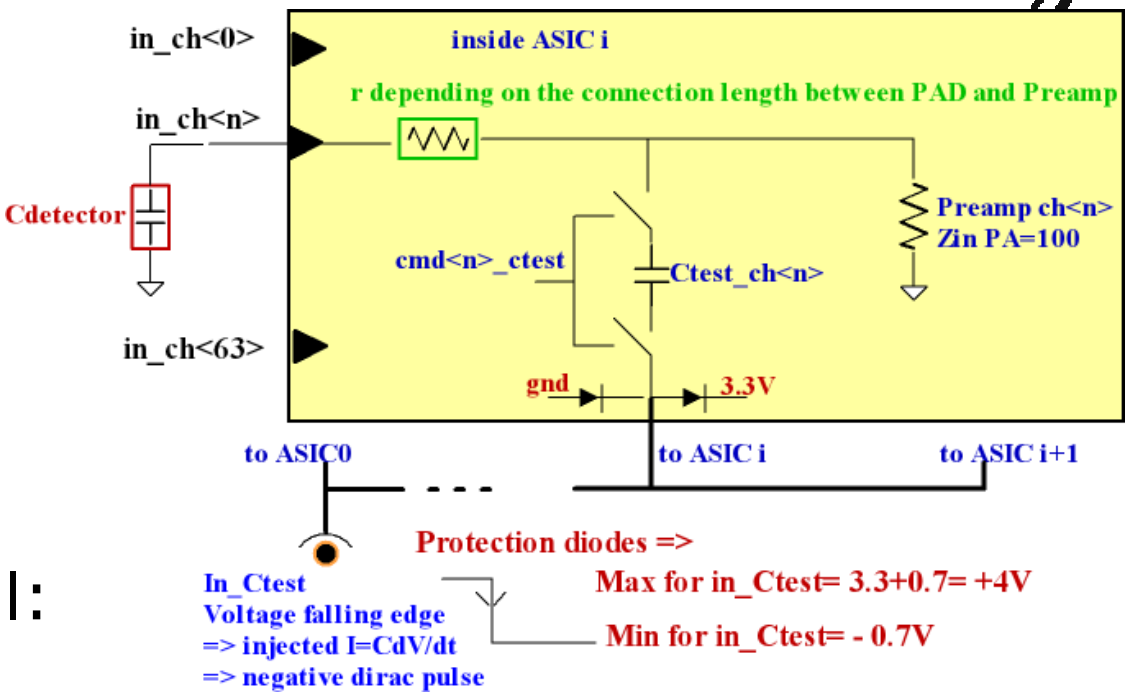


- From T2K large µmegas, **AC coupling necessary for detector > 10 cm²:**
  - **Maximum decoupling** capacitor that can be **integrated: ≈30pF** (50µm x 600 µm) and **lost of signal**
  - **EXTERNAL CAP=500 pF/ch** to ensure protection
  - Drawbacks of a decoupling cap: Xtalk, space

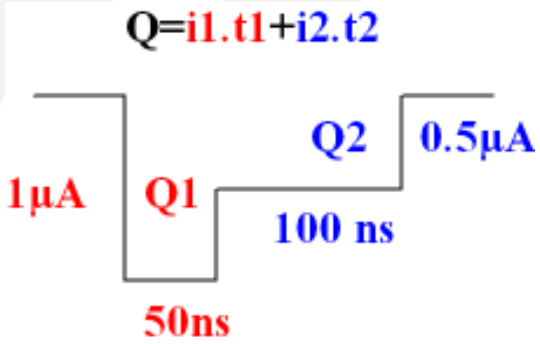


CALIBRATION

- RPC signal:
  - dirac current



- Micromegas signal:



=> FS is too fast compared to the signal