

# Omega

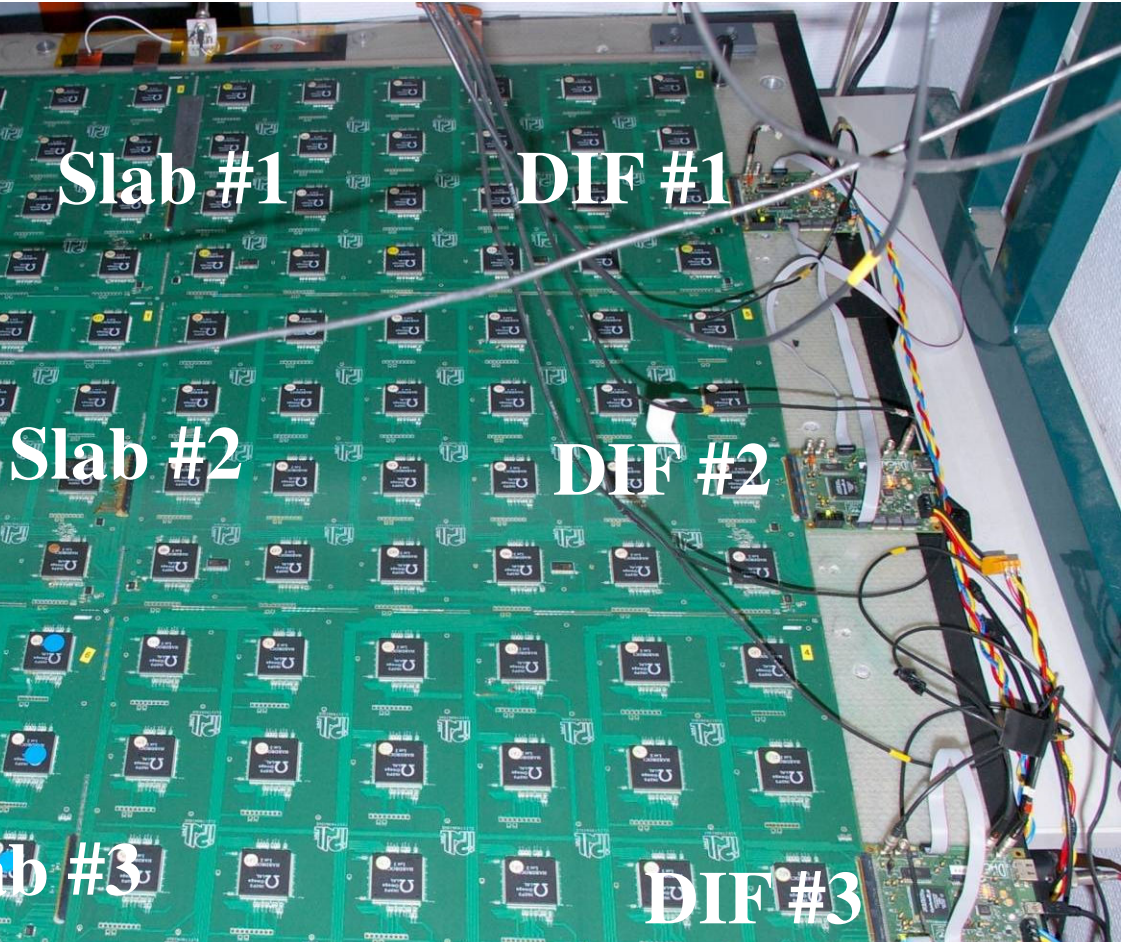
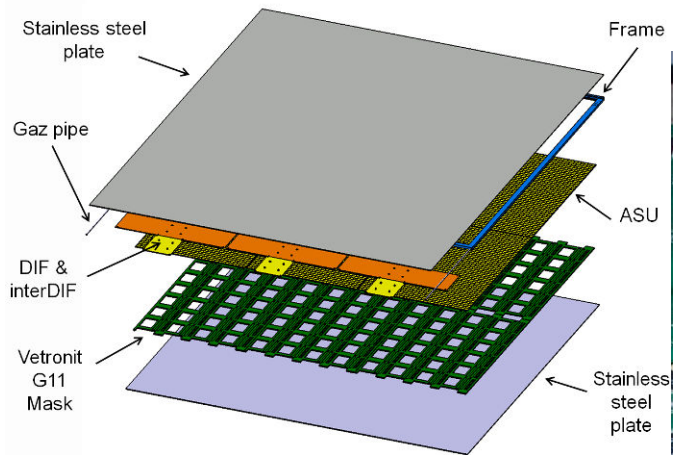
## HARDROC2: Before production

<http://omega.in2p3.fr/>

Nathalie Seguin-Moreau



*Orsay MicroElectronic Group Associated*

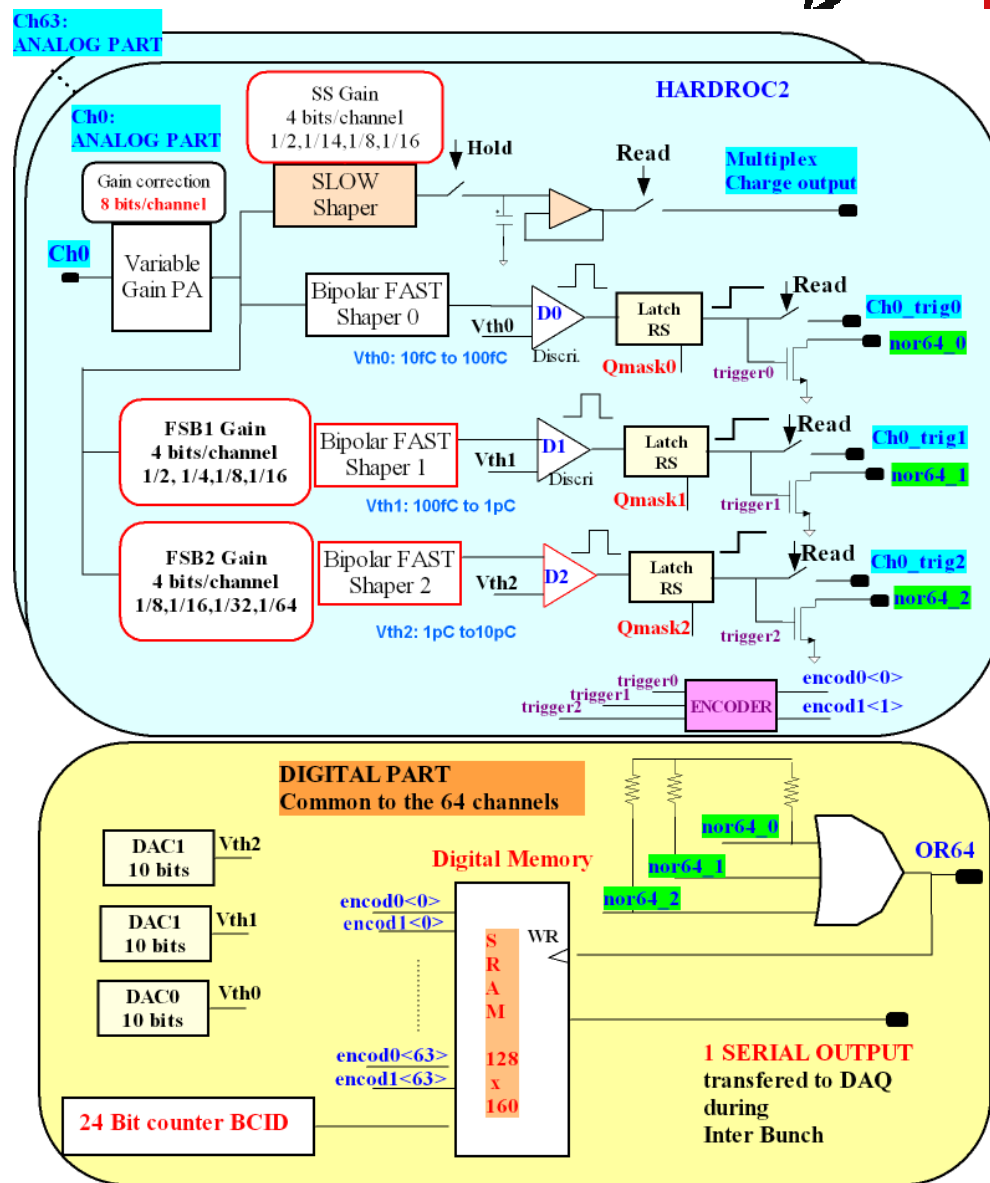


GRPC

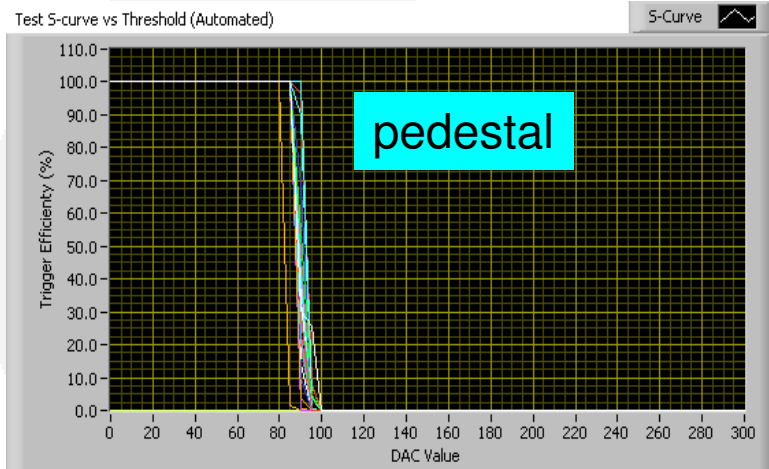
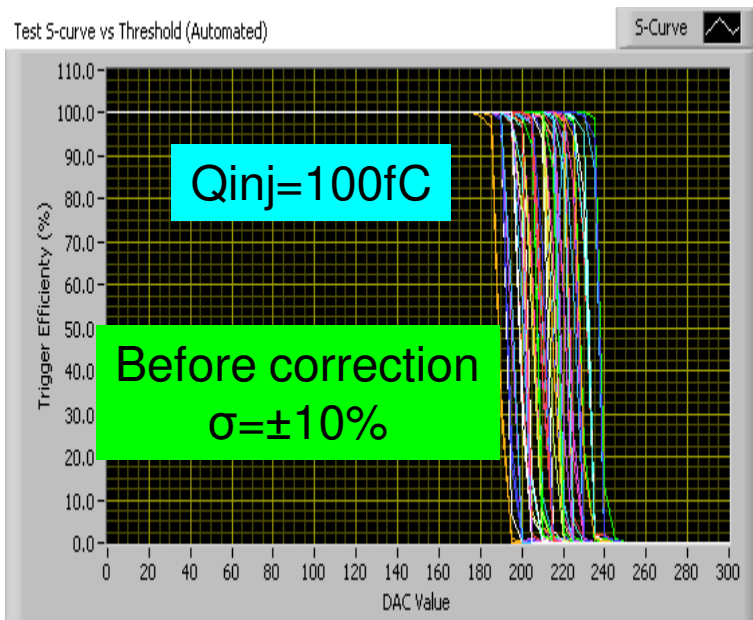
1m<sup>2</sup> scalable detector equipped and tested with cosmics and in testbeam in summer and autumn 2009. 144 chips/m<sup>2</sup>

About 6000 chips necessary to equip 40 plans of 1 m<sup>3</sup>

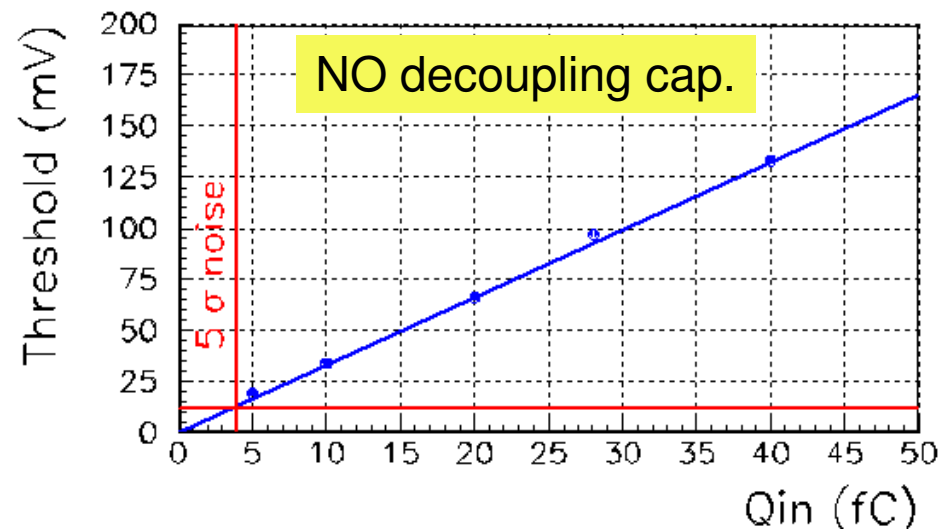
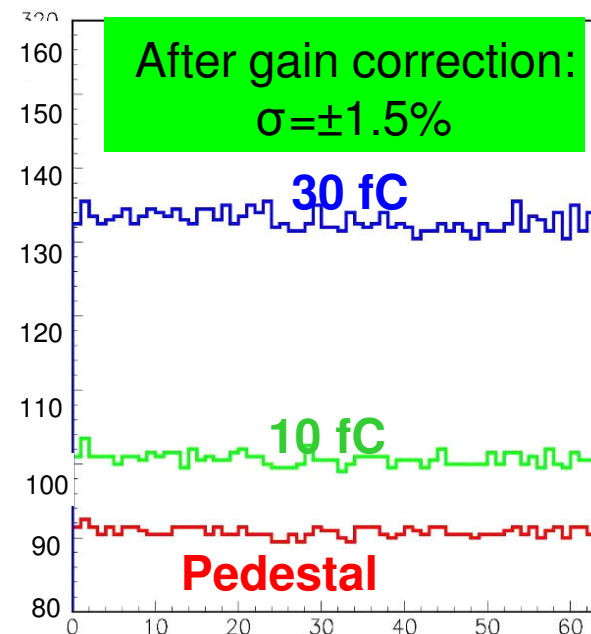
- 240 chips HARDROC1 produced in june 2007 to equip 4-chip and 24-chip RPC and Micromegas detectors
  - Package PQFP240
  - Not completely power-pulsed
- 400 chips HARDROC2 produced in june 2008 to equip 24-chip RPC and Micromegas PCBs for square meter
  - 3 thresholds (0.1-1-10 pC)
  - Power pulsed to 5-8  $\mu\text{W}/\text{ch}$
  - Package TQFP160
  - **Difficult SC loading: SOLVED in HARDROC2B**
- 200 HARDROC2b (medical application) in plastic package received beginning of jan 2010



# Trigger efficiency measurements (HR2)

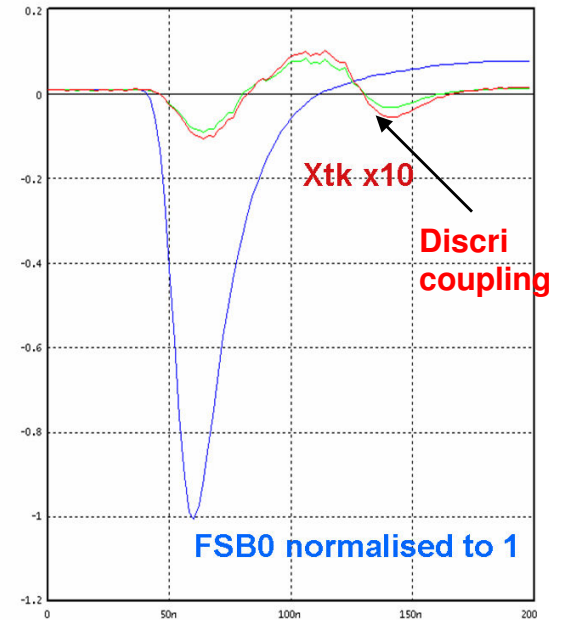
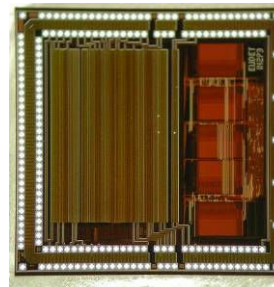


FSB0, 100K, 100fF, G=144

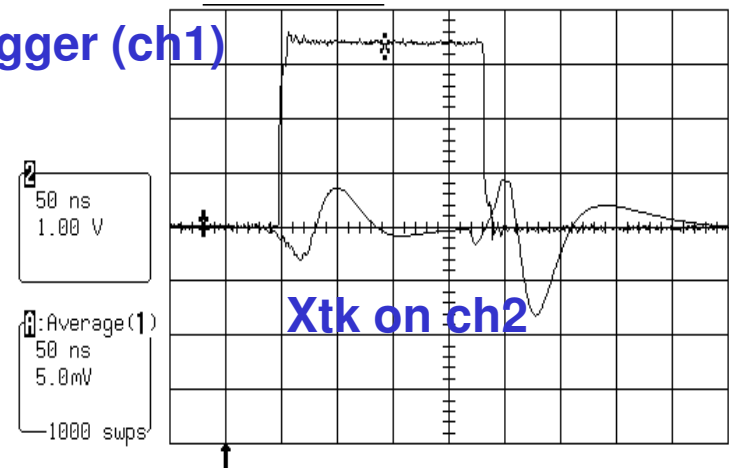


## Analog and Digital crosstalk (HR2)

- No decoupling capacitors (on bias and reference voltages)
- Crosstalk  $\sim 1\%$ 
  - Well differentiated, capacitive like
  - Dominated by the input
  - No long distance crosstalk
- Coupling of discriminator to inputs through ground or substrate
  - Trigger on CH1 and look at analog signal on CH2
  - 8 mV coupling = 3 fC
- Can limit the minimum threshold (not in this case as similar to noise)
- Needs careful chip layout

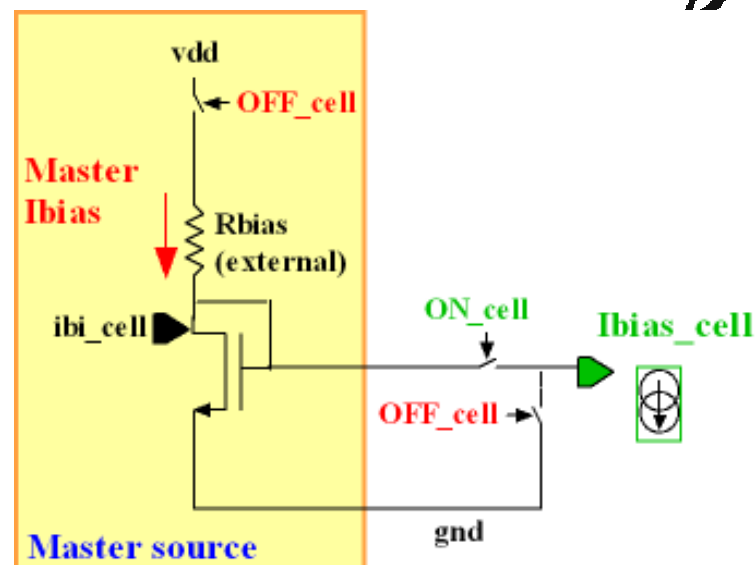


Trigger (ch1)



# POWER CONSUMPTION

HR2	ON
Vdd_pa	5.5mA
Vdd_fsbx3	12.3 mA
Vdd_d0,1,2	7.3 mA
Vddd	0.67 mA
vddd2	0.4mA (=0 if 40MHz OFF)
Vdd_dac	0.84 mA
Vdd_bandgap	1.2 mA
<b>Total (noPP)</b>	<b>29 mA</b>
<b>Total with 0.5% PP</b>	<b>145 <math>\mu</math>A</b>



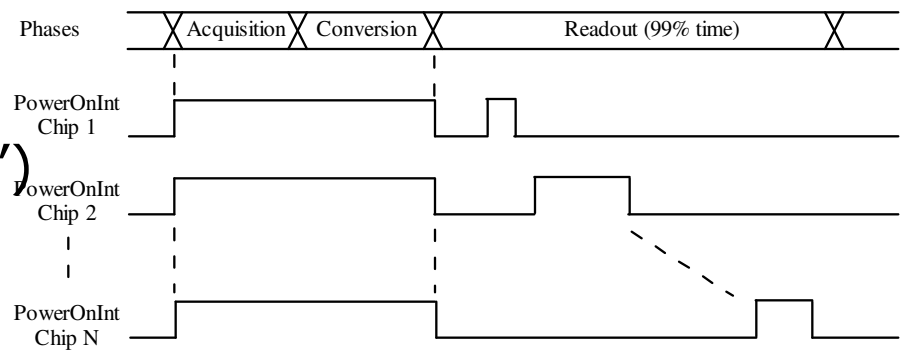
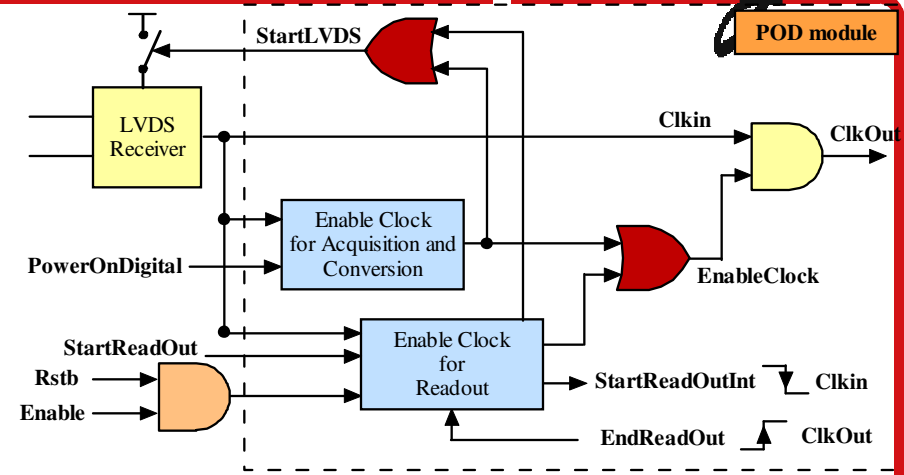
## HR2:

Pwr_on_a alone	14.9mA
Pwr_on_dac	1.025mA
Pwr_on_d	0.93mA
ALL ON (default config)	17 mA
<b>ALL OFF</b>	<b>&lt;4<math>\mu</math>A</b>

- **OFF** = Ibias \_cell switched off during interbunch
- **HR1**: a few forgotten switches (Bandgap, some reference voltages not power pulsed)
- **HR2**: switches added:
  - **ALL OFF** => 0
  - **5.5  $\mu$ W/ch with 0.5% duty cycle**

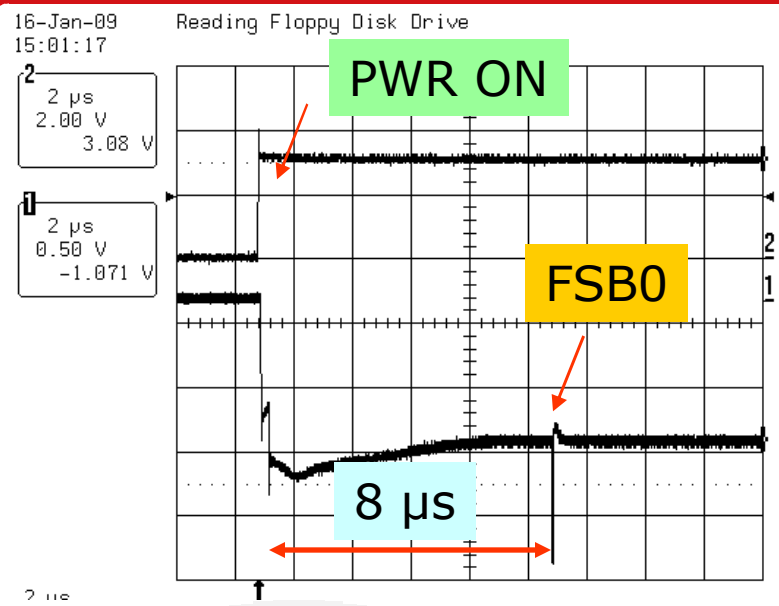
# Power On Digital:

- PowerON start/stop clocks and LVDS receiver bias current to meet power budget.
- LVDS receivers for RazChn/NoTrig and ValEvt ON during PowerOnAnalog (during bunch crossing)
- Clock is started asynchronously, enabled and stopped synchronously (at '0')
- 2 operation modes :
  - Acquisition, Conversion → common to all managed by DAQ
  - Readout → daisy chained managed by StartReadOut and EndReadOut



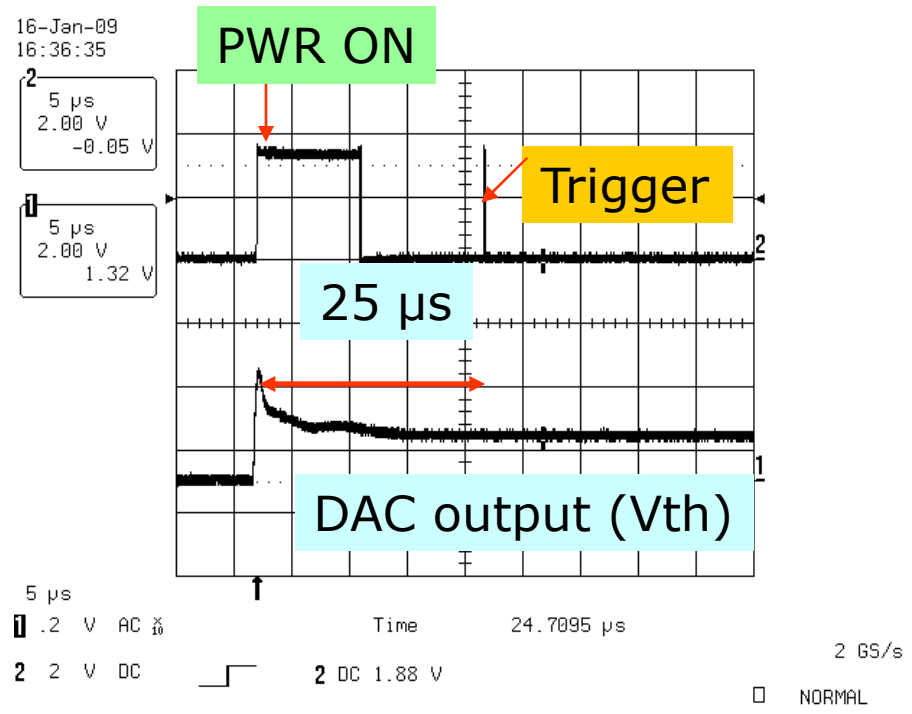
• **POD successfully tested on testbench**

# Power pulsing: « Awake » time



- All decoupling capacitors removed
- PWR ON: ILC like (1ms,199ms)
- PP of the analog part:
  - Input signal synchronised on PWR ON
  - => Awake time= 8 μs

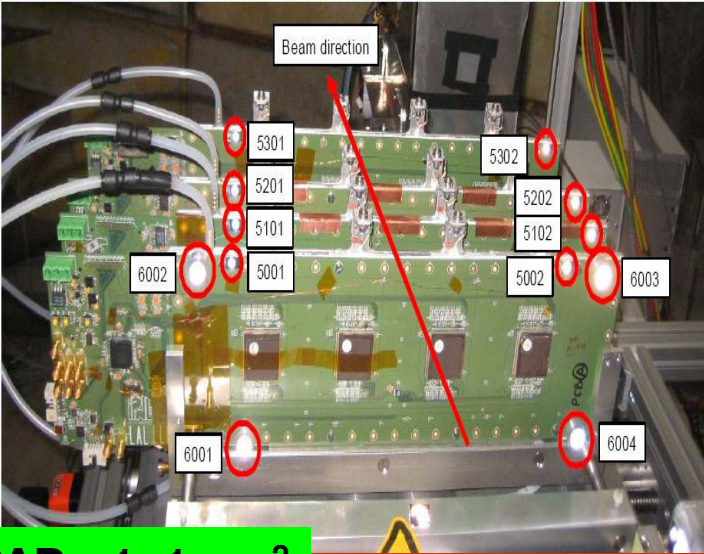
- Power pulsing of the DAC:
  - 25 μs (slew rate limited)





# PCB board associated to both RPC and $\mu$ Megas detectors

*Omega*

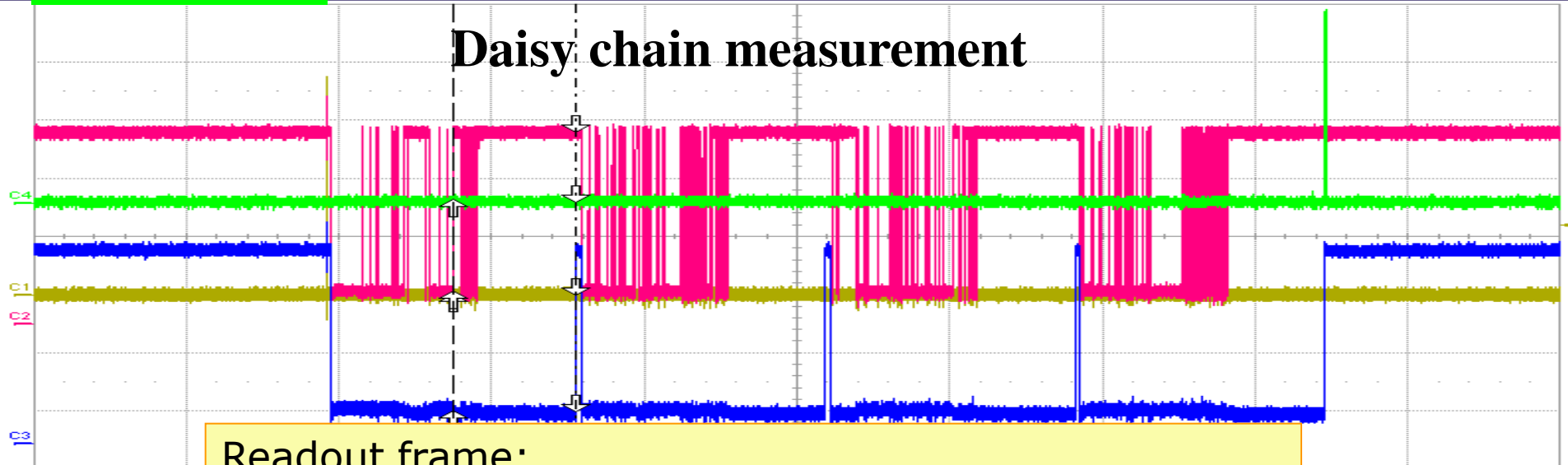


Semi-digital electronics readout system validated in beam conditions (daisy chain, stability, efficiency, no external component)

PADs 1x1 cm<sup>2</sup>

## Daisy chain measurement

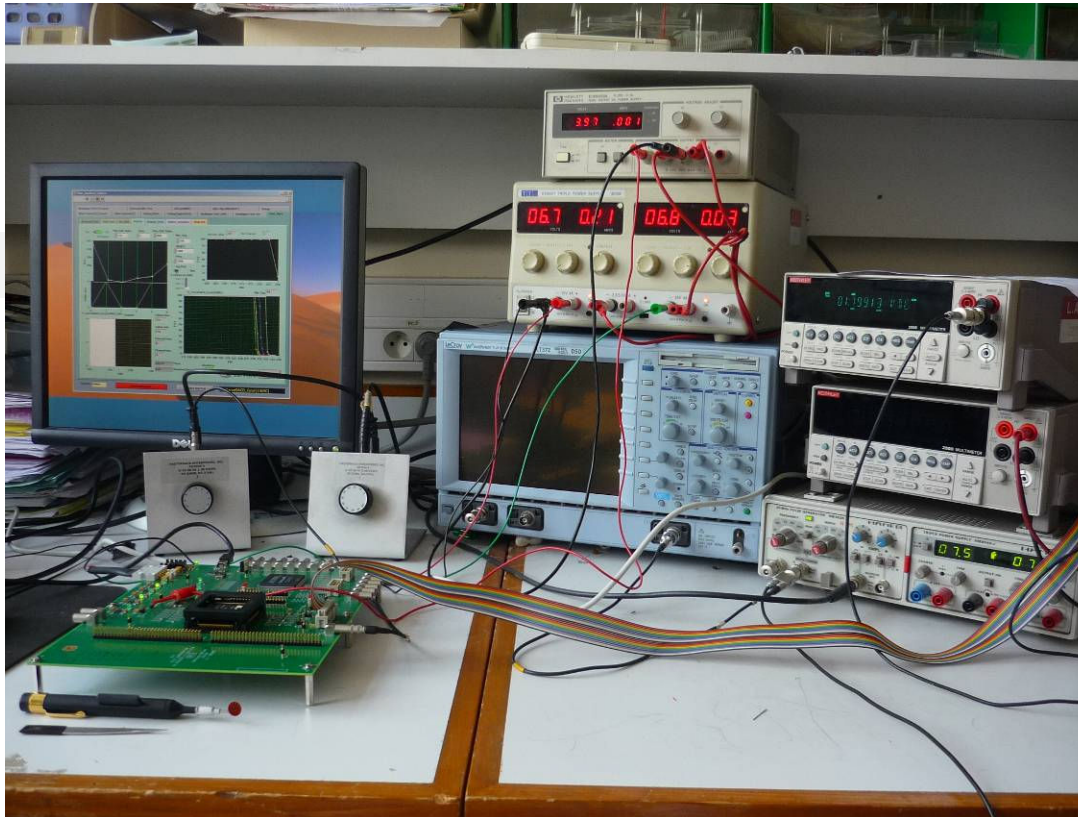
Readout frame:  
Header (8bits), then BCID (24bits),  
then 128 bits for trig0<0-63> and trig1<0-63>



LeCroy

616  $\mu$ s Déclenchement C1 DC  
1.00 V/div Normal 1.19 V  
-1.010 V ofst Front Positive  
12 mV  
-7 mV  
-7 mV  
 $\Delta X = -160.00 \mu$ s  
1/ $\Delta X = -6.2500$  kHz  
Waiting for Trigger

- 400 HR2 to equip 1m2 RPC and  $\mu$ egas detectors
- $\approx$ 300 chips tested this summer in ORSAY and in Lyon
- Good exercise before tests of productions (5000 chips)





Analogue Test : S-curve    External ADC Test    info pcb0807    info chip HARDROC2    Setup

Slow Control (1), Read    Slow Control (2)    Debug FPGA    Debug Digital ASIC    Analogue Test : DAC    Analogue Test : DC    Test\_Auto

Protocol Test    First Test    Lin\_DAC    **Scurve**    Resum\_Test    Relect\_measure    **ANALYSE**

Name Chip: **Hardr62**    Path TestAuto: C:\Documents and Settings\seguin\Bureau\Hardroc2\_final\mesures\    Name Stat: Stat\_h2.xls

**DAC Mesures**

Conso before load SC

Conso after load SC

V\_BG

DC\_FSB

DC\_SS

DAC0

DAC1

DAC2

Memory

**Scurve**

Freq: 100k    Nbr\_Trig 2: 100

G\_ref: 144    Géné\_Auto:     Burst:

Ped\_FSB0:  Start\_Dac: 85    FSB0:  Start\_Dac: 175    Qinj[C]: 100f    FSB0\_Gcor:

Ped\_FSB1:  Start\_Dac: 85    FSB1:  Start\_Dac: 330    Qinj[C]: 1p    FSB1\_Gcor:

Ped\_FSB2:  Start\_Dac: 85    FSB2:  Start\_Dac: 210    Qinj[C]: 1p    FSB2\_Gcor:

Test\_SlowControl:     Nbr\_test: 10

Val\_Gain: 170    Rate[ms]: 500

Name Slow Control: SlowControl .xls

Conso before load SC[mA]: 17,2

Conso after load SC[mA]: 34,7

V\_BG[V]: 2,39

DC\_FSB[V]: 0,34

DC\_SS[V]: 1,52

DAC: MAX[V]: 2,33    MIN[V]: 1,27    Slope: -2,09m

Cut\_Lin\_DAC

**CUT**

+/-[%]: 20

	MAX	MIN	MEAN	DEV
Ped_FSB0	98	86	93	1,5
Ped_FSB1	88	81	85	1,5
Ped_FSB2	95	86	92	1,5
FSB0	220	180	200	9
FSB0_Gcor	220	180	200	4
FSB1	430	330	370	17
FSB2	280	210	240	13
FSB1_Gcor	0	0	0	0
FSB2_Gcor	0	0	0	0

Cut\_S-Curve

VALID ALL

REMOVE ALL

**START TEST**

Nbr\_Test: 1    Nbr\_Test\_i: 8

- DC levels, power consumption, VBG, memory test, SC test with a « difficult config »

Protocol Test | First Test | Lin\_DAC | Scurve | Resum\_Test | Relect\_measure | ANALYSE

Conso before[mA] VALID ● DC\_FSB[V] 2 VALID ● v\_BG[V] 2 VALID ●

Conso before load SC 17,84537 DC\_FSB 3,23878

Conso after[mA] VALID ● DC\_SS[V] 2 VALID ● v\_BG 2,47070

Conso after load SC 30,28721 DC\_SS 3,23221

Test Slow Control Succed[%] 0 NumTest 10 VALID ●

Trig	CONFIG SLOW CONTROL	RESULT MEMORY
	DAC0:300,DAC1:1023,DAC2:1023 SS Gain:15,FSB1 Gain:8,FSB2 Gain:8 Trigger_write0:On,Trigger_write1:Off,Trigger_write2:Off All Channel Cap. Enabled All Channel Discriminator Active	Trig0:0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15,16,17,18,19,20,21,22,23,24,25,26,27,28,29,30,31,32,33,34,35,36,37,38,39,40,41,42,43,44,45,46,47,48,49,50,51,52,53,54,55,56,57,58,59,60,61,62,63 Trig1:Trig2:
	DAC0:1023,DAC1:200,DAC2:1023 SS Gain:15,FSB1 Gain:8,FSB2 Gain:8 Trigger_write0:Off,Trigger_write1:On,Trigger_write2:Off All Channel Cap. Enabled All Channel Discriminator Active	Trig0:Trig1:0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15,16,17,18,19,20,21,22,23,24,25,26,27,28,29,30,31,32,33,34,35,36,37,38,39,40,41,42,43,44,45,46,47,48,49,50,51,52,53,54,55,56,57,58,59,60,61,62,63 Trig2:
	DAC0:1023,DAC1:1023,DAC2:200 SS Gain:15,FSB1 Gain:8,FSB2 Gain:8 Trigger_write0:Off,Trigger_write1:Off,Trigger_write2:On All Channel Cap. Enabled All Channel Discriminator Active	Trig0:Trig1:Trig2:0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15,16,17,18,19,20,21,22,23,24,25,26,27,28,29,30,31,32,33,34,35,36,37,38,39,40,41,42,43,44,45,46,47,48,49,50,51,52,53,54,55,56,57,58,59,60,61,62,63

Test memory ● VALID

# 3 DACs linearity



Protocol Test | First Test | **Lin\_DAC** | Scurve | Resum\_Test | Relect\_measure | ANALYSE

Ampli: 1,26422

DetaMax[mV]: 545

Deta\_l[mV]: 532,7

Test DAC0

Test DAC1

Test DAC2

STOP

Maximum Value: 2,3141

Minimum Value: 1,26422

Standard Deviation: 338,572m

INL (LSB): 3,32623

DNL (LSB): 259,549

Fit Slope: -2,05245m

Fit Intercept: 2,31905

Fit Mean Square Error: 13,75u

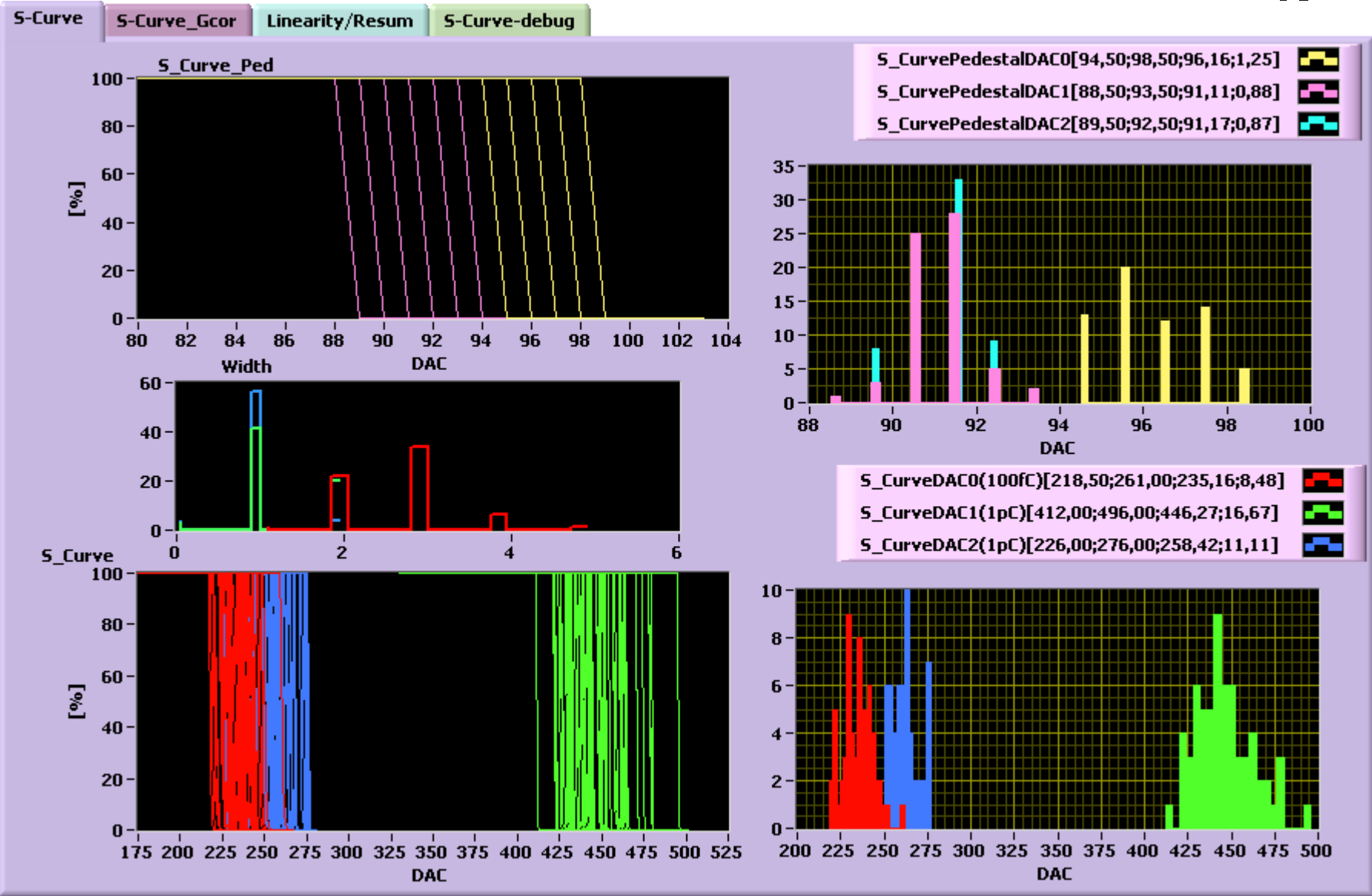
Test DAC Value: 512

LinDac2

DAC	Amplitude
1	2.31
50	2.18
100	2.05
150	1.92
200	1.79
250	1.66
300	1.53
350	1.40
400	1.27
450	1.14
512	1.26

LinDac2\_Resid

DAC	Amplitude (Residual)
1	-2.8m
50	5.8m
100	6.8m
150	6.8m
200	4.8m
250	3.8m
300	2.8m
350	1.8m
400	0.8m
450	-0.2m
512	-4.2m



# FSB0 Gain Correction



Analogue Test : S-curve    External ADC Test    info pcb0807    info chip HARDROC2    Setup

Slow Control (1), Read    Slow Control (2)    Debug FPGA    Debug Digital ASIC    Analogue Test : DAC    Analogue Test : DC    Test\_Auto

Protocol Test    First Test    Lin\_DAC    Scurve    Resum\_Test    Relect\_measure    **ANALYSE**

S-Curve    S-Curve\_Gcor    **Linearity/Resum**    S-Curve-debug

NameChip **Hardr194\_01**    [MAX;MIN;MEAN;DEV]

**S\_Curve\_Ped 2**

**S\_CurvePedestalDAC0[94,50;98,50;96,16;1,25]**

Gcor	138	138	144	148	152	159	146	137
	140	138	151	151	160	151	130	156
	139	151	136	144	142	159	161	144
	138	155	157	147	148	146	143	148
	150	159	147	140	141	138	142	137
	151	145	149	133	142	140	139	145
	153	138	140	138	133	132	134	135
	149	161	145	151	143	122	140	139

**S\_Curve 2**

**S\_CurveDAC0\_Gcor(100fc)[231,50;242,50;235,03;2,09]**

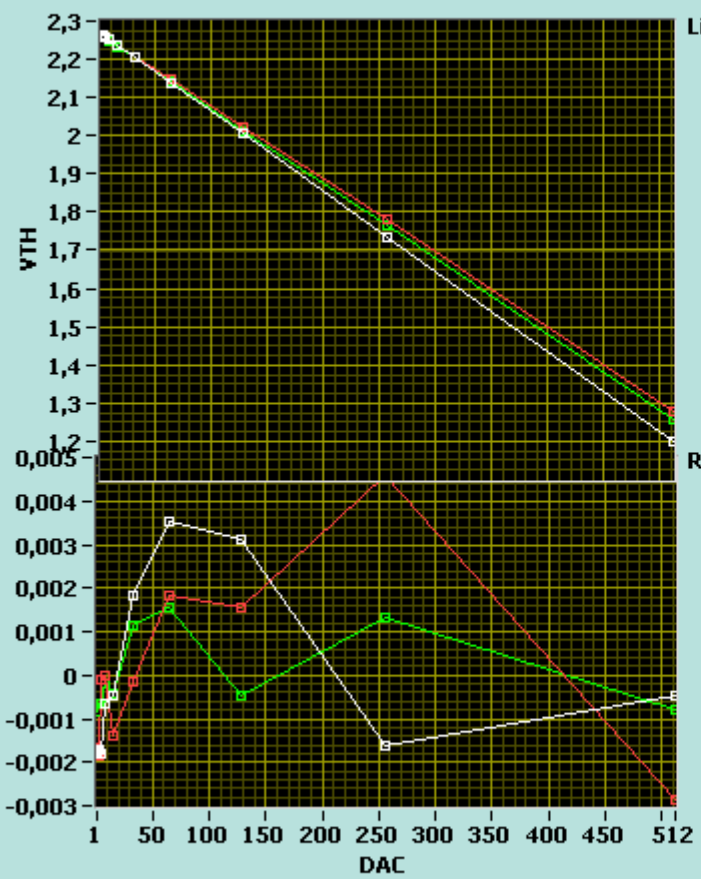
**S\_CurveDAC0(100fc)[218,50;261,00;235,16;8,48]**

START    Filtre Analyse  OFF

# Read back of the measurements



S-Curve   S-Curve\_Gcor   **Linearity/Resum**   S-Curve-debug



**Linearity**

LinDac0

LinDac1

LinDac2

**Residual**

Res\_LinDac0

Res\_LinDac1

Res\_LinDac2

## Resum

```

Hardr211
11/09/2009 08:54:56
-----
Name_SlowControlRef : SlowControl
-----
Conso before load SC
Delay=0:5:887

Value : 13,94 mA
..... Valid .....

-----
Conso after load SC
Delay=0:6:343

Value : 27,61 mA
..... Failed .....

-----
V_BG
Delay=0:3:886

Value : 2,42 V
..... Valid .....

-----
DC_F5B
Delay=0:3:880

Value : 3,24 V
..... Failed .....

-----
DC_55
Delay=0:3:743

Value : 3,23 V
..... Failed .....
    
```



Protocol Test | First Test | Lin\_DAC | Scurve | Resum\_Test | **Relect\_measure** | ANALYSE

List measure

- memory
- Lin\_DAC0\_MAX
- Lin\_DAC0\_MIN
- Lin\_DAC0\_Slope
- Lin\_DAC1\_MAX
- Lin\_DAC1\_MIN
- Lin\_DAC1\_Slope
- Lin\_DAC2\_MAX
- Lin\_DAC2\_MIN
- Lin\_DAC2\_Slope
- Ch\_SCped\_DAC0\_MAX
- SCped\_DAC0\_MAX
- Ch\_SCped\_DAC0\_MIN
- SCped\_DAC0\_MIN
- SCped\_DAC0\_Mean**
- SCped\_DAC0\_Dev

Name Chip 2

Analyse

Restart Analyse

Build | End of Analyse |  Analyse Build

CUT: measure[Min;Max] : Nbr

SCped\_DAC0\_Mean [70,5E+0;102,2E+0] :108

Mean: 92,4394  
Dev: 3,73415  
Max: 102,2  
Min: 84,64

IN ← CUT

UNDO | NEXT

**Ch\_SC\_DAC0\_MIN=f(SC\_DAC0\_MAX)**

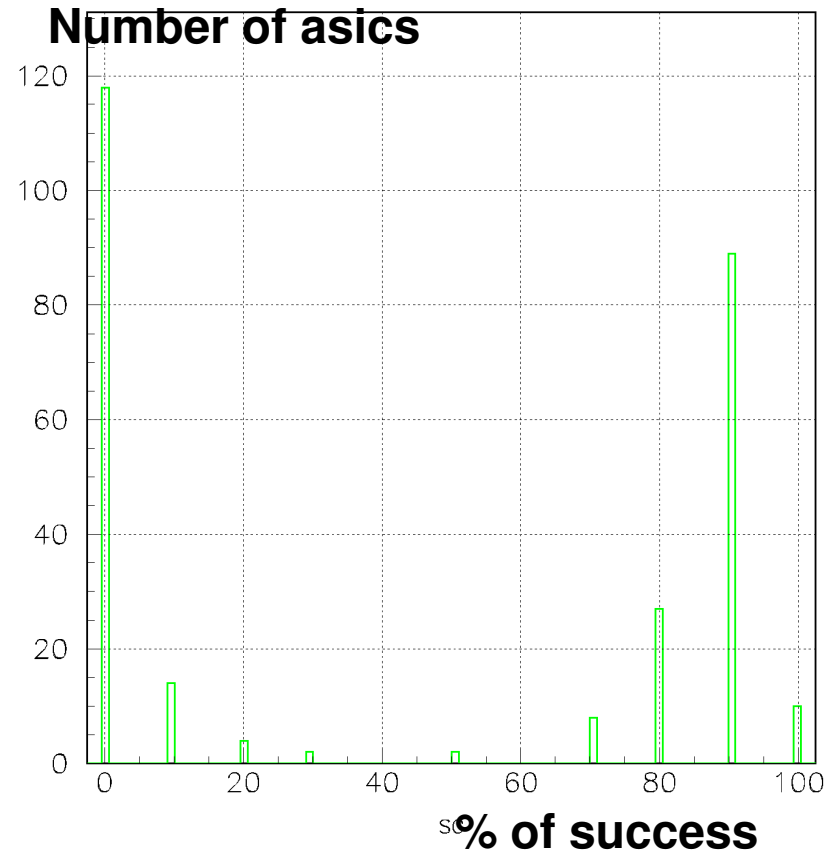
reverse | modify

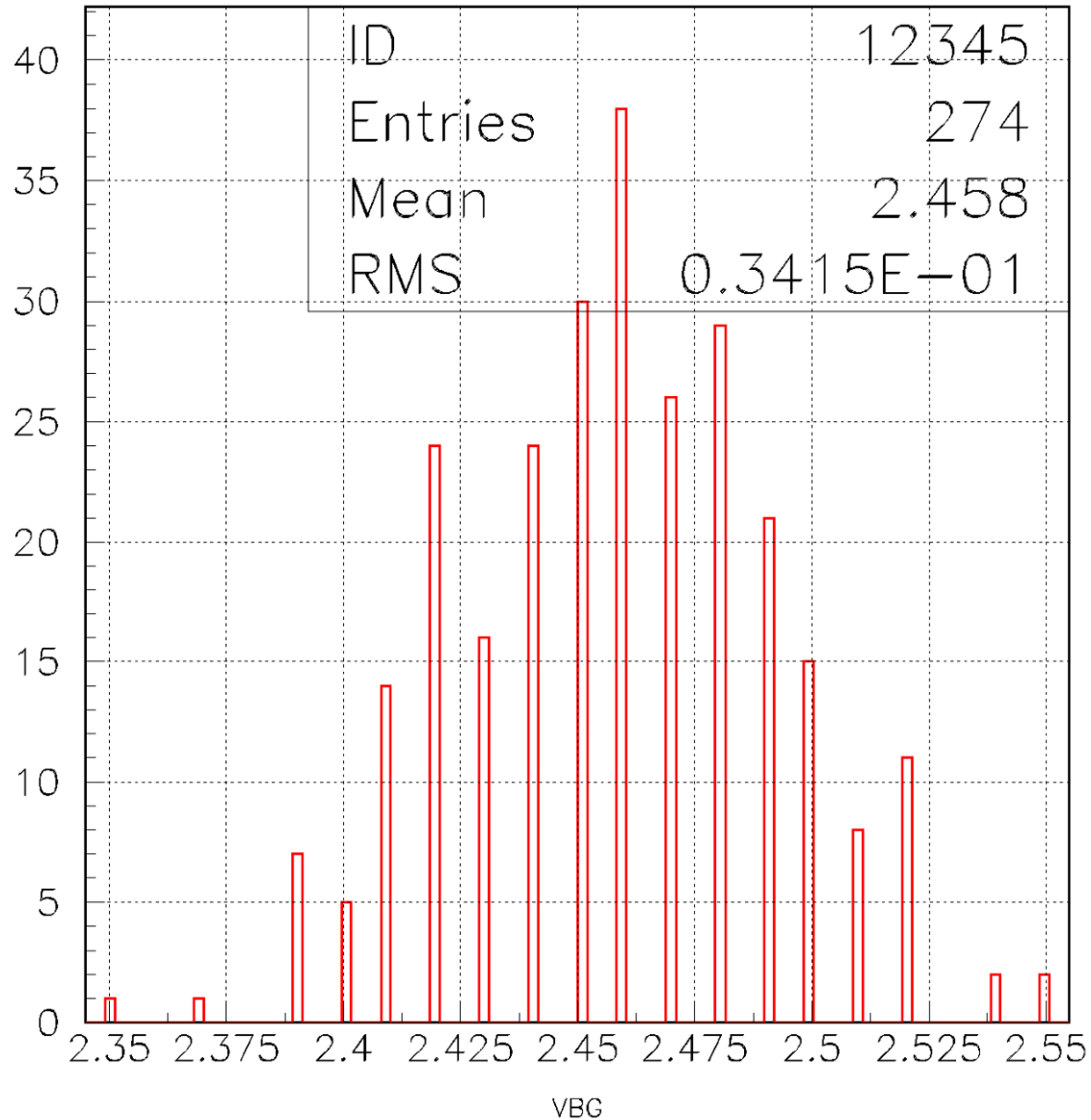
Correlation: OFF

High	-0,0311573	102,2
Low	19,515	84,64
Hardr317_01		
Cours 0	107	102,2

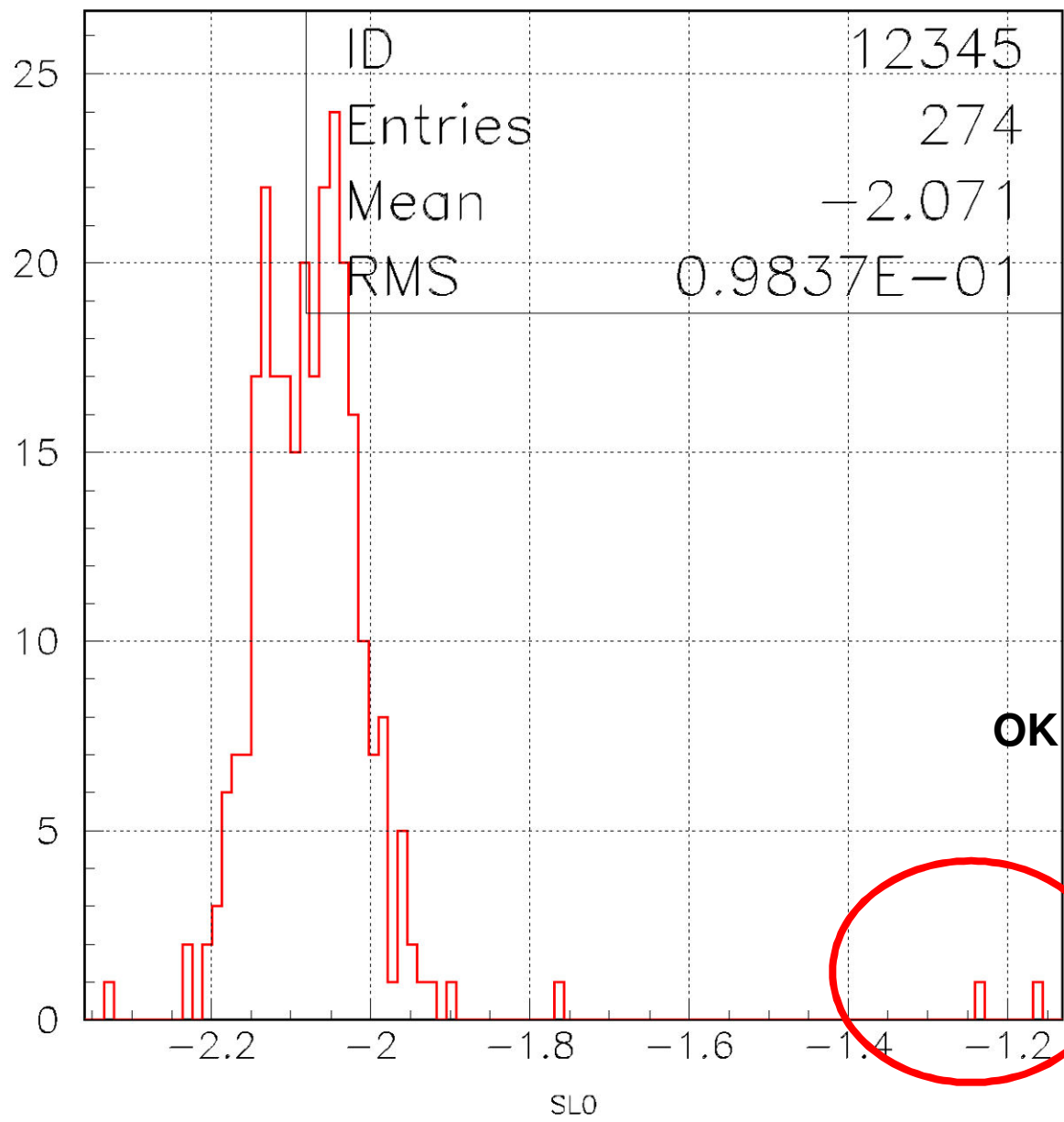
Nbr\_Chip: **108**

- Some gain configurations are sometimes difficult to load in hardroc2
  - Due to long connections between flip flops inside the chip: can be corrected with additional buffers on clk and data signals
  - **necessity to increase digital vdd to 4V.**
- But still,  $\approx 50\%$  of the chips exhibit pb with the loading of « difficult » SC config.
  - Gain=170 = 10101010 loaded 10 times, calculation of the ratio of success.
  - **Anyway 90% of the chips OK for the other tests performed with various SC configs have to be loaded**

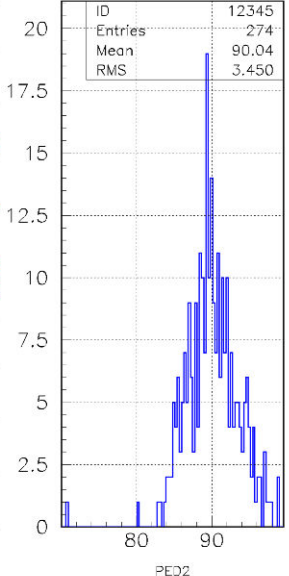
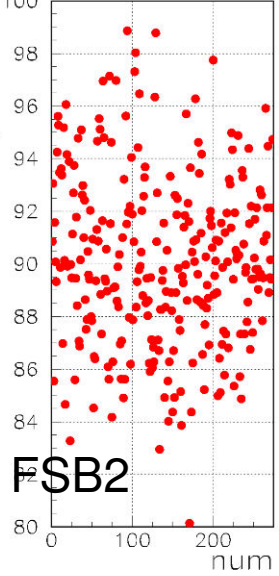
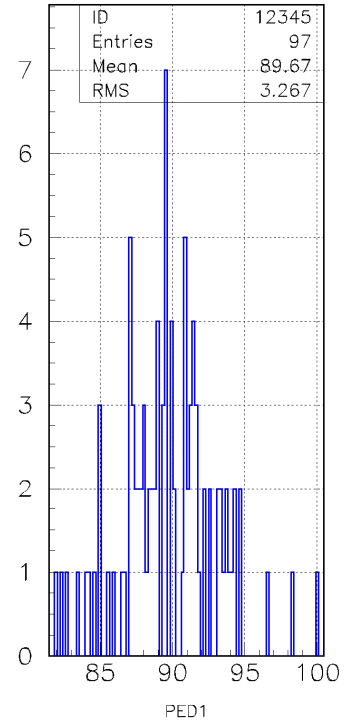
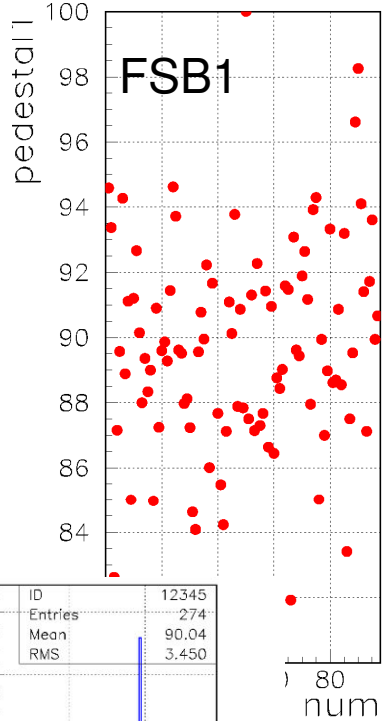
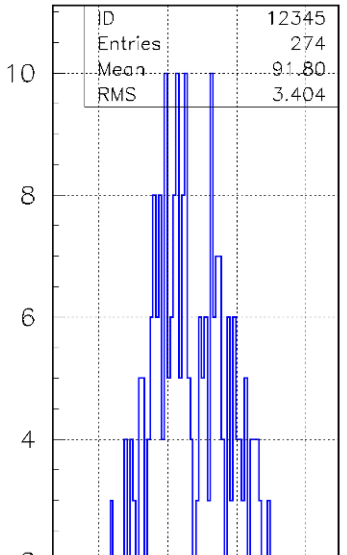
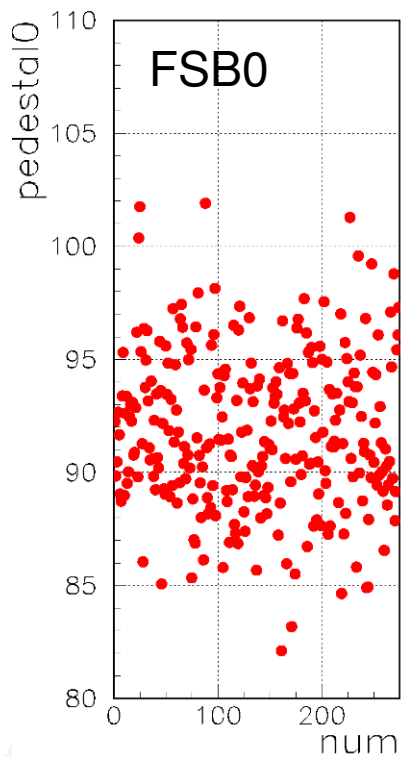




**Rms=34 mV**  
**Offset to be improved**

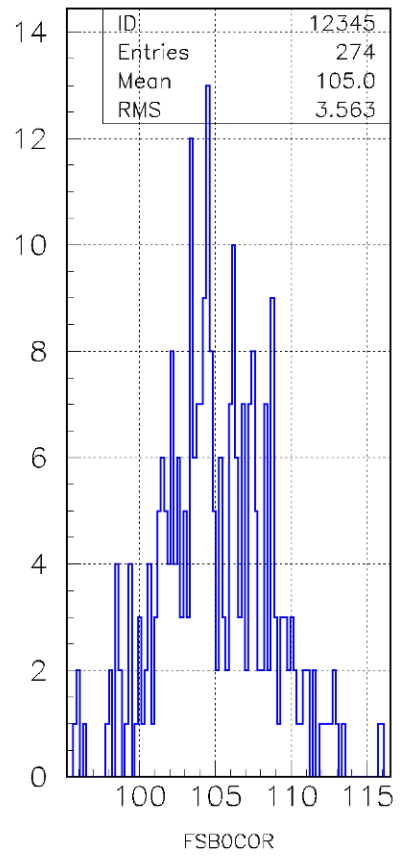
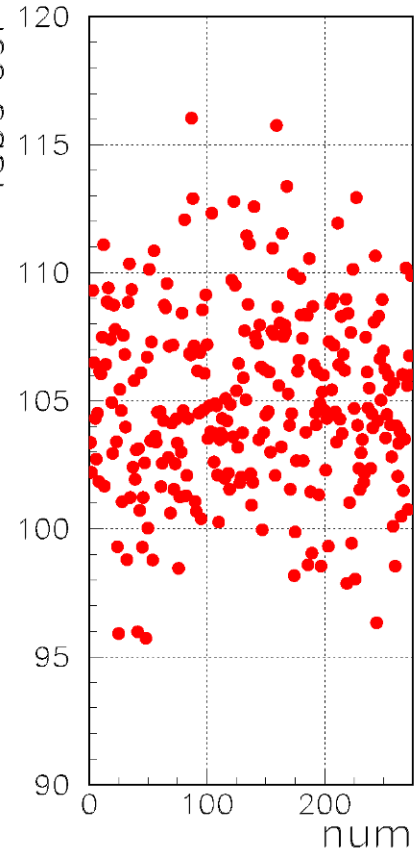
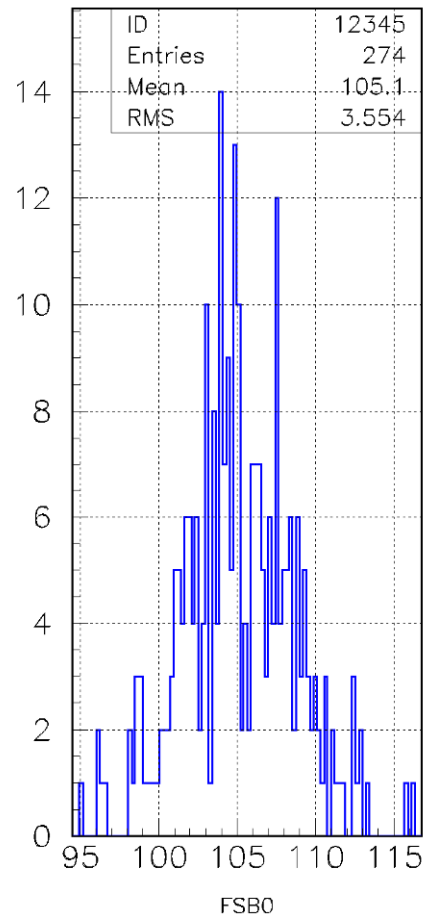
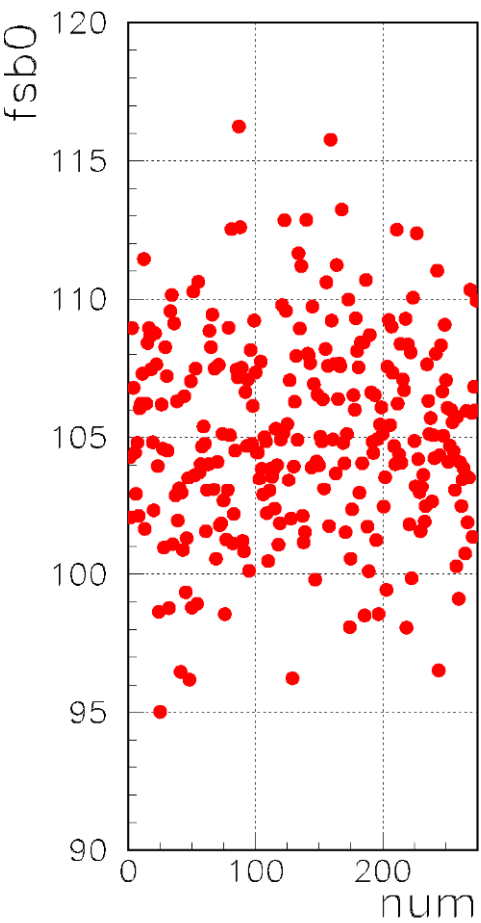


# FSB0,1,2 PEDESTALS dispersion between chips



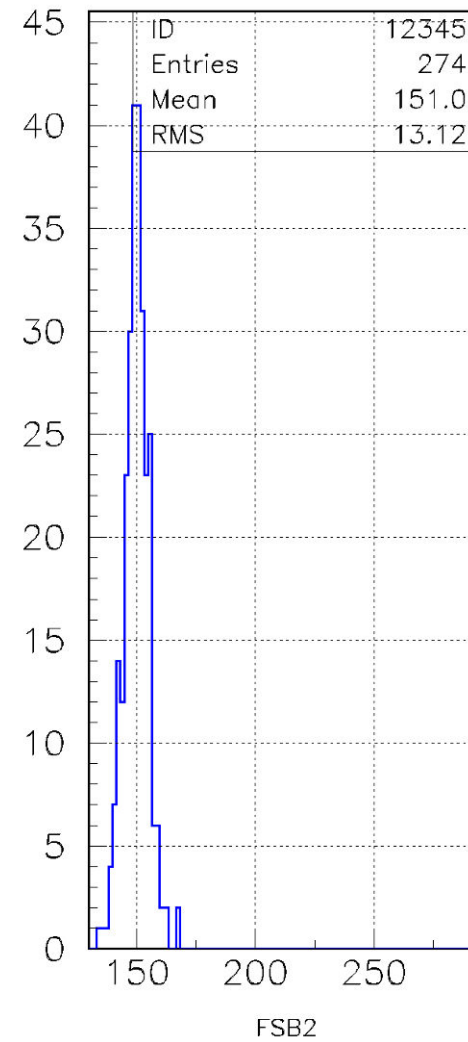
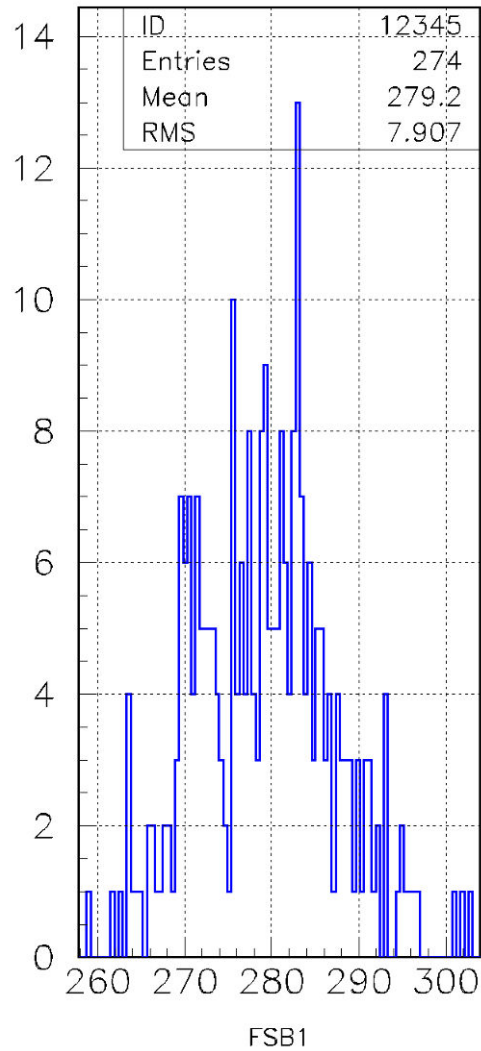
**Mean=90, rms=3**

# FSB0: before and after gain cor

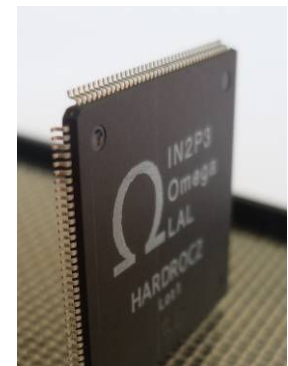
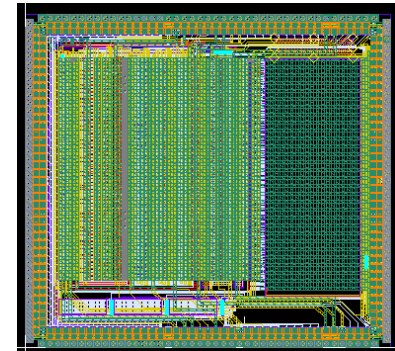
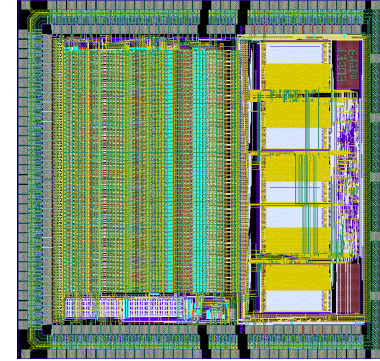


pedestal subtracted

# FSB1 and 2 (pedestal subtracted)



- 240 chips HARDROC1 produced in june 2007 to equip 4-chip and 24-chip RPC and Micromegas detectors
  - Package PQFP240
  - Not completely power-pulsed
- 400 chips HARDROC2 produced in june 2008 to equip 24-chip RPC and Micromegas PCBs for square meter
  - 3 thresholds (0.1-1-10 pC)
  - Power pulsed to 5-8  $\mu\text{W}/\text{ch}$
  - Package TQFP160
  - **Difficult SC loading: SOLVED in HARDROC2B**
- 200 HARDROC2b (medical application) in plastic package received beginning of jan 2010.



TQFP: t=1.4 mm

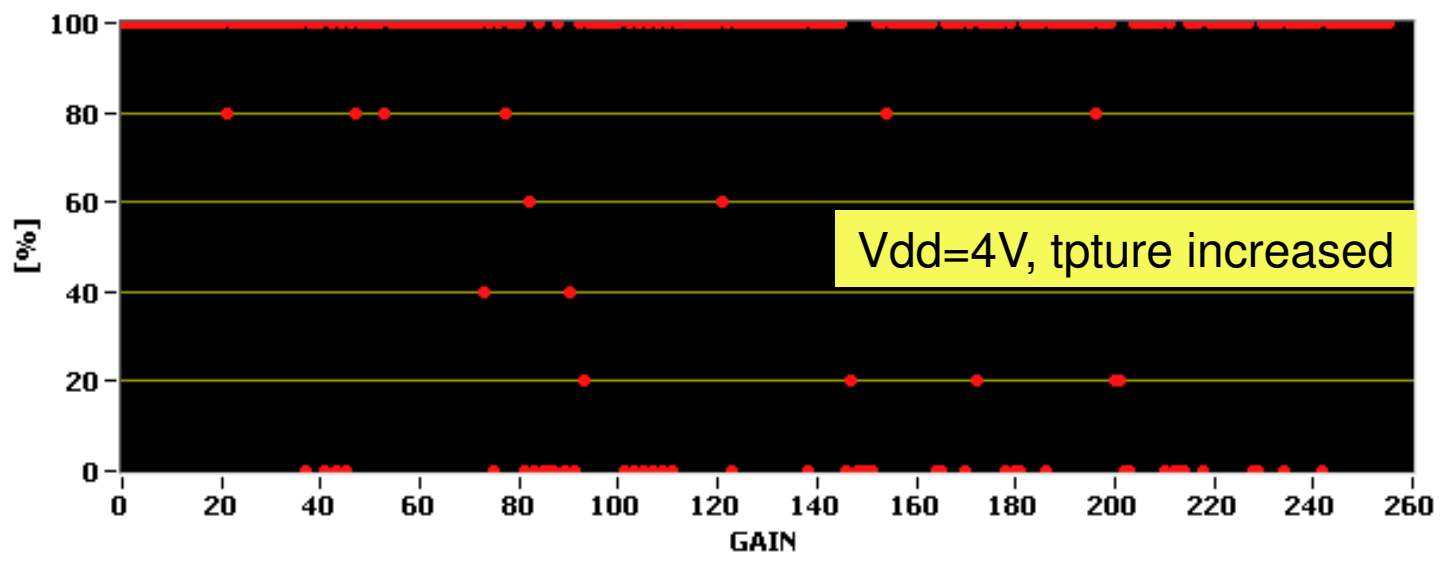
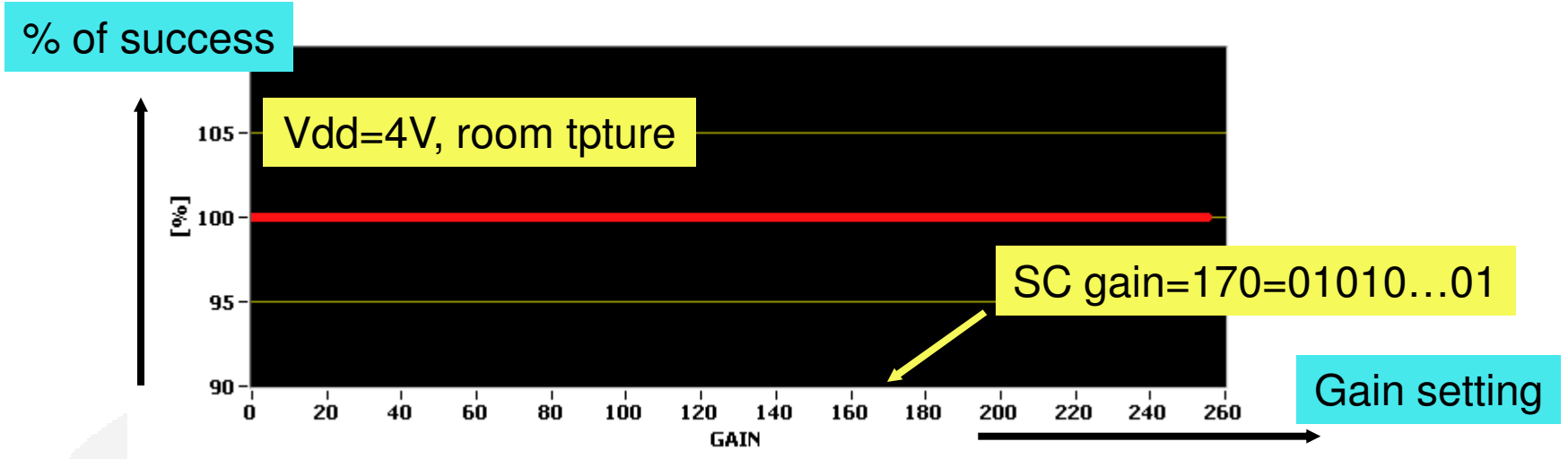


- Hardroc2b submitted mid June for a medical application, minor modifications
  - Pinout UNCHANGED
  - Bandgap: offset minimised
  - Read/SC selection bug corrected
  - **SC control register: buffers added on the Clk**
- 200 HR2b in plastic package received at the beginning of january 2010
- On going test in Lyon

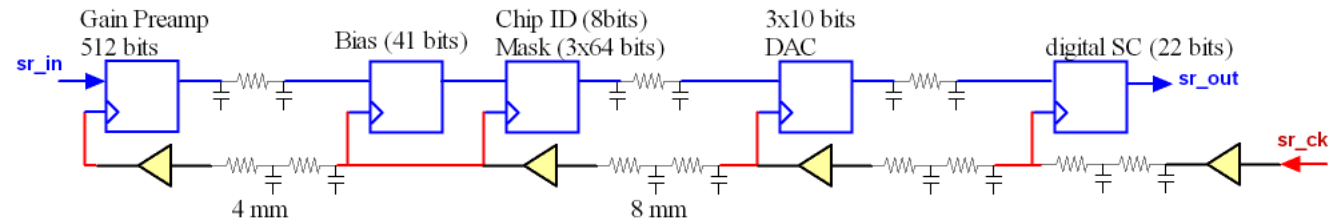
# SC pb with HARDROC2



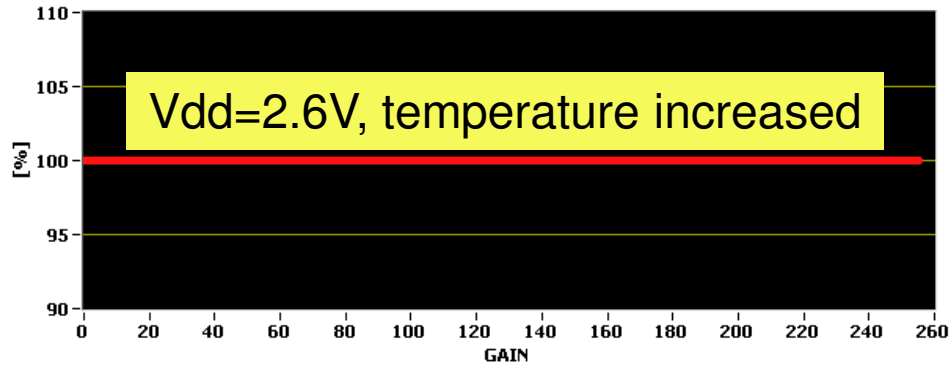
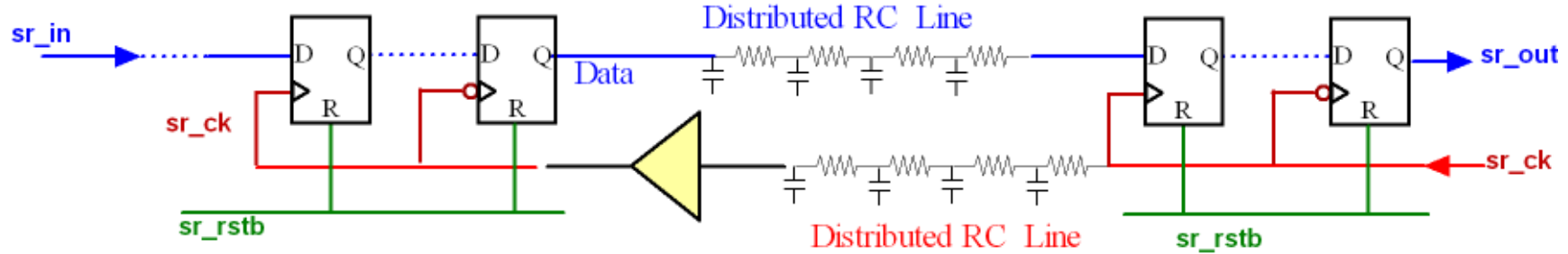
- Test of the SC: 64x8 Gain bits, Gain set from 0 to 255, SC config sent 10 times => Loading success



- Buffers added on the Clk only



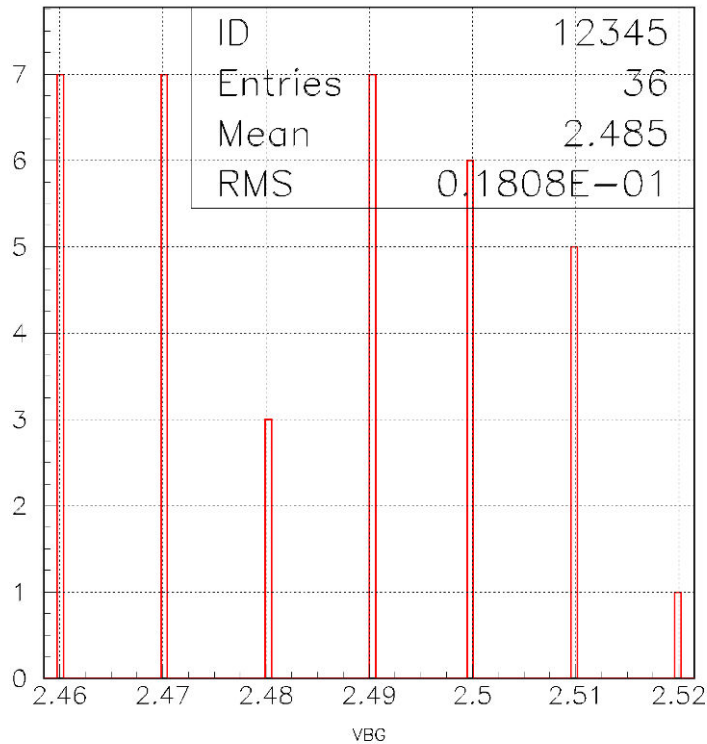
64 x 8 bits = 512 SC parameters for Gain correction



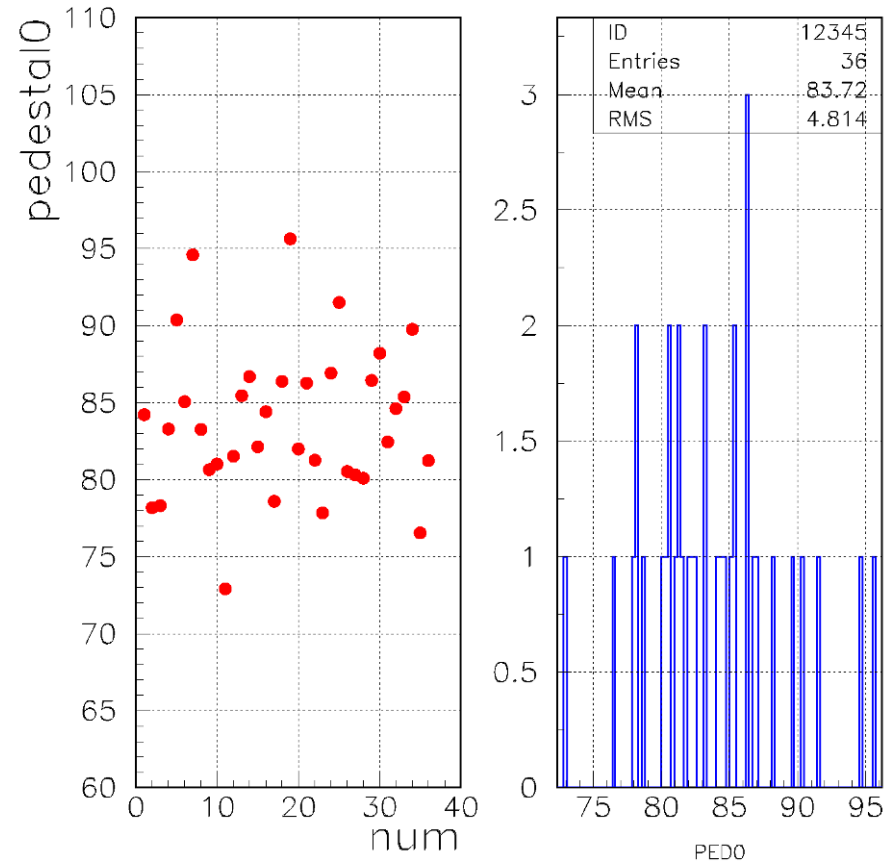
- 36 HR2b measured in Lyon: 100% success when sending the difficult SC config=10101...10, 100 times

# HR2b measurements (1):

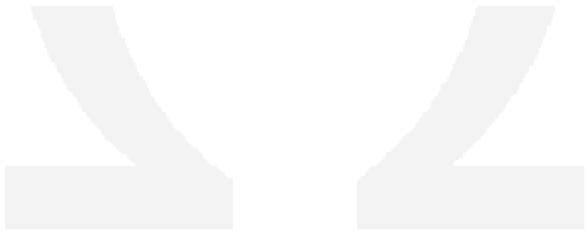
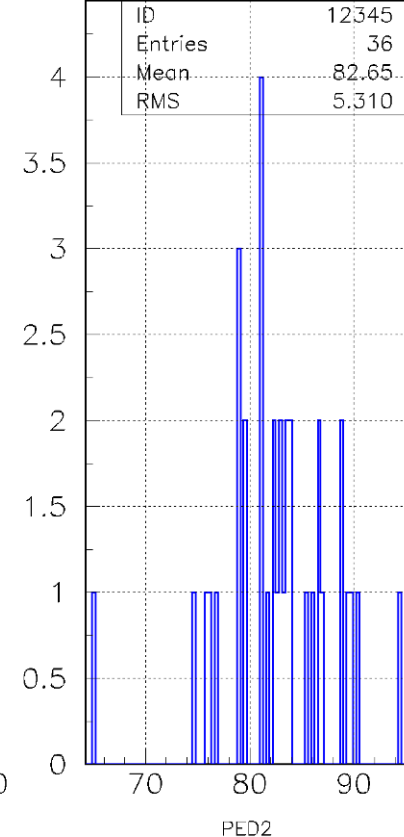
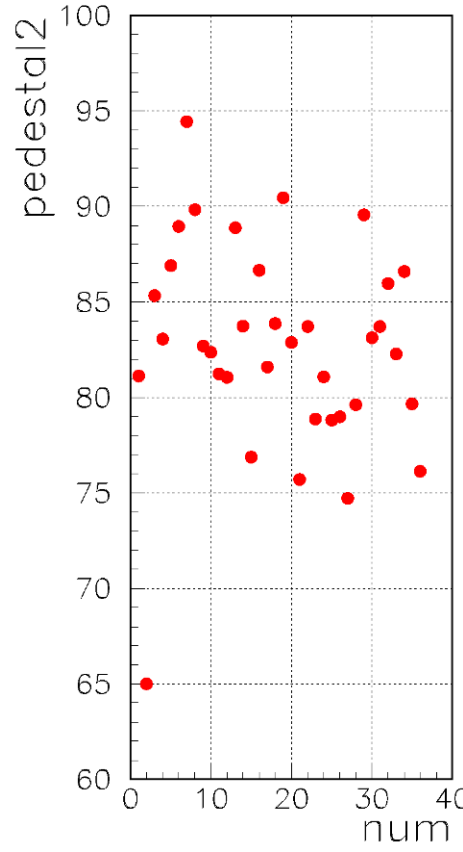
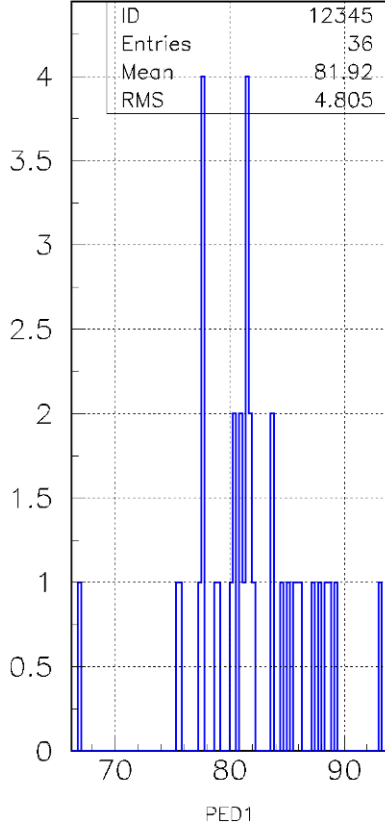
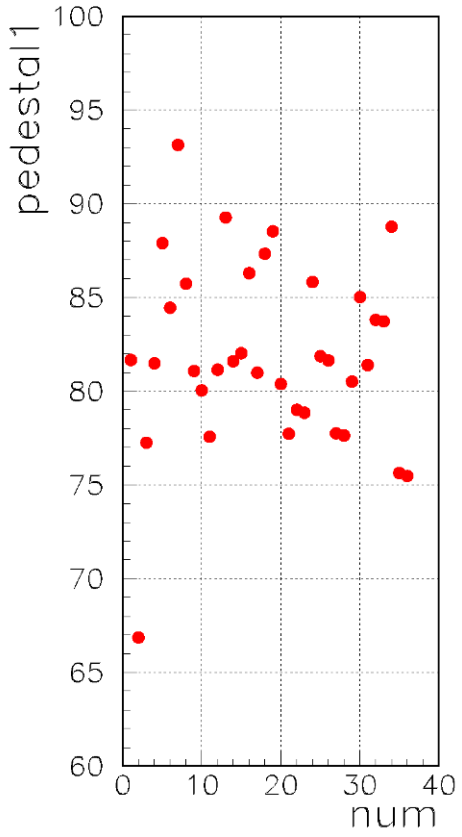
- Vbg measurement:  
rms=18mV instead of 34 mV  
in HR2



- Pedestal of FSB0

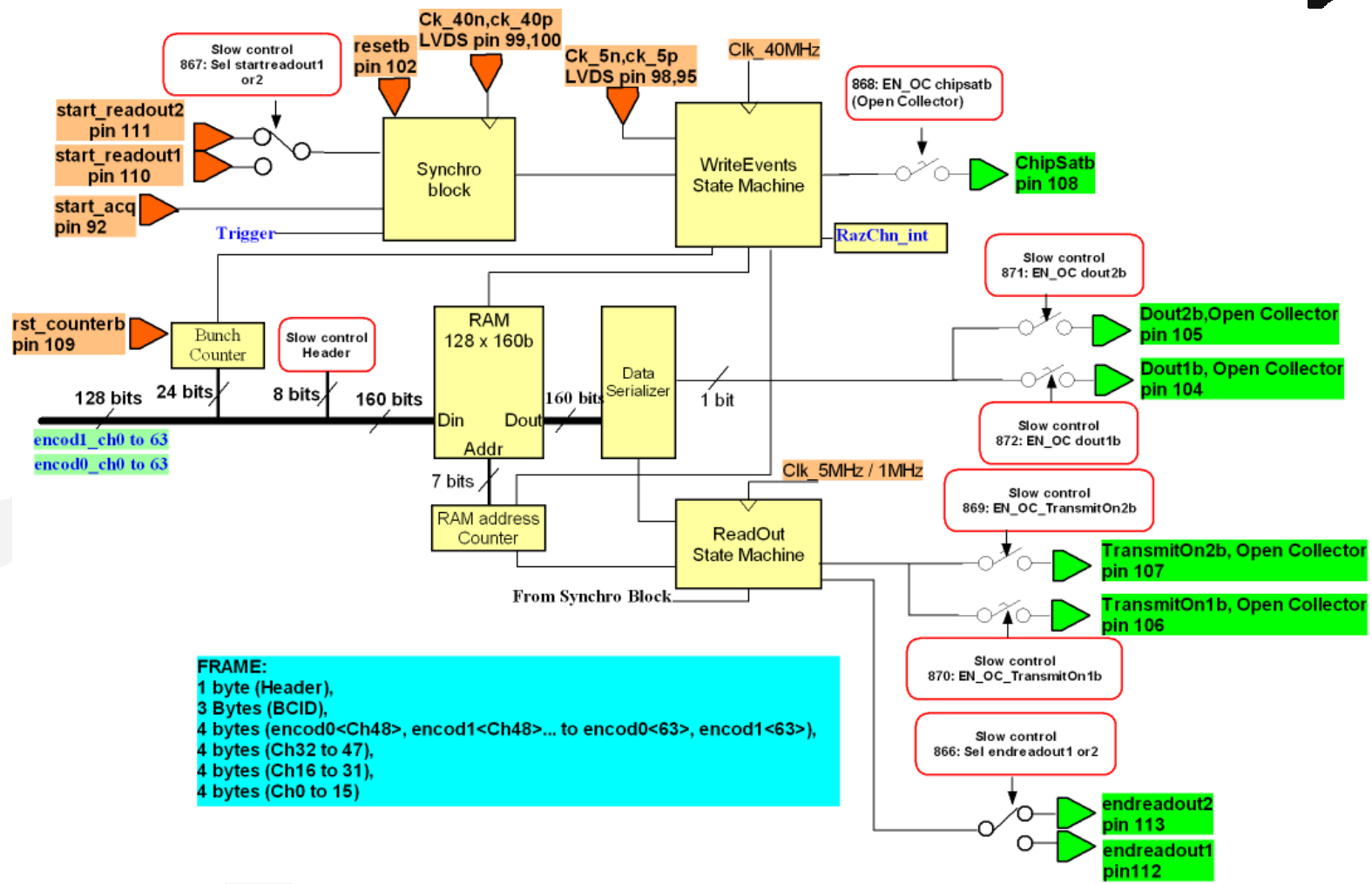


# HR2b measurements (2):



- Analog and digital performance of HR2 validated on test bench and testbeam
- SC pb solved in HARDROC2B
- On going test of the 200 HR2b: in Lyon
- => HARDROC for prod= HARDROC2B
- Test setup with a robot to test 10000 chips (IPN Lyon)

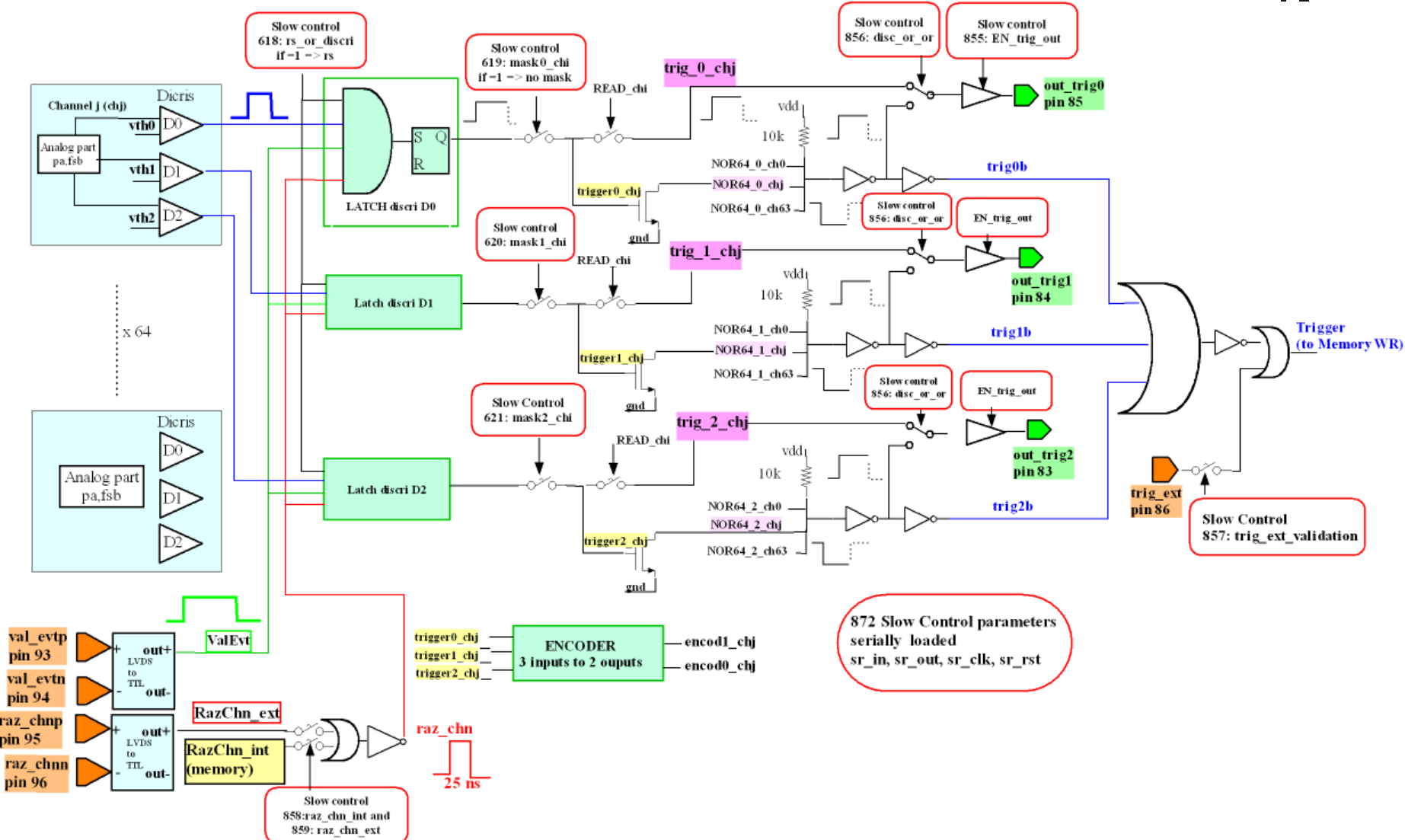




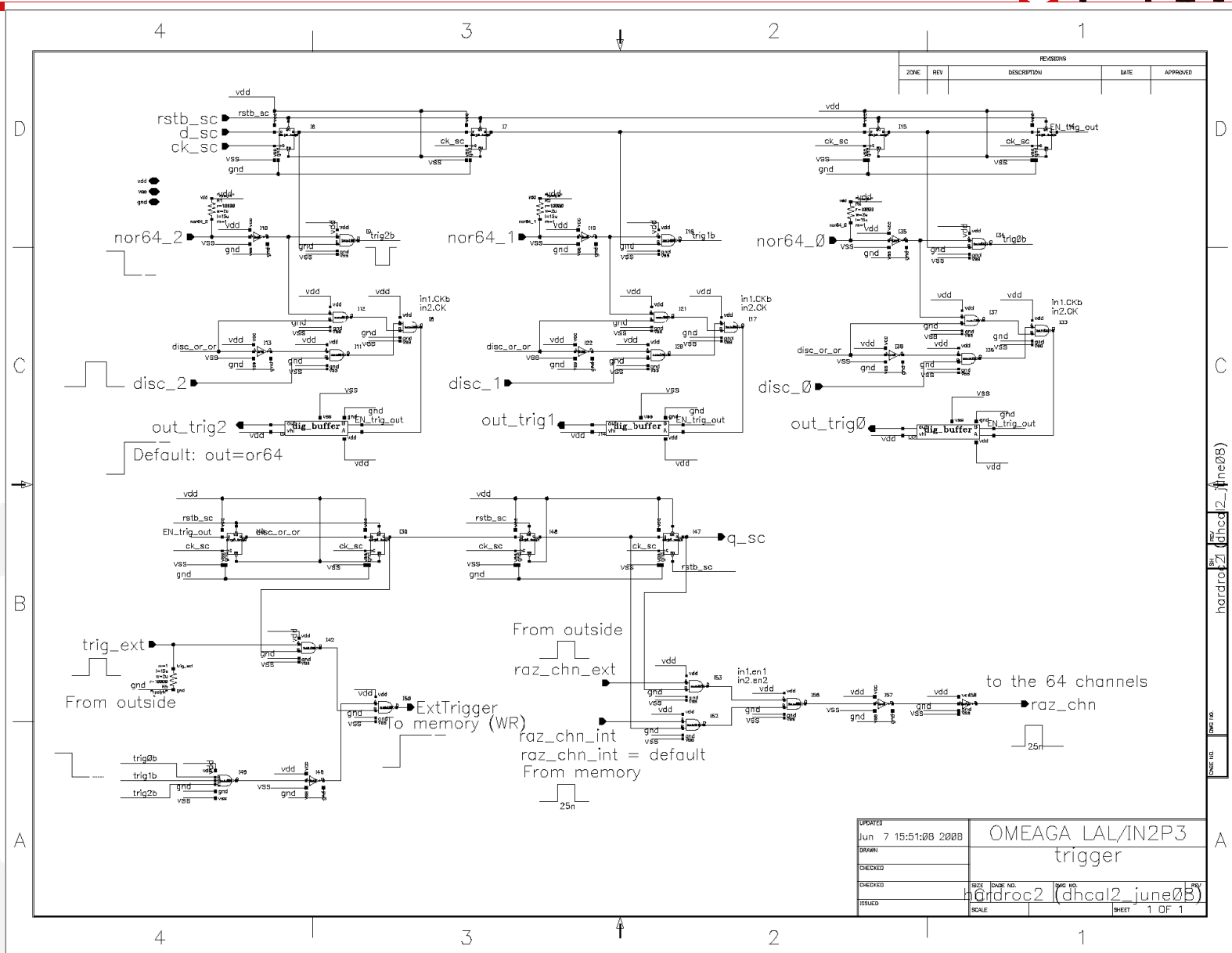
**FRAME:**  
 1 byte (Header),  
 3 Bytes (BCID),  
 4 bytes (encod0<Ch48>, encod1<Ch48>... to encod0<63>, encod1<63>),  
 4 bytes (Ch32 to 47),  
 4 bytes (Ch16 to 31),  
 4 bytes (Ch0 to 15)



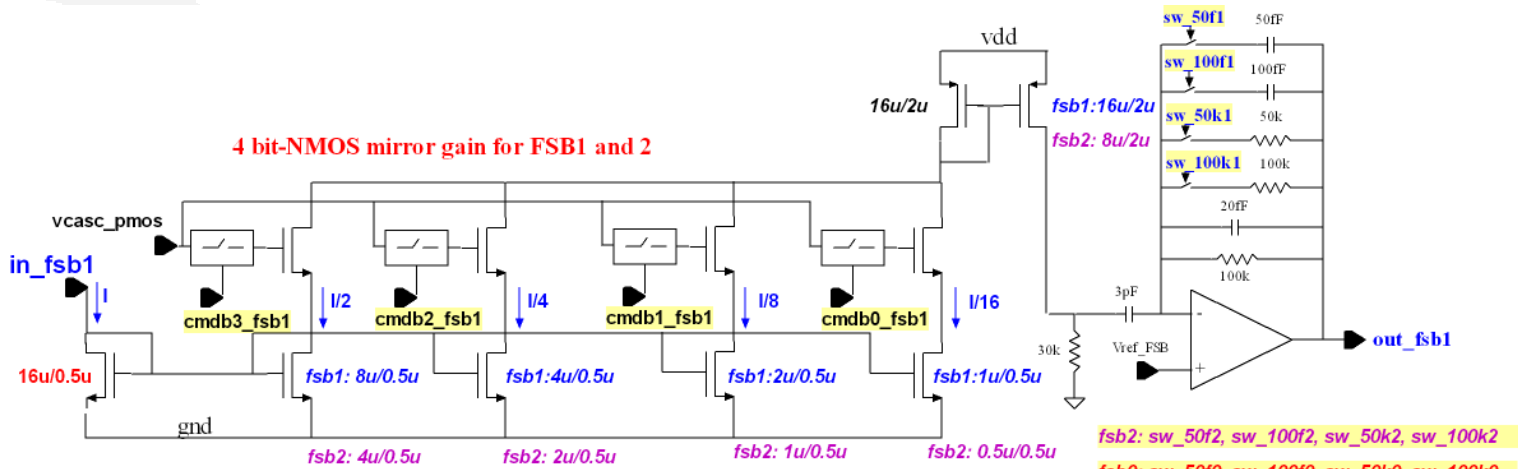
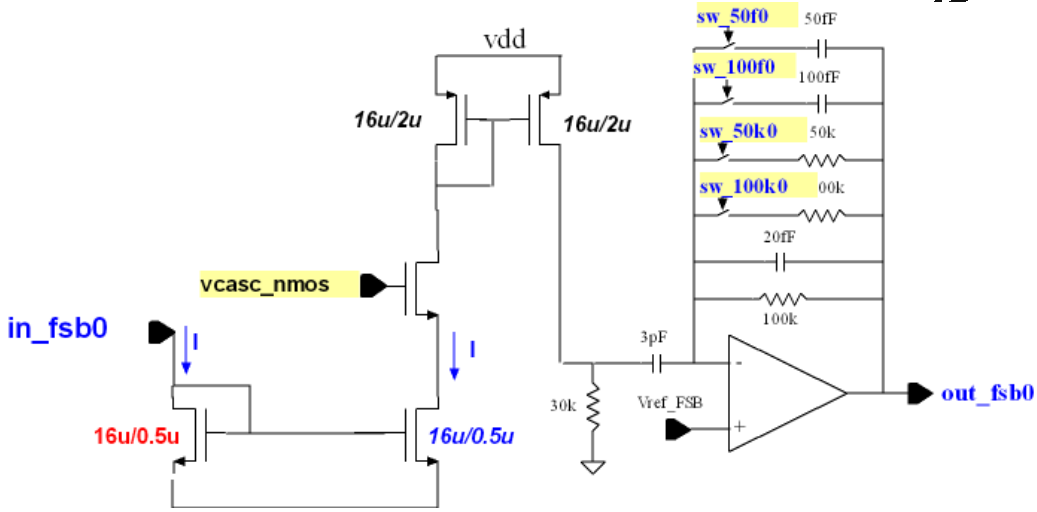
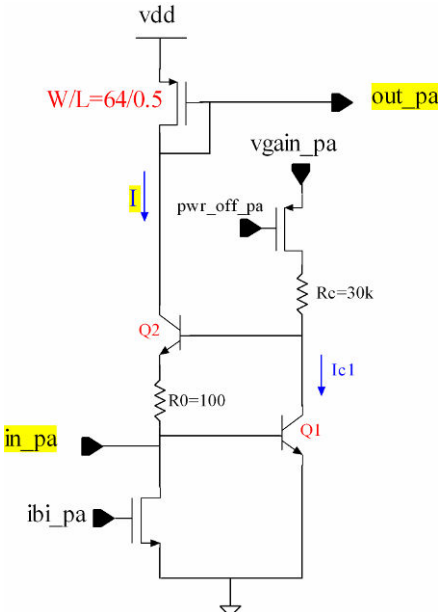
# Analog to Digital schematics



# TRIGGER and RazChn



# PA+FSB schematics

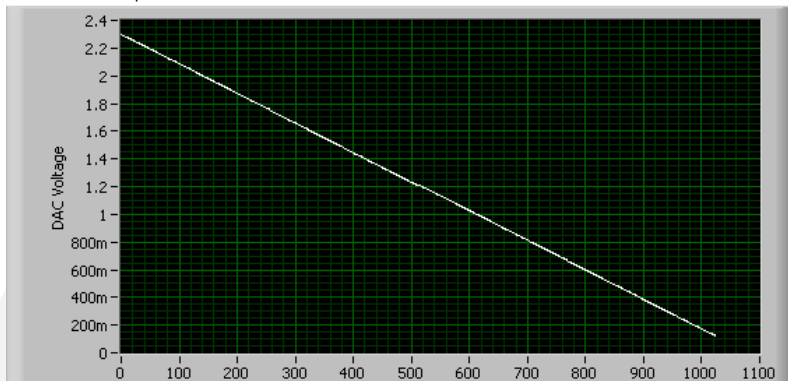


FSB1: default NMOS  $G_{nmos} = 0100$  ie 1/4 of FSB0  
 FSB2: default NMOS  $G_{nmos} = 0100$  ie 1/8 \* 1/2 = 1/16 of FSB0

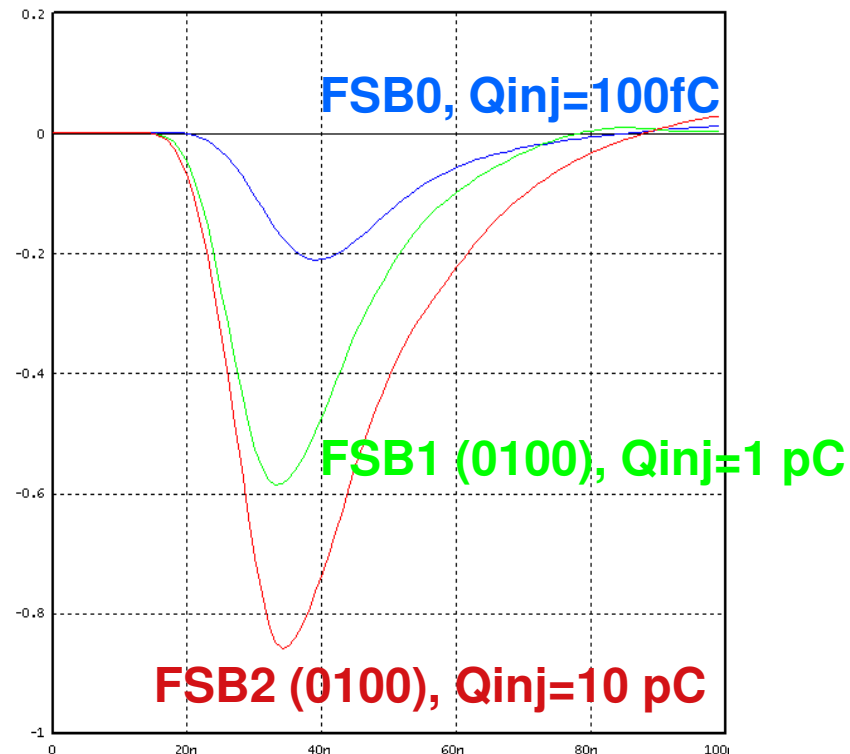
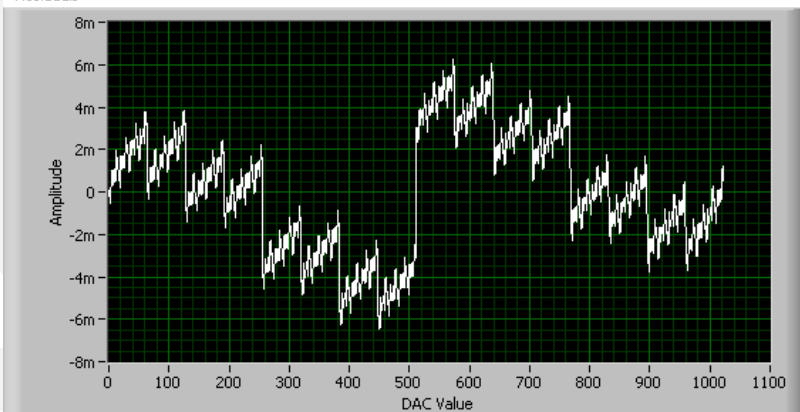
fsb2: sw\_50f2, sw\_100f2, sw\_50k2, sw\_100k2  
 fsb0: sw\_50f0, sw\_100f0, sw\_50k0, sw\_100k0

- Charge injected in one channel: 100fC
  - **Fsb0: Typically 2mV/fC** (variable by a factor 10)
- Scurves performed by varying the DAC value (Threshold)
  - 3 integrated DACs to deliver threshold voltages
  - Residuals within  $\pm 5$  mV / 2.2V dynamic range. INL= 0.2% (2LSB)
  - **2.1 mV/DAC Unit ie 1 fC/DAC Unit (fsb0)**

Test DAC Linearity

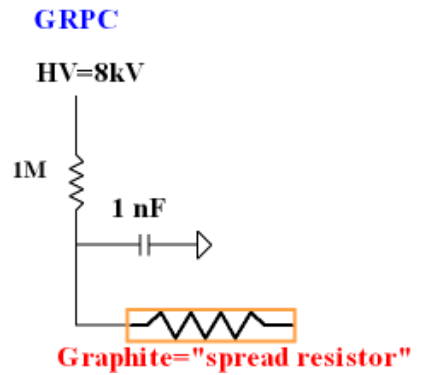
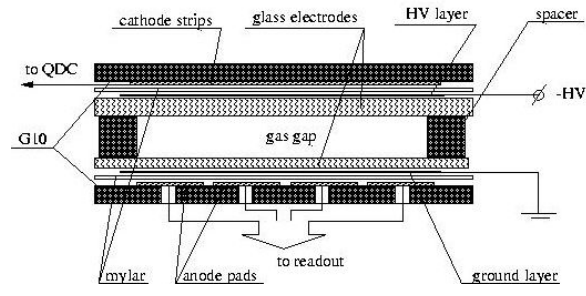


Residuals

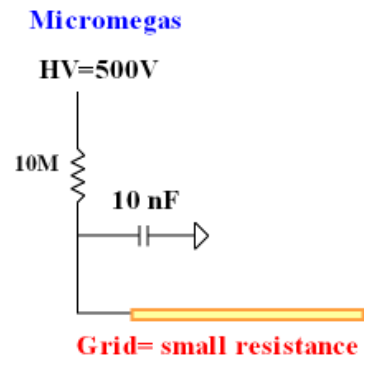
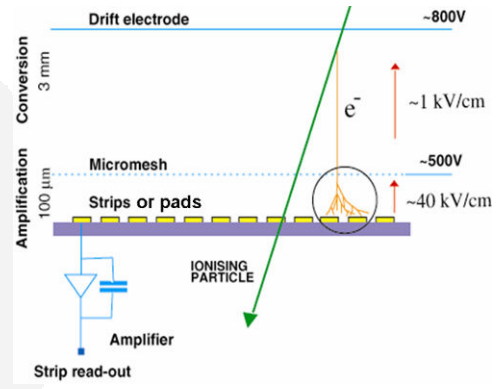


# HV sparks (ESD)

- **GRPC:** HV=8 kV, PADs= a few pF
  - High spread resistor= isolates FE inputs



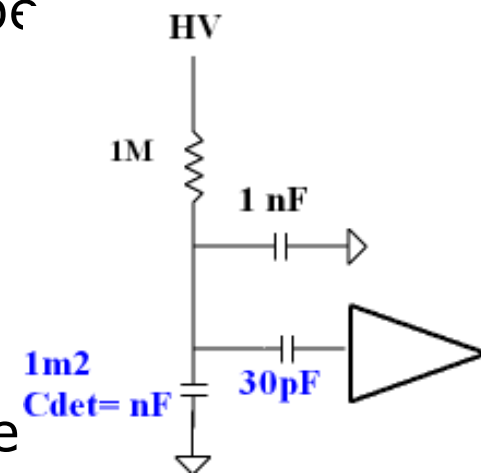
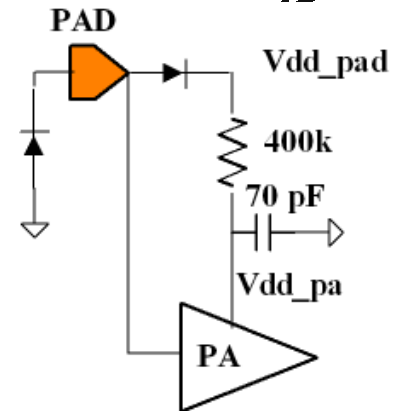
- **Micromegas:** HV=400V, Pads= a few pF
  - Small spread resistor= NO ISOLATION of the FE inputs



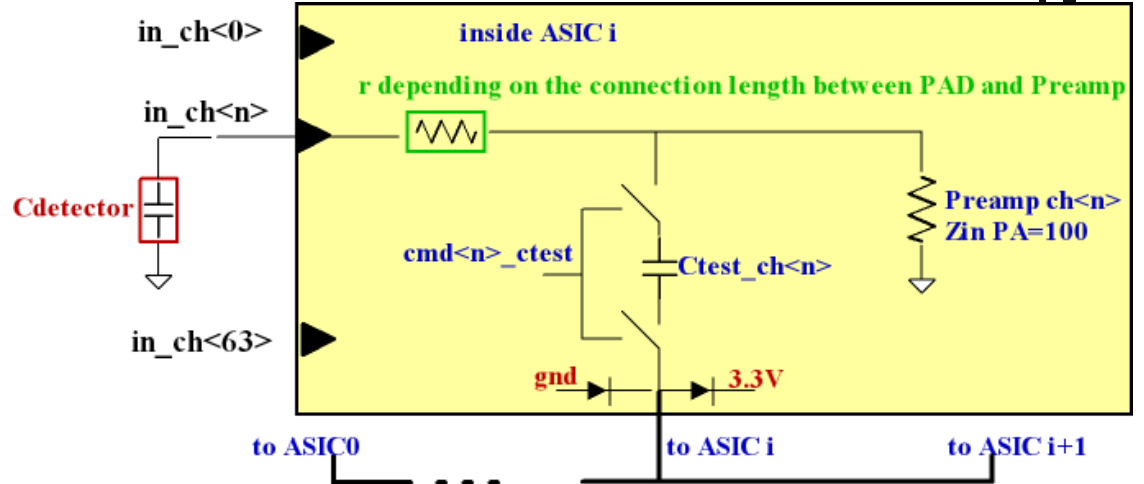
- $1m^2 \Rightarrow C_{HV} \sim 1nF$

# HV sparks (ESD)

- ASIC inputs:
  - protection PADs (AMS library): robustness up to 2kV HBM (100pF)
- From T2K large  $\mu$ megas, **AC coupling necessary for detector  $> 10 \text{ cm}^2$ :**
  - **Maximum decoupling** capacitor that can be **integrated:  $\approx 30 \text{ pF}$**  ( $50 \mu\text{m} \times 600 \mu\text{m}$ ) and **lost of signal**
  - **EXTERNAL CAP=500 pF/ch** to ensure protection
  - Drawbacks of a decoupling cap: Xtalk, space

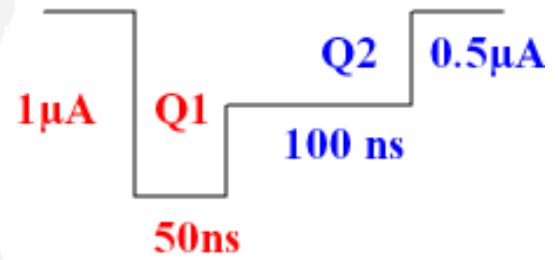


- RPC signal:
  - dirac current



- Micromegas signal:

$$Q = i_1 \cdot t_1 + i_2 \cdot t_2$$



=> FS is too fast compared to the signal

Protection diodes =>

Max for in\_Ctest = 3.3 + 0.7 = +4V

Min for in\_Ctest = -0.7V

In\_Ctest Voltage falling edge => injected I = CdV/dt => negative dirac pulse