IN2P3

Omega

Status of SPIROC

Michel Bouchel, Stéphane Callier, Frédéric Dulucq, Julien Fleury, Gisele Martin-Chassard, Christophe de La Taille, Ludovic Raux

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Orsay MicroElectronic Group Associated

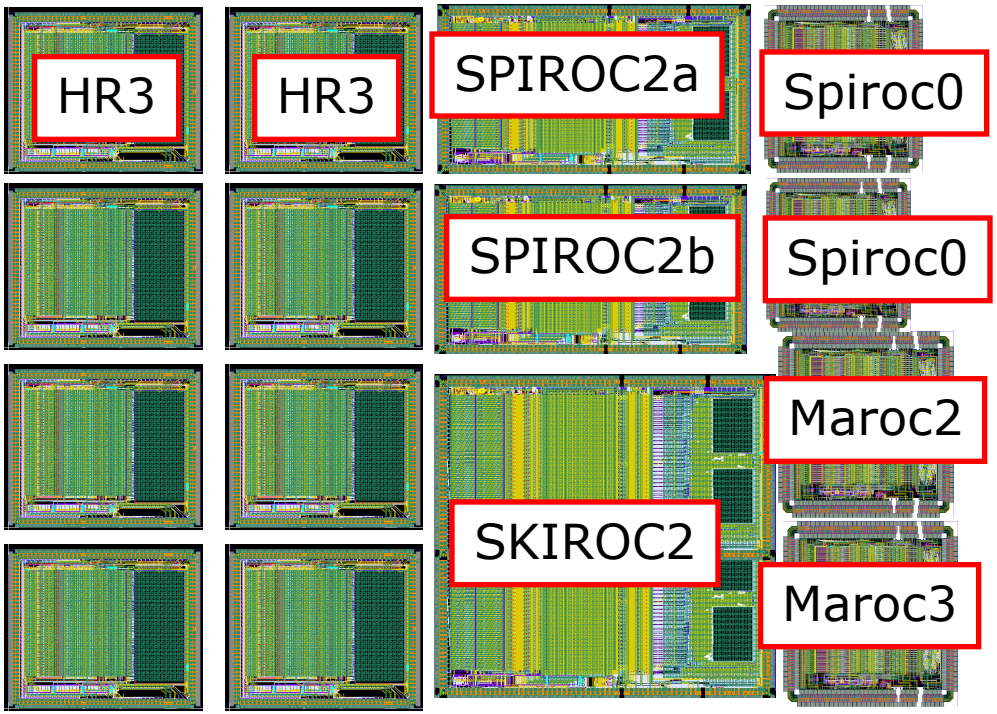
- Plan for 2010 :
  - February 2010 dedicated production run: 2 prototypes will be submitted:
    - A conservative prototype (SPIROC 2a) in which the major bugs of SPIROC 2 will be fixed
    - A little more agressive prototype (SPIROC 2b) in which the major bugs of SPIROC 2 will be fixed and some light improvements will be added
  - Before the end of the year, submission of a SPIROC 3 with more agressive modifications and improvements

Engineering run

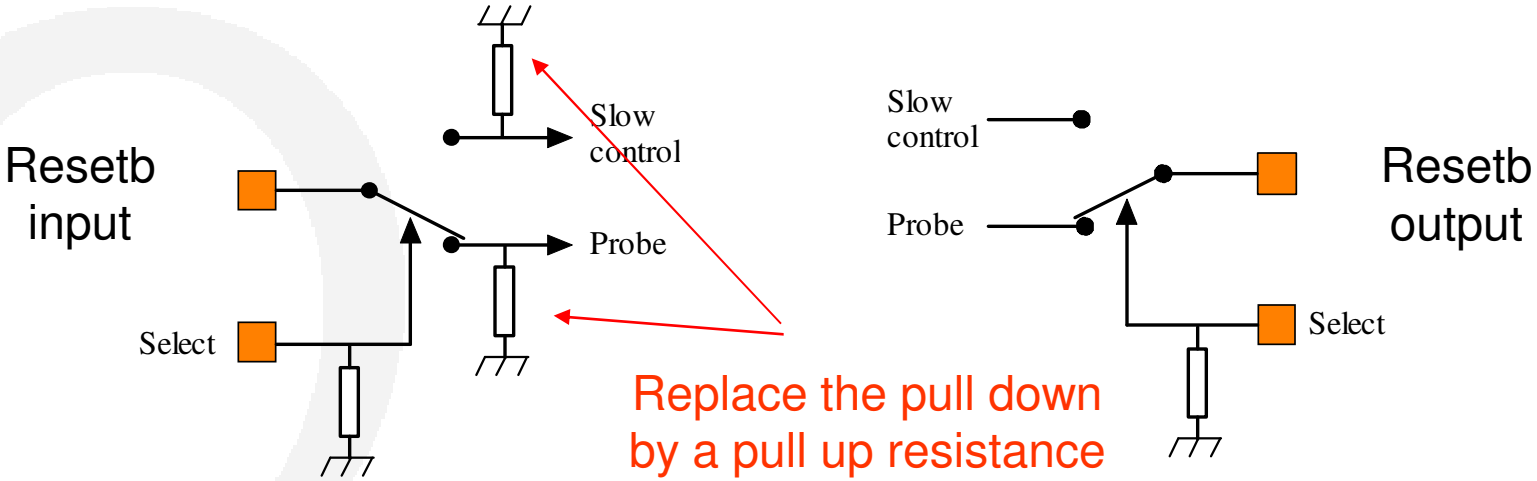
- Reticle size : 18x25 mm2
  - 50-55 reticles/Wafer
  - 25 wafers needed

- Arrangement to be finalized
  - 8 Hardroc 2b => 10000 chips
  - **1 Spiroc 2a**
  - **1 Spiroc 2b**
  - 1 Skiroc 2
  - 1 Maroc 2
  - 1 Maroc 3
  - 2 Spiroc 0 (SPIROC « light » version) or 1 SPIROC 0 + 1 ParisRoc

- Will be launched as soon as measurements are complete !
  - Exp. Beg.2010

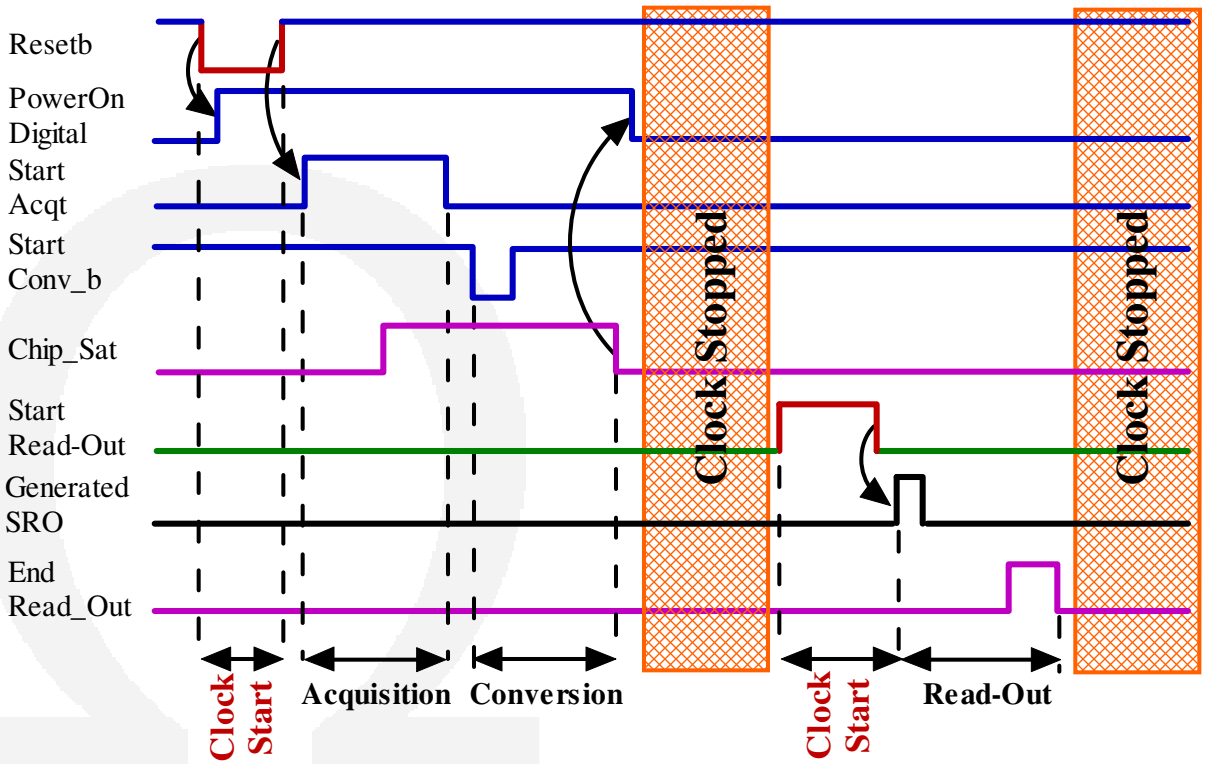


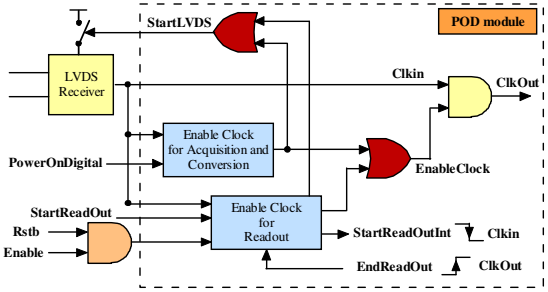
- Conservative version of SPIROC 2:
  - fix the slow control and probe bus :
    - By adding buffers in critical points as done in HARDROC2B
    - By correcting the Bug on the reset signal of the multiplexed probe and slow control register
      - » **Active low reset forced to 0 when not selected**
      - » **Intempestive reset when register is unselected**



- By putting a default Slow control set-up

- Conservative version of SPIROC 2:
  - add the POD module for the 2 clock LVDS receivers to reduce idle power dissipation (already tested on Hardroc2)





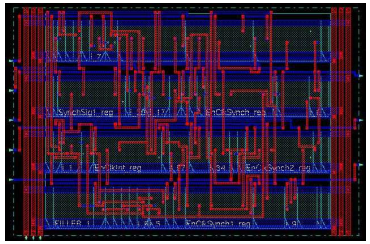
Calibrated (LVDS start time)

From DAQ

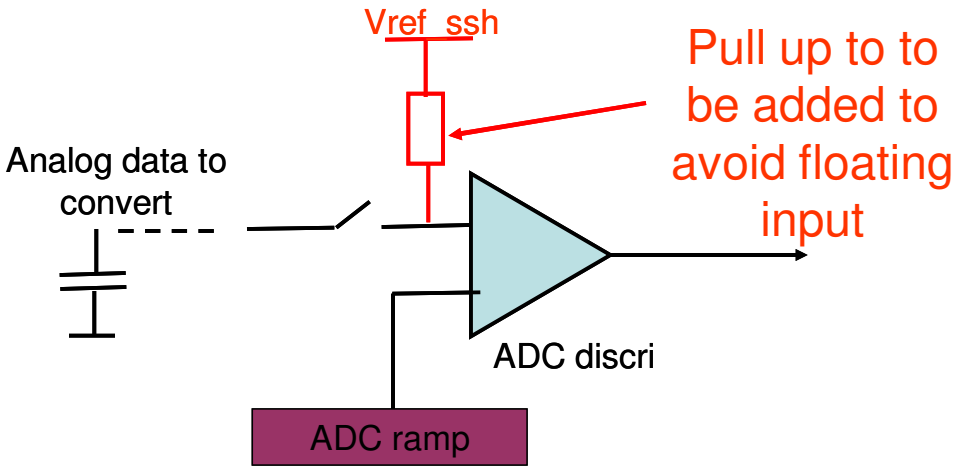
From daisy chain

From ASIC

From POD



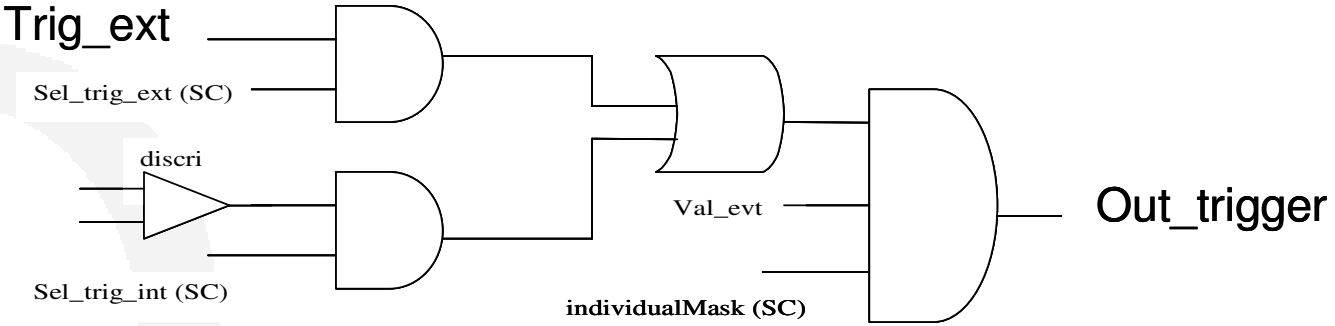
- Conservative version of SPIROC 2:
  - fix the first "zero-frame" by adding a pull-up to reference voltage on ADC discri input



  - Put a OR36 output on a non selected
  - Decrease the consumption of the low gain preamplifier

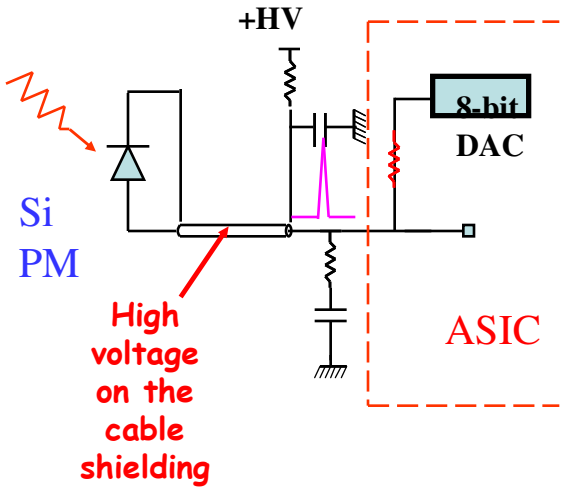
This spiroc2a prototype is ready to be submitted

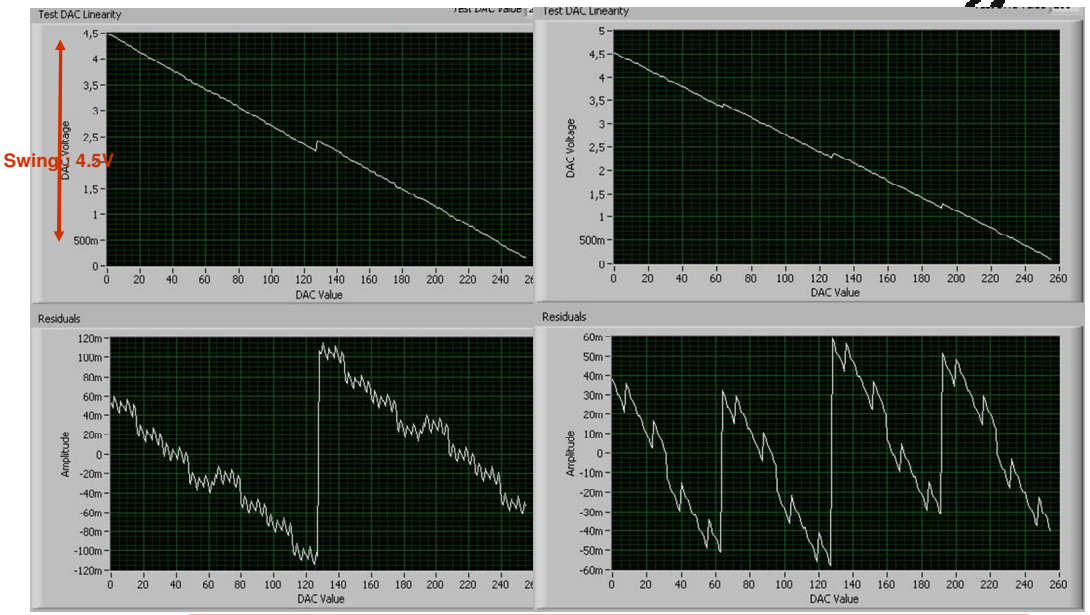
- SPIROC 2a with the following improvements:
  - **New bandgap**
  - **Replace the ADC ramp by an optimized one**
  - **Replace the ADC discriminators by an improved one (PARISROC)**
  - **External trigger input (LVDS)**



  - **put the improved version of 8-bit input DAC**
  - **put the improved version of threshold 10-bit DAC**

SPIROC 1&2 input DAC performances





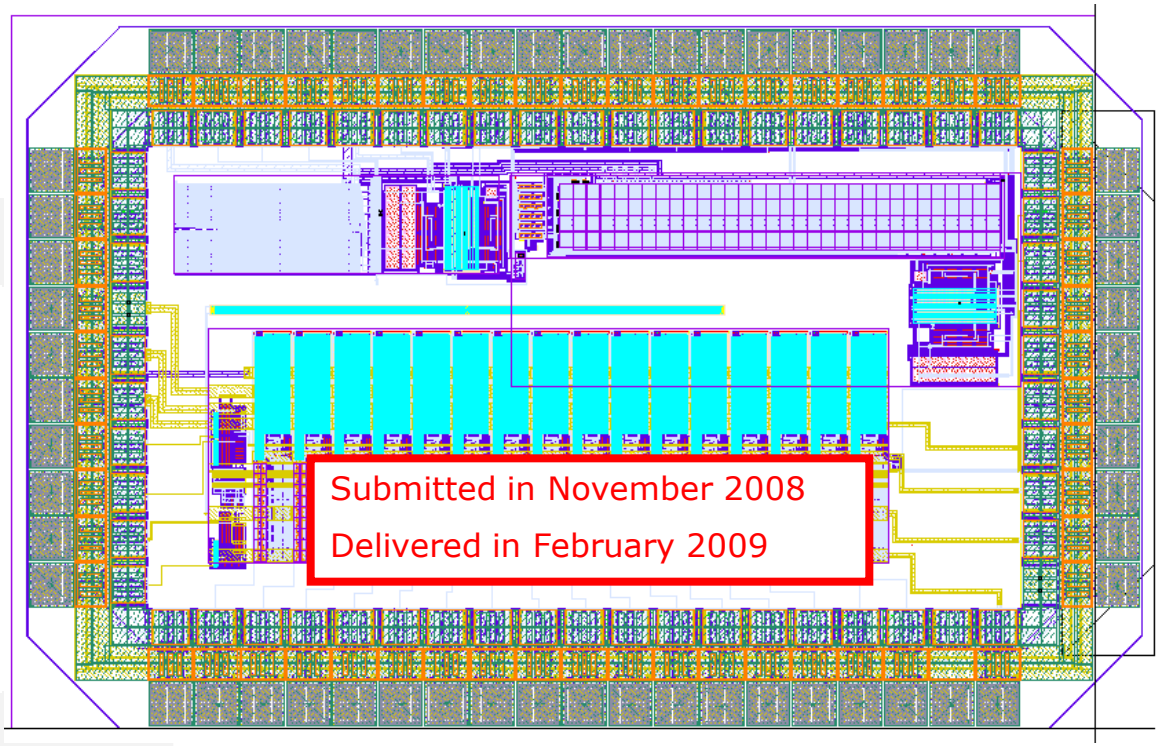
Linearity residuals vary from -/+ 60mV
1 to -/+ 120mV (from 1.5 to 3%)

- **Input DAC to optimize SiPM bias voltage**
- **8-bit DAC, 5V range**
- **LSB=20mV**
- **36 DAC : one per channel**
- **Ultra low power (1µW) : no power pulsing**
- **Can sink 10 µA leakage current**
- **DAC uniformity between the 36 channels : ~3%**

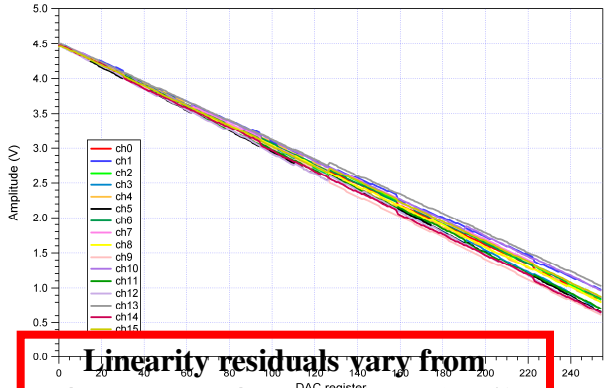
Improvement for the « ROC family » DACs

- « Building block » funded by IN2P3 submitted november 2008
  - 2 12-bit DACs for the threshold trigger:
    - **NMOS**
    - **Bipolar**
  - 16 8-bit low power input DAC for SiPM bias

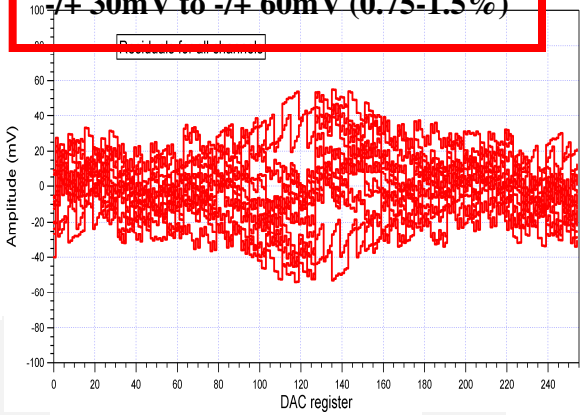
- Improved performance (linearity, uniformity channel by channel) were expected with a new layout rearrangment for a better matching

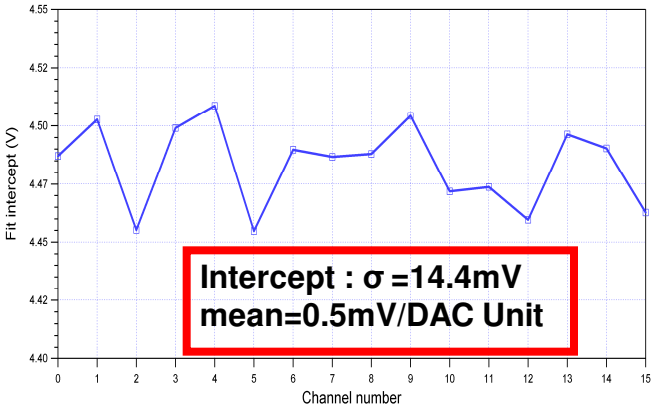


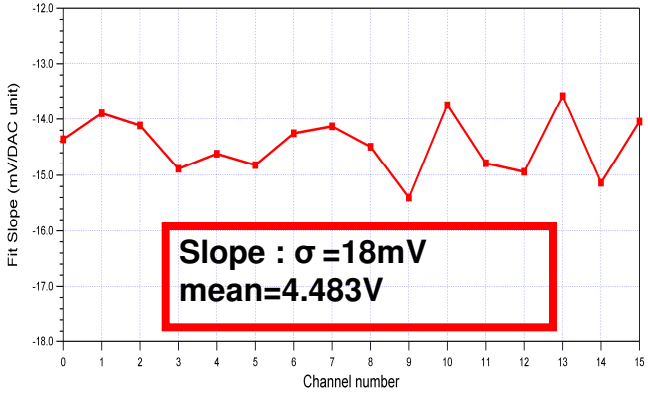
« Building block » input DAC Performance



Linearity residuals vary from -/+ 30mV to -/+ 60mV (0.75-1.5%)







- Disappointing performances on the « building block » DAC only a factor 2 won
- Have to be improved by a new geometrical re-arrangement
  - New layout ready to be implemented on **SPIROC2b**

SPIROC 3: modifications and improvements

- SPIROC 2a + SPIROC 2b with the following improvements:
  - Preamplifier gain adjustment per channel
  - New TDC to have 100 ps accuracy (just submitted last November on PARISROC 2 Chip)
  - 8-bit input DAC : auto-regulation with respect to detector temperature
  - "Powering-up mode" of SCA columns to save power:
    - SCA columns are powered only when they are used
  - New improved and optimized digital part
  - Possibly Wei's input stage after testing
  - Possibly new I2C slow control interface

Conclusion

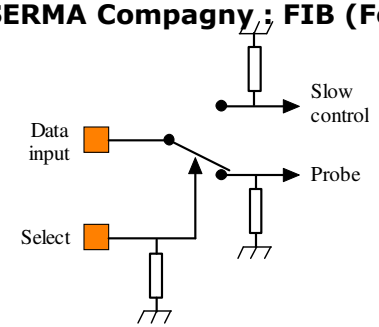
- During February : PRODUCTION RUN
- SPIROC 2a chip :
  - Conservative prototype : major bugs fixed
- SPIROC 2b chip :
  - Conservative prototype with « controlled » improvements submitted at the same time of the Hardroc2b production run
- SPIROC 3 chip :
  - Agressive modifications and improvements (before the end 2010?)

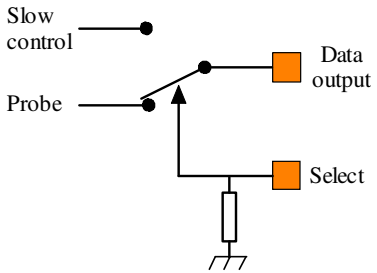
DAC performance

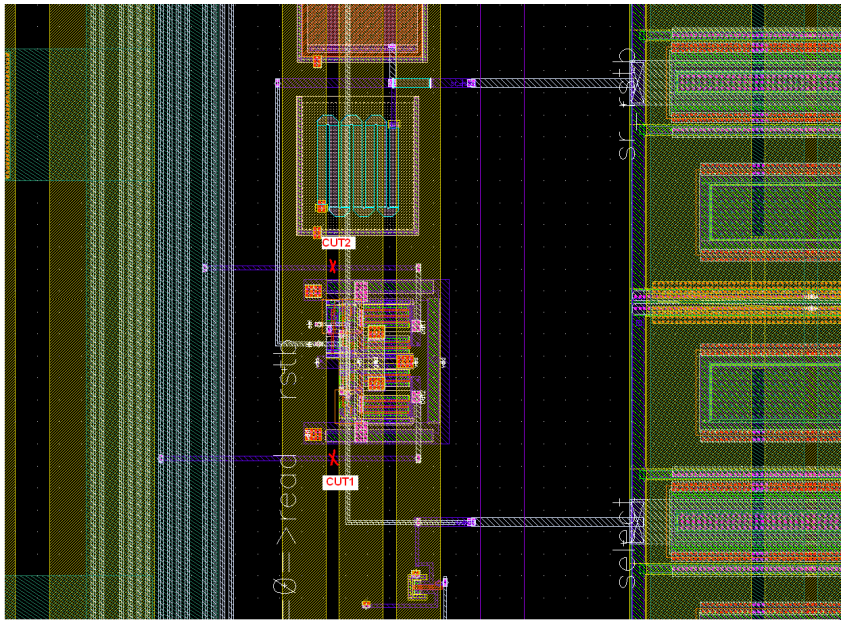
- Disappointing performances for the « building block » DAC
- Have to be improved by a new geometrical re-arrangement
  - New layout in progress…
  - DAC, auto-regulation with respect to detector temperature

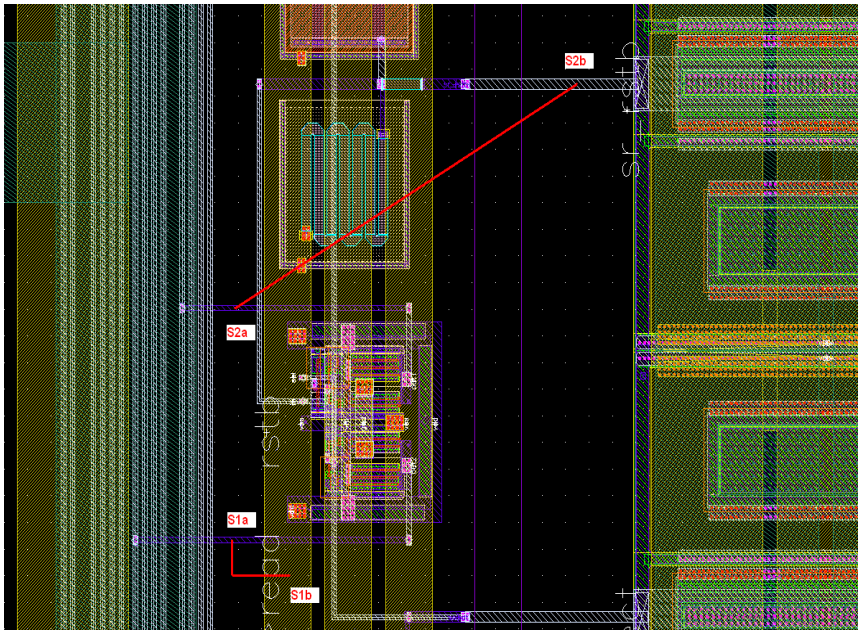
SPIROC 2 : slow control register

- **Bug on the reset signal of the new multiplexed probe and slow control register**
  - **Active low reset forced to 0 when not selected**
  - **Intempestive reset when register is unselected**
  - **Same problem on Hardroc 2**
- **Correction by SERMA Compagny : FIB (Focused Ion Beam)**



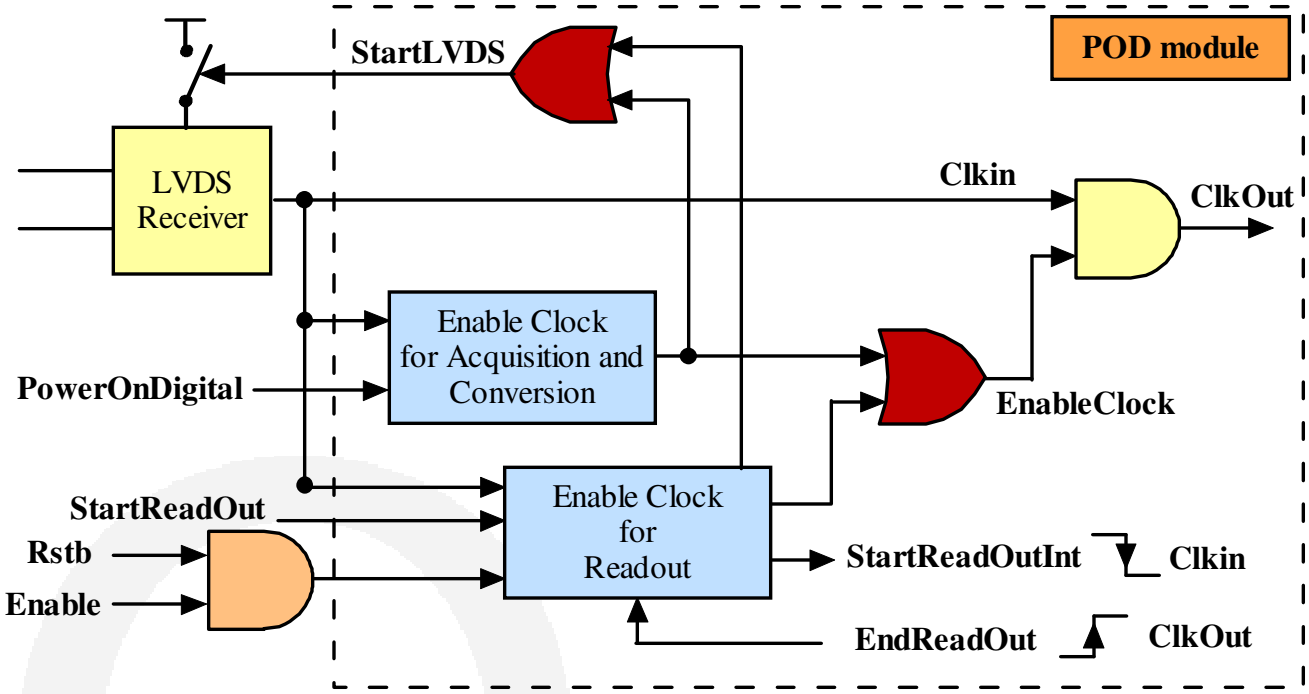


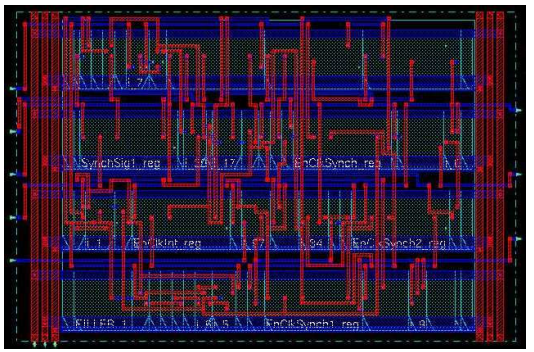




Power On Digital: POD block diagram

- POD module inserted for the 2 clock LVDS receivers

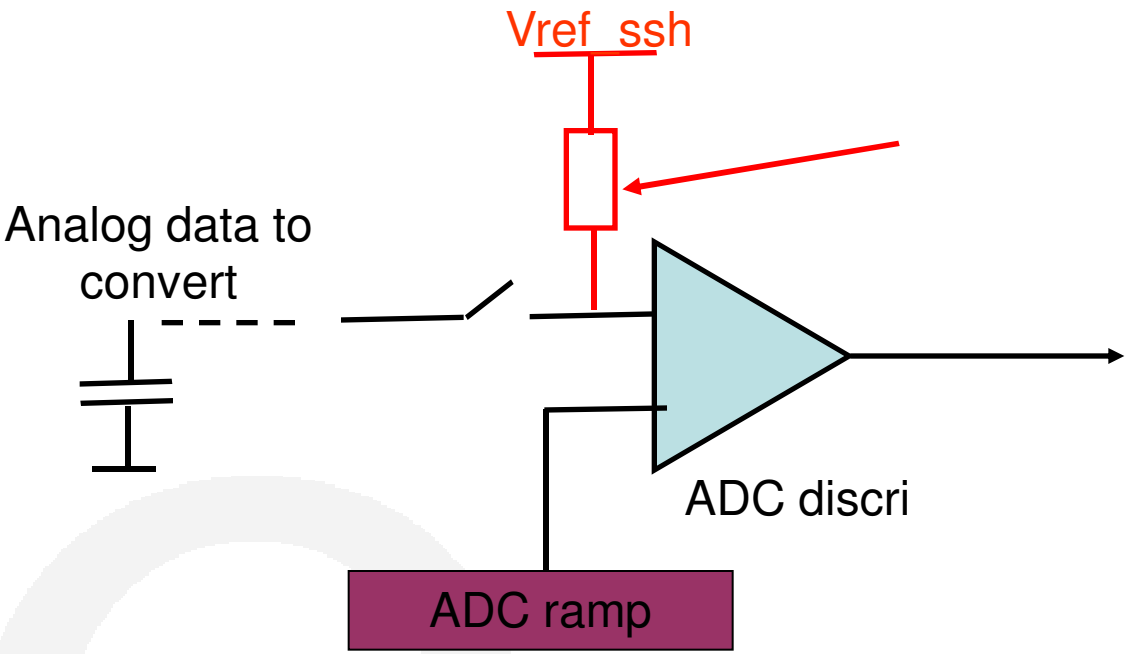




- Clock is started asynchronously, enabled and stopped synchronously (at '0')

- 2 others LVDS receivers (RazChn/NoTrig and ValEvt) active during PowerOnAnalog (during bunch crossing)

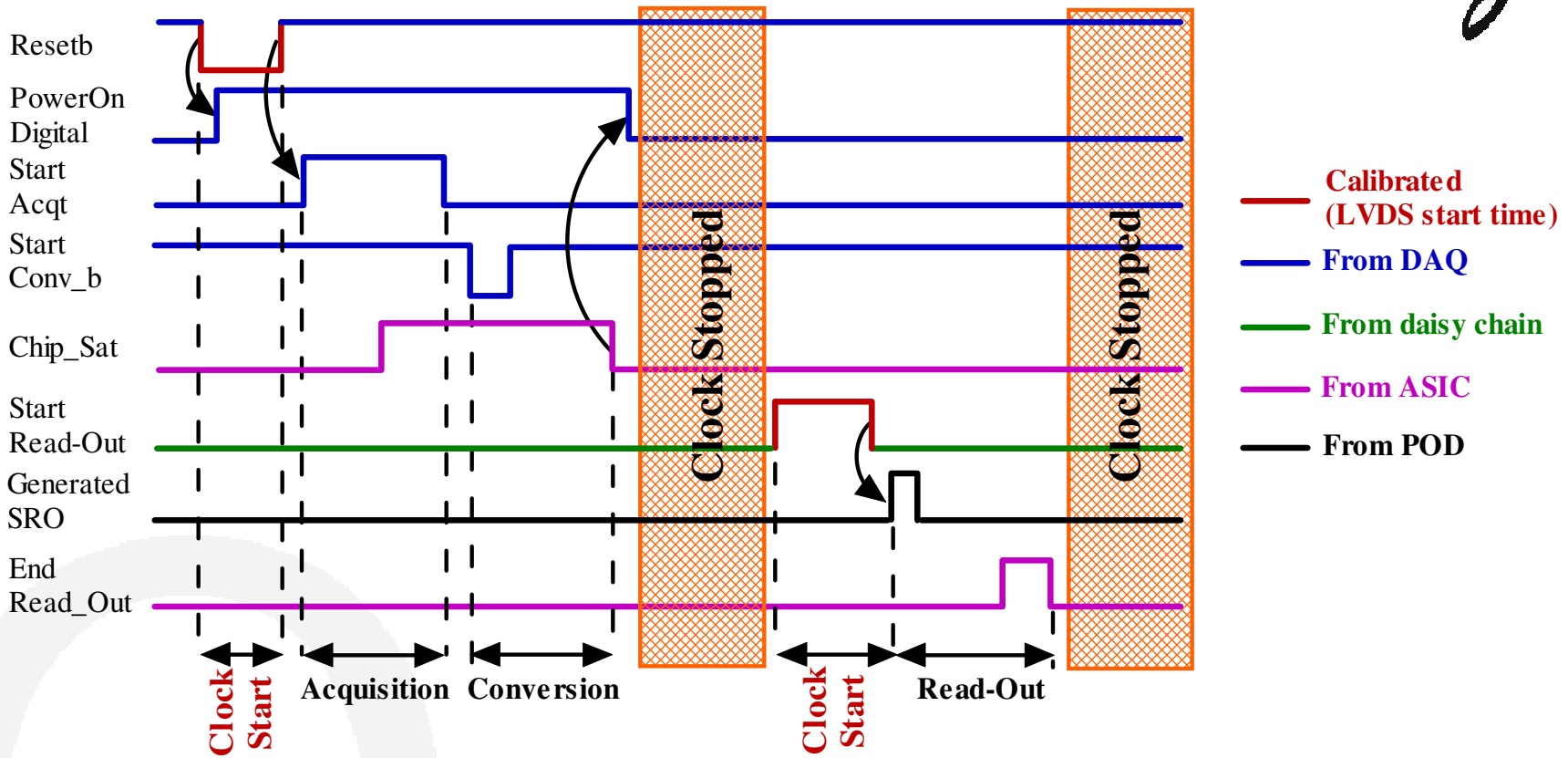
SPIROC 2a : modifications and improvements (3/3)



- Conservative version of SPIROC 2:
  - fix the first "zero-frame" by adding a pull-up to reference voltage on ADC discri input
  - utput on a non selected
  - Decrease the consumption of the low gain preamplifier

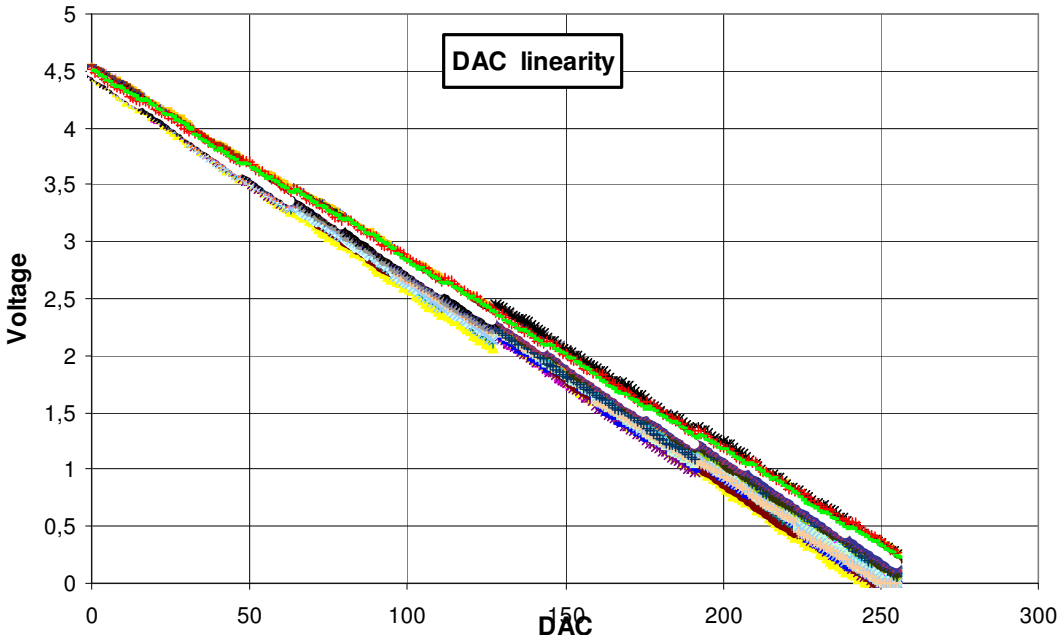
This prototype is ready to be submitted

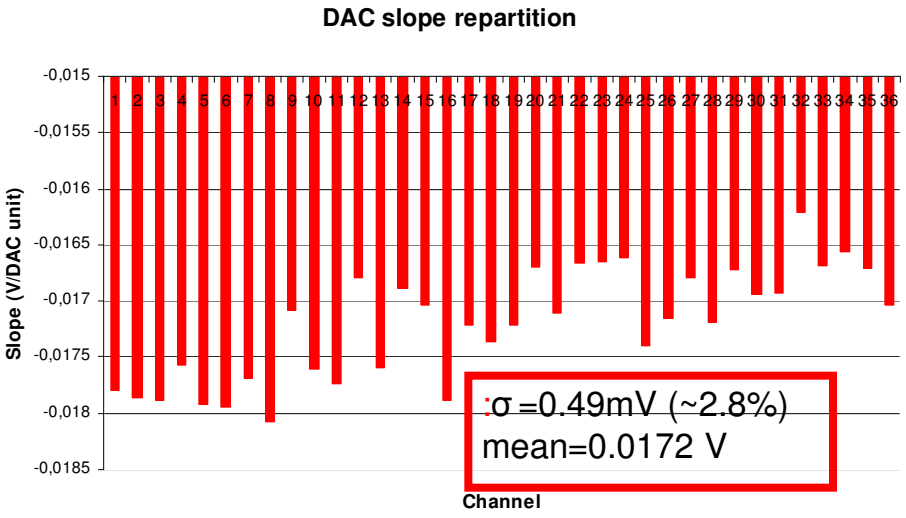
Power On digital: sequence



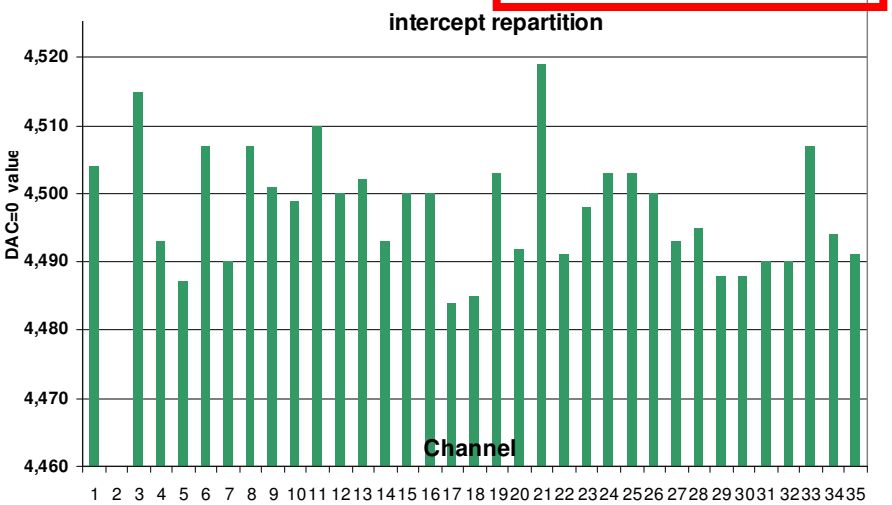
- Some security added:
  - StartReadOut managed asynchronously ➔ low pass filter added
  - Possibility to use StartReadOut instead of the one generated by POD (like first prototype of ROC chips)
  - PowerOnDigital at '1' can force the clock

SPIROC 1&2 input DAC performances



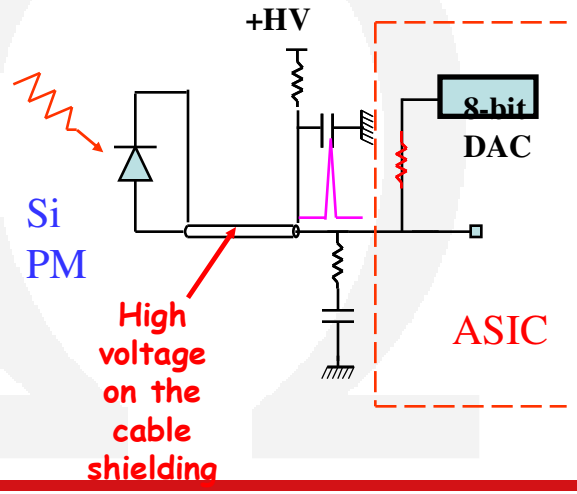


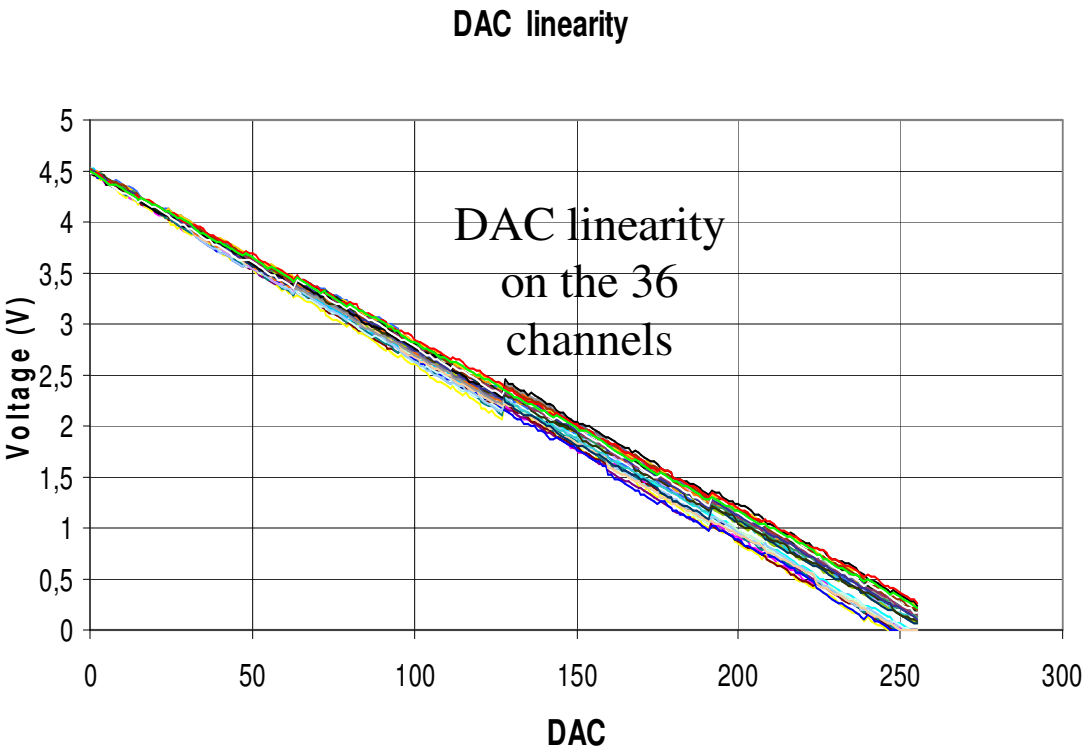
σ =8mV (~0.2%)
mean=4.49V



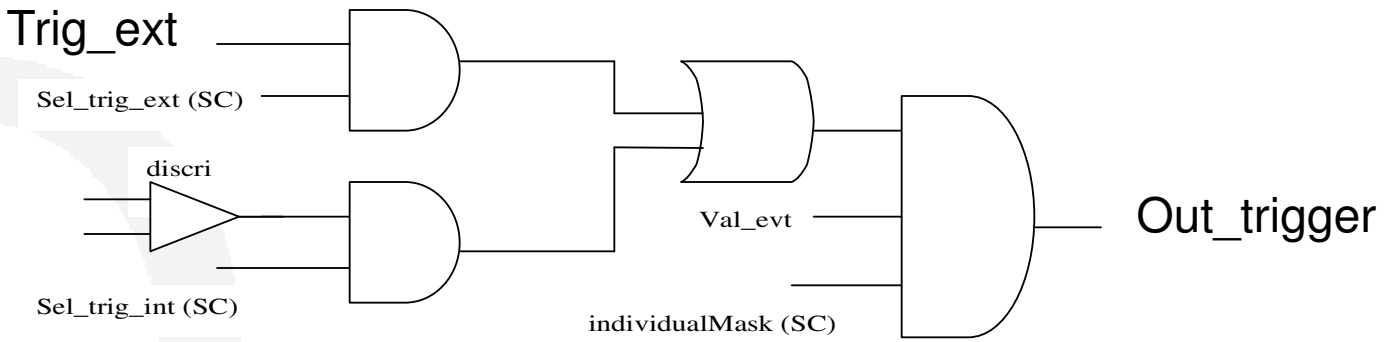
Input DAC

- **Input DAC to optimize SiPM bias voltage**
- **8-bit DAC, 5V range**
- **LSB=20mV**
- **36 DAC : one per channel**
- **Ultra low power (1µW) : no power pulsing**
- **Can sink 10 µA leakage current**
- **Linearity : ± 2%**
- **DAC uniformity between the 36 channels : ~3%**



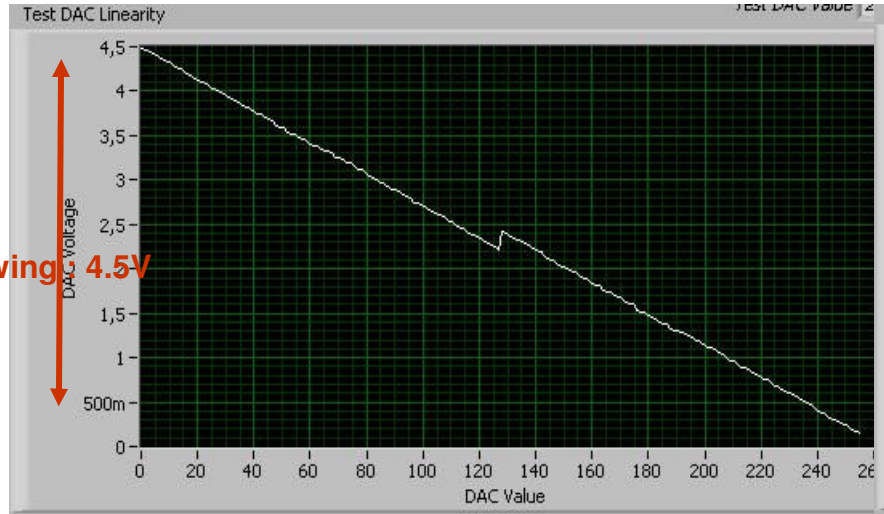


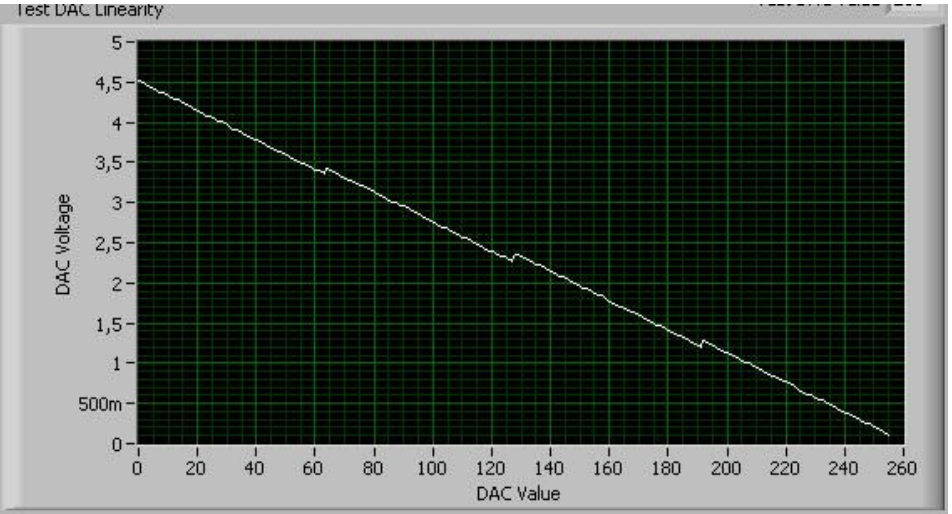
Improvement for the « ROC family » DACs

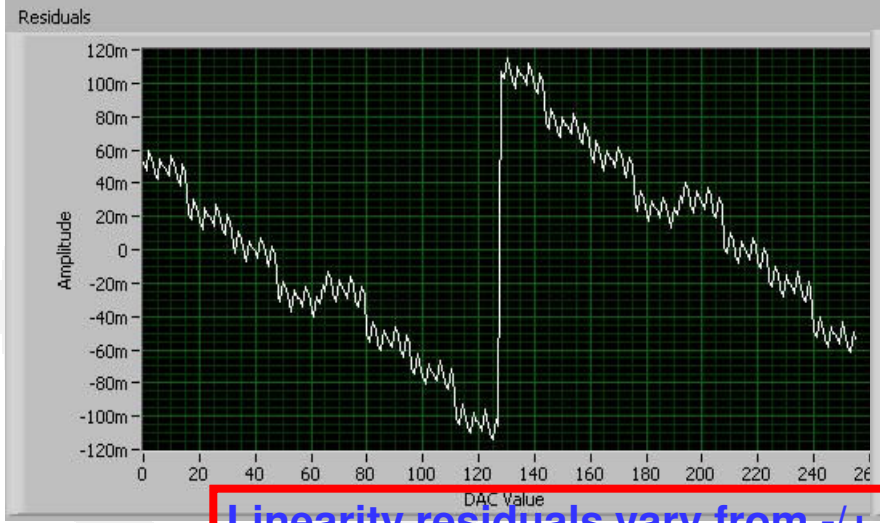


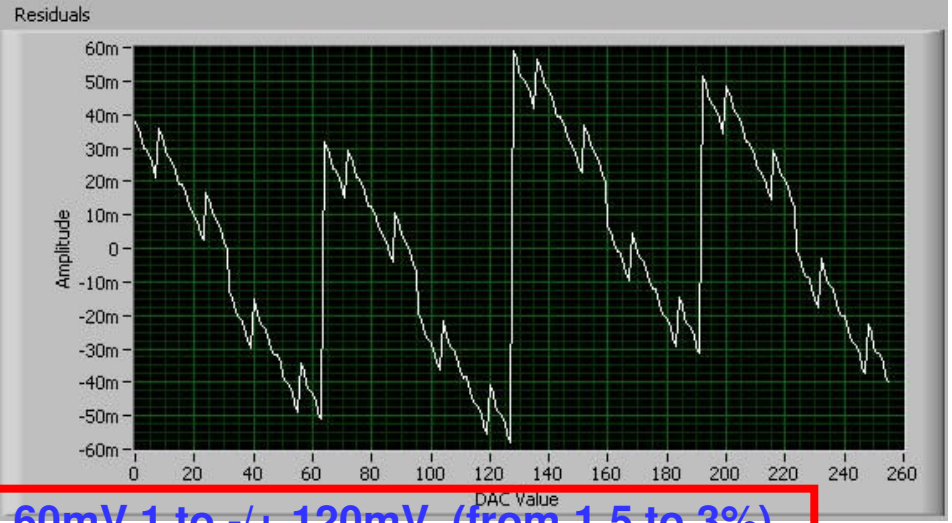
- Better performances but disappointing….
- Have to be improved by a new geometrical re-arrangement
  - New layout ready to be implemented
  - auto-regulation with respect to detector temperature

SPIROC 1&2 input DAC performances









Linearity residuals vary from -/+ 60mV 1 to -/+ 120mV (from 1.5 to 3%)