PCB DEVELOPMENTS AT *IPNL*
(PCB and ASIC)

- PCB for 1m2 of RPC with HR1-HR2-HR2b

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Collaboration with LAL

1 m² PCB MAIN SPECIFICATIONS

(HR1-HR2-HR2b)

ASU PCB Design

- 24 x 64 1 sq cm pads
- 24 Hardrocs Asics chained in plastic package (very thin 1.2 mm)

1 m2 PCB board :

- 6 ASUs
- 144 Hardroc Asics

DIF boards :

- 1 DIF for 2 ASU : 3 DIFs

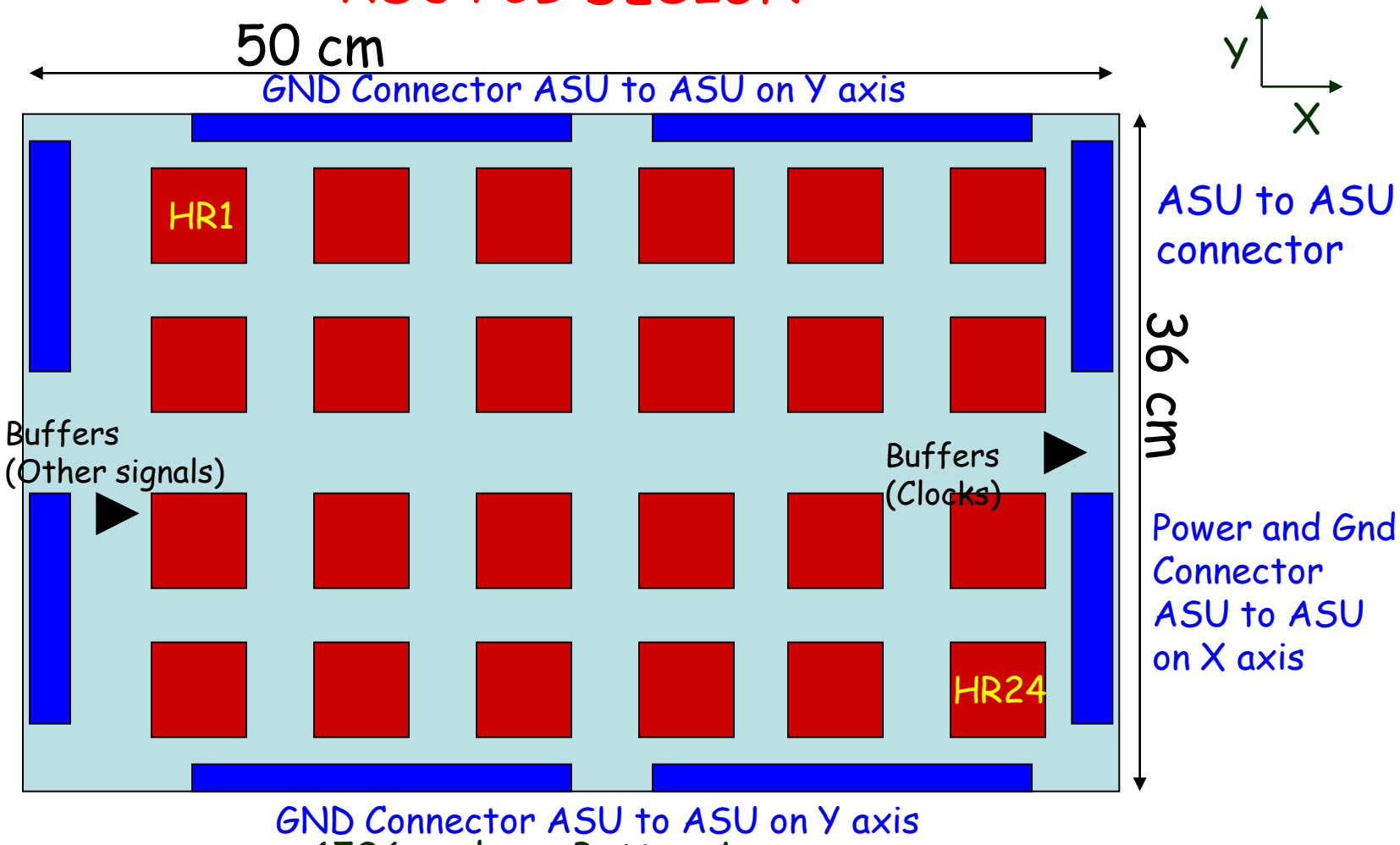
HR2 :

✓ All modifications are implemented

✓ SC bypass

✓ SC Clocking and so on

ASU PCB DESIGN

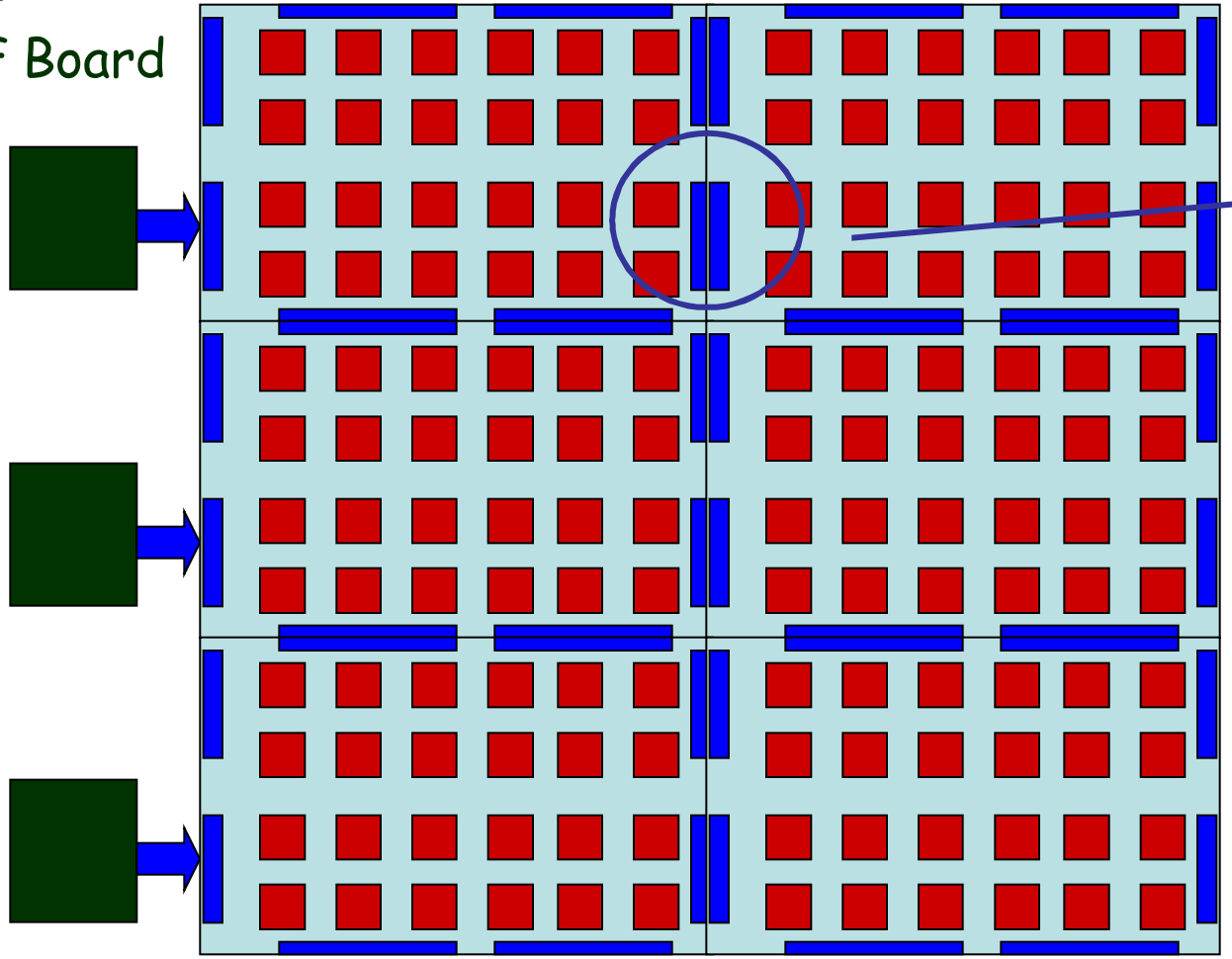


- Buried and Blind Vias (Same as the first PCB with 4 HR1)
- *Buffers are implemented (HR1) but the board must work without buffers (HR2-HR2b)*

1 m² PCB DESIGN interconnection

1 DIF for 2 ASUs

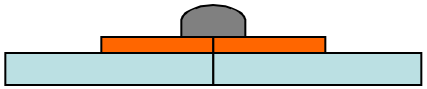
DIF Board



9216 pads on Bottom Layer

ASU to ASU Connection HR1

Solder or 0 ohm resistor



ASU 1 ASU 2

Mechanical Problems

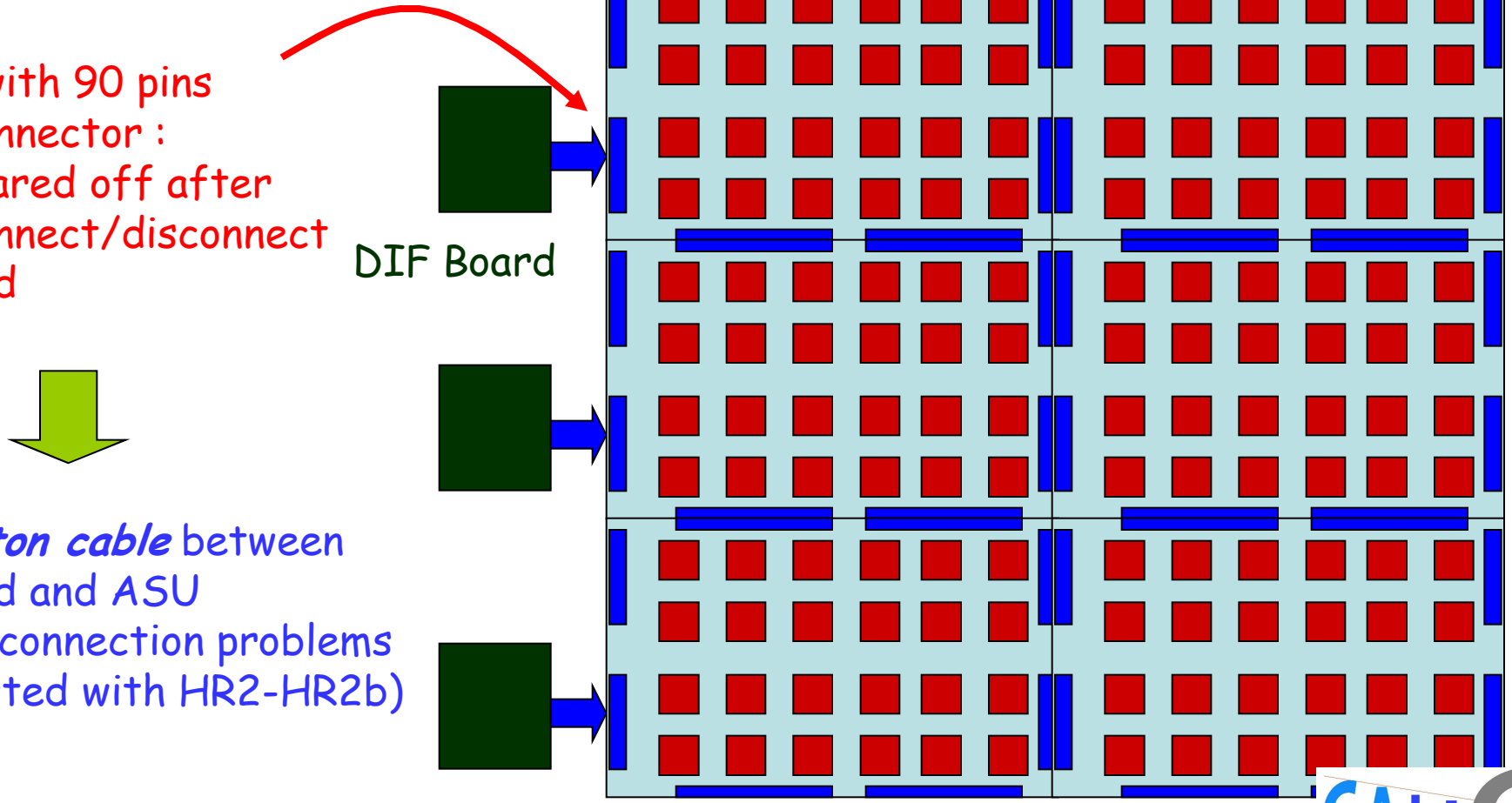
Kapton cable

(Test in progress with HR2)

1 m2 PCB DESIGN interconnection

1 DIF for 2 ASUs

Problems with 90 pins
Samtek connector :
Pad are teared off after
Several connect/disconnect
DIFF board



Add a ***kapton cable*** between
DIFF board and ASU
To reduce connection problems
(will be tested with HR2-HR2b)

1 m² PCB DESIGN (Layers and next steps)

- Layer 1 (TOP) : interconnect
- Layer 2 : GND
- Layer 3 : Digital signal
- Layer 4 : Power
- Layer 5 : GND
- Layer 6 : PADs to Hardroc
- Layer 7 : GND
- Layer 8 (BOTTOM) : PADs

Pads to HR interconnects are the same for the entire PCB (hierarchical design)

- *1 sq meter with HR2 in progress*
- *First board with HR2b will be assembled very soon*
- Manufacturing the other 5 boards (HR2b) after tests results

1 m² PCB DESIGN (Layers and next steps)

- Before starting the production
  - 1 sq meter with HR1 : in test (beam and cosmic)
  - 1 sq meter with HR2 : available in a few days (***Power Pulsing under test***)
  - 1 sq meter with HR2b : assembly started

Next steps before starting production of 1 cubic meter

- 2 boards with pins for ASU to ASU connection
- 2 boards with connector for ASU to ASU connection

This 2 new designs are in study and must be ready by the end of January

ASIC DEVELOPMENT IN LYON

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(CNRS IN2P3 IPNL)

Collaboration with LAL/LAPP

Université Claude Bernard Lyon 1

Université Blaise Pascal

Mixed signal Asic design

This ASIC include : (for details see talk on previous Calice meeting in Lyon)

- Digital part for DIRAC design
- I2C serial link for slow control parameters
- CSA :
  - same analog block as DIRAC3
  - slow control parameters (4 gains) controlled through I2C

AMS 0.35 µm in CMOS process
Cadence design flow for digital and analog parts

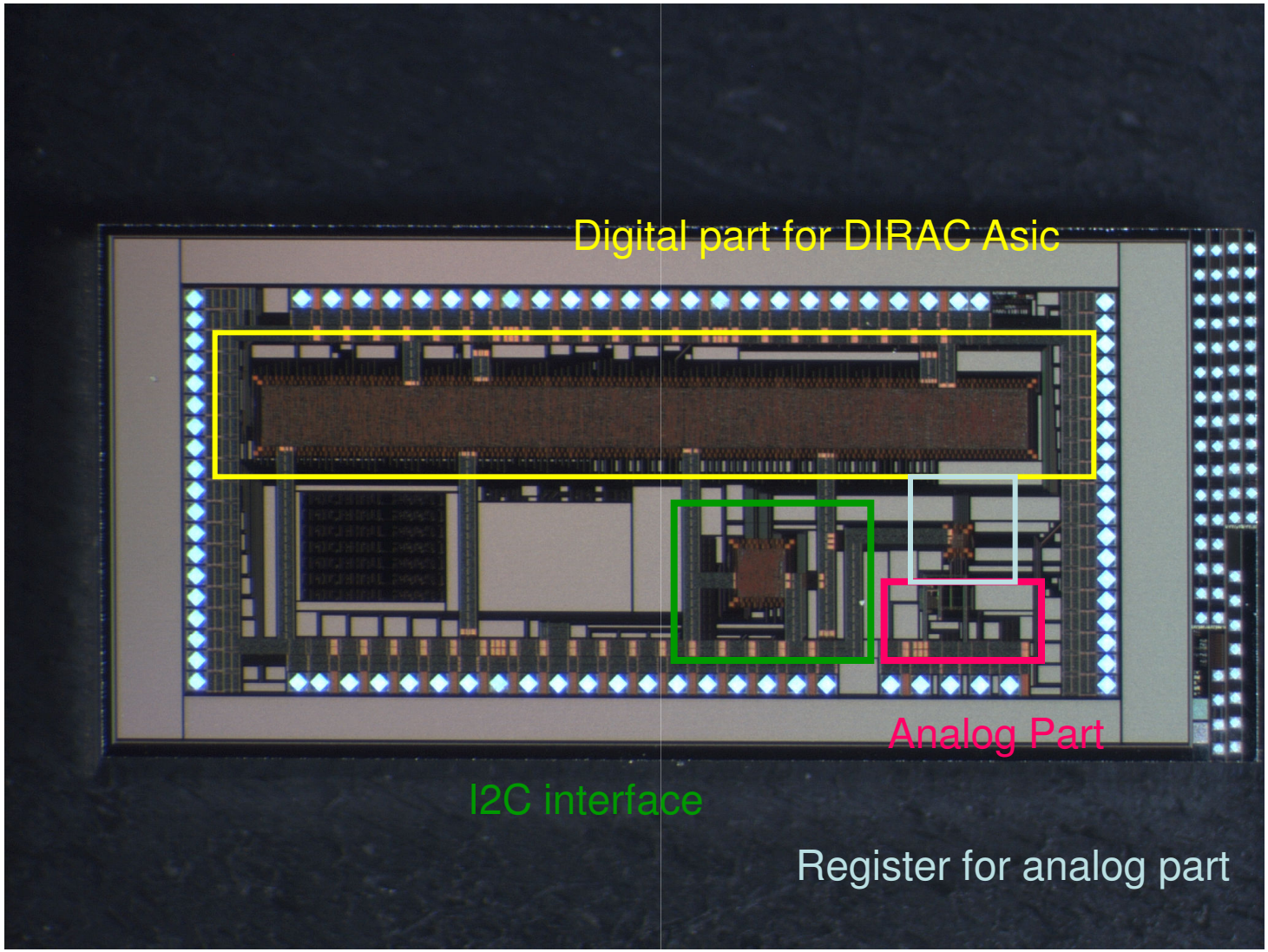
Advantages of the serial interface vs a shift register

- Individually addressed readout and slow control.
  - More flexibility for the user
  - Easier for the driver firmware design (DIF board)
- The readout of the sent parameters is possible without rewriting them.
- Easier board routing (without chips chaining).
- Less sensitive to the risk of failure propagation.

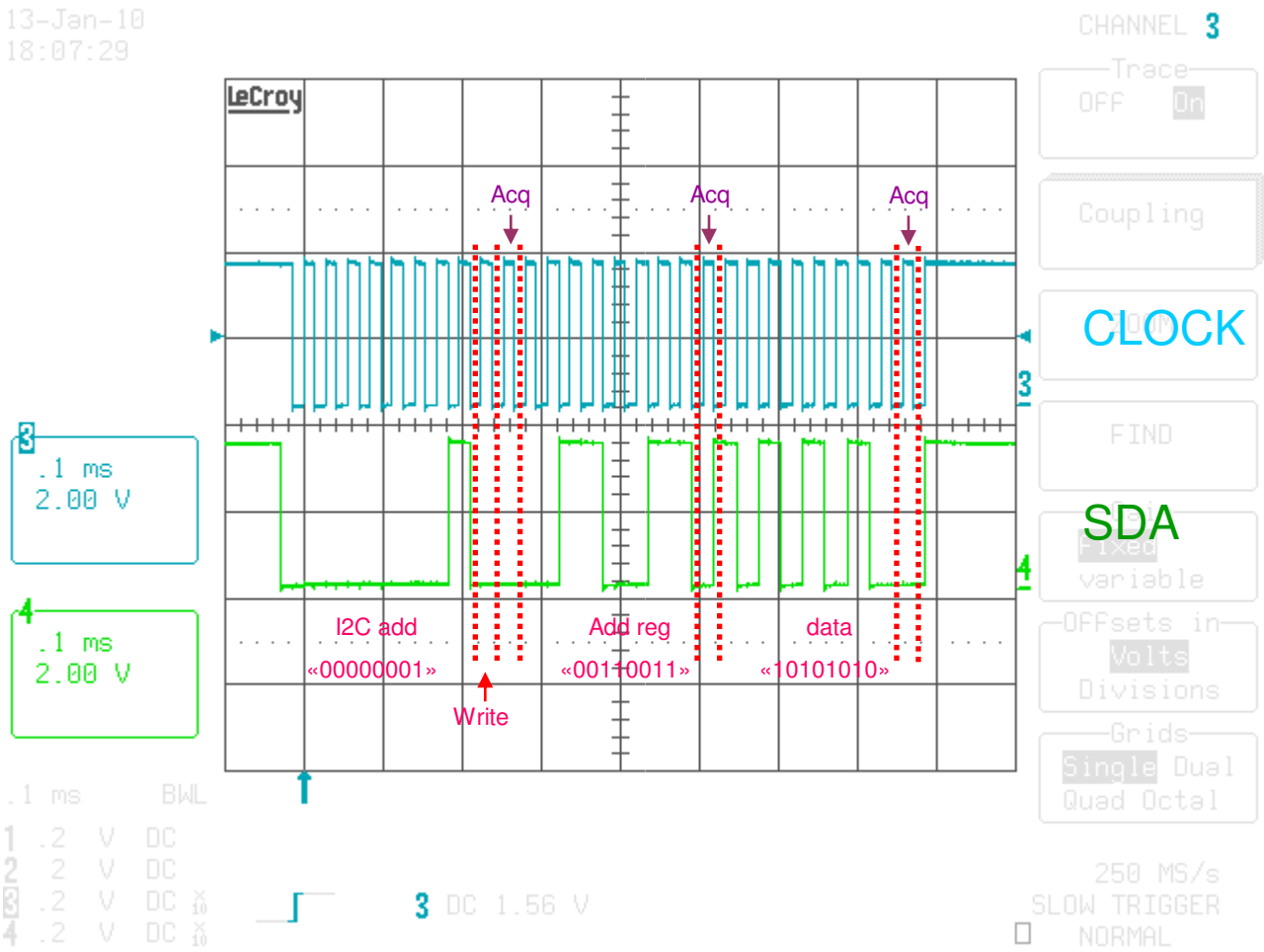
CSA for RPC/µMEGAS

- Switched integrator
- Folded cascode with feed forward compensation technique
- 4 gains (10pF 200fF 100fF 50fF)
  - 100 mV/pC, 4 mV/fC, 7 mV/fC, 10 mV/fC
- Main goal is to detect pulses as low as 2fC
- Return from fab in October 2009
  - Tests will be performed with standard comparator

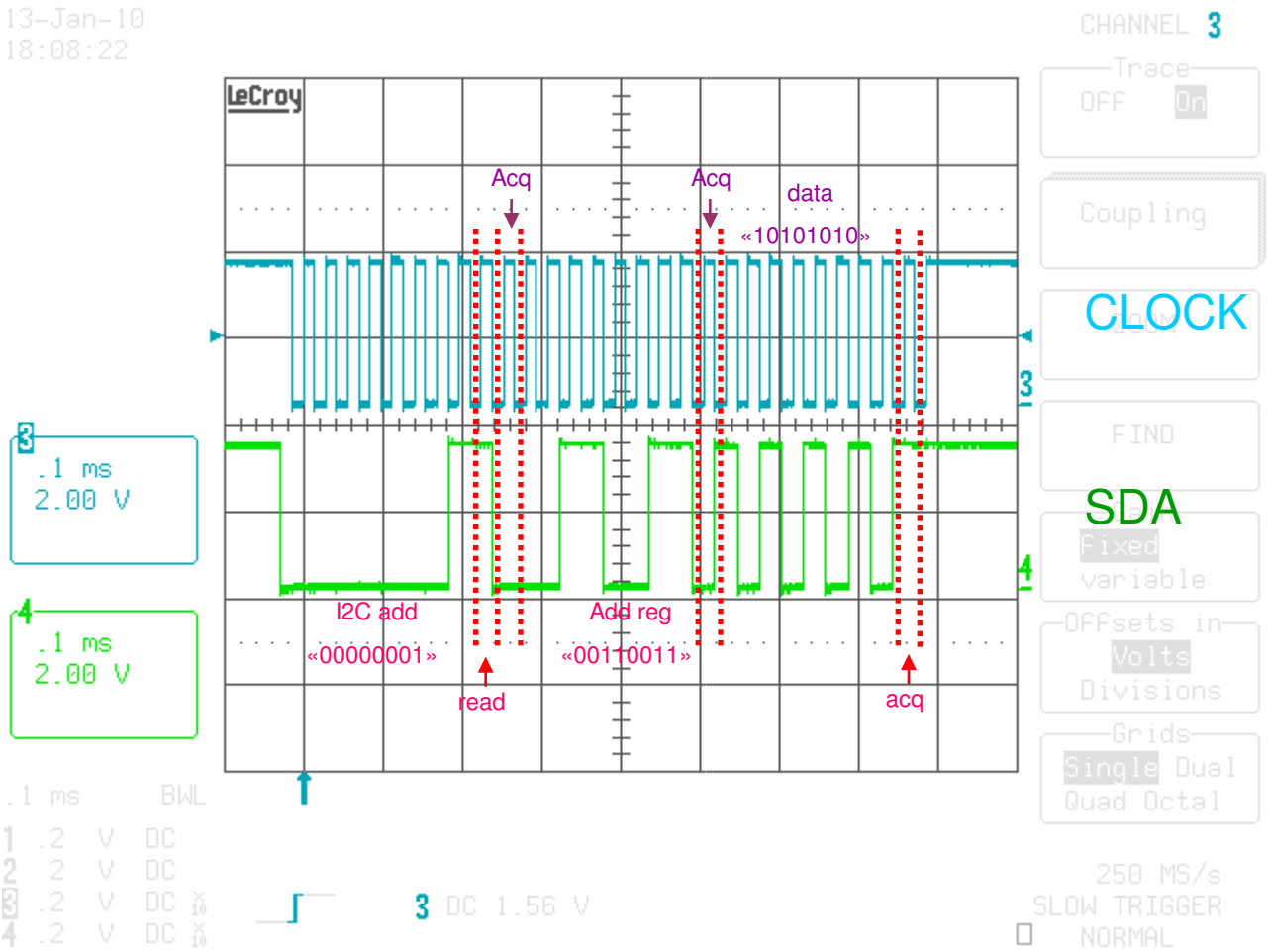
ASIC picture



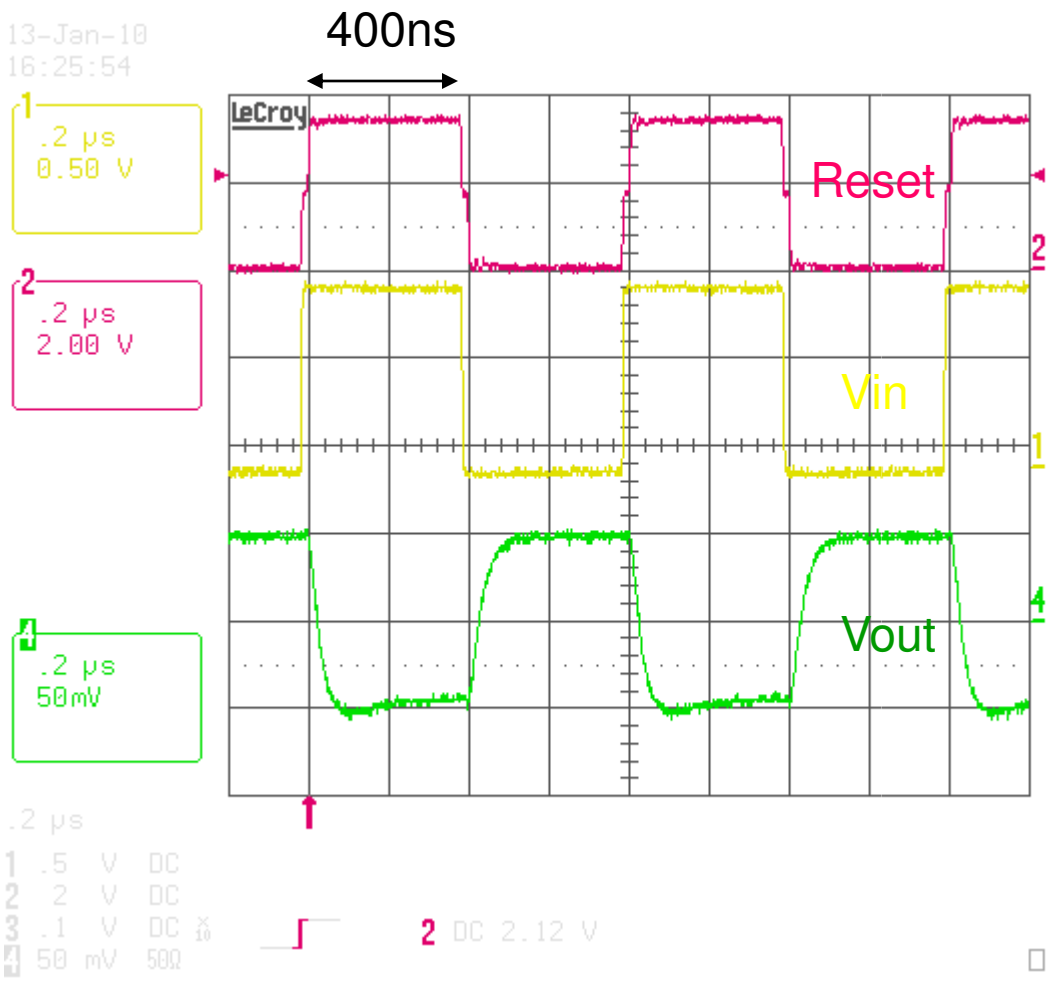
Preliminary results (Digital I2C write)



Preliminary results (Digital I2C read)



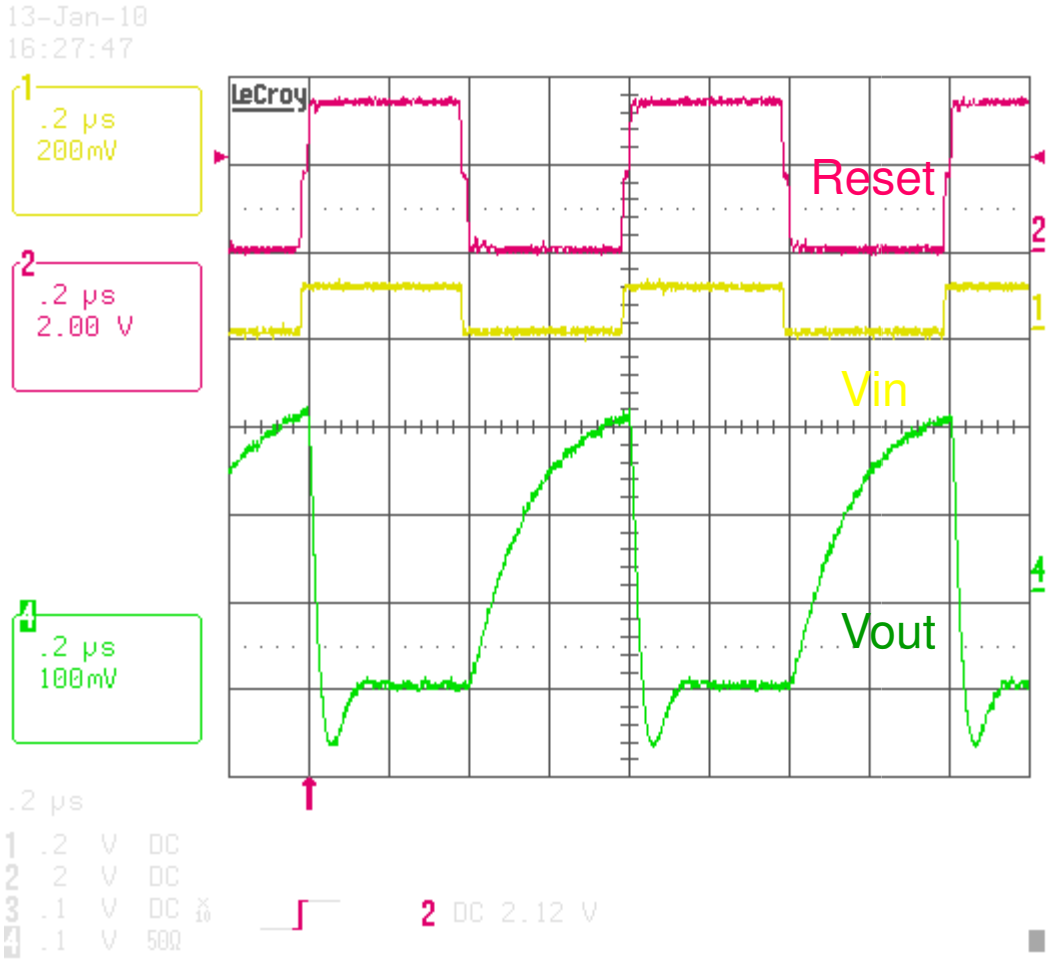
Preliminary results (analog)



Qin=1 pC
Cf= 10pF

Gconv = 100mV/pC
(same value as parasitic simulation)
Rise Time = 100ns

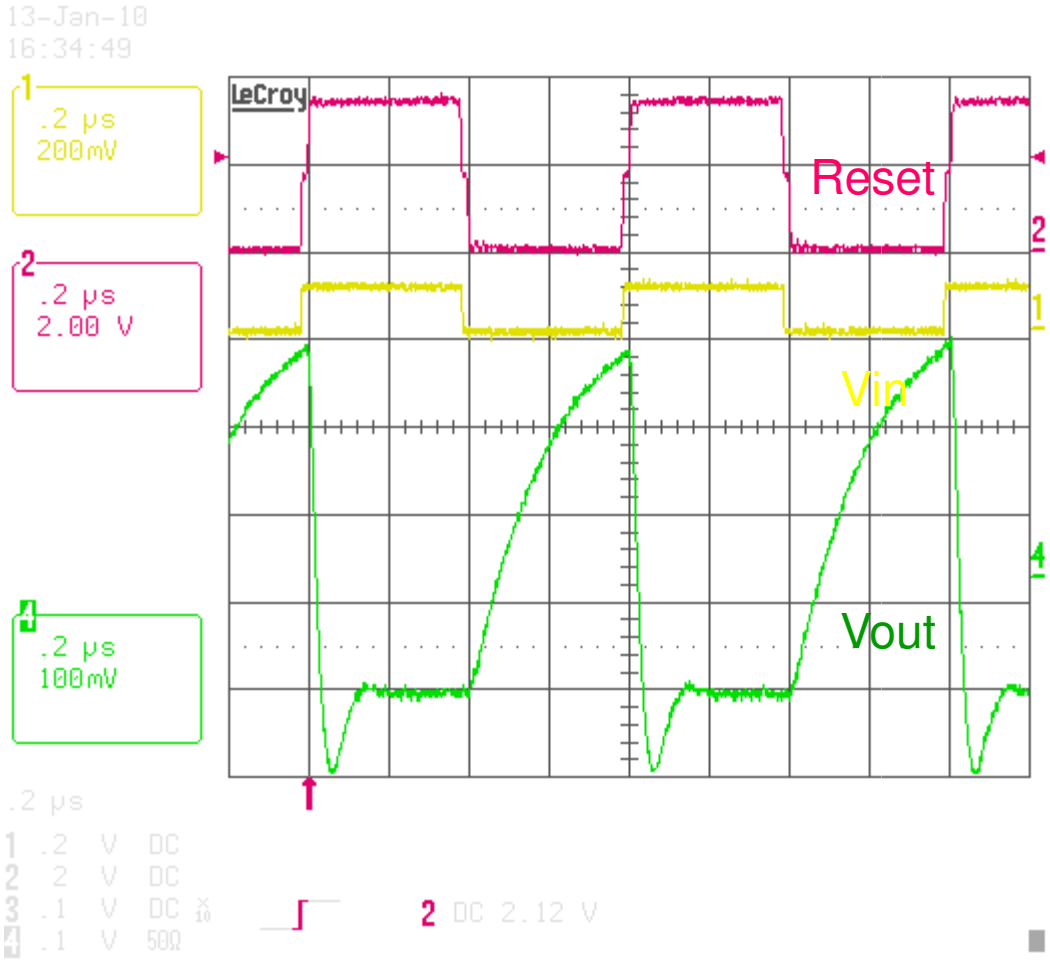
Preliminary results (analog)



Qin=100 fC
Cf= 200fF

Gconv = 3.1mV/fC
(4 mV/fC in schematic)
Rise Time > 200ns

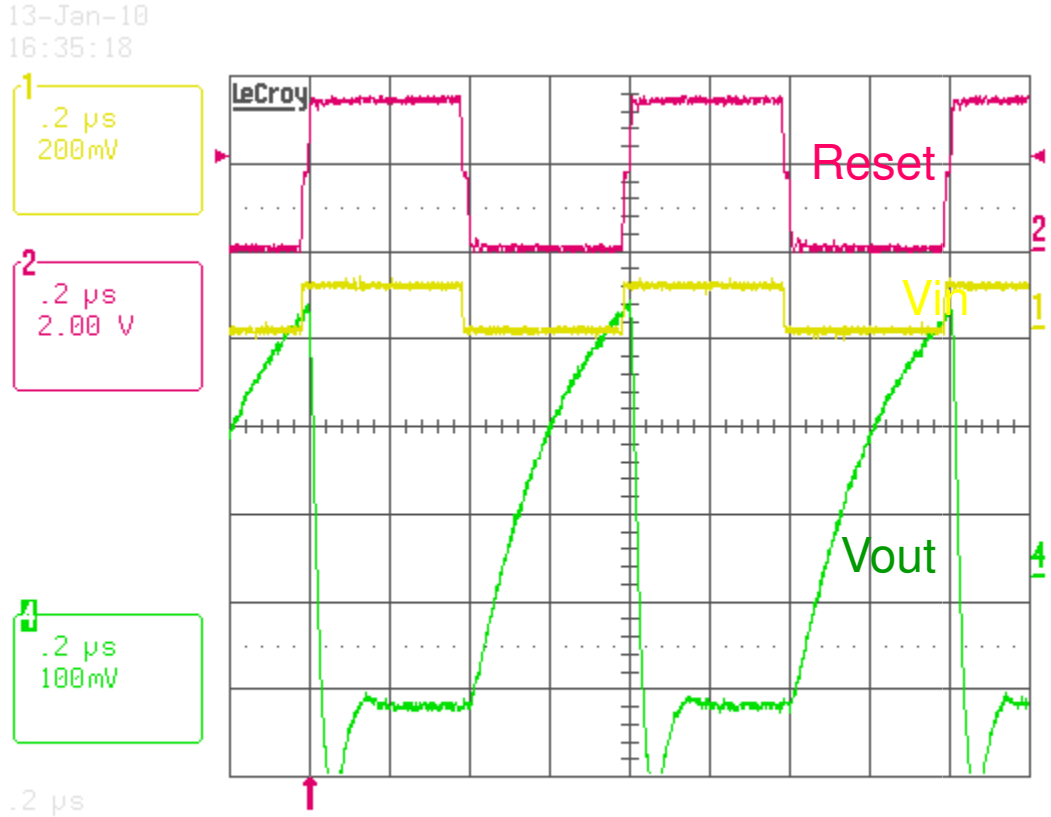
Preliminary results (analog)



Qin=100 fC
Cf= 100fF

Gconv = 4mV/fC
(7 mV/fC in schematic)
Rise Time > 200ns

Preliminary results (analog)



Qin=100 fC
Cf= 50fF

Gconv = 4.3mV/fC
(10 mV/fC in schematic)
Rise Time > 200ns

Conclusion

ASIC :

- Return from fab : October 2009
- Test is started since 1 week
  - Digital part :
    - I2C is working : CSA can be controlled by I2C
      - Power, max frequency : still to be measured
    - Digital part for DIRAC will be tested soon
  - Analog part :
    - Close to parasitic simulation (Gconv)
    - To be be measured :
      - Noise
      - Linearity
      - Minimum pulse detection with standard comparator
- In case of ILC timing the CSA must be improved
- Slow rise time could explained the minimum pulse detection

- Next step
  - Digital part can be implemented in DIRACx/HARDROCx
  - This link can be doubled to introduce redundancy (reduce risks of failure)