# DAQ Technical Update and Discussion

*Matt Warren, on behalf of CALICE-UK*

# ODR

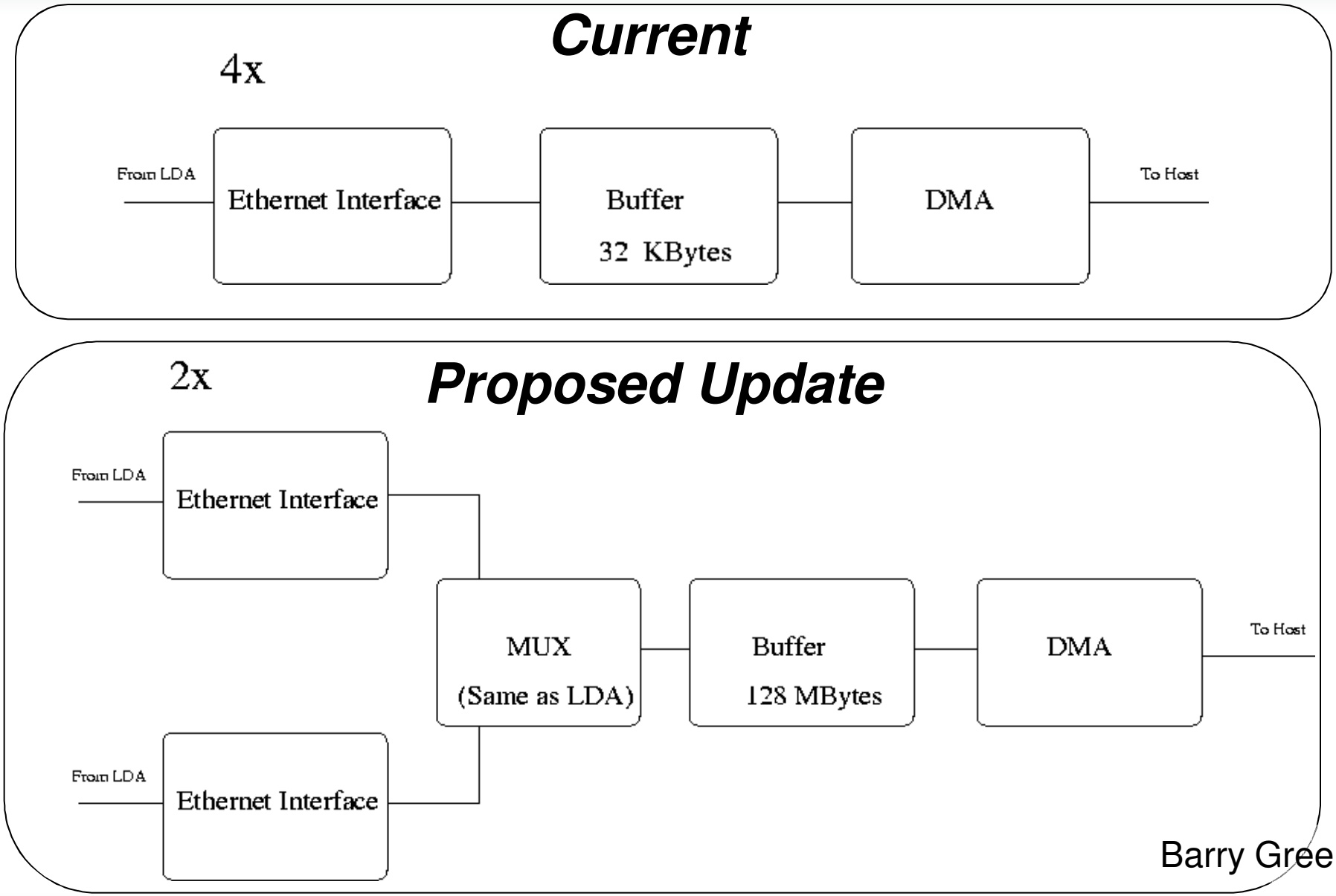
Firmware code is structured and maintainable

- Stored in CERN SVN
- Structured to cater for differing hardware
  - ODR v1 (125MHz) and v2 (250MHz)
  - Opto plug-ins v1.0 and v1.1 (differing pinout)
- Modular - PCIe, Ethernet, Core blocks synthesised separately
- Xilinx tools used for build

Still to do

- v1.1 opto plug-in firmware – SFP_HSI - 3 more fibre ports (2 in use)
  - Pinout has changed from original version
  - Now uses MGTs in both MGT clock domains - makes modular build difficult
  - Investigating options - may need to use 3rd SFP
- Auto-neg for the Ethernet module - already have code, needs integration
- Use the larger DDR2 memory on board system (buffer increase) - see next

# ODR – Updated Hardware Structure(1)



# ODR Updated Structure (2)

Advantages:

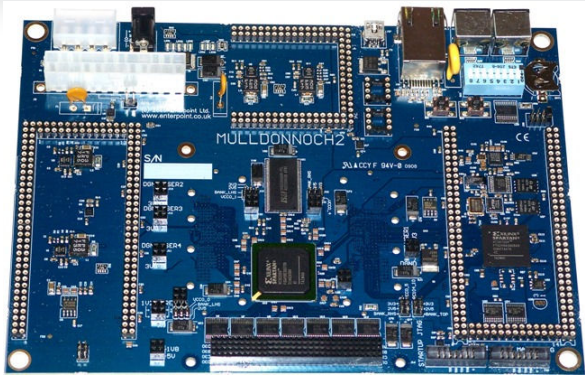
- Greater Buffering means inter-spill gap can be used to continue to write data to storage
- More ODRs (& LDAs & DIFs etc.) per PC

Status:

- 80% Complete
- DDR2 Interface implemented
- Need to connect in place of small buffer

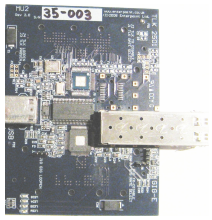
# LDA (1)

LDA comprises 4 boards(!)

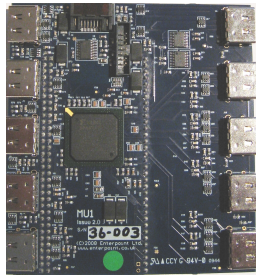



- LDA Baseboard: Enterpoint Mulldonnach2 development board

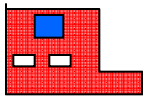
- Ethernet: Add-on with a GigE chipset + SFP cage



- HDMI: Add-on with 10x HDMI connectors + FPGA for connectivity



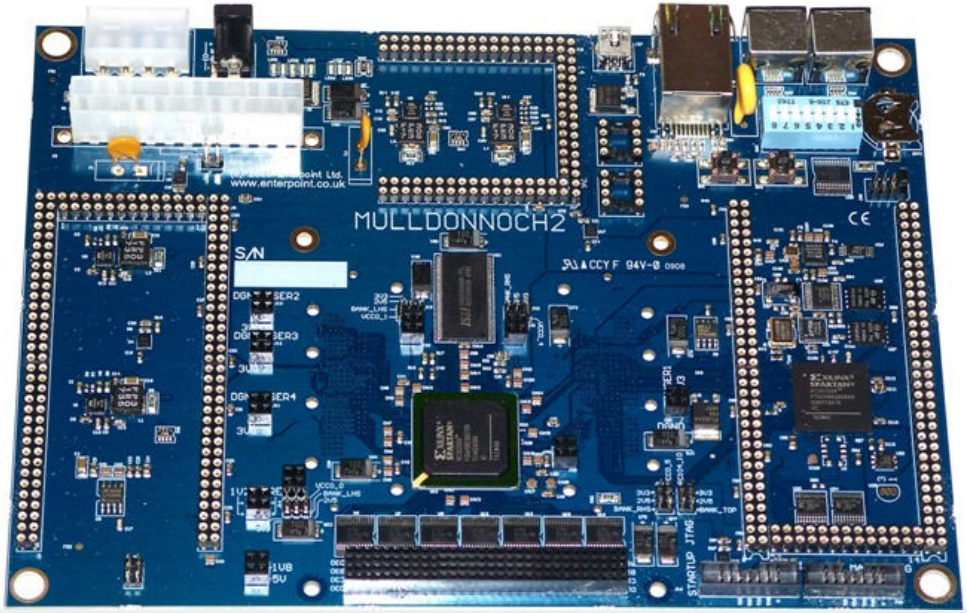
- CCI: Add-on Clock & Control Interface with HDMI receptacle



# LDA (2) – Baseboard

Firmware mainly working (Passes all the tests we can do):

- DIF link stable
- Can send fast commands to the DIF from PC
  - Packet sent from PC
  - LDA decodes and turns into fast command K + ID
  - LDA distributes to DIFs
- Data from DIF is transferred to PC
  - Packets from DIF are wrapped in Ethernet headers and sent to PC
- Internal control registers functional
  - Enable disable links etc.
  - Send test data to PC

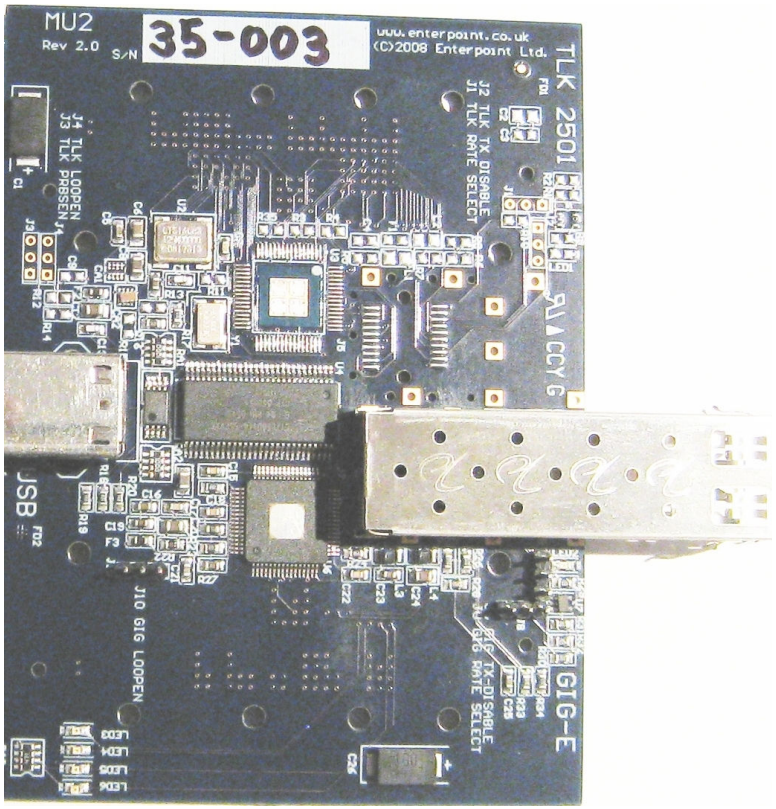


# LDA (3) – Ethernet

Prototype boards work, BUT

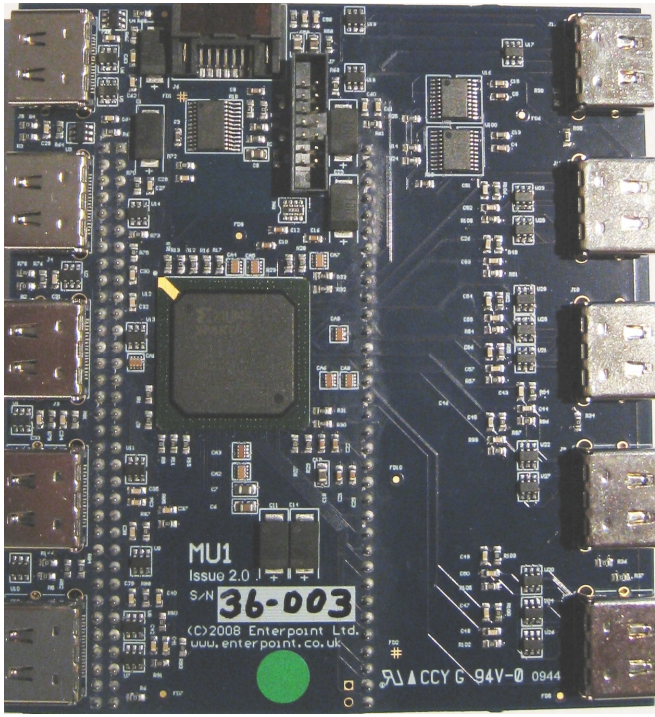
- Need pair of terminating resistors added - not easy

- New boards work
  - have pads for these resistors, which we easily fit



# LDA (4) – HDMI

- Old boards have no AC coupling and HDMI connectors were wired backwards
- New boards have a new FPGA
  - was 3S400, now 3S1500
  - likely have same pinout, but waiting on details from manufacturer
- Still untested

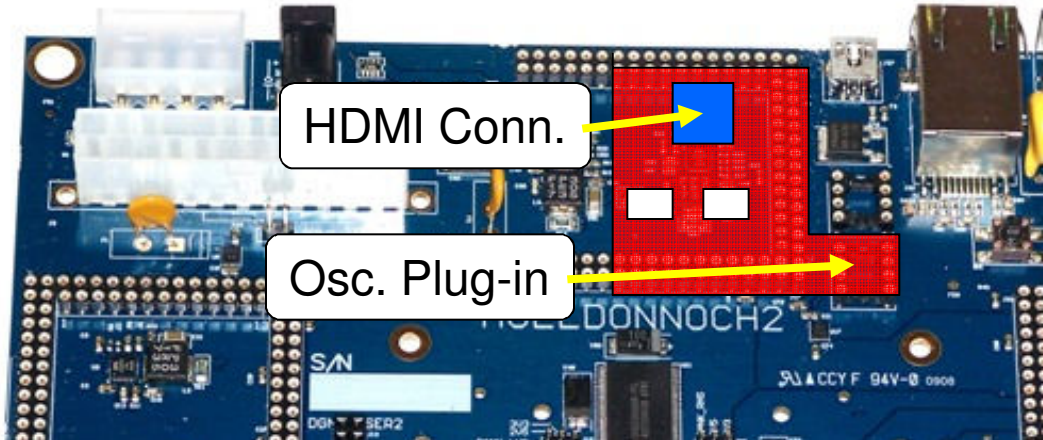


# LDA(5) – Clock & Control Interface

Small and simple board, provides:

- AC coupled connection to CCC
- LDVS to single ended (and vice versa) buffering of all HDMI signals.

- Clock feeds into LDA via osc connector
  - Because no FPGA clock pins on most convenient connector
- DC design tested OK using existing HDMI-LVDS test hardware with LDA



# DIF

New hardware passes all our tests

- Test firmware checks ALL connections
  - HDMI
  - flash RAM
  - USB
  - connections to the ASU
  - DIF-DIF linkLink to LDA working
- Link is negotiated and the stable (sending 'idles‘)
- Fast command decoder works
- Data generator works
- Fast command from PC/ODR/LDA initiates sending a packet to the LDA/ODR/PC

Still to do:

- Plenty, but UK funding situation is a problem – we stop at the LDA link
- This means we have testing LDA->DIF data transfer left to do

# CCC

Working

- fans-out clocks, fast commands and control signals
- fans-in busy
- simple RS232 control

Still to do:

- The idea is that the CCC can plug into both the LDA and DIFs
  - AC coupled signalling
  - LDA-DIF link in the CCC.
- BUT the CPLD on the CCC is too small, so a work-around is needed.
  - Possibly hard-code a few 8b/10b strings into the CCC firmware and serialise them as needed.
  - Not sure if the idles need to be sent ...
  - May exceed our manpower in the UK

# System Test

- ODR test software sends hardcoded packets to the LDA
- Returned data feed a network card in a PC
  - Viewed using wireshark.

Still to do:

- Multiple DIFs on an LDA
  - address different DIFs
  - Broadcast
  - receive data from  multiples difs in the FPGA
    - Tests fifo/multiplex on LDA
- Multiple LDAs in a system
  - multiple ODR streams active (async/concurrently)
  - needs decoding/sorting test software
- Connect CCC to all LDAs
  - common clock, synchronous trigger

Discussion …