DCC board status

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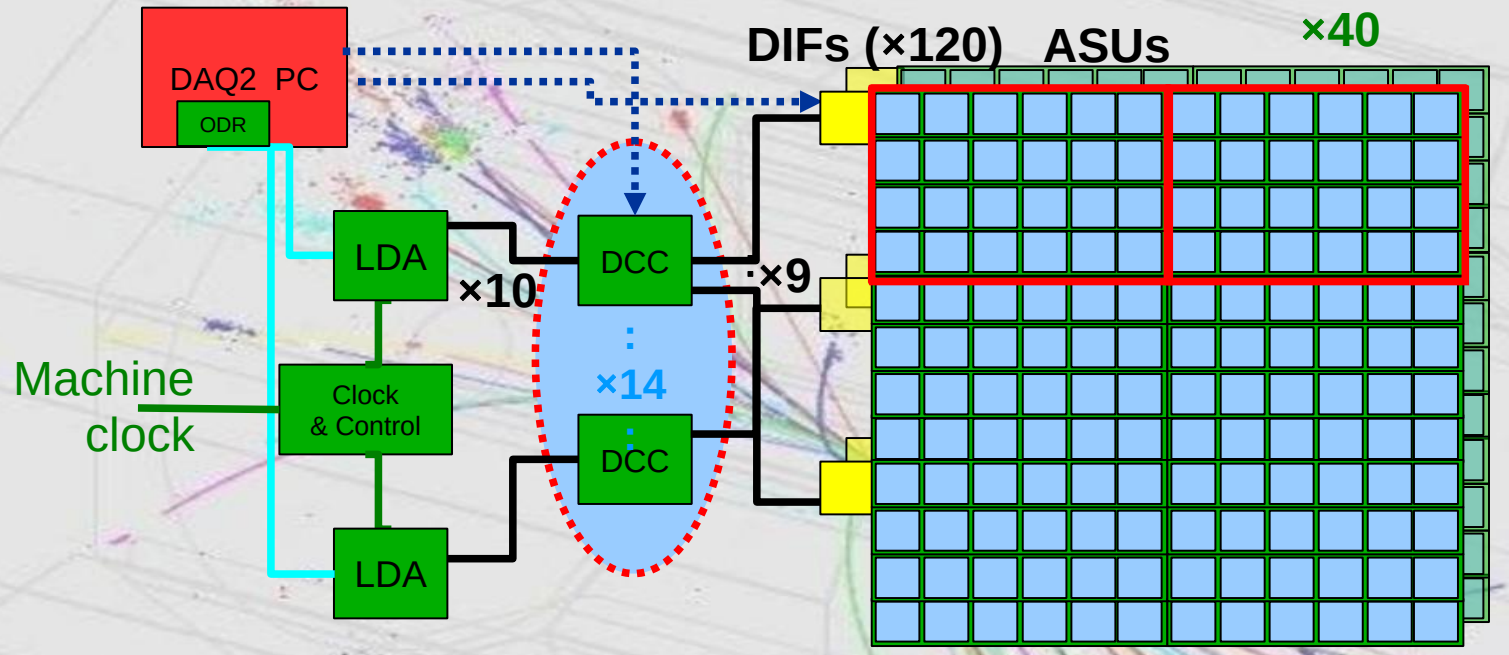
DAQ overview



Digital (Config, Control, Data, trigger, spill) over HDMI

Clock & Sync over HDMI

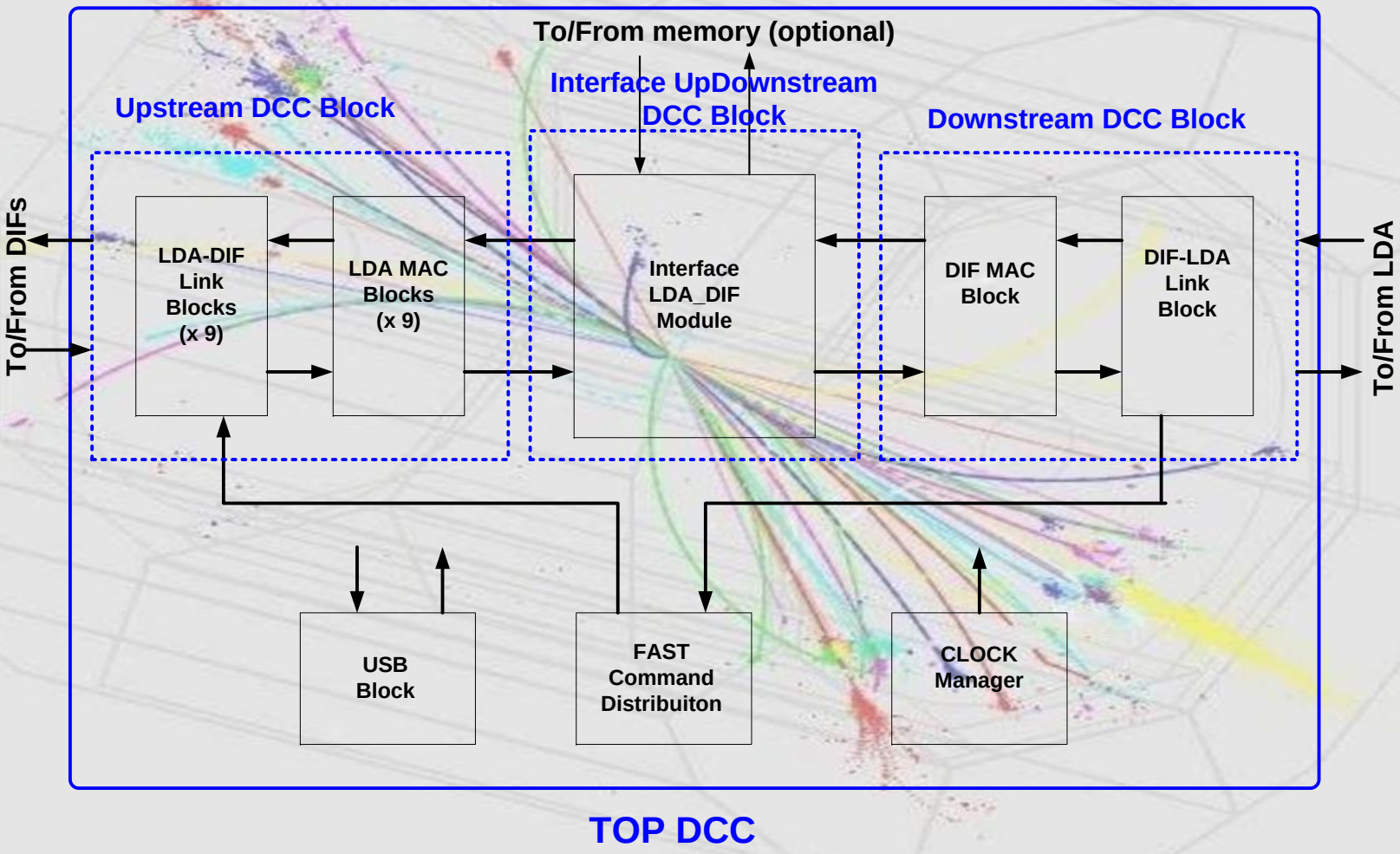
Optique GigE

Debug USB

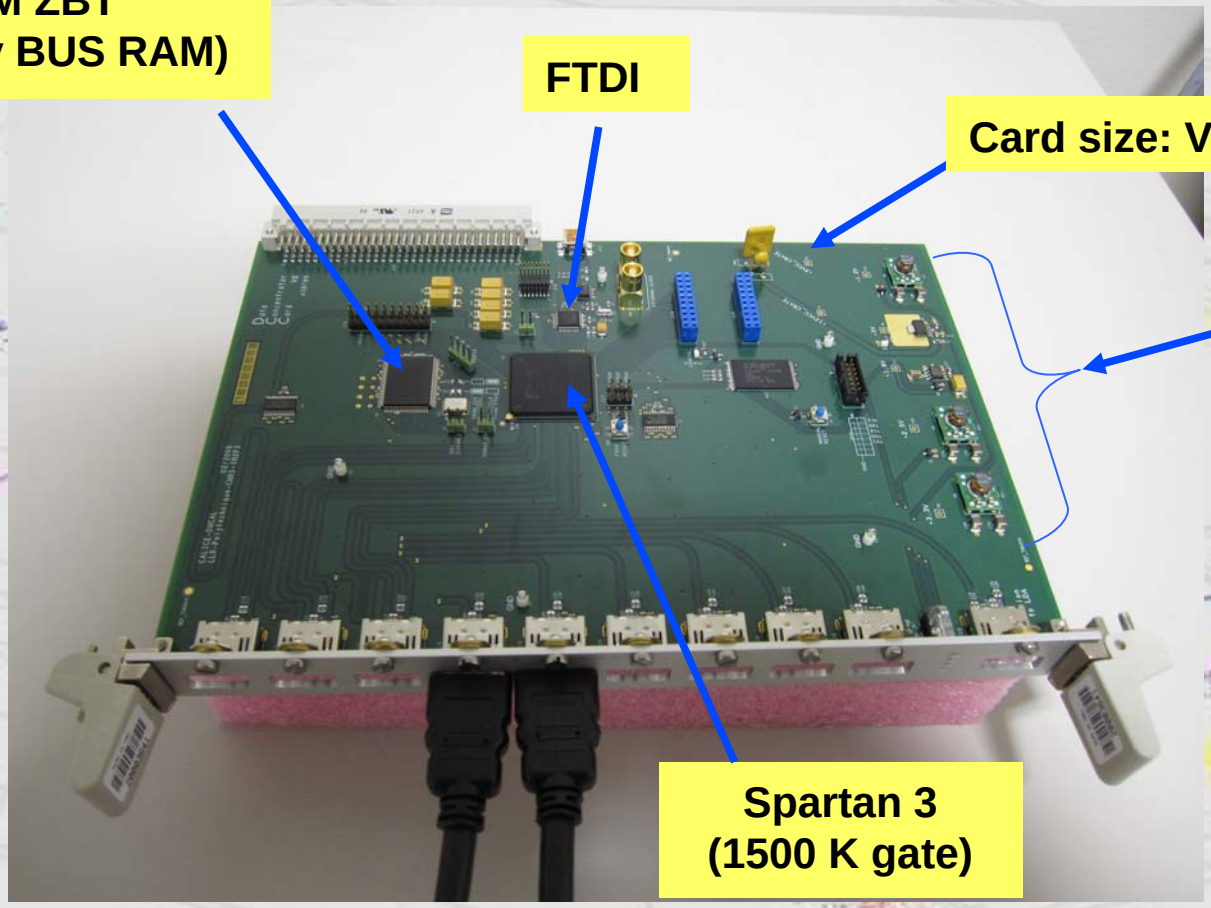
120 DIF → 12 LDA → 4 ODR

120 DIF → 14 DCC → 2 LDA → 1 ODR

FPGA architecture by functionalities



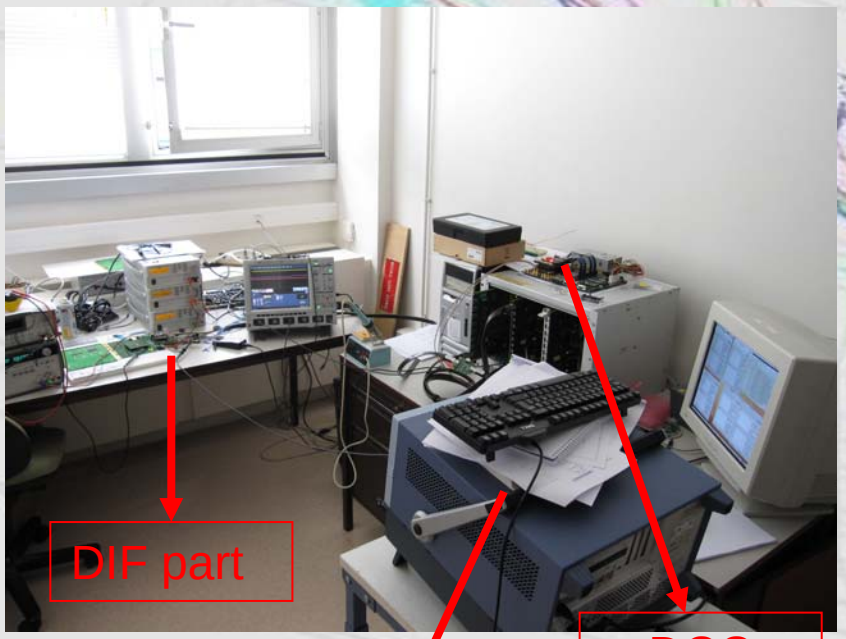
DCC prototype



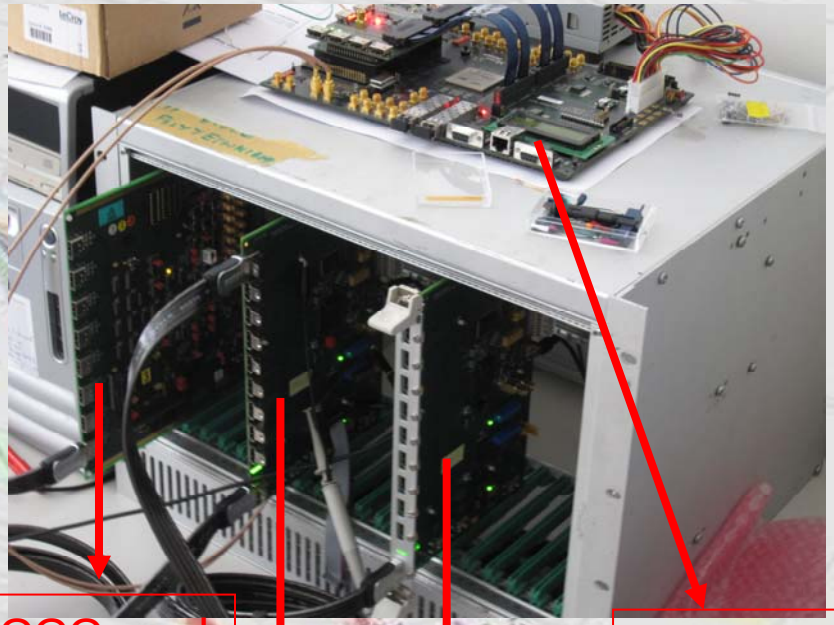
Test bench at LLR

Remark : All test are made via USB access

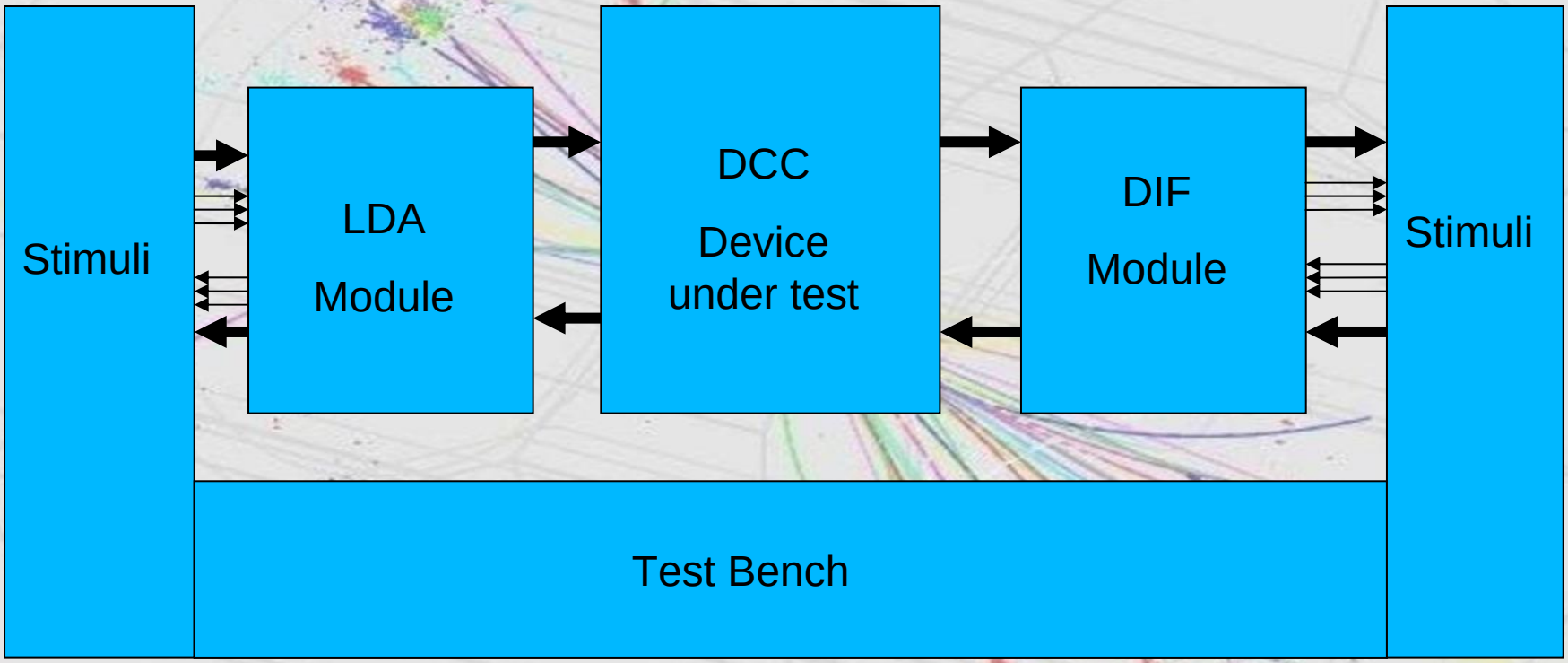
Test Bench overview



CCC & DCC Chassis



VHDL Test Bench

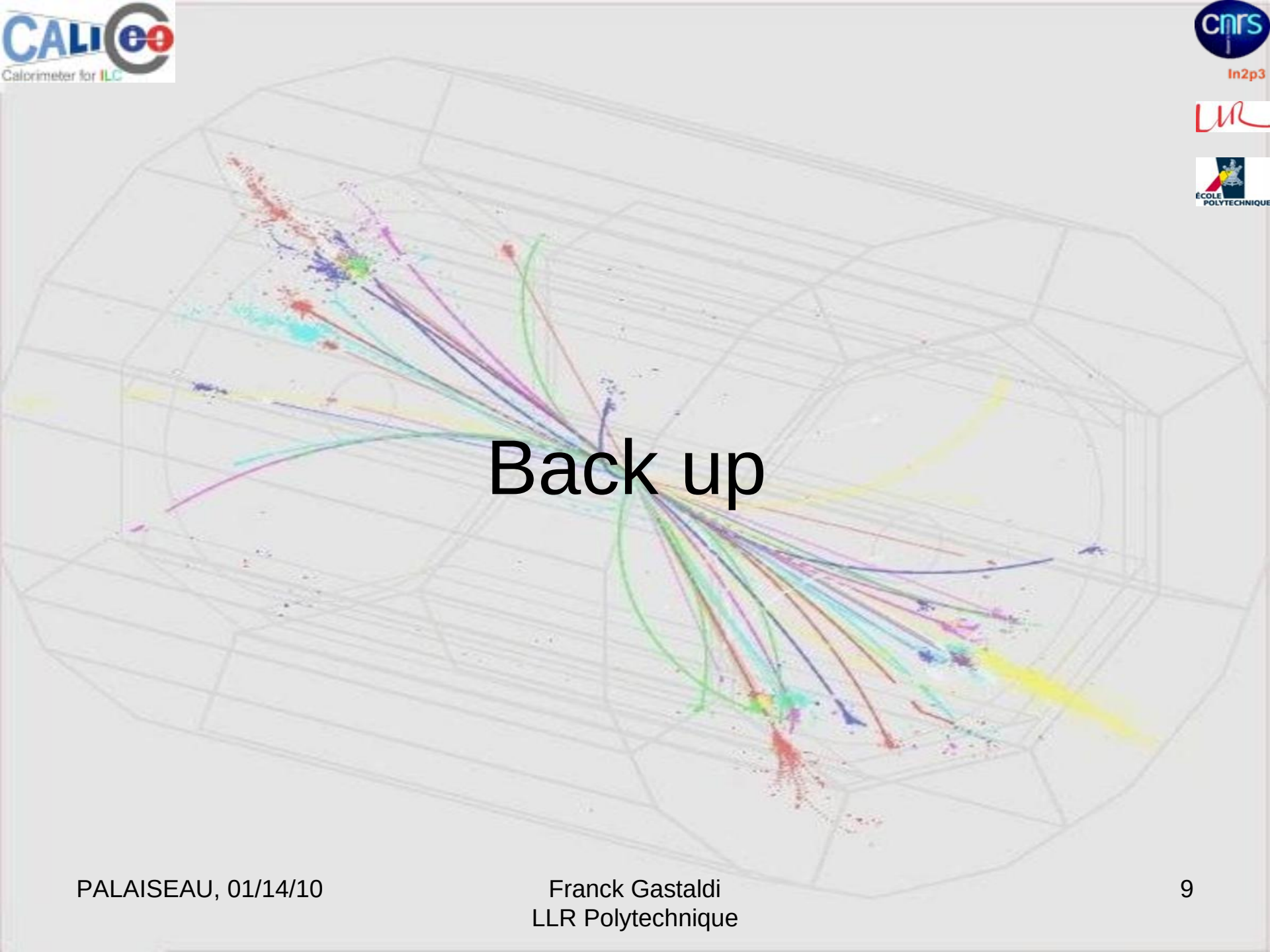


VHDL Blocks

- All VHDL blocks are designed
- Some bugs are resolved or they will be it
- The prototype card can read up to 4 DIFs
- Some problems are meet for the block transfer from LDA with more one channel
  - The simulation works correctly up to “placement and routing” and is corrupted for the full-timing simulation
  - After some analysis on the timing report, it would seems that some net have a hold time violation.
  - The next days will be dedicate to resolve this violation.

Conclusion

- Next days : priority to resolve the timing violation
- Until to the DCC production:
  - Tests & validation of VHDL code implemented on the DCC
  - Improvement of DCC card (layout) before production
- DCC Production:
  - February 2010 : PCB production
  - March 2010 : PCB cabling
  - April – July 2010: tests at LLR
    - Test of Multi-channel on the DCC
    - Test of a real DAQ Chain (LDA,DCC,DIF)
- Full DAQ : estimated for summer 2010



Back up

Everything is resumed here

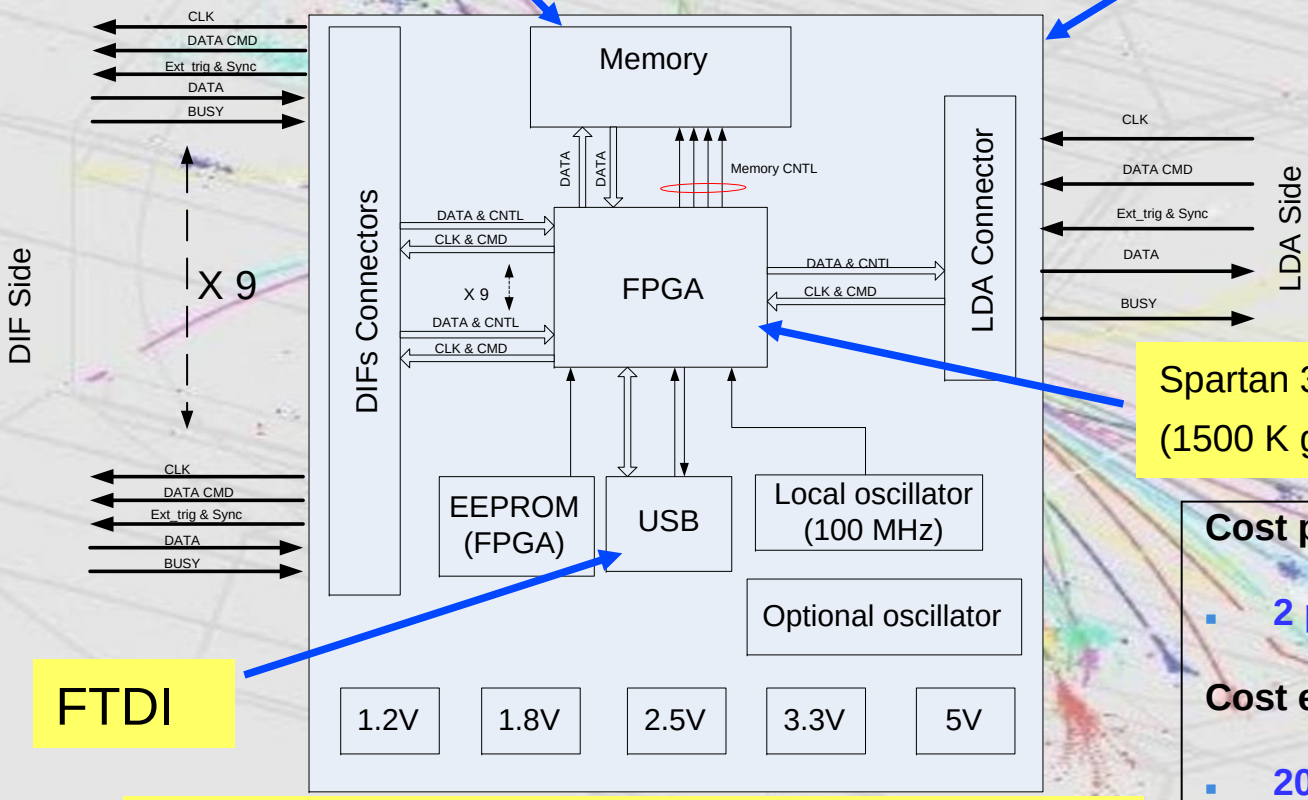
- Main specification :
  Reduce the number of LDA and ODR for the DHCAL & optimize the data flux
- Without DCC :
  3 Difs/layer (40 Layers)
  10 Difs/LDA => 12 LDA and 3 ODR
- With DCC, we need :
- 9 DIFs/DCC => 14 DCC => 2 LDA and 1 ODR
- Characteristics :
  - To be transparent between DIF and LDA
  - Broadcast all fast commands from LDA to all DIFs
  - Send the packet R/O one after the other
  - Read 9 DIFs (objective)
  - Availability of USB access
- Firmware : Re-use as far as possible existing VHDL blocks (Marc)
- Homemade card
  - Cheaper: objective (max 600 € /card) for the production

Card overview

16×1M ZBT
(no latency BUS RAM)

DCC

Card size: VME 6U



Spartan 3
(1500 K gate)

FTDI

Cost proto I:

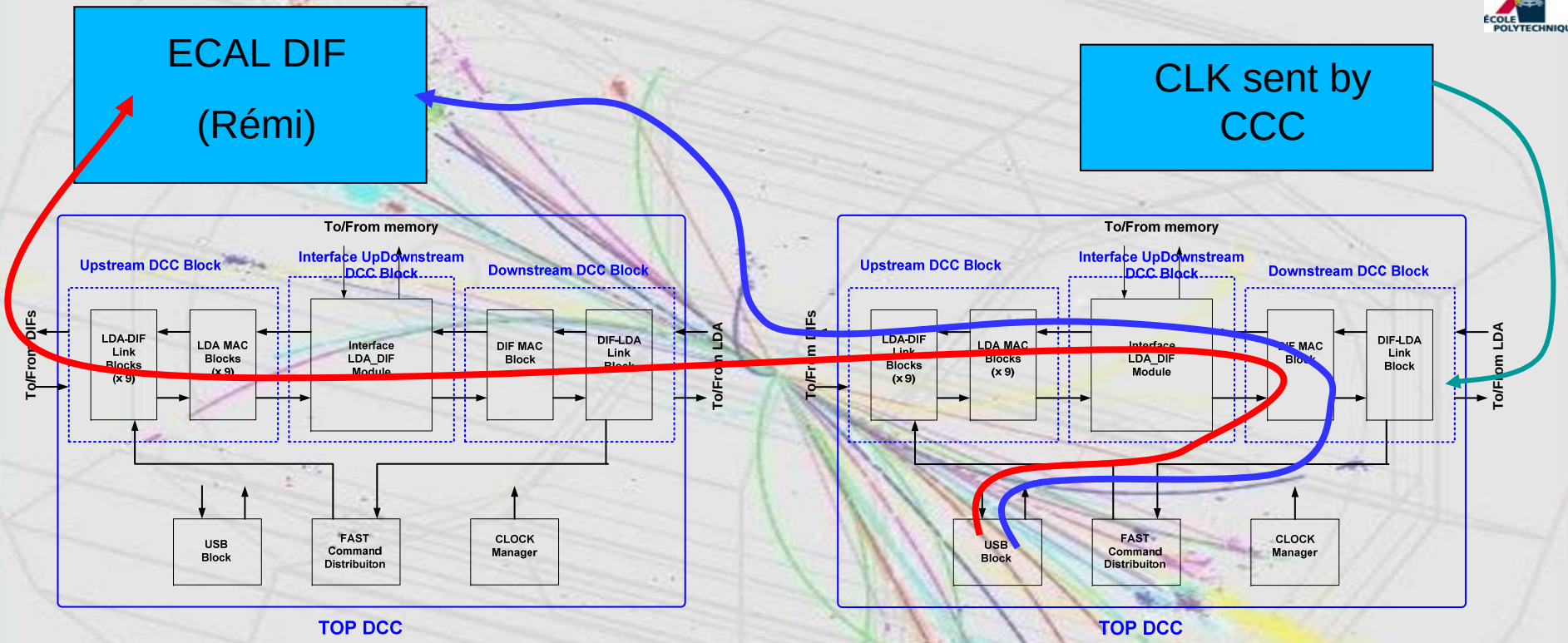
- **2 protos: ~ 1900€/card**

Cost est.:

- **20 prods: ~600€/card**

Est: 1.2A 10mA 400mA 2.25A 30mA

Test with two DCC and one DIF



Link DCC(LDA) to DCC (full) to DIF via USB

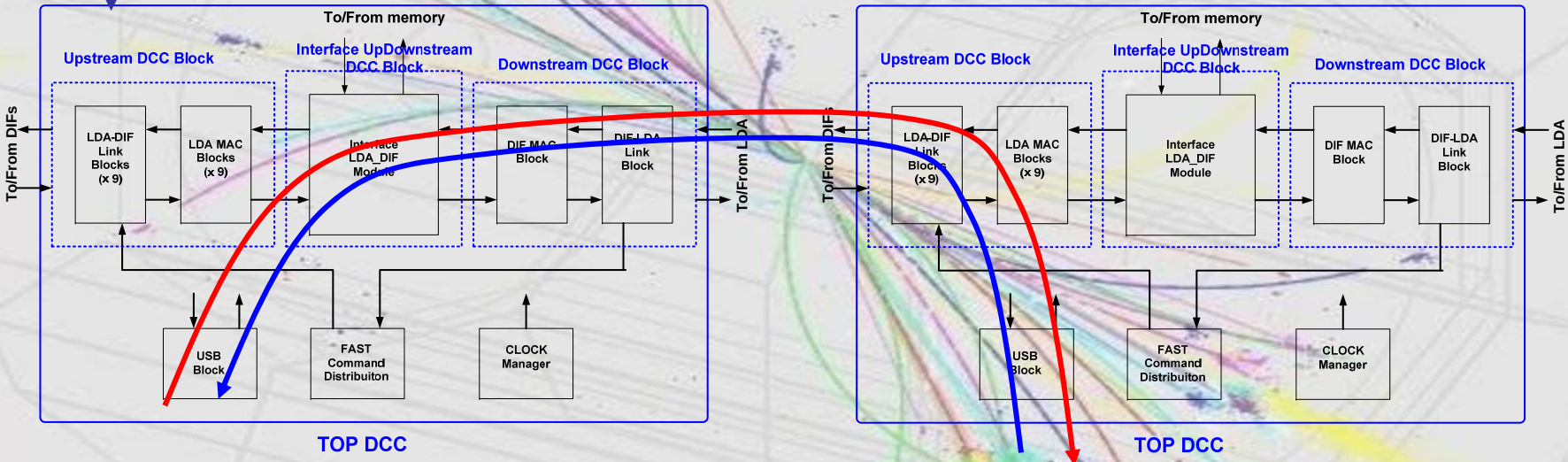
Link DCC(LDA) to DIF via USB

Test with two DCC

CLK

sent by the CCC

Everything is controlled via USB
Data sent by the DCC (Lda) or DCC (Dif) and controlled by a probe on serial link
Serial data decoded with a serial data analyzer



Link DCC(LDA) to DCC(DIF) via USB
Link DCC(DIF) to DCC(LDA) via USB