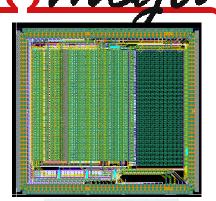


Orsay Micro Electronic Group associated

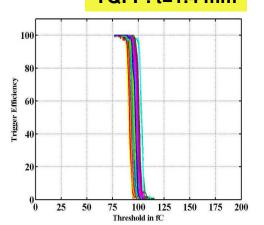
### HaRDROC status

- 400 chips HARDROC2 produced in june 2008 to equip 24-chip RPC and Micromegas PCBs for square meter
  - 3 thresholds (0.1-1-10 pC)
  - Power pulsed to 5-8 μW/ch
  - Package TQFP160
  - Some difficulties loading Slow ControlSOLVED in HARDROC2B
  - Readout and DAQ2 validation
- 200 HARDROC2B received in dec 09
  - Ready to equip one RPC prototype
  - Final for production : see PRR tomorrow
- Full production run: in 2010
  - See talk by N. Seguin-Moreau



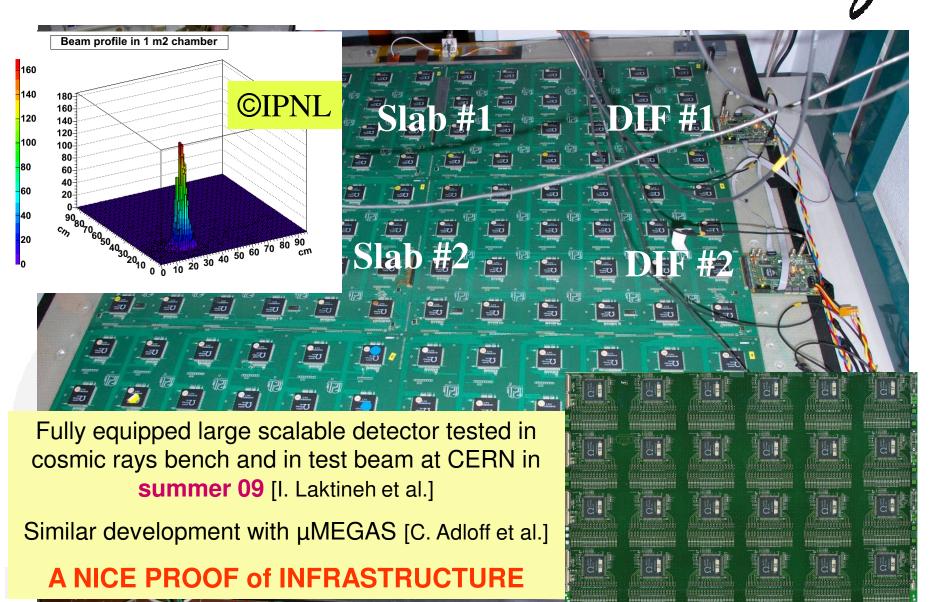


**TQFP: t=1.4 mm** 



# Towards DHCAL technological prototype



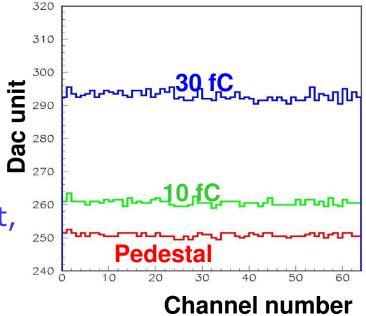


## Remaining issues

- Full detector test with power pulsing
  - Tests on going at Lyon
- Not optimized for micromegas
  - Late information on signal amplitude and speed (150 ns)
  - => Thresholds around 2 fC
  - => sslower "fast" shaper needed
  - => High voltage protection
  - Needs charge preamp
- Performance with detector :

See talks by C. Combaret, C. Drancourt,

H. Mathez,



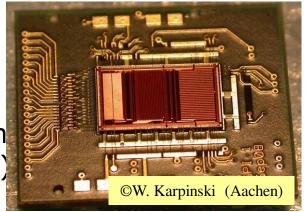
#### SPIROC status

- Omega
- 50 chips SPIROC2 produced in june 2008 to equip AHCAL and ECAL EUDET modules
  - Fulfiled EUDET milestone
  - Package TQFP208 (w=1.4 mm)
  - Difficult slow control loading (cf HR
  - Measurements (slowly) coming in
  - Complex chip
  - Collab LAL, DESY, Heidelberg
  - See talk by M. Reinecke



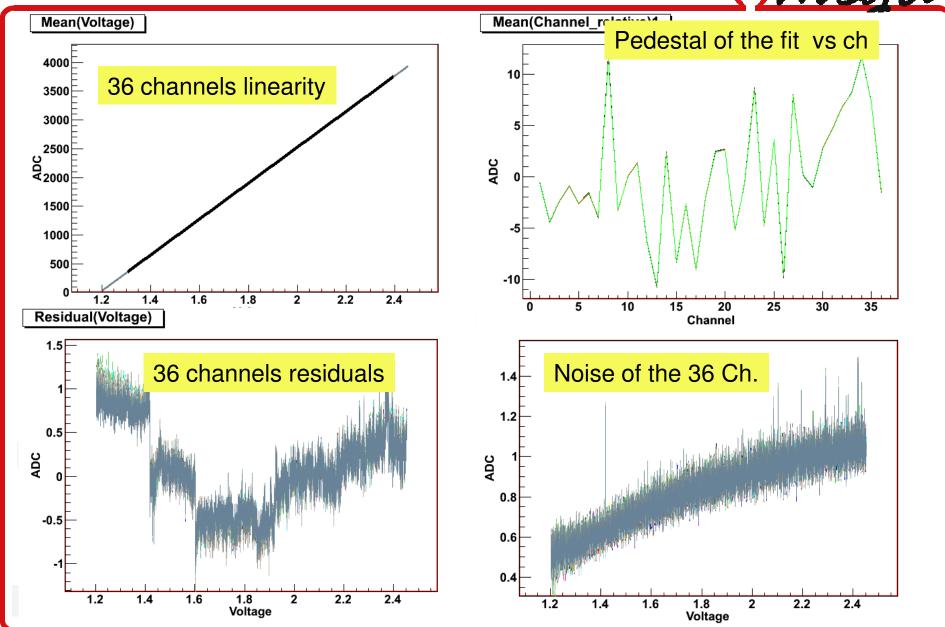
### External users :

 astrophysics PEBS (Aachen), medical im Pisa, Valencia...), nuclear physics (IPNO) (Napoli)

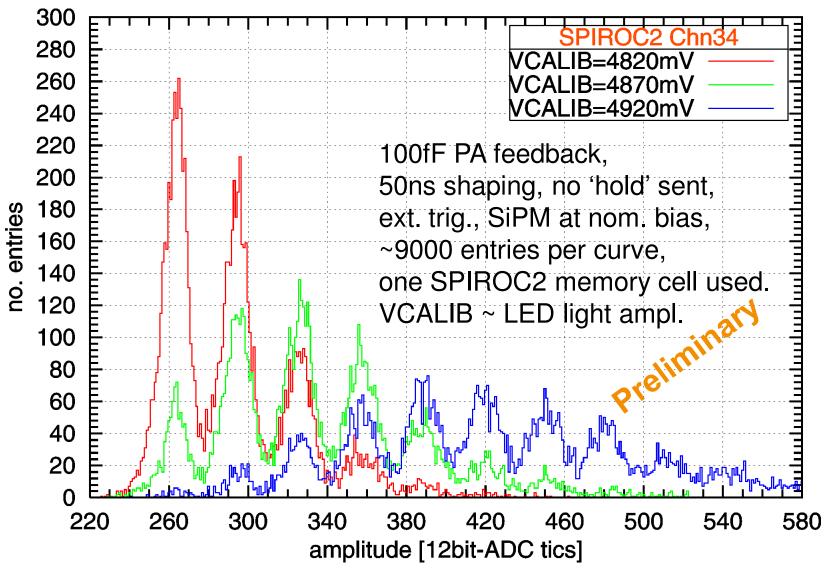


# Internal 12-bit ADC performance





## Single-Photon Peaks I



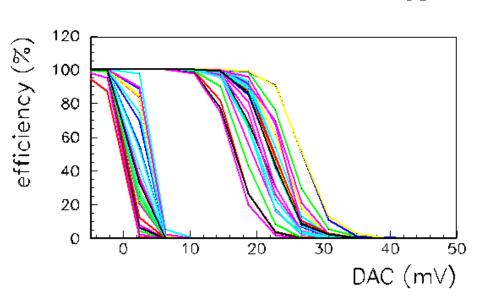
# Spiroc pending issues

Omega

- Autotrigger mode
- Linearity
  - Tests by Riccardo
- Power pulsing
- Time measurement



- SPIROC2A
- SPIROC2B



#### SKIROC status



- SKIROC1 useless with detector (no readout)
- SPIROC2 used as SKIROC emulator
  - 95% identical to SKIROC (only preamp differs)
  - 36 channels instead of 64
  - Limited dynamic range (~500 MIPs)
  - Tests starting with FEV7 to address embedding issues
  - Noise tests on testboard proceeding (ENC ~ 1 ke-)
- R&D will continue within CALICE
  - SKIROC2 to be submitted with production run
    - 64 channels
    - Very large dynamic range: HG for 0.5 to 500 MIP, LG for 500 to 3000 Mip
  - Simulations are on going
  - Expensive ASIC (70 mm2 = 70 k€) => MPW not worth it

### ECAL board: FEV7 with SPIROC2

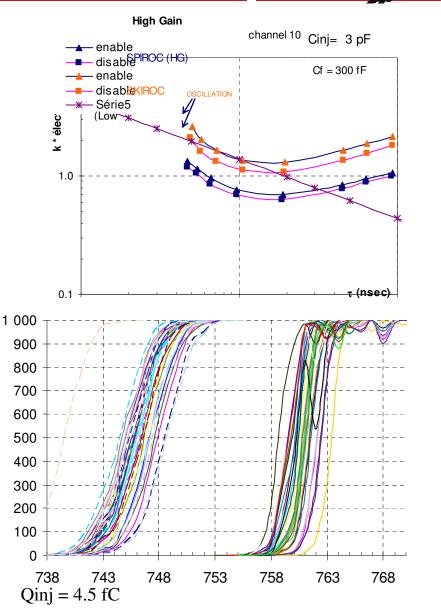
- Omega
- Version 1: June 2009, with packaged chips (TQFP 208) for the U structure (3mm available for the electronics)
- Version 2: September 2009, with COB: see talk by S. Callier
- SPIROC2 used in SKIROC mode



### SPIROC in SKIROC mode

mega

- Measurements on test board
  - Preamp noise
  - S curves
  - Noise: 0.5 fC
  - MIP = 4fC
- See talk by M. Cohen-Solal

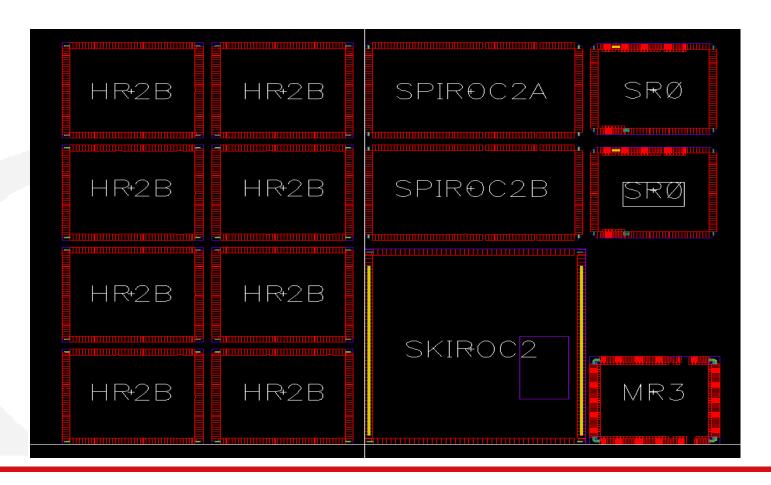


14 jan 2010

CdLT: electronics overview LLR EUDET meeting

# Engineering run: feb 2010

- Omega
- Reticle: 22 x 18 mm2, 50 reticles per wafer
- 25 wafers produced (cost: 150k masks + 100k wafers)
- 1250 chips of each type



### Conclusion

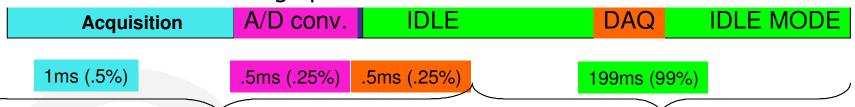
- Omega
- Production run coming up very soon : feb 2010
  - Chips (bare dies) expected may 2010
  - Selective dicing + packaging to proceed



## Test beam with technological prototype



- Data rate (Spiroc/Skiroc): naive estimate
  - Volume: 36ch\*16sca\*50bits=30 kbit/chip
  - Conversion time :  $16*100 \mu s = 1.6 ms$
  - Readout speed 5 MHz (could be increased to 10-20 MHz)
  - 8 chips/DIF line (one FEV only)
  - Total: 1.5ms + 30000\*200ns\*8 = 50 ms/16 events = 3 ms/evt=> 300 Hz during spill



- Overall readout rate
  - « Add » 1-10% power pulsing : 3-30 Hz effective rate
  - Pessimistic as assuming all chips full
  - interesting tests to be done
- Note: readout electronics designed for ILC low-occupancy, low rate detector ≠Testbeam!!

# Read out: token ring

mega Readout architecture common to all calorimeters Minimize data lines & power Sevents 3 events I event Time between 2 bunch crosings: ILC beam 337 ns Chip 0 Chip 1 Chip 2 Chip 3 Chip 4 Time between 2 trains: 200 ms 2820x337ns=950µs Data bus A/D conv. Chip 0 **IDLE MODE** DAQ **Acquisition** A/D conv. Chip 1 **IDLE MODE IDLE** DAQ **Acquisition** Chip 2 A/D conv. **IDLE** IDLE MODE **Acquisition** A/D conv. **IDLE MODE** Chip 3 **IDLE Acquisition** Chip 4 A/D conv. **IDLE** DAQ **IDLE MODE Acquisition** 

1ms (.5%)

.5ms (.25%)

.5ms (.25%)

1% dutý cycle

199ms (99%)

99% duty cycle