Testbeam Timing Issues.

Discussion based on AHCAL setup

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for the AHCAL developers
EUDET electronics and DAQ meeting
Palaiseau, Jan. 14th, 2010

HELMHOLTZ GEMEINSCHAFT

CALICE Calorimeter for ILC

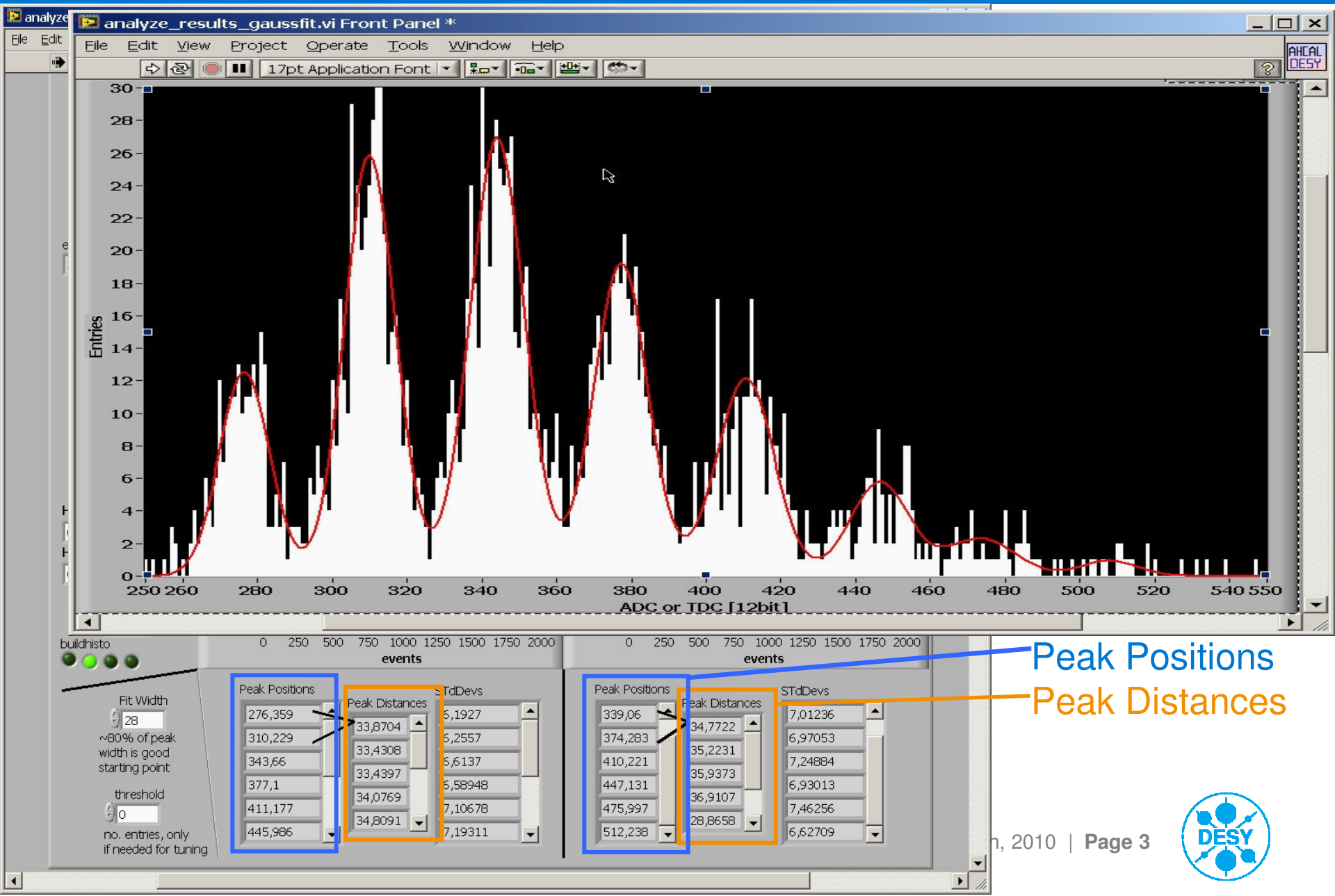
EUDET

DESY

Outline

- Status AHCAL DAQ (Labview and USB)
- DIF development
- **Testbeam timing issues**
- Conclusions and Outlook

AHCAL DAQ status



AHCAL DAQ status

- AHCAL DAQ is still based Labview and USB.
- **AHCAL DAQ1** for laboratory setup:
  Ready for data taking and characterization runs (tests of tiles, SPIROC, LED system, …)
- **AHCAL DAQ2** for DESY testbeam setup:
  Adaptation of DIF firmware for testbeam signals (trigger, busy) still ongoing, should be finished within 2 weeks.

=> Two different DIF and Labview Codes are developed.

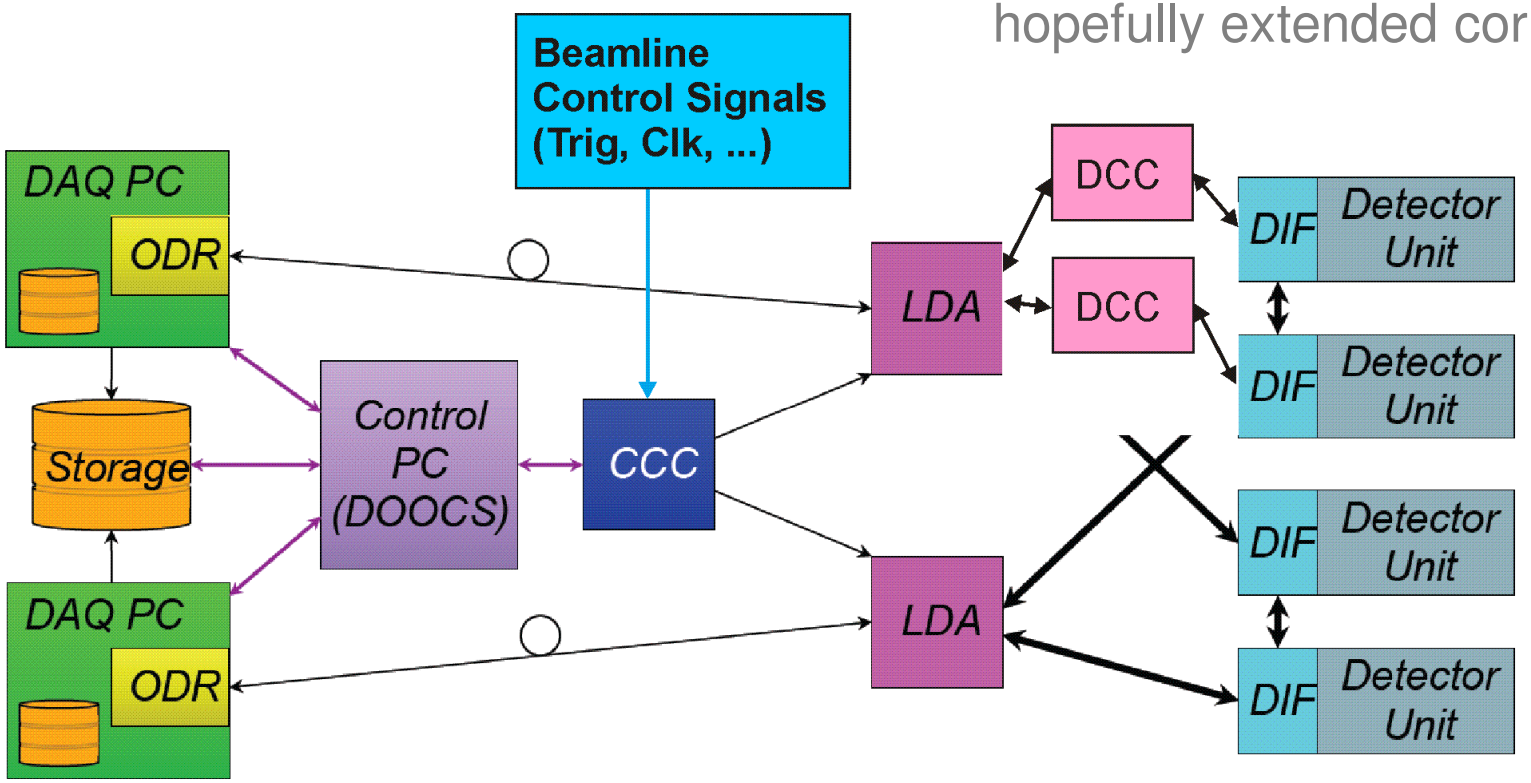
DIF development

- DIF task force meeting Nov. 27th, 2009 @LLR


- Remi made a proposal about general FPGA firmware block structure.
- AHCAL code can be adapted to this scheme with smaller changes (mainly adding some extensions to existing structures)
- Details about interfaces (e.g. simple things like signal/bus names) and DOCUMENTATION of shared blocks have to be clarified.
- USB can be detector specific at first in order to save time.
- DIF firmware generalization collides with testbeam efforts.

Testbeam Synchronization (CALICE DAQ setup)

Concept: M. Wing et al.,
hopefully extended correctly



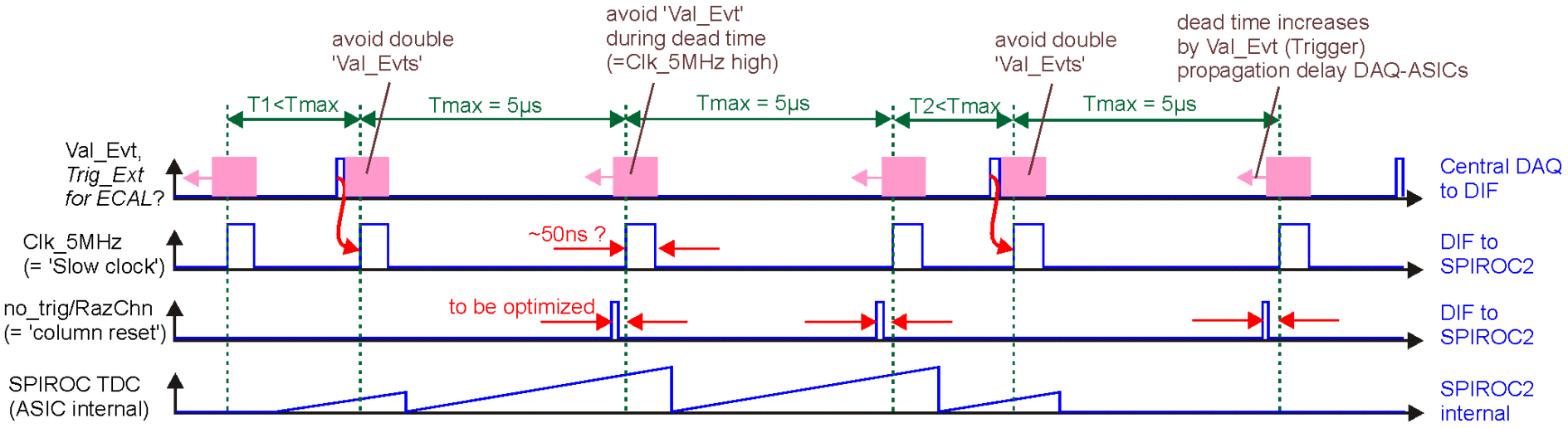
- All timing critical signals are distributed from central DAQ (via CCC).
- All detector units (+DIFs) run synchronously.

external Trigger usage

- external trigger delay (DAQ to AHCAL) is too large for AHCAL.
- ext_Trig is used for validation of event in AHCAL.
- ECAL and DHCAL can use ext_Trig as a ‘real’ trigger.

Testbeam: Internal Trigger in Validation Mode

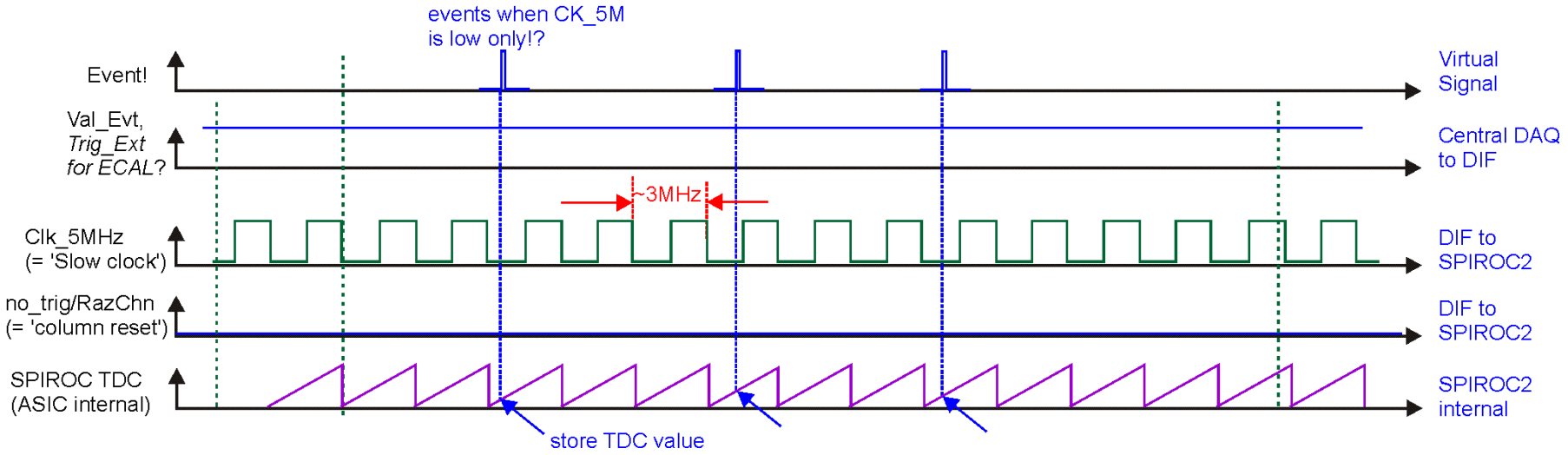
AHCAL timing scheme for common CALICE testbeam



- Internal Trigger with “Validate_Event”. **Pink boxes: deadtime!**
- ECAL (DHCAL as well?): Continuous CK_5M (3-5MHz?)
- CALICE DAQ: Synchronize Val_Evt on global clock (multi-DIF synchron.).
- Event time information: Store in DAQ: Validation time points (AHCAL), ECAL: has a (continuous) clock counter.

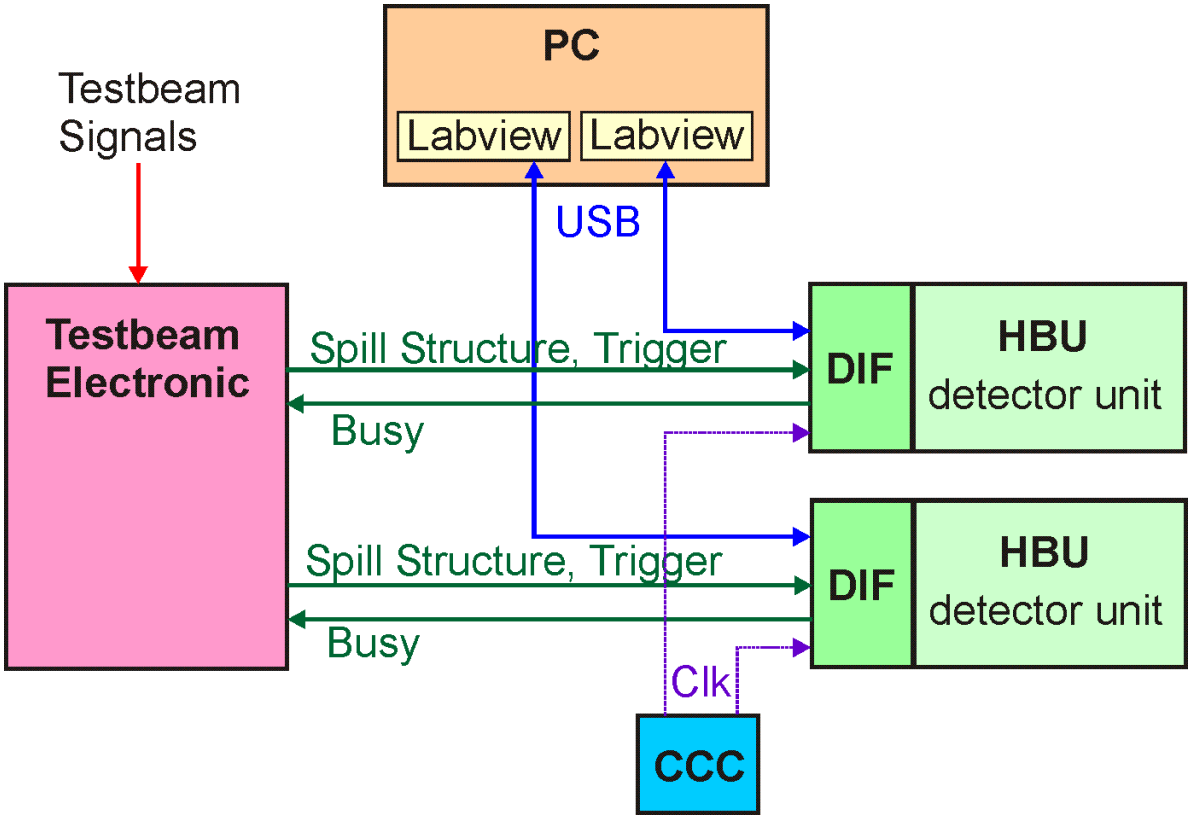
Testbeam: Internal Trigger in ILC Mode

AHCAL timing scheme for common CALICE testbeam



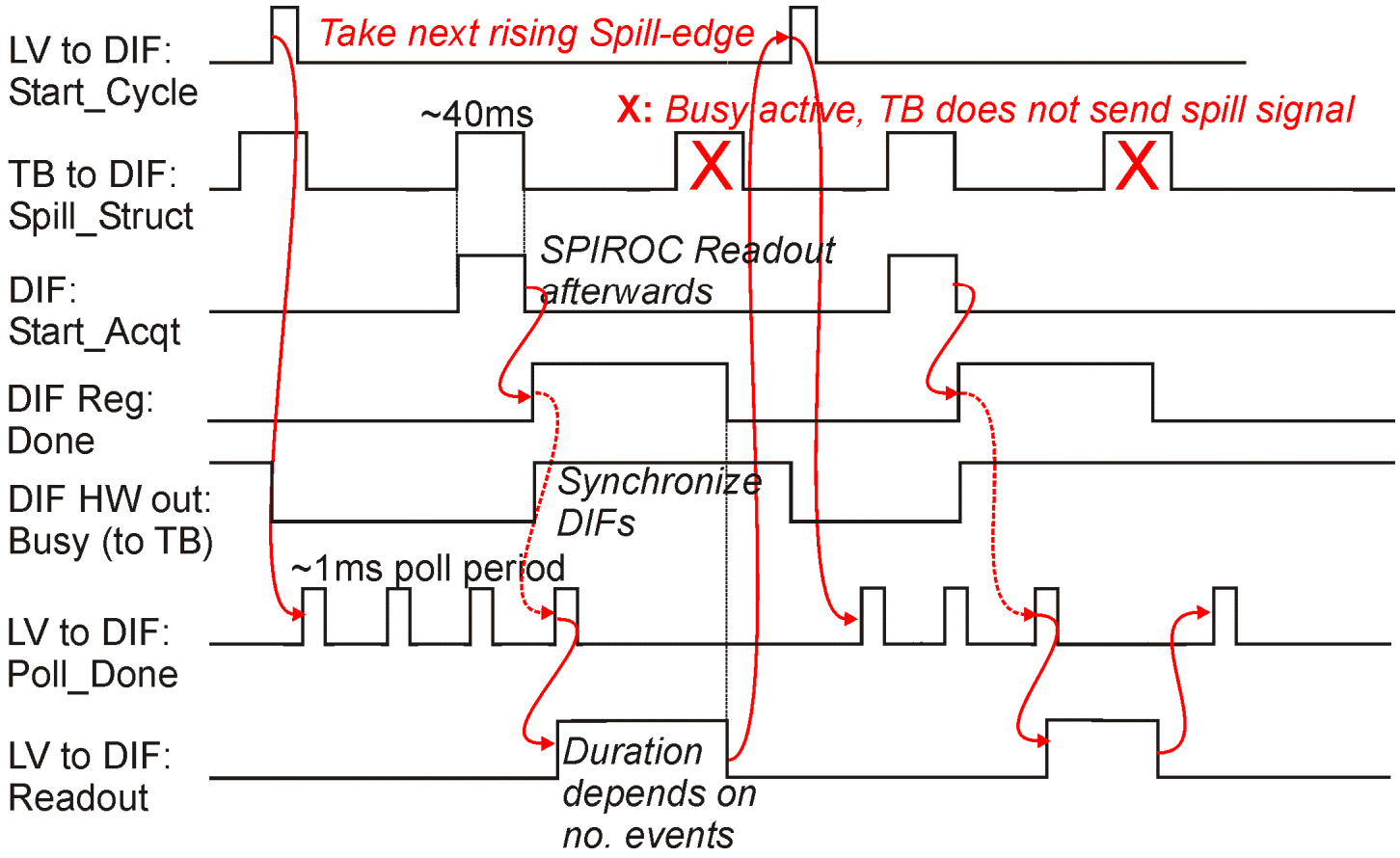
- AHCAL stores every event above threshold (events and noise), no validation. SPIROC is filled after 16 triggers.
- Since overall deadtime is readout-dominated, this mode is not the most efficient for AHCAL (many noise hits due to SiPMs).
- Setup is the same for ECAL and DHCAL.

DESY Testbeam Synchronization (Labview setup)



- Synchronization done by temporary hardware signals to/from DIF.
- First: Only one DIF/HBU used. With two HBUs the CCC is needed.
- Readout Speed limited due to USB/Serial Interface.

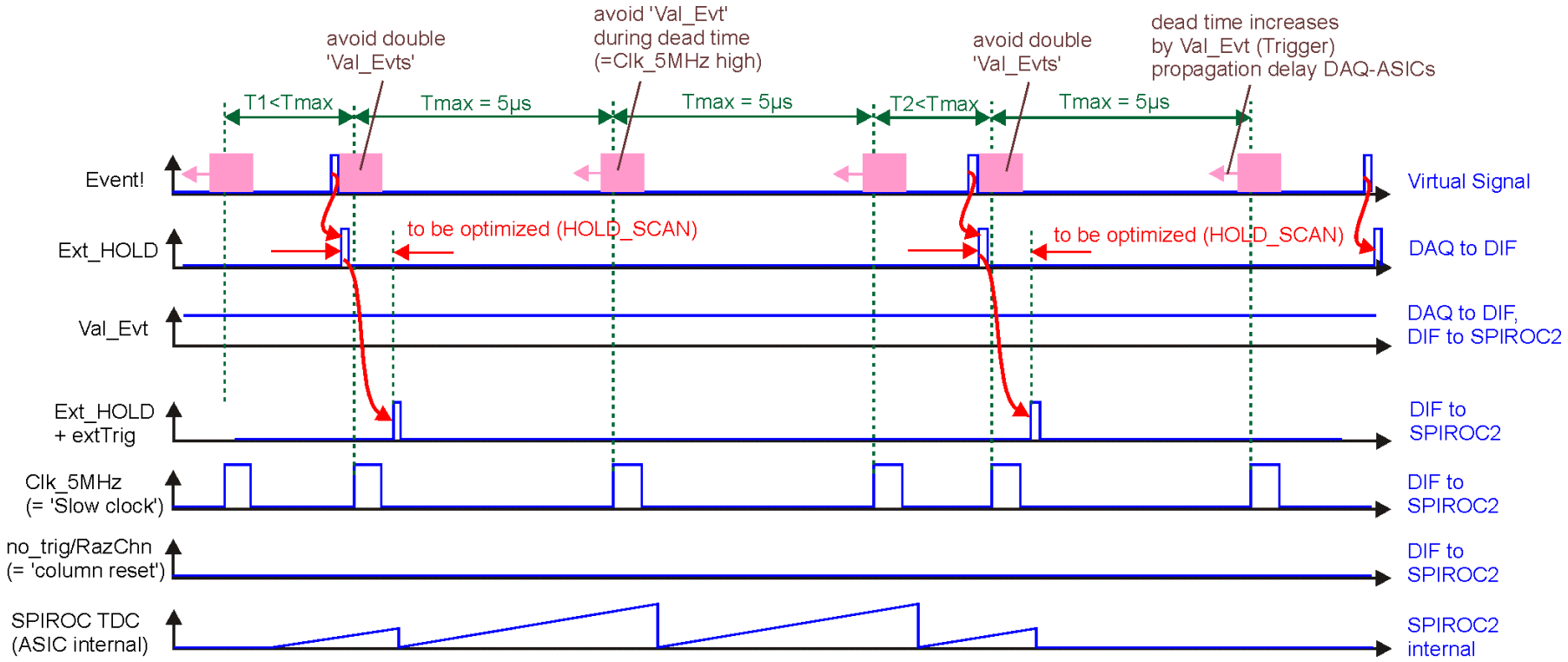
DESY Testbeam Synchronization (Labview setup)



LV: Labview
TB: Testbeam Electronics
HW: Hardware

- Due to shutdown of DESYII: HBU testbeam tests end of Feb 2010.
- External and Internal trigger will be tested.

DESY testbeam: AHCAL with external Trigger



- Data taking with external trigger at DESY testbeam *during spill.*
- Internal trigger: see timing schemes for CALICE DAQ setup.

Conclusions and Outlook

- AHCAL: 2 setups in operation!
- DIF generalization is prepared / has to be coordinated with testbeam firmware developments.
- Timing issues for common testbeam should be discussed now!

SPIROC Manual