Laboratoire d'Annecy-le-Vieux de Physique des Particules

CALICE Calorimeter for ILC

DHCAL DIF Status

1. Future CCC Use in DHCAL Setup
2. Calice DAQ Firmware Implementation News
3. DHCAL DIF Production for the M^3

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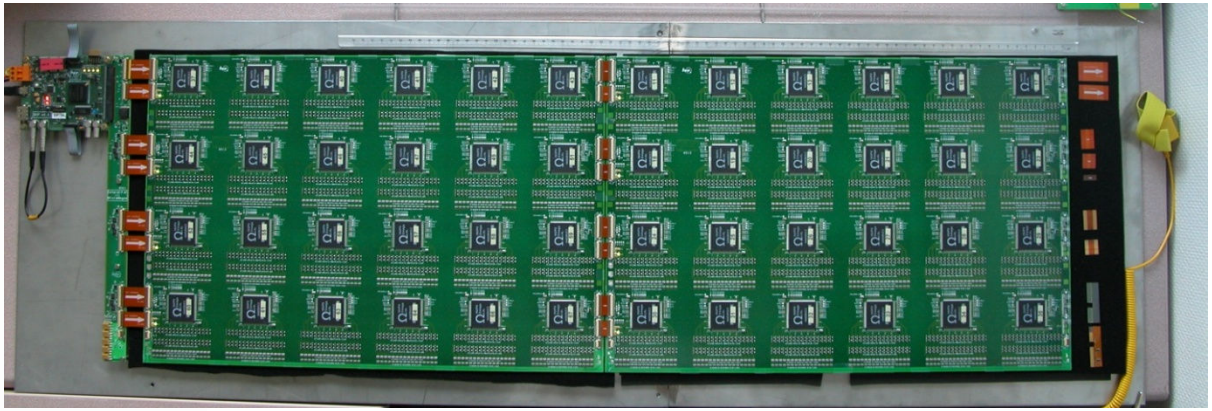
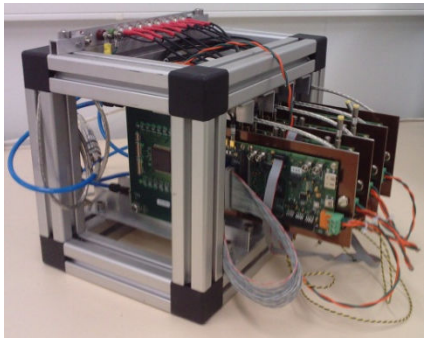
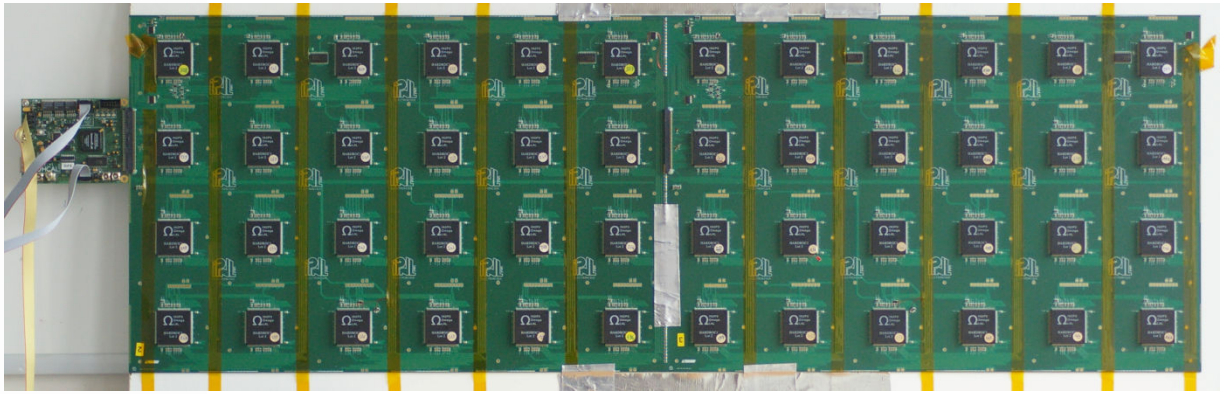
DHCAL DIF Use



Micromegas Dectector with 2*24 Hardrocs 2.

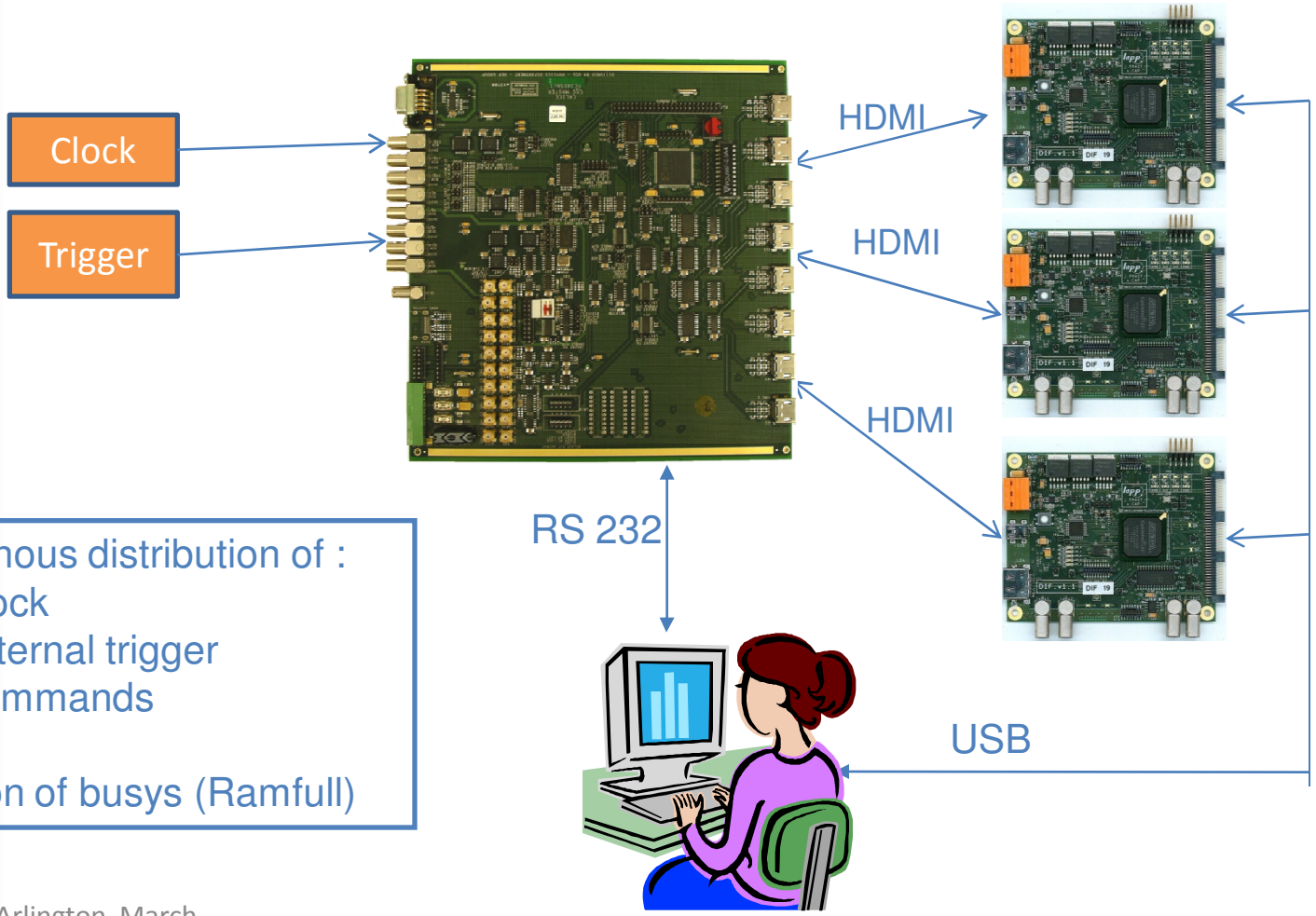


Micromegas with DIRAC



RPC detector with Hardrocs (IPNL)

Next step for the DHCAL Setup : Integration of the CCC board



Synchronous distribution of :
- Clock
- External trigger
- Commands

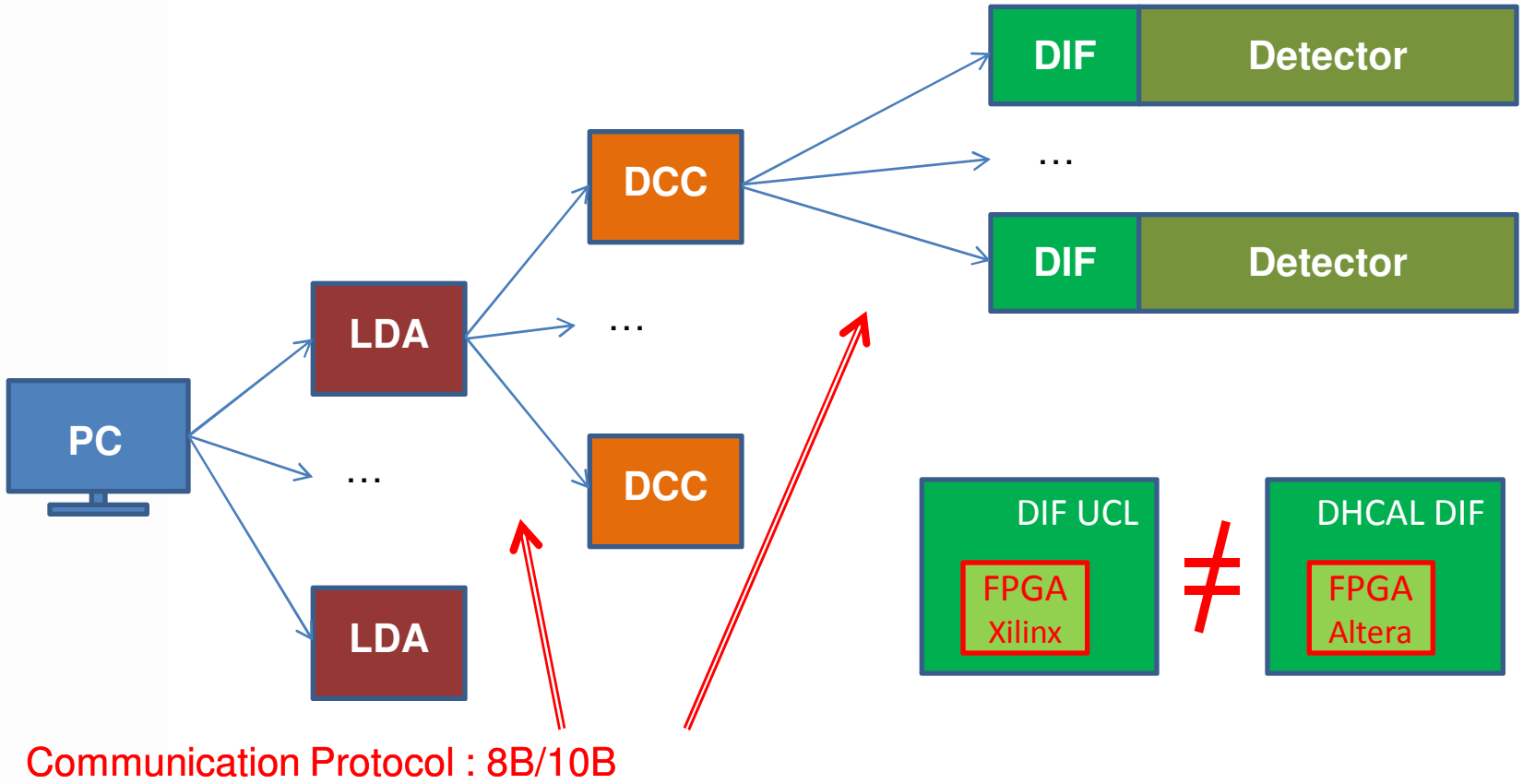
Reception of busys (Ramfull)

CCC Test at LAPP

- Reception of 50 MHz Clock
- Reception of Triggers
- Busy not yet tested.
- Commands will be generated with a home made serial protocol.
  - VHDL to be developed inside the UCL Xilinx ISE project.
  - Project received last Monday (thank you Matthew !)
  - Code to be optimized to fit in the small FPGA.

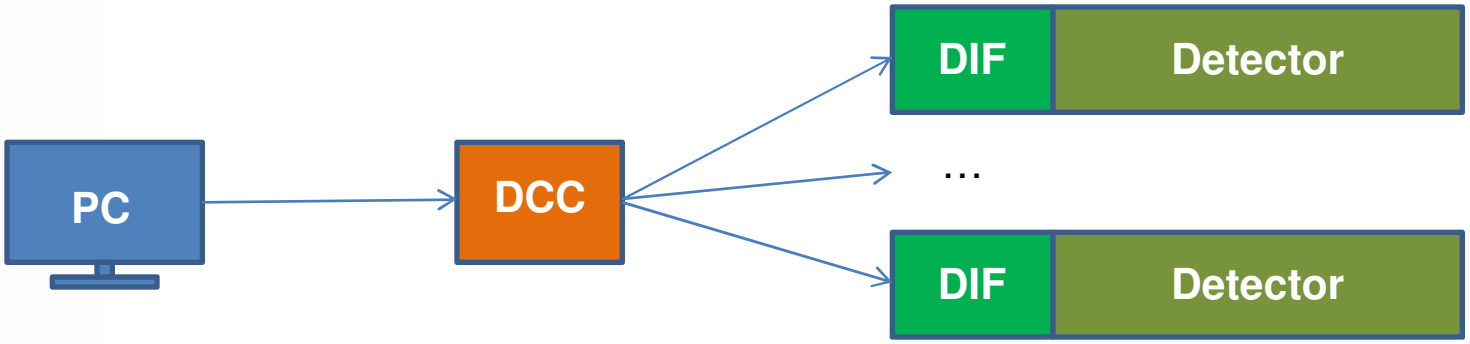
  => Hope to be used in next DHCAL test beam in May.

Final step : CALICE DAQ Architecture



First, the protocol has been developed with a Xilinx IP (because that was developed with a Xilinx FPGA)
Some work was needed to integrate the 8b/10b Altera IP (a bit different from the Xilinx one, timing, operation…) in the DAQ code.

8b/10b Communication Protocol

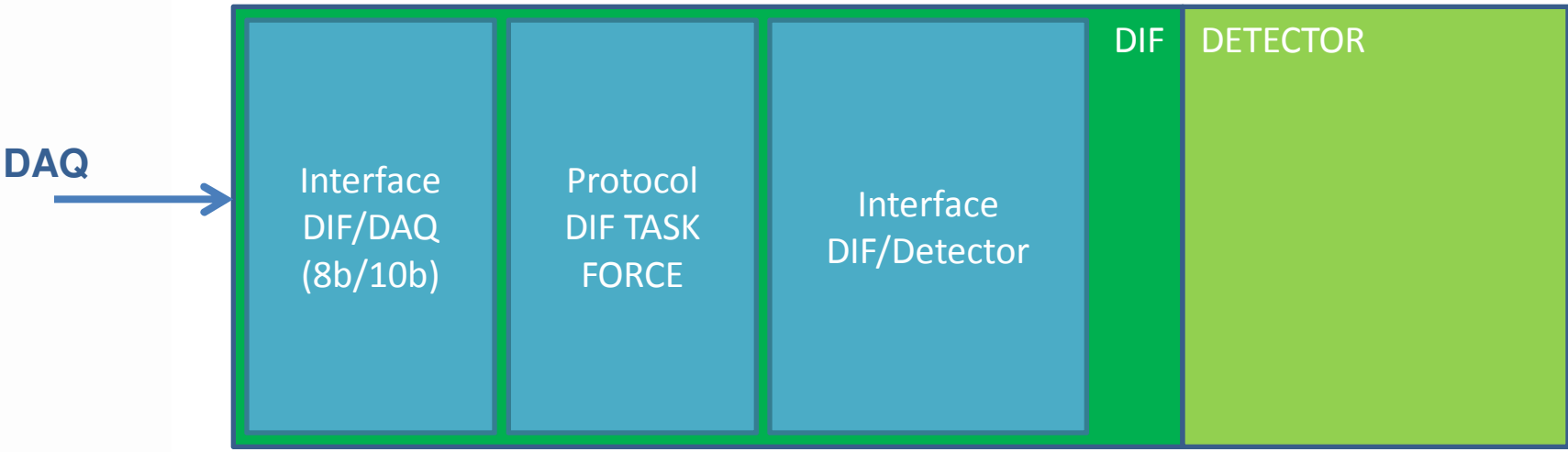


After debugging the code at LLR with the setup above (thanks to Rémi and Franck for their precious help), the DHCAL DIF is now working in the CALICE DAQ architecture.

Tests done with success :

- Link between DCC and DIF (this link is needed before any communication between both cards)
- Fast Command sent from PC to DIF through DCC (First way to talk with the DIF)
- Block Transfer sent from PC to DIF through DCC (Second way to talk with the DIF)
- Data sent from the DIF to the DCC

Next Steps in Firmware development



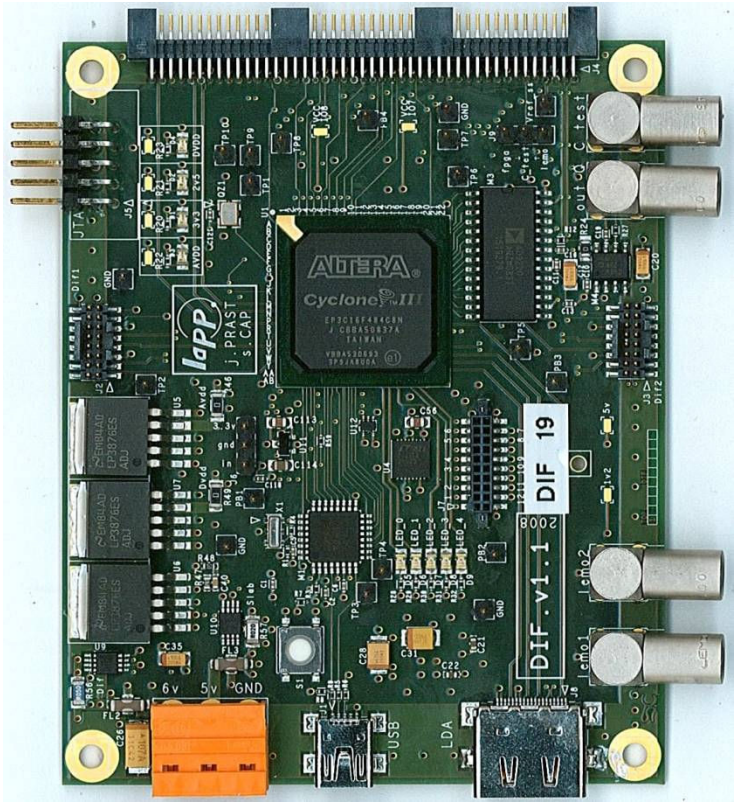
Now people in the DIF Task Force is going to work together to developed common code in the DIF.

<u>3 parts are to be developed :</u>

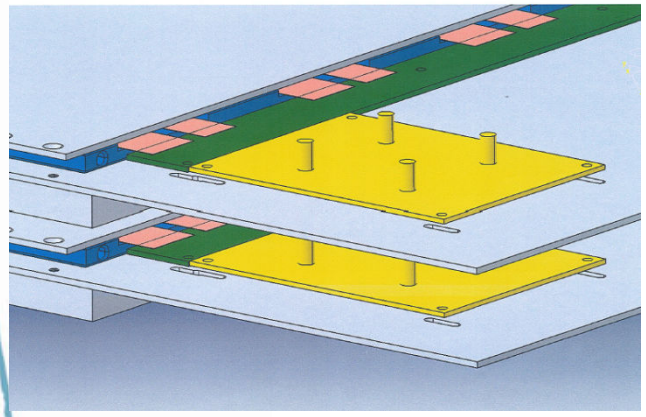
- Interface DIF/DAQ, already developed but need debug.
- Protocol DIF TASK FORCE, this part is the one to decode the data received and encode the data to send, according a protocol. The protocol is already defined and the code is on going.
- Interface DIF/DETECTOR, the code for some detectors is already done and is going to be reused.

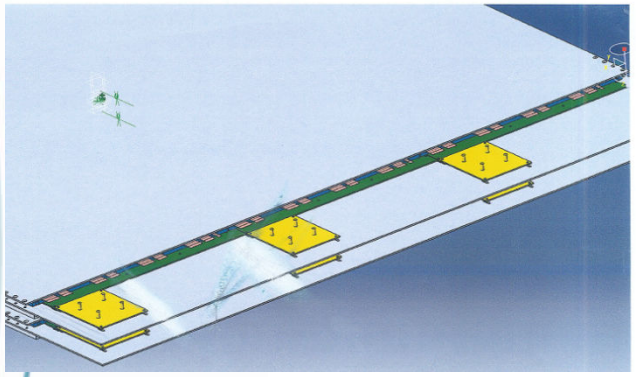
M^3 : DHCAL DIF Production

- 120 DIFs have to be produced for the m^3 readout (+ spares).
- The DIF will be produced as they are currently.
  - The board works quite well.
  - 8b/10b protocol between Altera and Xilinx FPGA validated.
  - No time to make a new prototype (schedule + manpower).
  - ADC (analog readout) not soldered.



Agenda for the DIF Production





DIF integration in the m^3

- First batch of 20 DIFs is being produced
  - Face urgent need of boards, in particular for HR2/HR2b m^2 readout at IPNL.
  - Will be received at the end of march.
- Production of 150 boards this summer.
  - Number to be adjusted
  - Whole production (PCB, components, soldering) handled by one single manufacturer.
  - Cost around 170 € per board.
  - Tests this summer + September if required
  - Use of Boundary Scan facilities to test electrical connection of the FPGA and connectors around.

=> All the boards should be available for September