



SDHCAL status in Lyon

-

Power pulsing, DAQ and m3

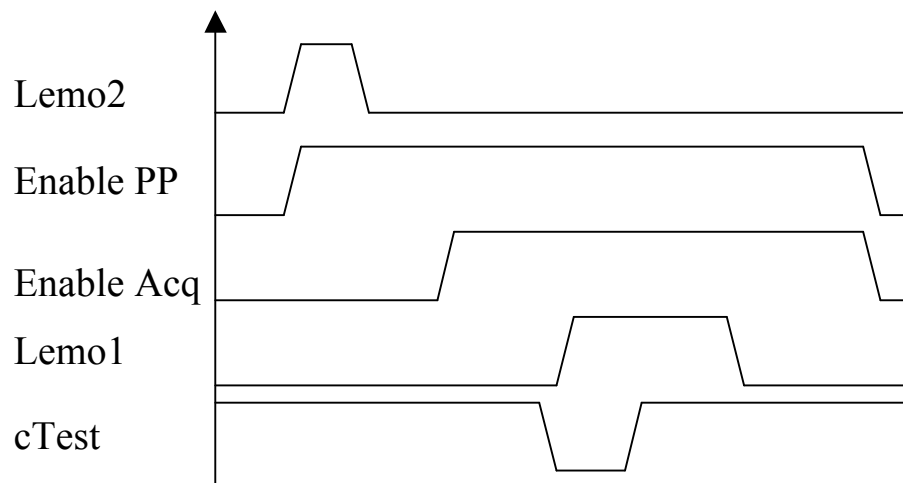
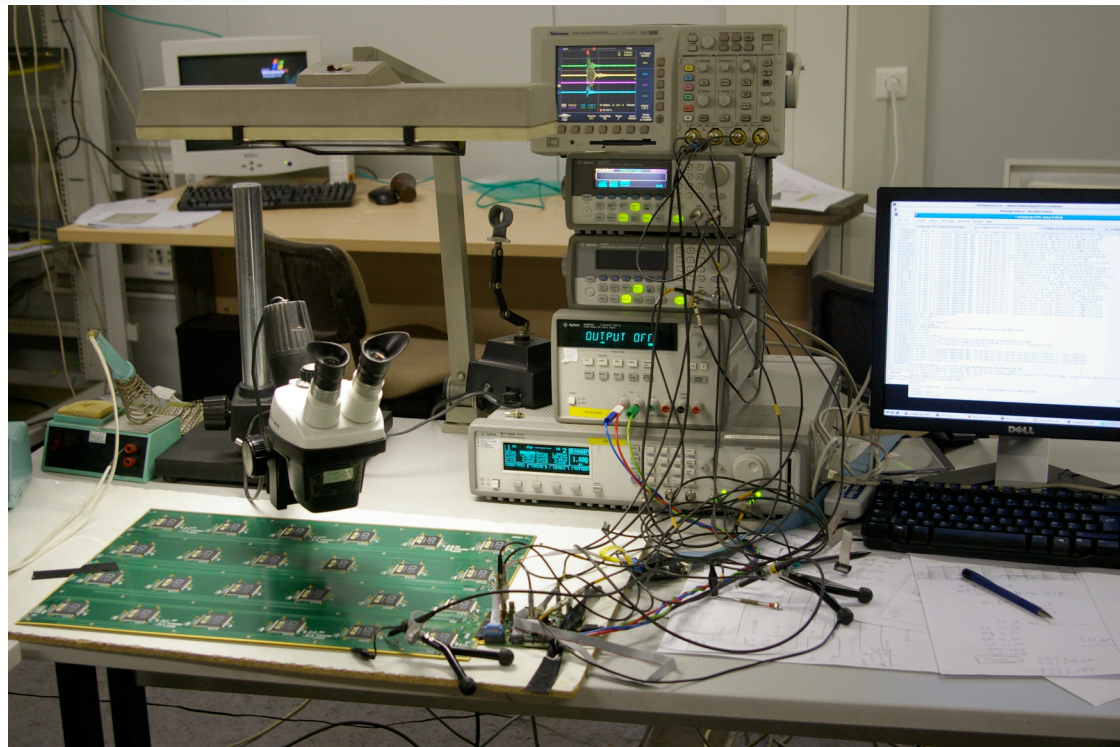
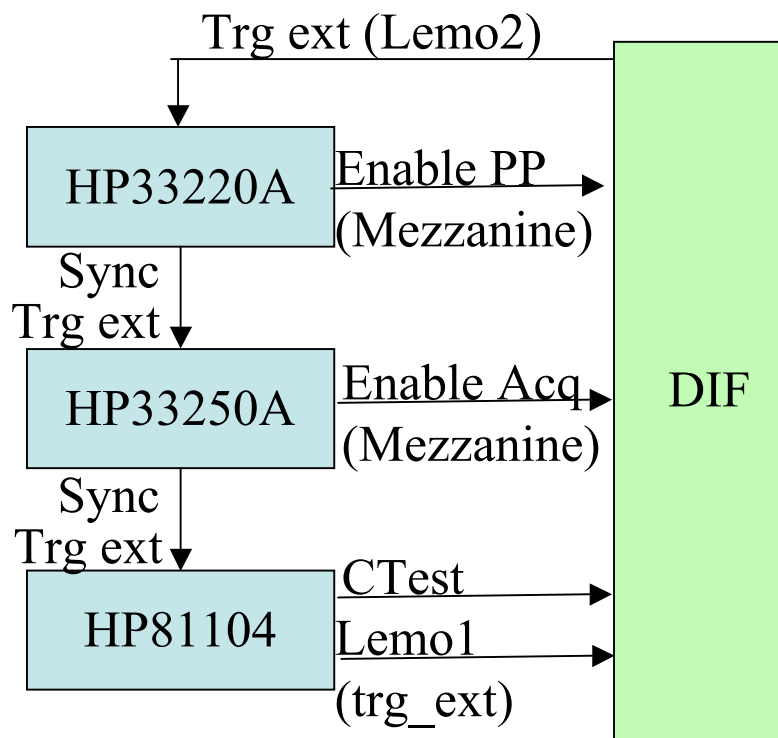
C. Combaret, for the IPNL team



Power pulsing on Hardroc 2 ASU : method

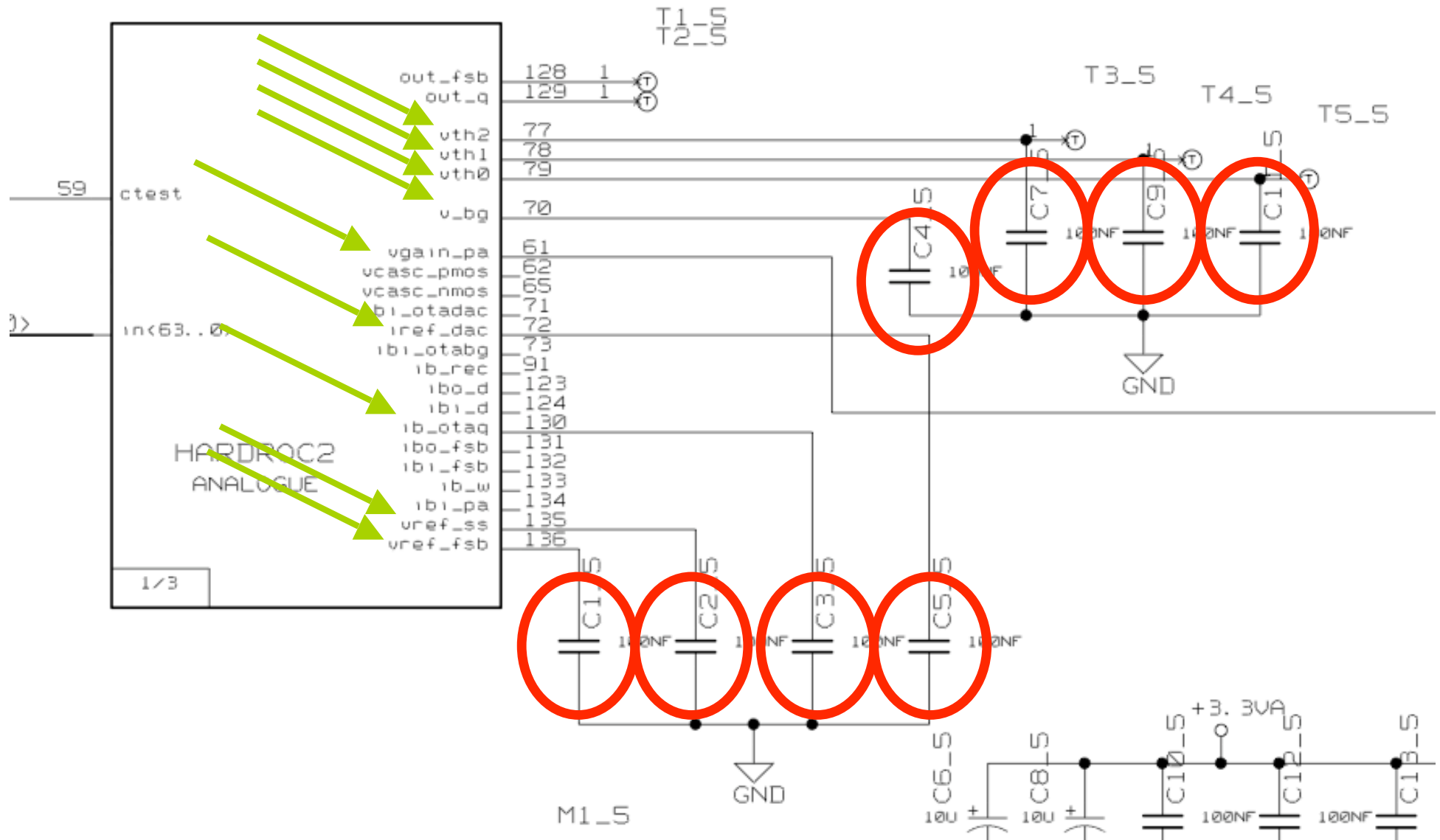
As discussed with Hardroc2 Asic designers :

1. Record (reference) SCurves and Bias levels with no hardware modifications (i.e. capacitors) on 1 test ASU
2. Enable PP hardware on DIF (use of Mezzanine pins to control PwrOn signals and Val_evt)
3. Enable PP in DIF firmware : PowerOn_x = register OR Mezzanine pin
4. Try PP with no capacitor removed (check that the firmware is OK)
5. Remove Capacitors on one HR2 (one by one) and check the corresponding analog signal
6. Record SCurves
7. Remove Capacitors on all asics
8. Record analog bias signal
9. Record SCurves



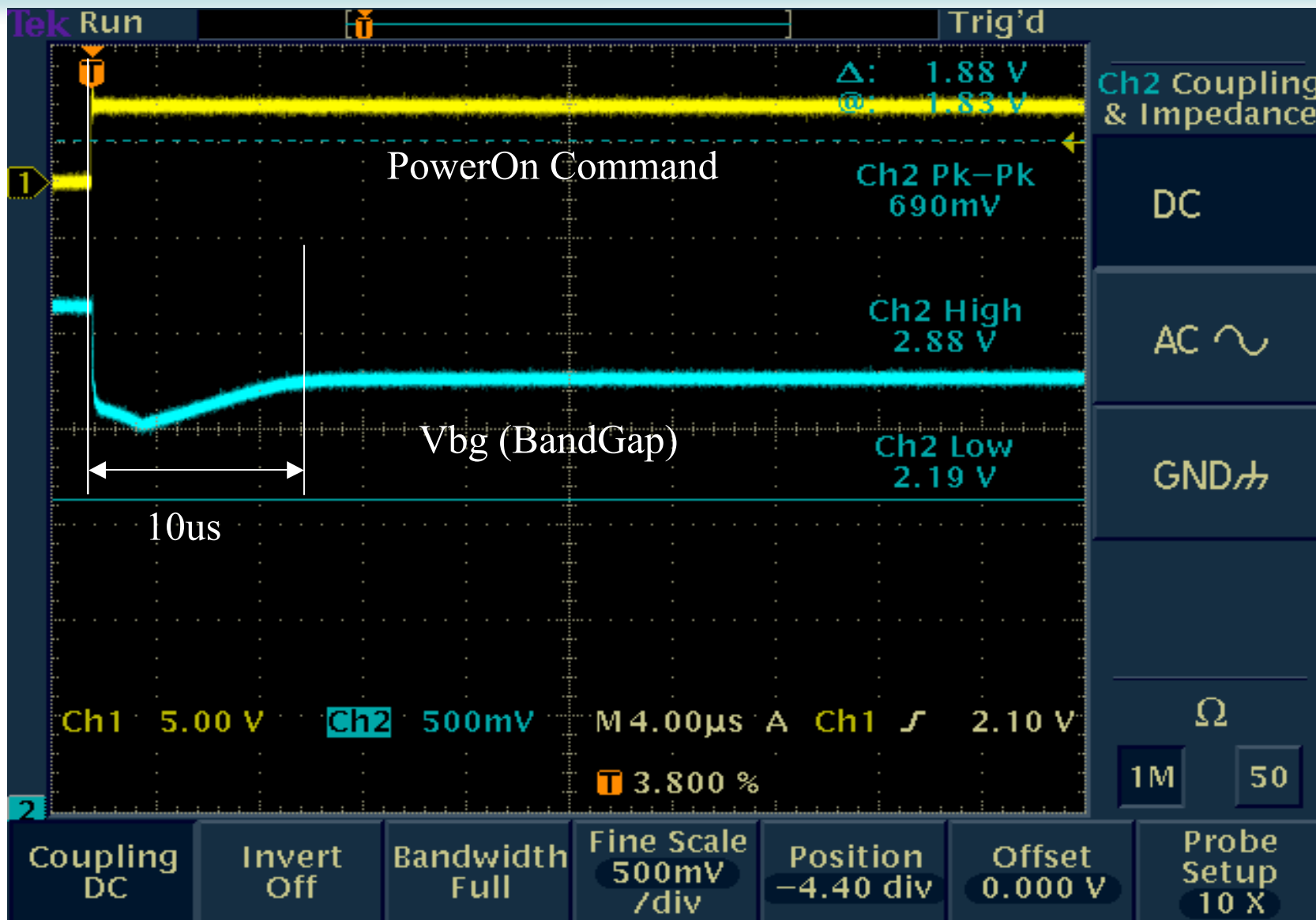


Power pulsing on Hardroc 2 ASU : method





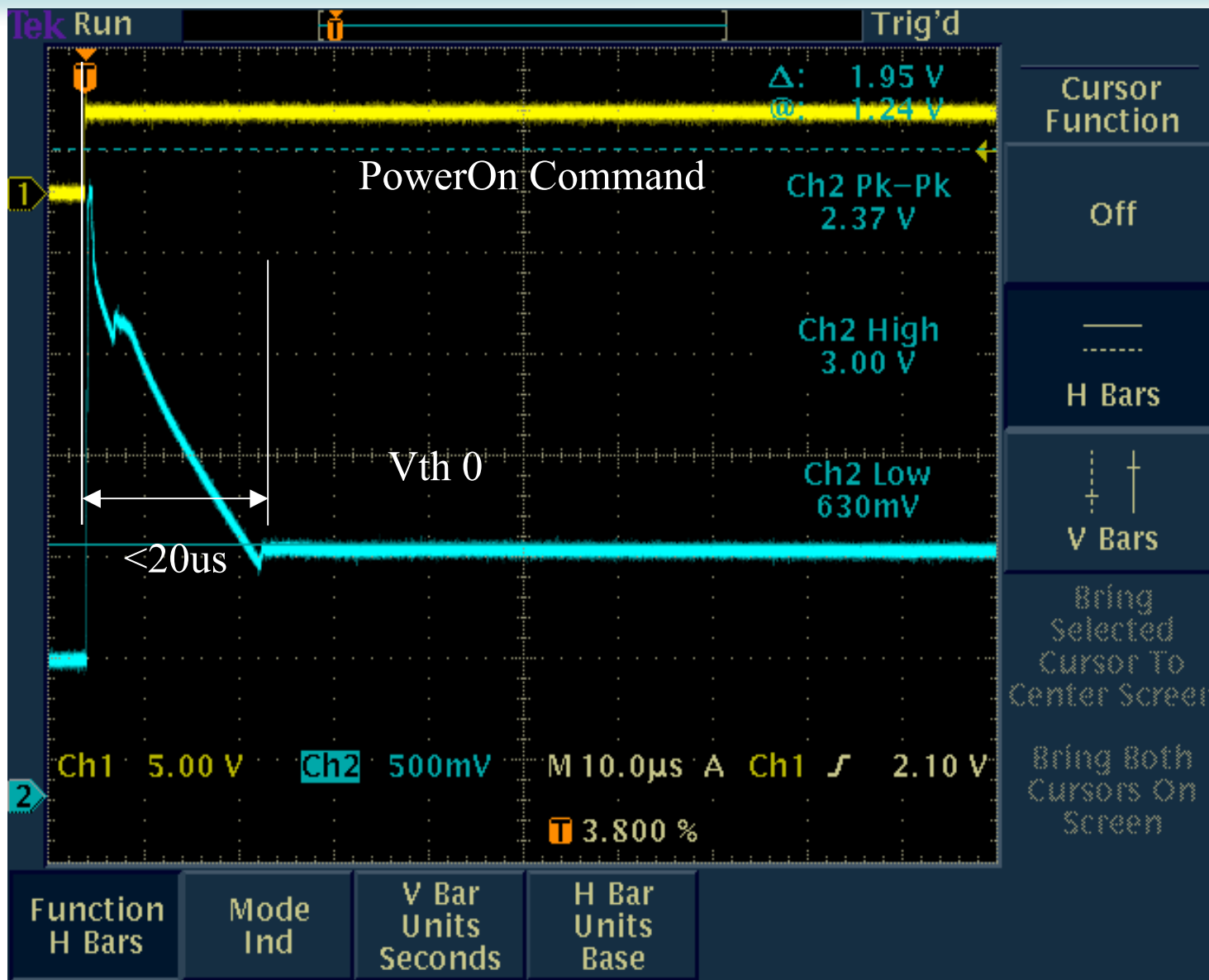
Power pulsing on Hardroc 2 ASU : preliminary results



Capacitors removed on one asic (first of the ASU)



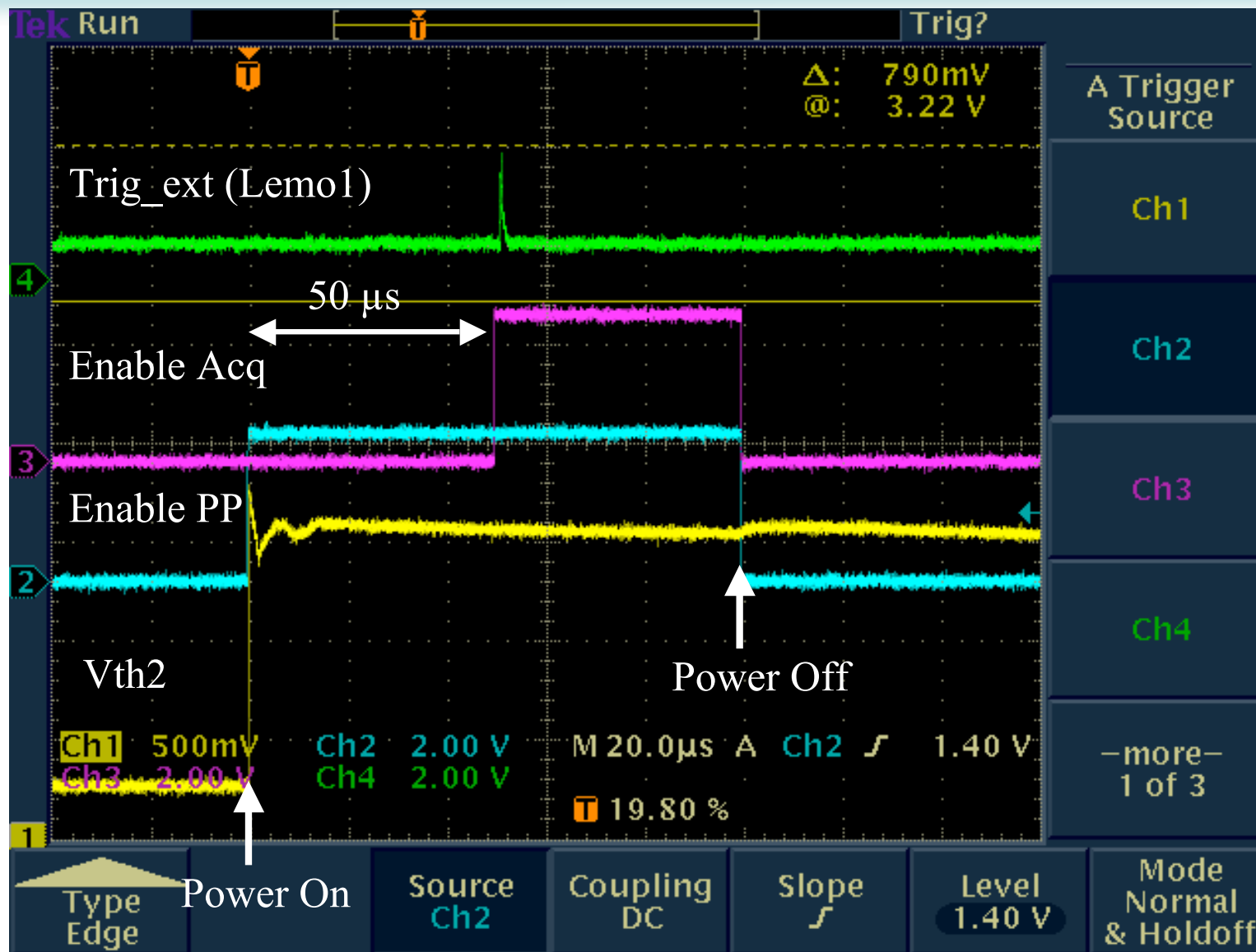
Power pulsing on Hardroc 2 ASU : preliminary results



Capacitors removed on one asic (first of the ASU)



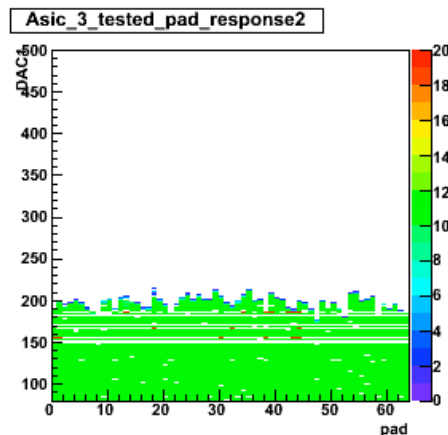
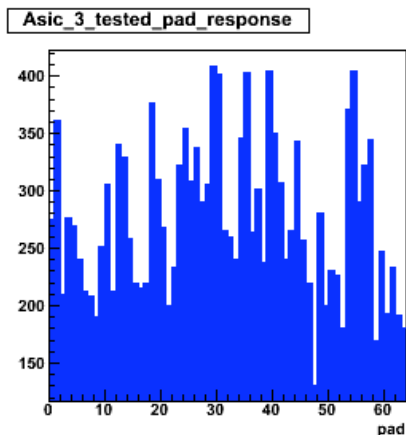
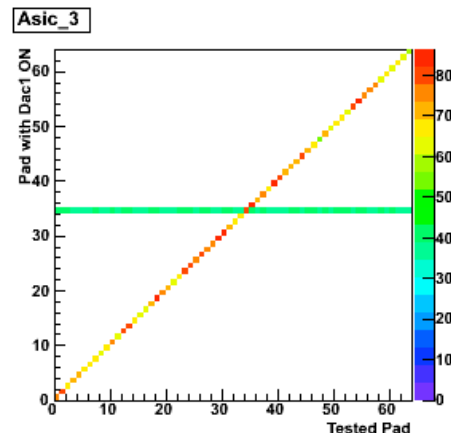
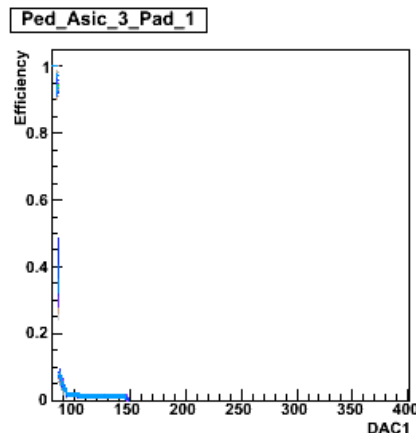
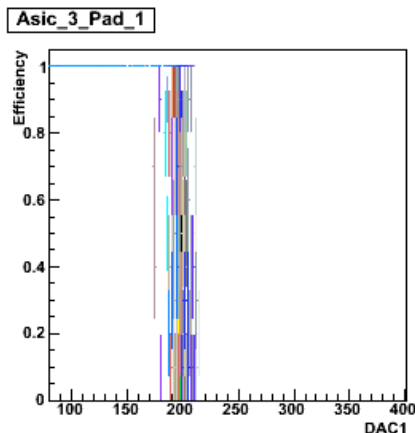
Power pulsing on Hardroc 2 ASU : preliminary results



Capacitors removed on all asics



Power pulsing on Hardroc 2 ASU : preliminary results



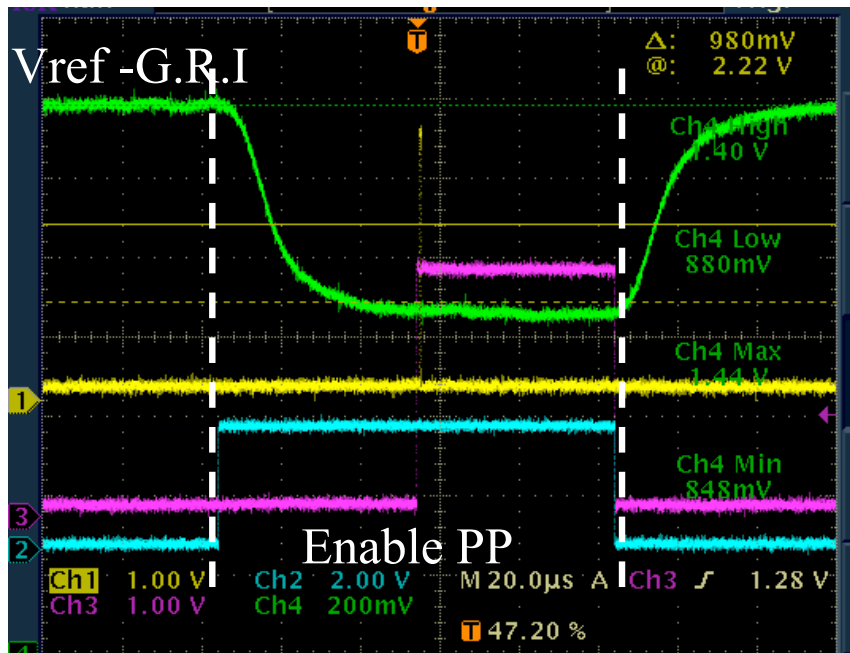
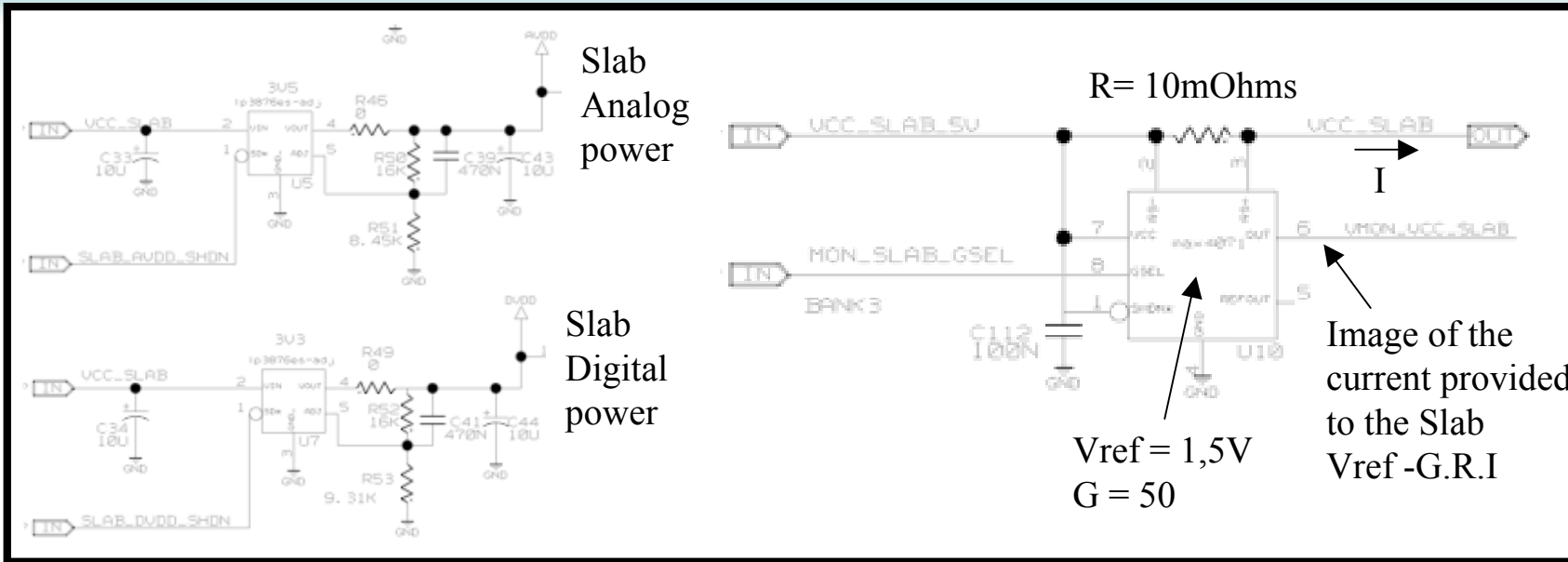
ASIC HR2 #3
DAC1Min = 80
DAC1Max = 400
DAC1Step = 1
GainMin = 128
GainMax = 128
GainStep = 1
Injection = 0.5V

SCurves seem OK,
Pedestals seem OK

NB : Because of slow control bug in HR2, some (many) SLC configurations can not be used, leading to discontinuities in SCurves



Power pulsing on Hardroc 2 ASU : Power consumption



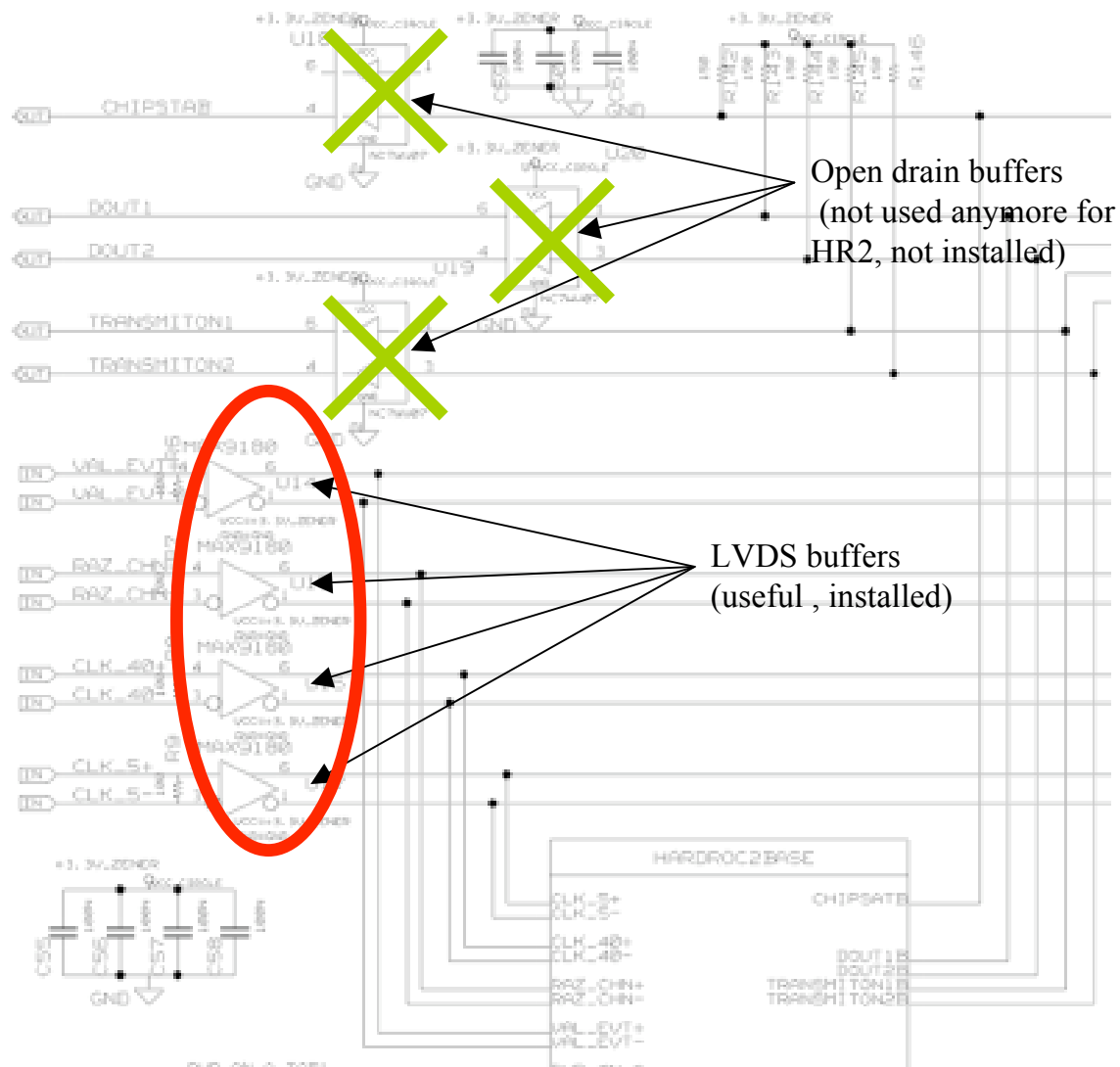
← 100 mV - 200 mA ← Permanent consumption

← 620 mV - 1,20 A

These 200 mA would lead to around $400\mu\text{W}/\text{ch}$
-> Not acceptable, where do they come from?



Power pulsing on Hardroc 2 ASU : Power consumption



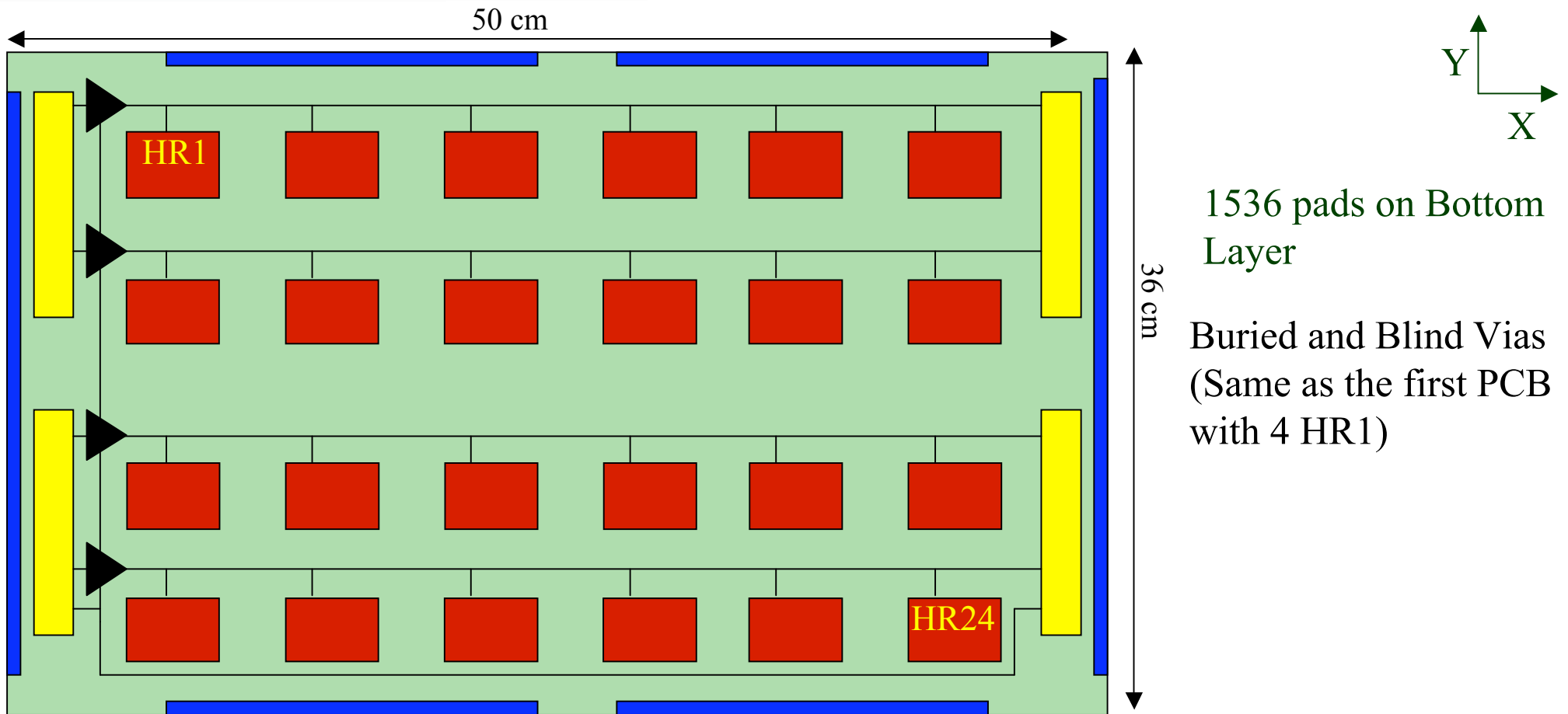
By luck, because of SLC bug on HR2 (4V needed for hardrocs), we installed LDO regulators for LVDS buffers (3,3V needed).
! It is possible to add a shunt resistor (6,8 Ohms) on the buffers power supply line and monitor their consumption .

! Gives around 50 mA for 6 HR2 (200 mA for a whole ASU)

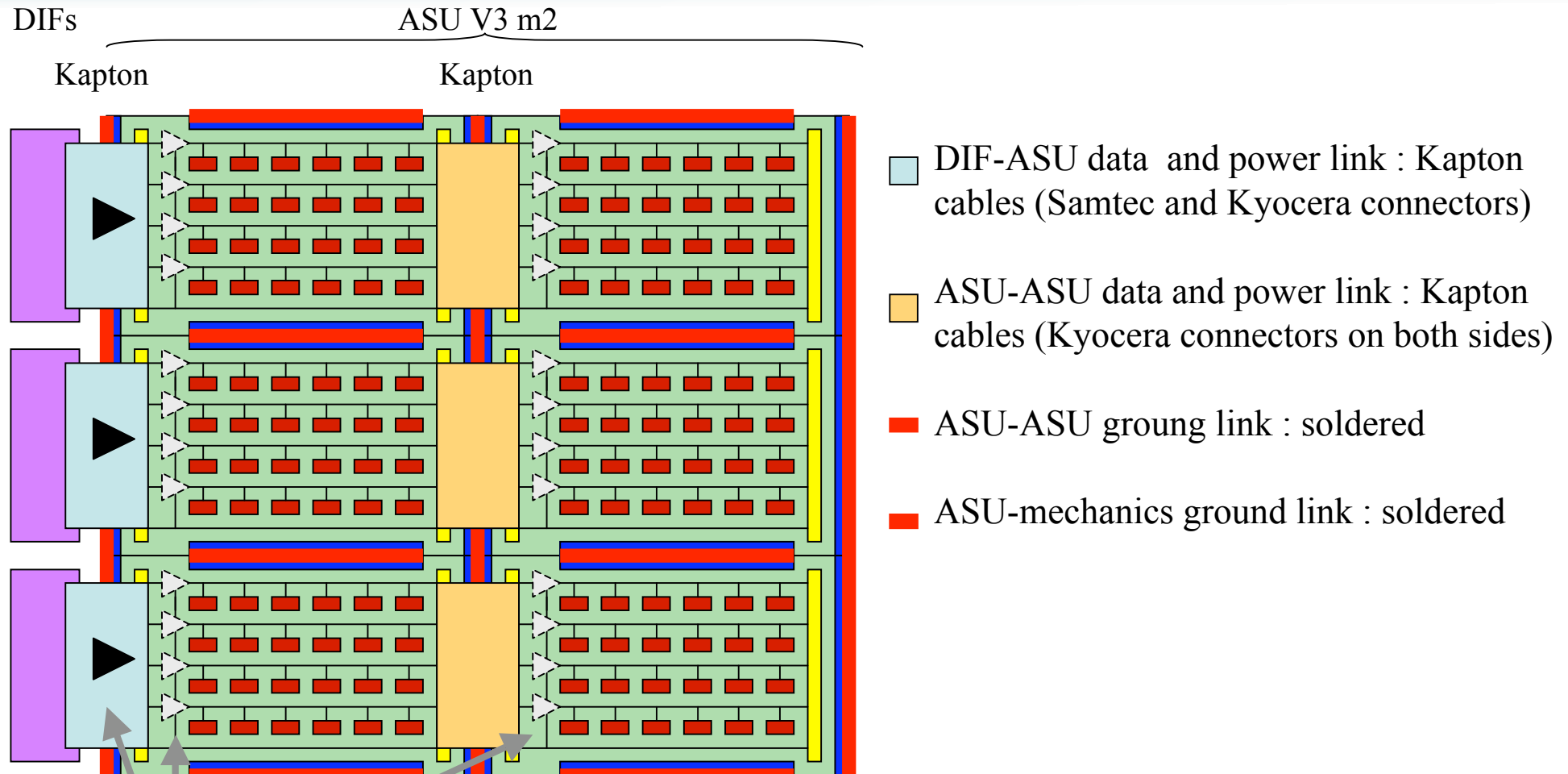
! Most (all) permanent power is lost in the LVDS buffers.

! A solution is under study to solve this problem (separate LVDS lines on the ASU to easily match impedances and reduce parasitic capacitance, add buffers with low power mode). Implemented in the next ASU design.

! LVDS buffer is usefull only for clocks (40MHz and 5MHz), not for Val_Event and Raz_Channel



- GND link ASU-ASU on both X and Y axis
- Signal and Power link ASU-ASU and DIF-ASU on X axis (flat cables with Kyocera connectors)
- ▶ LVDS-LVDS buffer with power down mode (footprint on ASU, even if not used, in case of need for repeaters for 3m long slab tests)



LVDS buffers will be put or on the DIF-ASU kapton cable, footprint foreseen on the ASU itself (could be put on the DIF itself later)



I2C serial interface for DHCAL ASICs (H. Mathez, Y. Zoccarato)

Advantages of the I2C link vs shift registers :

Individually addressed readout and slow control.

More flexibility for the user

Easier for the driver firmware design (DIF board)

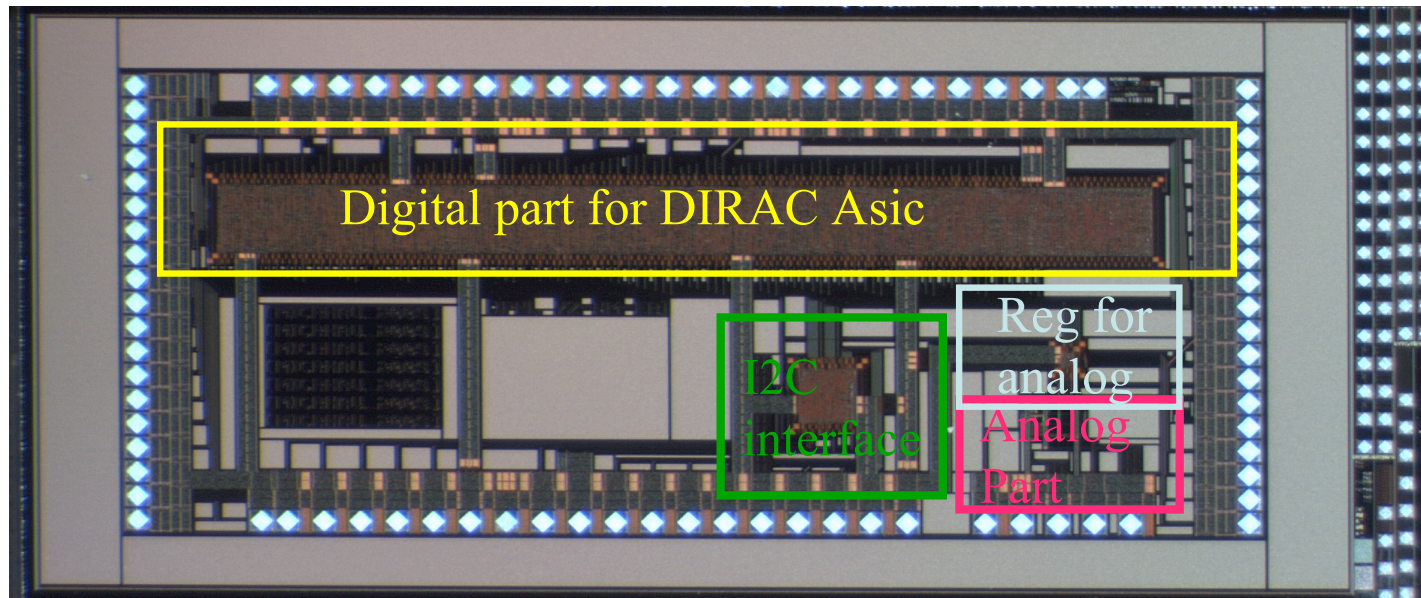
Readout of the sent parameters is possible without rewriting them.

Easier board routing (without chips chaining).

Less sensitive to the risk of failure propagation.

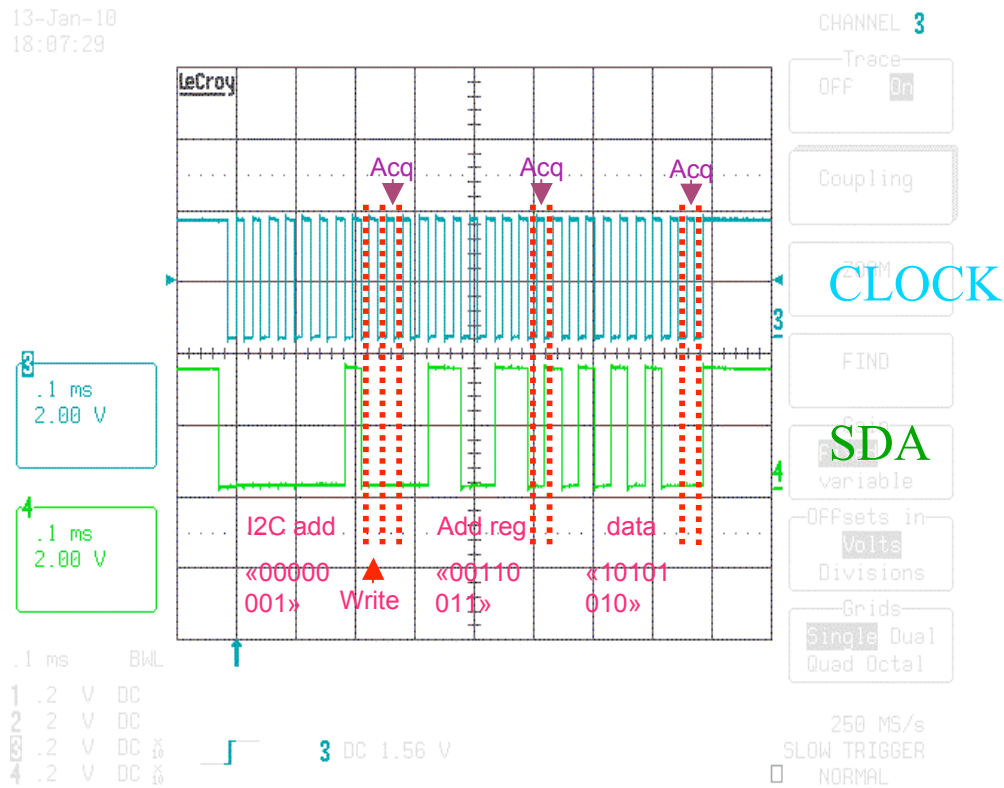
Could be used for readout

As for SRs, needs to be doubled

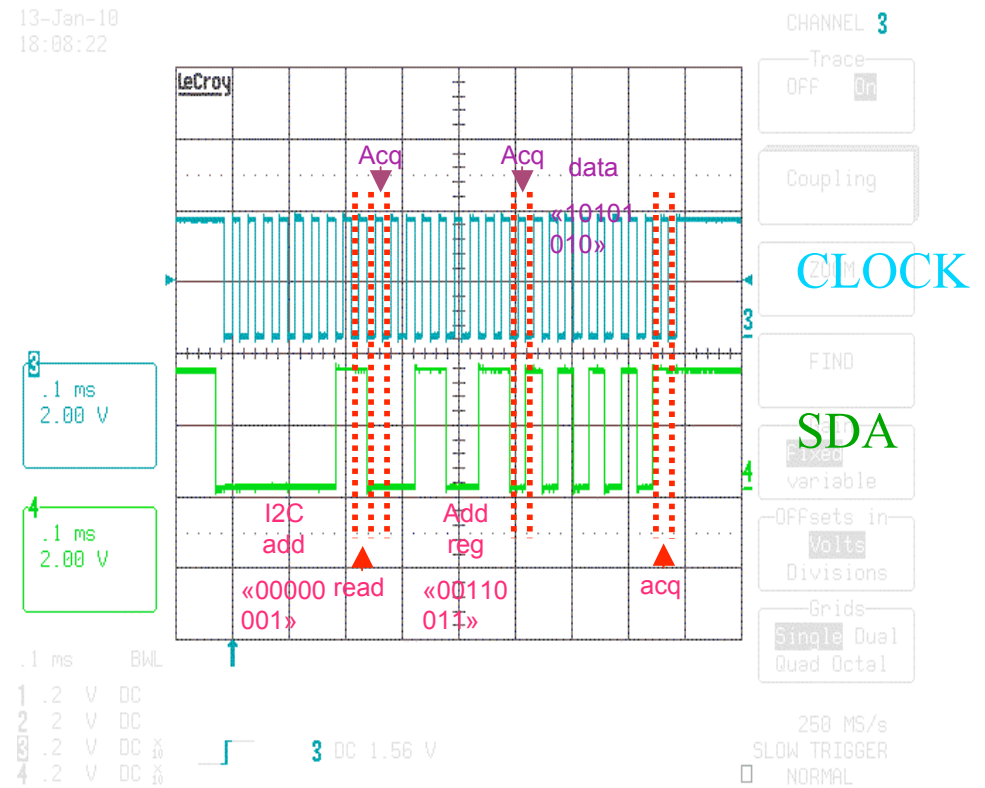




I2C serial interface for DHCAL ASICs (H. Mathez, Y. Zoccarato)



Write



Read

I2C block is working (has been used to control the CSA)



Xdaq basics

Executives

- Main XDAQ process
 - Support http: Start a web server on a given port, configuration via XML
 - Lyoac22> xdaq.exe -p 5000 -c mydaq.xml à accessible on
 - » <http://lyoac22:5000/>
 - Additional transport (tcp, atcp) for binary exchange
 - Dynamic loading of shared libraries (application)

Applications

- Load dynamically as a shared library (XML tag in the executive configuration)
- Each application acts as a web service
 - Embedded web page definition or Web 2 access
 - GUI for hardware access is visible on the web
 - Curl configuration
 - Accept or emit SOAP messages
 - Remote control of command
- It can be declared on the tcp transport and exchange binary message with other applications
 - Inside the executive: zero-copy (shared memory)
 - On the same PC: unix sockets
 - On the network: tcp sockets



Xdaq Architecture

Each application can be controlled by an FSM

Global configuration using SOAP message from the LocalManager

The Event Builder (EVM/RU/BU/FU) is provided and maintained by XDAQ

Software triggers/tokens exchange between EVM and LocalManager

Some generic software developed (I2O interfaces from RUCollector and RU and from FU to RootAnalyzer, Local manager trigger loop)

Main constraint: Trigger driven

Trigger veto board needed (controlled by the LocalManager)

Ok for external trigger, further development needed for auto trigger EVB

XDAQ is the CMS data acquisition framework and will be supported in the coming years.

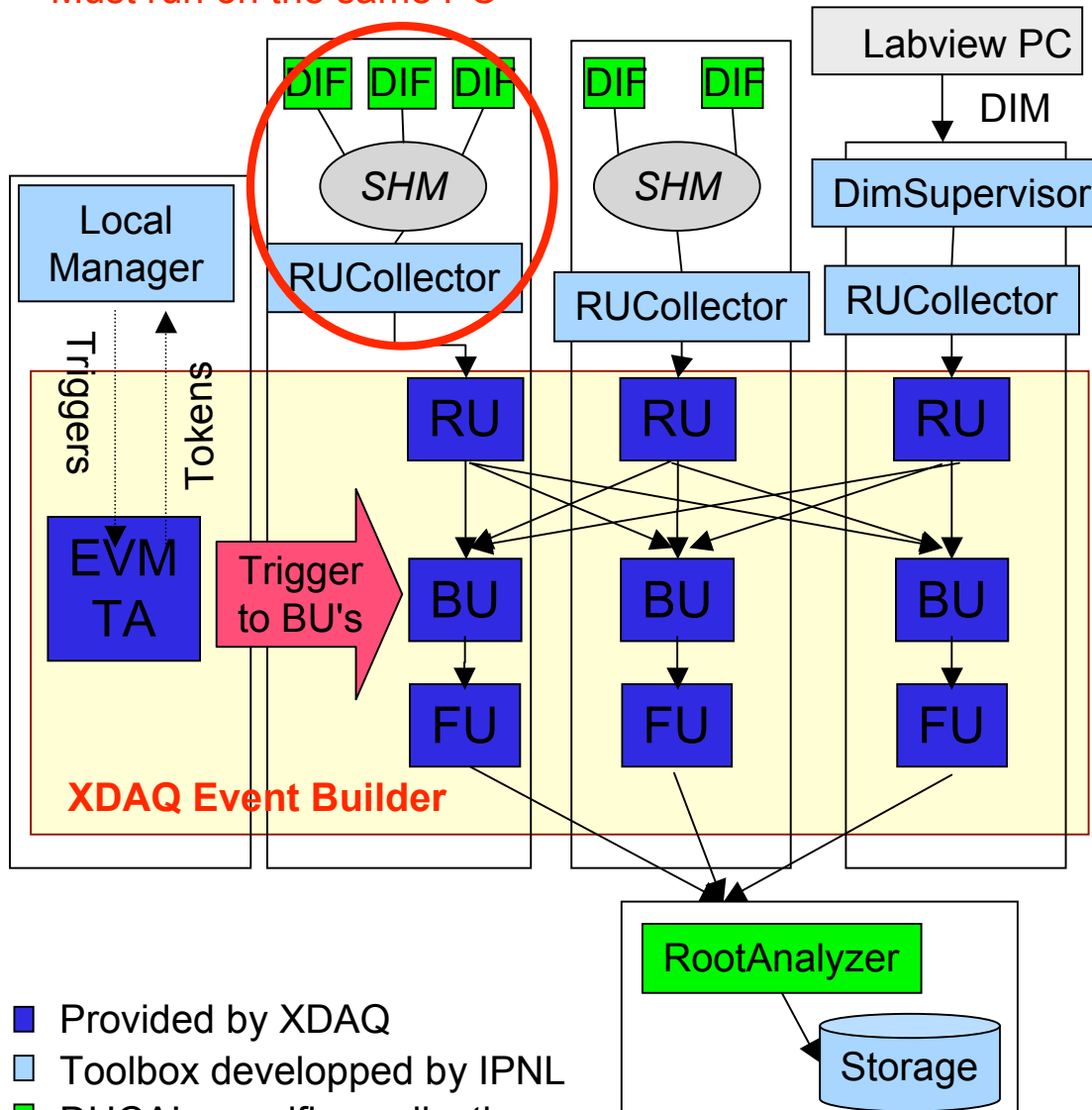
Code is free.

Proven to be scalable

Binaries are provided as RPMs on Scientific Linux CERN releases (yum installation). Recompile is needed for other Linux platform. IPNL add-ons can be provided as sources or RPMs if needed.

Integration of XDAQ event builder (L. Mirabito)

Must run on the same PC



Readout Unit (RU): Collects data from any source with predefined message format and buffered it in a FIFO, feeds 1 BU on trigger request

Builder Unit (BU): Collects data from all RU of a given partition for a given trigger. Assembles data fragment, buffers the event and feed FU registered to it (tokens)

Filter Unit (FU): Processes build event. Has some processing slots and provides tokens to its associated BU according to free slots.

Event Manager (EVM): Controls the whole system. Receives trigger from an external source (Trigger Acceptor) and triggers the transfer of RU buffers to BU. Once event built it receives a token from the BU it forwards to the TA to allow further triggers.

Trigger Acceptor (TA): Trigger control with predefined messages with the EVM in order to receive tokens and send triggers

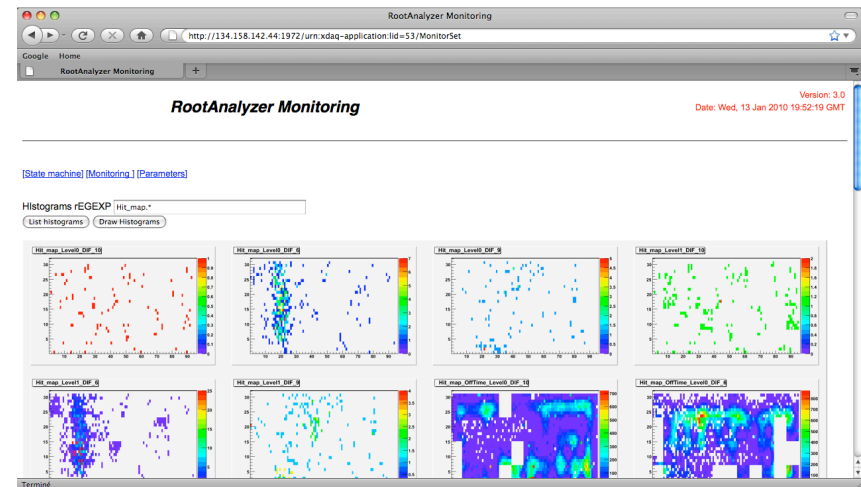
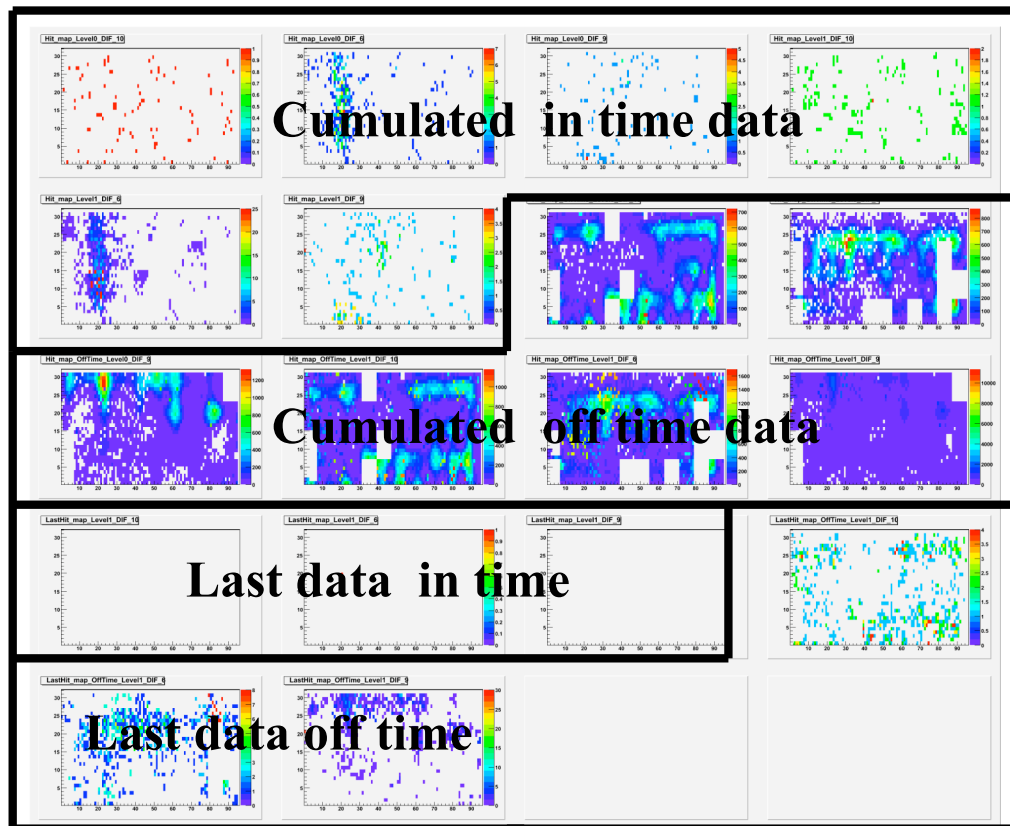
- Provided by XDAQ
- Toolbox developed by IPNL
- DHCAL specific application
- Processes



Online analysis with Root (L. Mirabito)

For each DIF :

NumberOfAsic_InTime	Hit_map_Level0/1
NumberOfFrame_vs_Asic_InTime	Hit_map_OffTime_Level0/1
NumberOfHit_per_Frame_InTime	LastHit_map_Level0/1
NumberOfHit_per_Frame_OffTime	LastHit_map_OffTime_Level0/1
NumberOfHit_vs_Asic_InTim	NumberOfFrame_vs_Asic



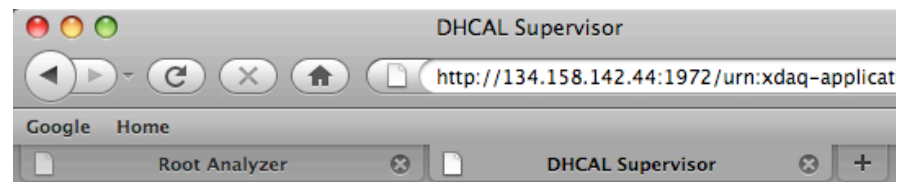
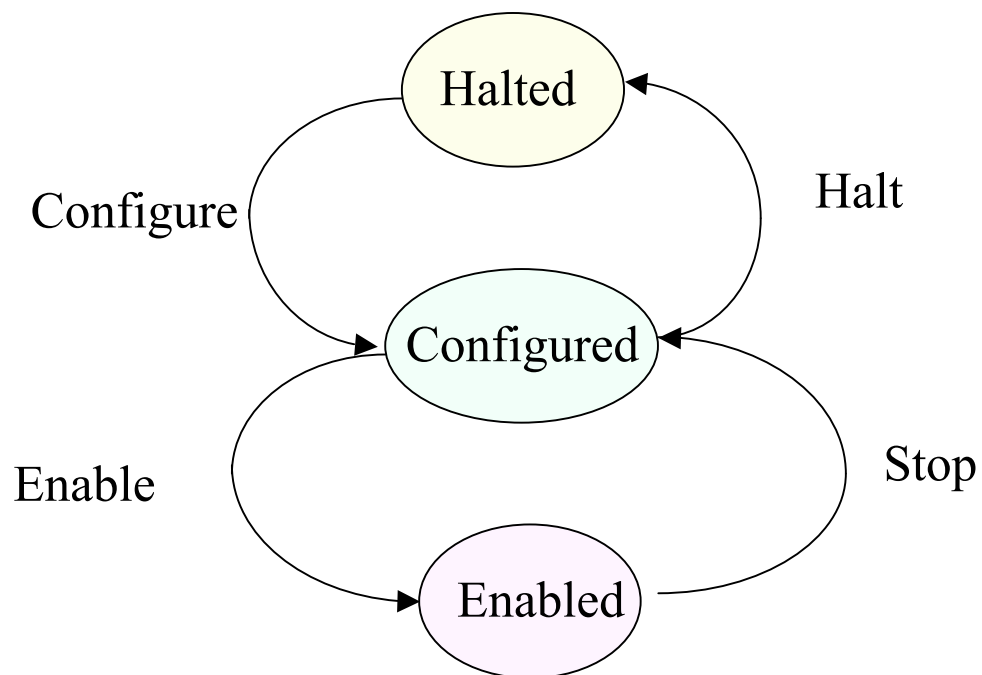
Use of Xdaq main FSM

Each Xdaq application can be controlled by the main FSM.

To do this, it must only know the following states : **Halted**, **Configured** and **Enabled**

And implement the following transitions: **Configure**, **Enable**, **Halt** et **Stop**.

Use of RunControl (from CMS) for larger applications



Main DHCAL Supervisor

Date: Sun, 08 Nov 2009 :

[\[State machine\]](#) [\[Parameters\]](#)

DHCAL Supervisor Finite State Machine

Enabled				
<input type="button" value="Configure"/>	<input type="button" value="Enable"/>	<input type="button" value="Halt"/>	<input type="button" value="Initialise"/>	<input type="button" value="Stop"/>



M3 construction database

Developed at IPNL (mainly by G. Baulieu and N. Giraud)

Extensively used during construction of CMS Tracker



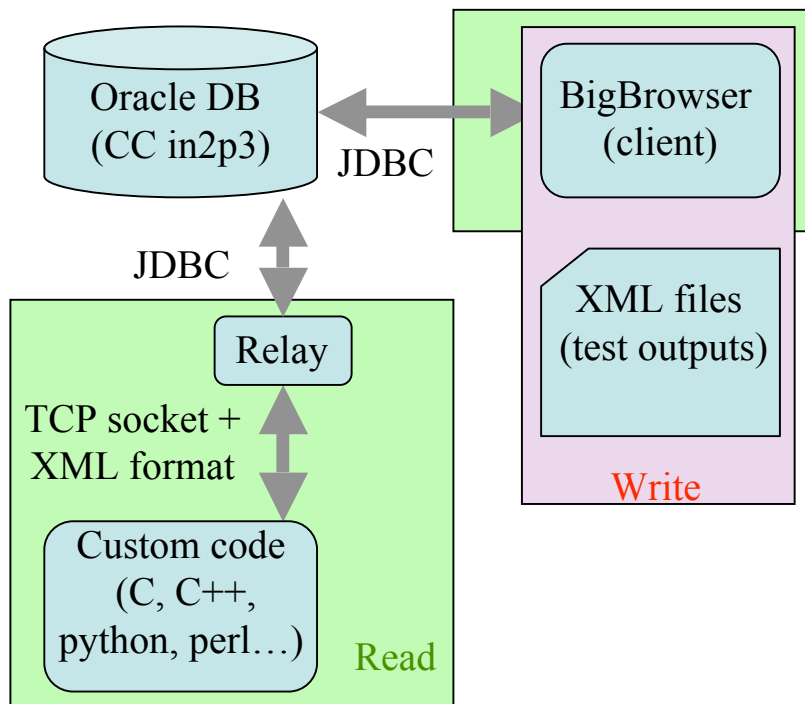
Java User interface available on different platforms (Windows, Linux, MacOs)

Relay available to interface with existing code (TCP sockets + XML format)

Can record status and location of each object composing the detector, its history and tests performed.

HR1 ASU1

The only constraints is to have a unique barcode on each object (choosed 2D, QR code)



12	11	10	9	8	7	6	5	4	3	2	1	0
M1	M0	U1	U0	T2	T1	T0	O5	O4	O3	O2	O1	O0

M1..0 : Complete module where the device will be (001 for m3)

U1..0 : Use of the device (tests, prototype, m3 production...)

T2..0 : type of the device (Asic HR1... , ASU HR1..., DIF

HR1..., detector Statguard...,Kapton, DIF..., Case,...transfer between sites)

O5..0 : numbering of the device



Conclusions and next steps

Power pulsing is functional. Power consumption is understood and will be solved within next ASU step.

I2C block is functional. Need to discuss with people from LAL to integrate it.

Xdaq DAQ system is stable and reliable.

Next steps will be :

- Implement the CCC card in the DAQ system (clock distribution and fast commands)
- Switch to LCIO format
- Add a database for runs parameters, asics configuration, and data
- Use the high speed serial link to communicate with the DIF
- Produce, test and validate electronics for the m3.



Thank you for your attention



Backup slides



Transferring data from slab to DIF

48 chips

128 events

20 bytes per event

8 bits per byte

-> $48 * 128 * 20 * 8 = 983040$ bits per slab if all asics full

5MHz clock -> 200 ns /bit -> 19,6 ms max to transmit data to the DIF