# ECAL SILICON- TUNGSTEN STATUS

Jean-Claude Brient ( for ECAL group)

## OUTLINE

- **Wafers**
- **PCB FEV7..8..** see Stephane Callier (LAL-Omega)
- **ASU ( Active System Unit)**
- **Integration**
- **Mechanics** see Julien Giraud (LPSC)
- **VFE** see Stephane Callier (LAL-Omega)
- **DAQ** see Remi Cornat (LLR)

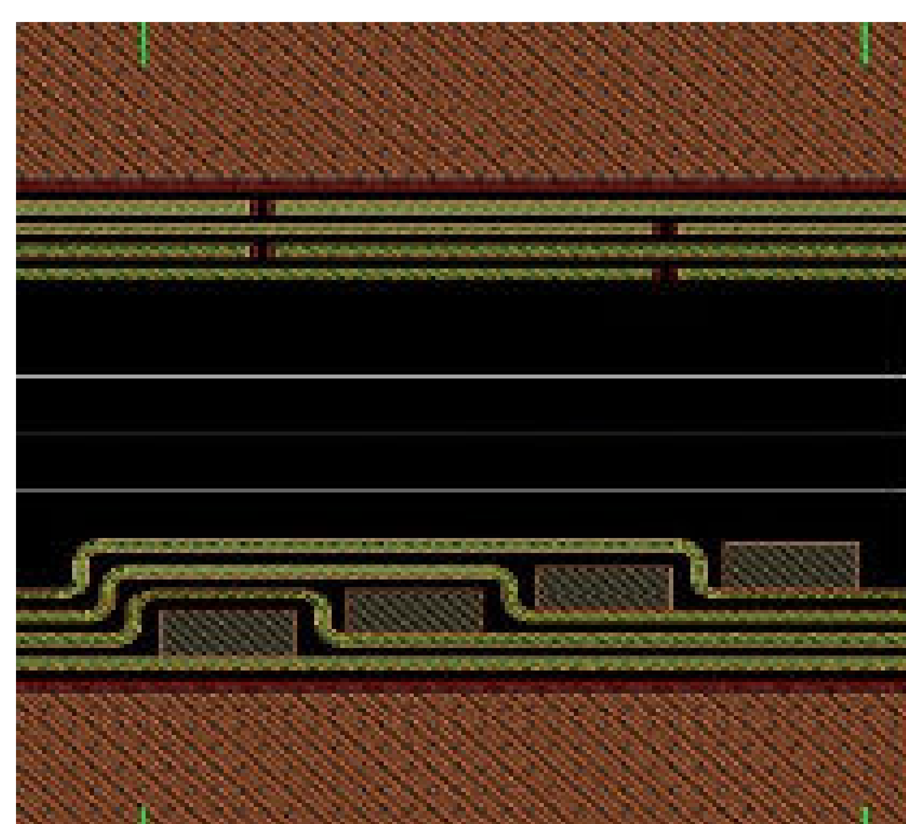
# Wafers :

- 40(-1) wafers 9x9 cm² from HPK ,
  - > Larger wafer give better ratio Active/dead zone
  - > ALAS, continuous guardring !!! (not as announced by HPK-France)

- R&D for wafers with discontinuous guardring at LLR

  proposals for common R&D with Czech , India, Korea

- R&D on wafers design to reduce the cost has just not started !! (CERN )



Guard rings protect Silicon sensors against breakdown

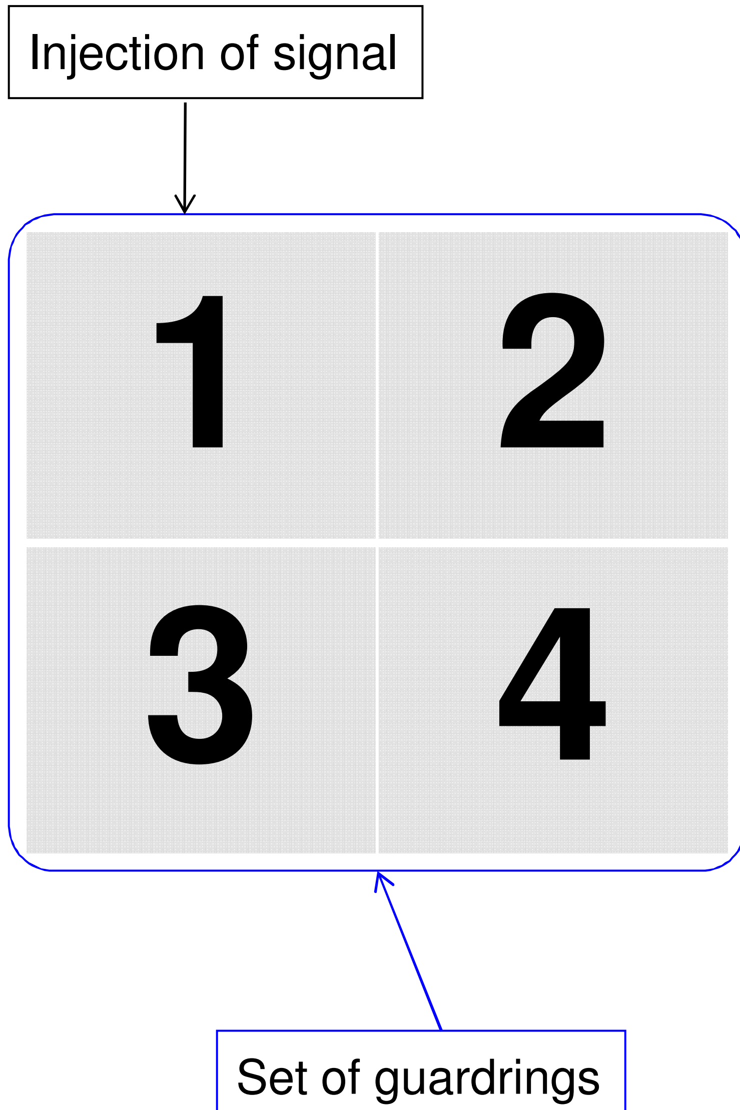
“Square events” when shower energy deposited in guard ring

Coupling between continuous ring and edge pixels

Studies underway to reduce effect with segmented guard rings
But what is the effect on surface leakage current ???

# Test with wafer from BARC-India

(Mumbai Atomic Research Center is member of CALICE)




Total crosstalk vs pixel number

dB

Pixel #

Seg. 3 mm
Seg. 1 cm
Continuous

# ASU :

- Gluing silicon wafer on ASU

- Validation of ASU before integration :

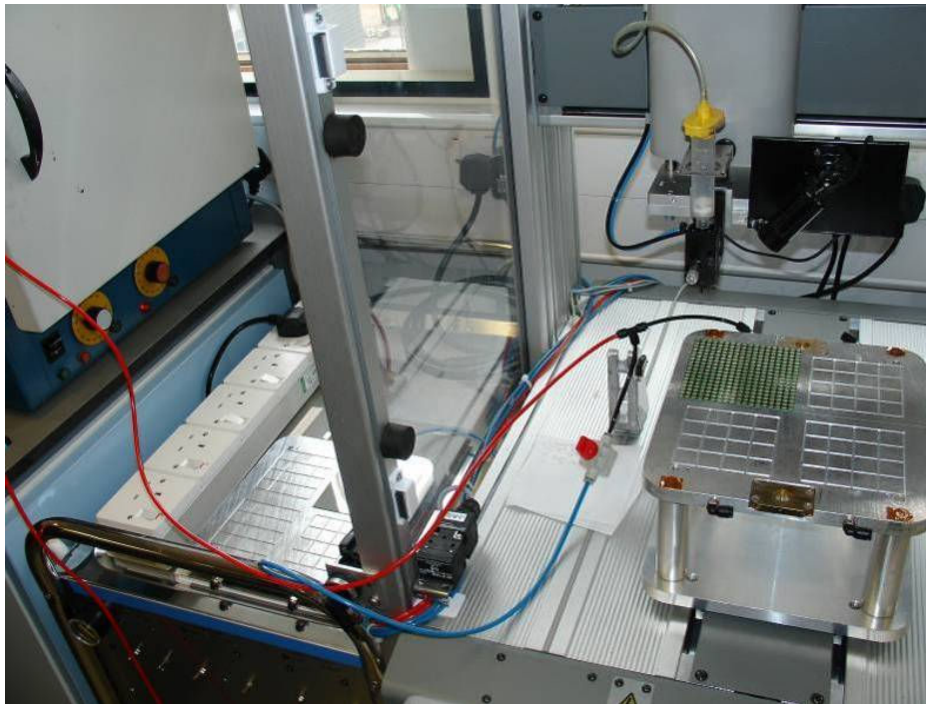
  >>>>> Connection at the end of the layer

- Connection between ASU

# Gluing silicon wafers on ASU :

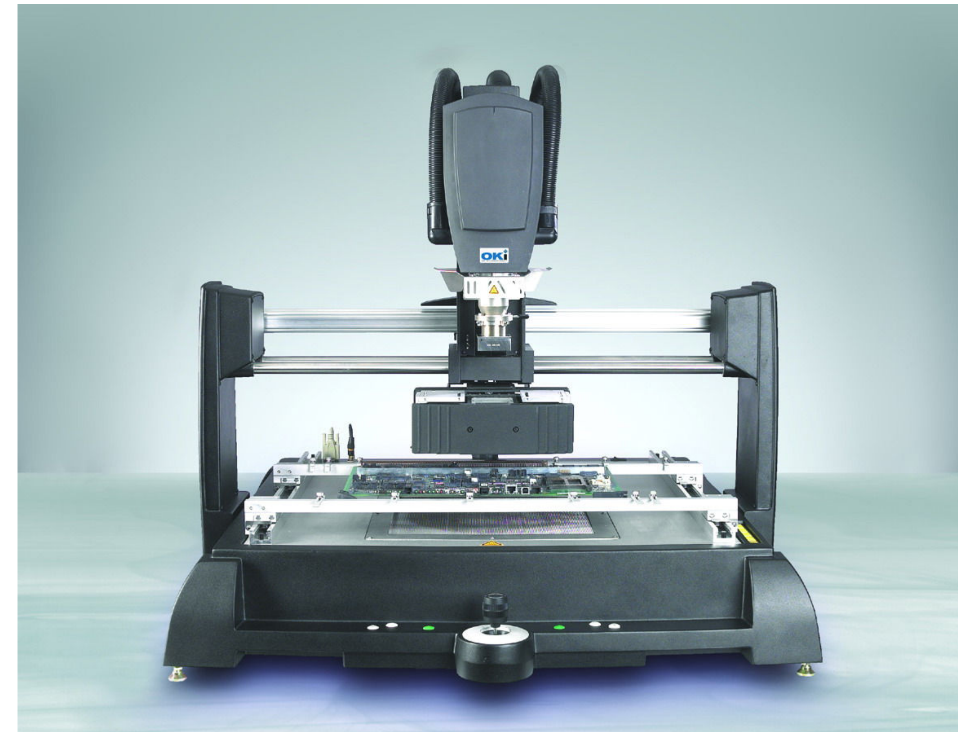
- Controlled glue dot deposition on the PCB
- The (four) Si Wafers are picked up, aligned and placed on the PCB
- Accurate thickness and planarity control via vacuum jigs
- The assembled ASU is allowed to cure

Test board with Dispenser Robot



"Gluing" rate 0.4 Hz

BGA Workstation for Wafer Placement




Precise Wafer Placement
by Split Field Optics

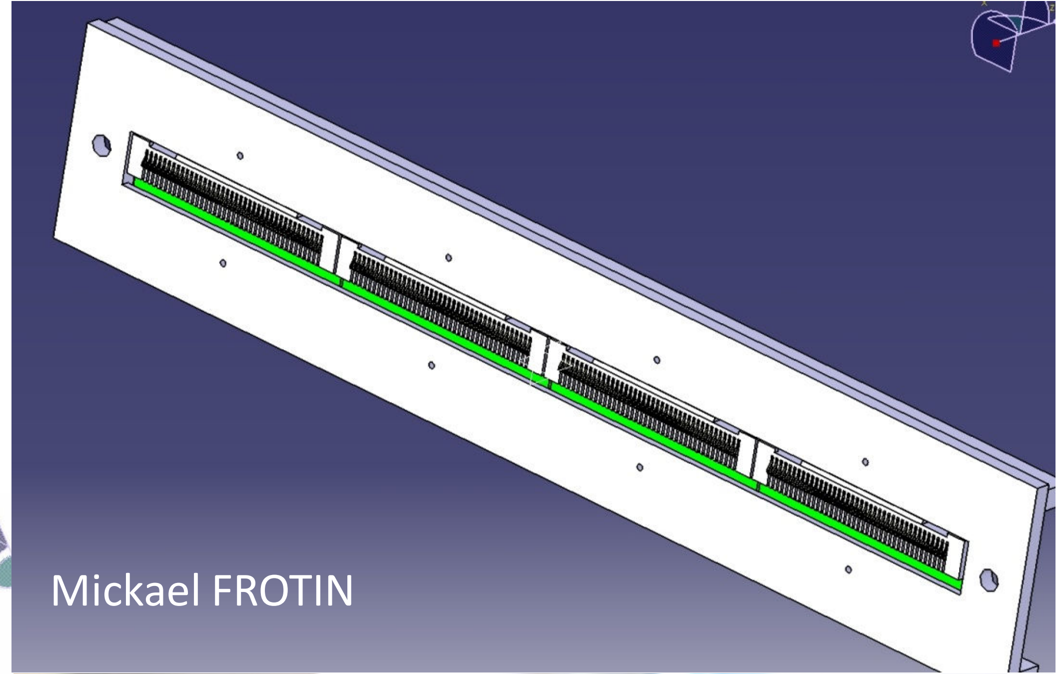
# ASU VALIDATION

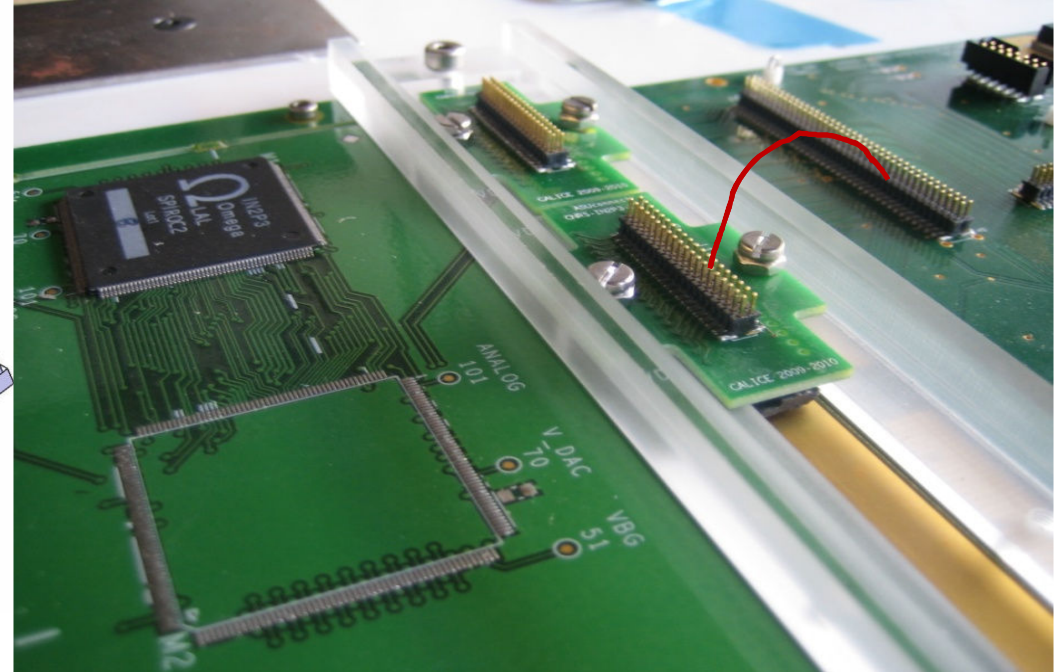
# Solderless connector (@LLR)

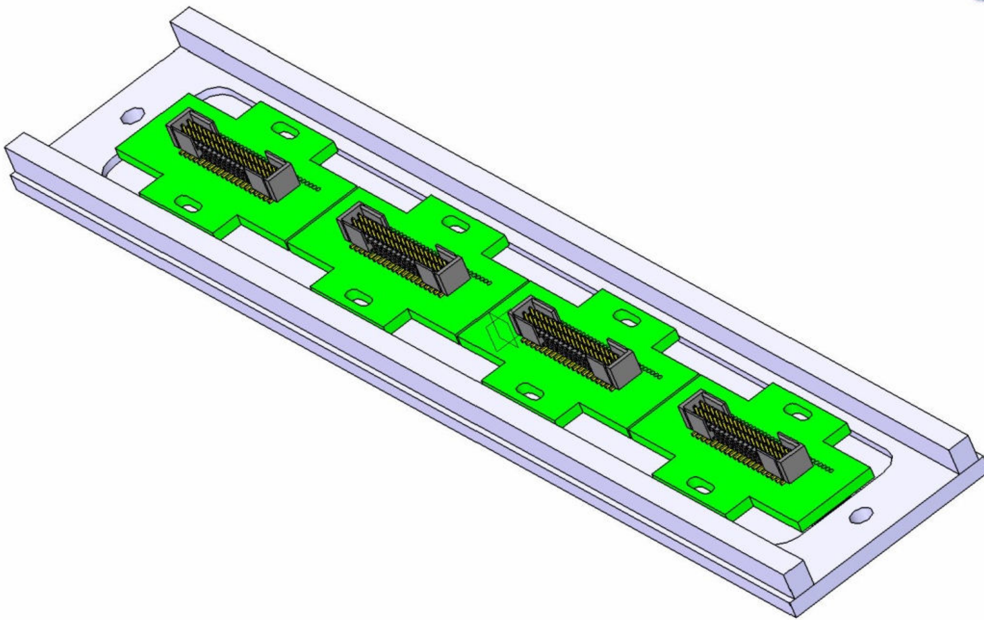
(quality test )

- Ready
- Start tests with

ASU 'CIP' version soon



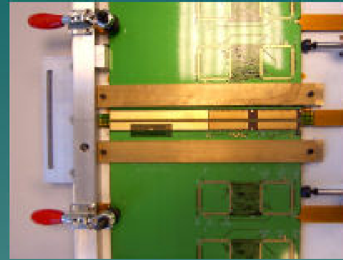
**Patch cables to be added**

# Assembly procedure

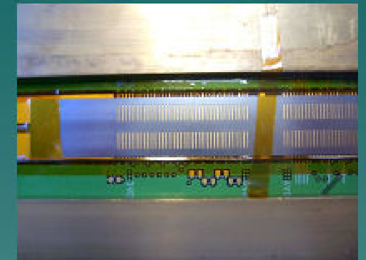
## @LAL, Cambridge

Rehearsal of the assembly of a slab
Some experience acquired thanks to the assembly of specific slabs for thermal test

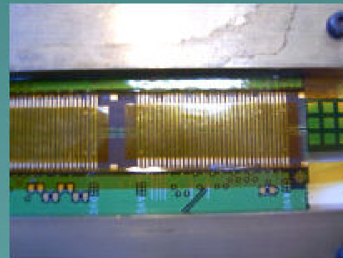
A procedure has been established including the calibration of the exposure time to the heating lamp



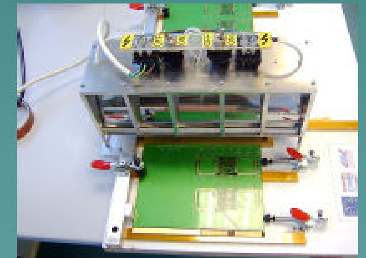
2 cards FEV7 CIP
on soldering bench



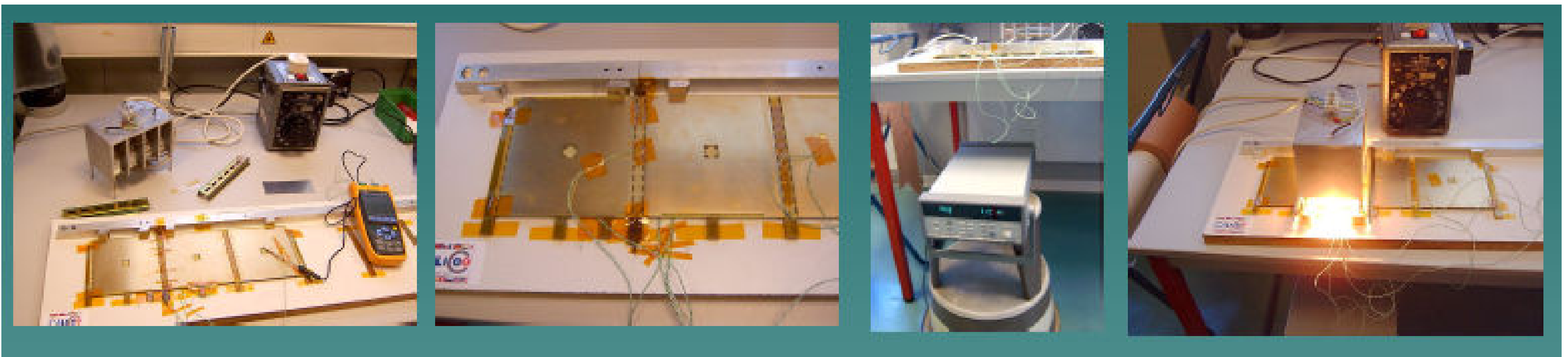
Raises the Screen printing
on board



Raises the kapton connectors

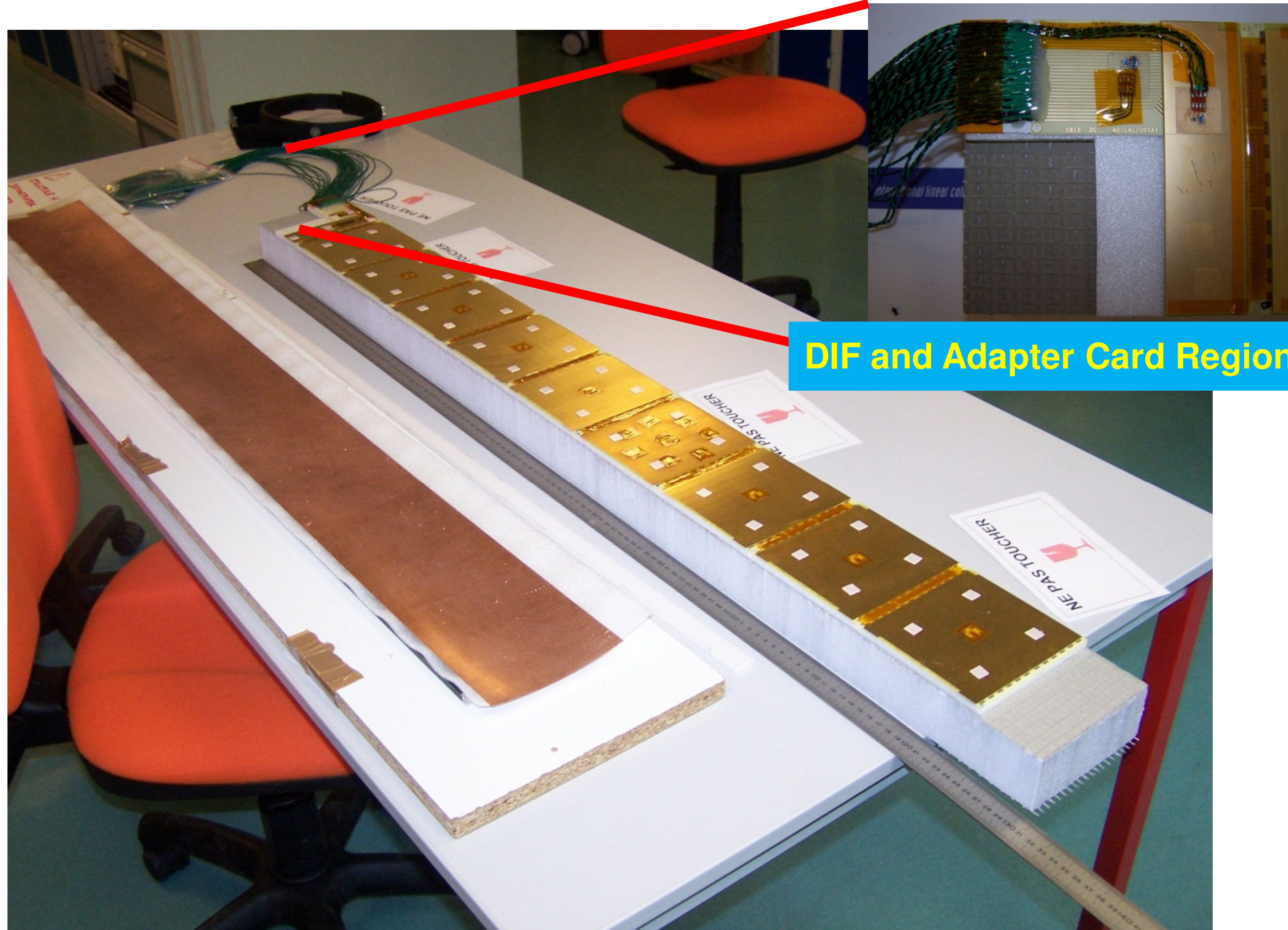


Set up for the lamp



# INTEGRATION : first test

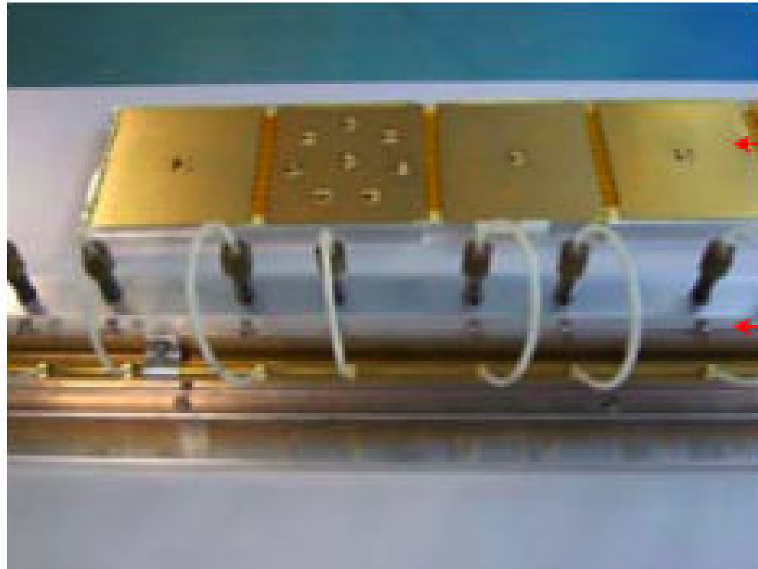
Thermal Layer –
Developping the Techniques for Layer Construction




Proof-of-principle to build long layers

# Example for Assembly Tools – Handling of fragile layers

## Handling by vacuum lifter



Line of ASU

Vacuum Lifter

Positioning of Vacuum Lifter on ASU Line

Vacuum Lifter

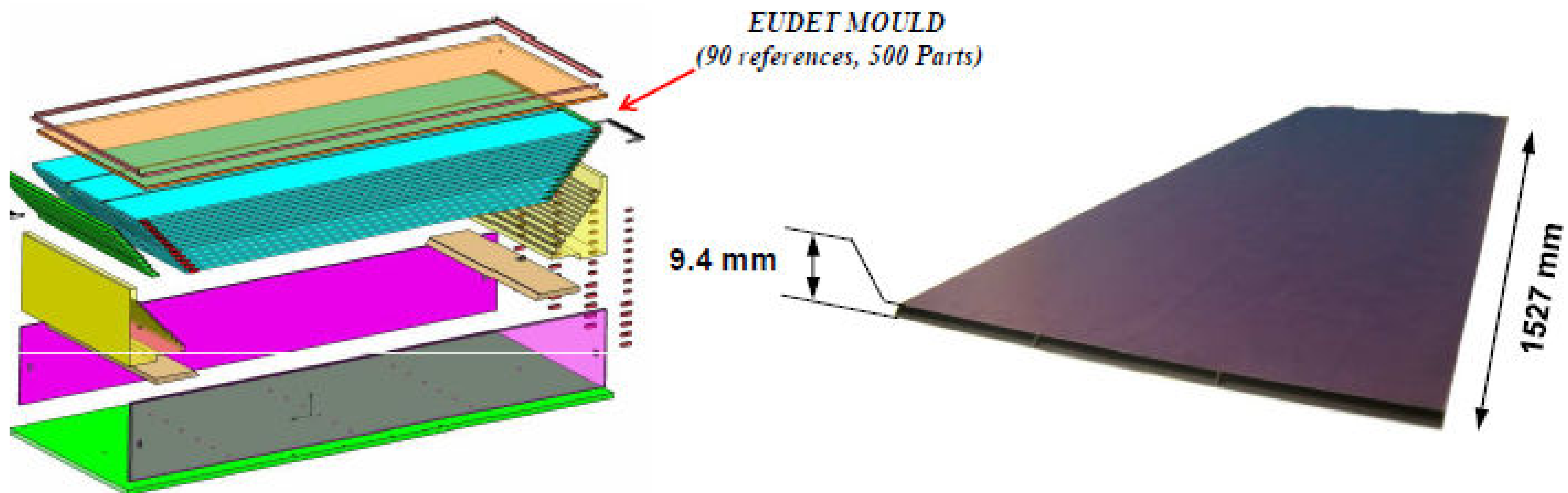
Line of ASU

**(Careful) handling of ASU Line established**

# MECHANICS :

Assembly mould is designed, the procedure for the call of offer has being launched.

The production of the first single layers will start very soon.




- ⇨ Global design : ***OK***
- ⇨ W and Carbon Needs : ***OK***
- ⇨ Detailed design description : ***OK***
- ⇨ Technical drawing : ***OK***
- ⇨ Ordered : ***MARS 10***

- ⇨ Global design : ***OK***
- ⇨ 1/15 "Alveolar EUDET layer" : ***OK***
- ⇨ Cutting Layer operation: ***OK***
- ⇨ The supplier for cutting layer : ***OK***
- ⇨ Layers Production : ***Mars 10***

**Assembling the structure next september**

**(with prior , a test in autoclave with only the mould)**

Foreseen next is the destructive test of the demonstrator (after use for Thermal R&D)

If you want to test something there … contact us ASAP

# Summary and conclusions - 1

- First test with ASU , SPIROC and new generation DAQ in fall 2010 (with SKIROC ??)
- Feed the structure with one SLAB (not all silicon equipped, but all the ASU) 1/2011
- Feed with scintillator SLAB 2/2011
- Test with a 24X0 tower in test beam ?? May be end of 2011 or start of 2012 ??

(with power pulsing, new silicon wafers, etc…)

# Summary and conclusions - 2

- Essentials R&D on silicon are on stand-by (low resource both on material and Manpower)

- Funding will be a problem to proceed with the mandatory R&D (silicon, slab integration, mechanics, etc…) i.e. the budget 2010 from CNRS for material has been reduce by 2/3
  But remember, when **including the manpower salaries, the budget is still above 1Meuro/year**

- Travel budget will not allows FNAL Test Beam (except if laboratories will use their own resource…)

- Where are the ECAL contributions from Russia, Czech group , EWHA ?
  Cambridge in UK is alone, very low resource in France LLR/LAL/LPSC ….
  New contribution possible in future from Korea, etc… but today , the situation is critical
  Therefore , We decide with Japanese groups to have only **ONE ECAL** project

European contract **AIDA** is the only possible way to continue on silicon sensors !!
(if negotiation don't reduce too much and if the repartition allows ECAL to do something)

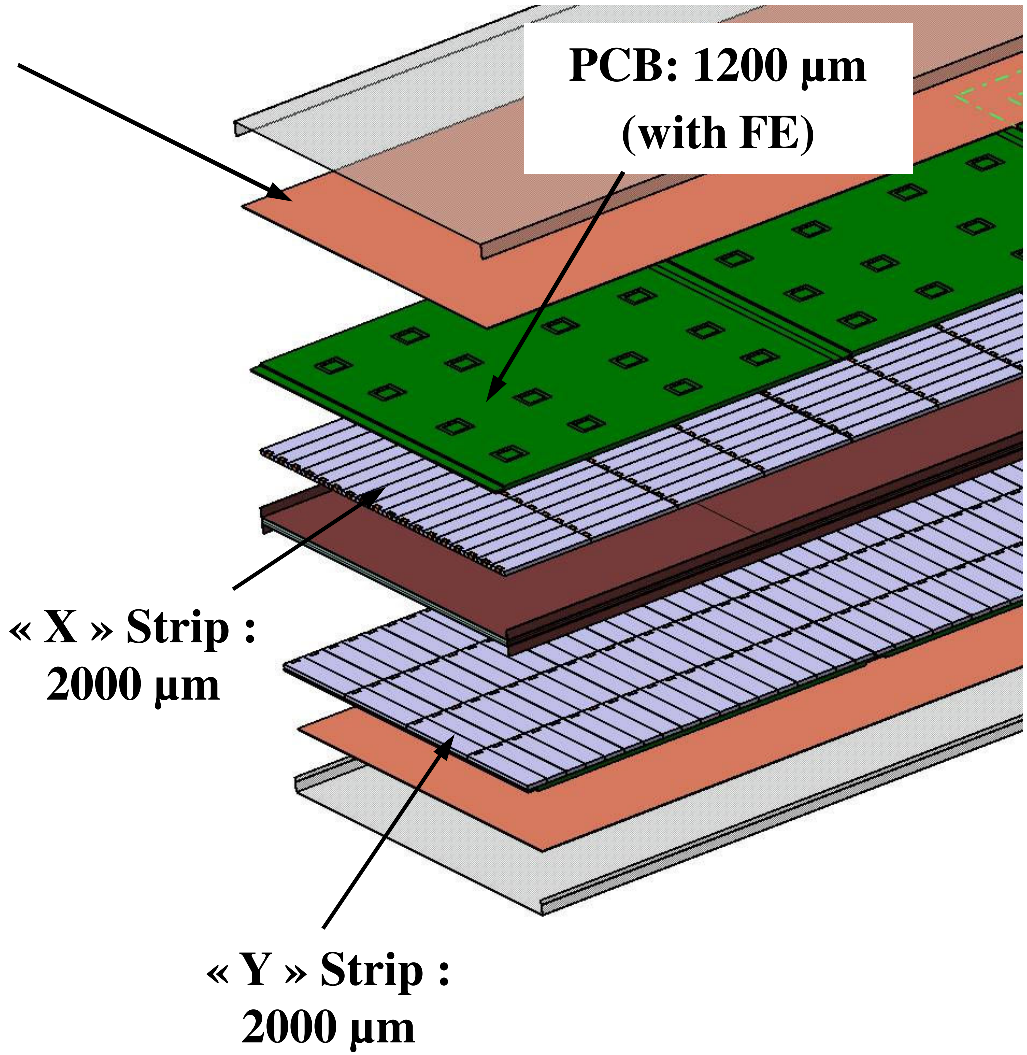
CLIC never speak about ECAL …. May be they will have to do it, one these days !!!

# Common design for silicon or scintillator :

**ECAL W/Si**

**ECAL W/Scin**

**Heat shield: 100+400 µm (copper)**



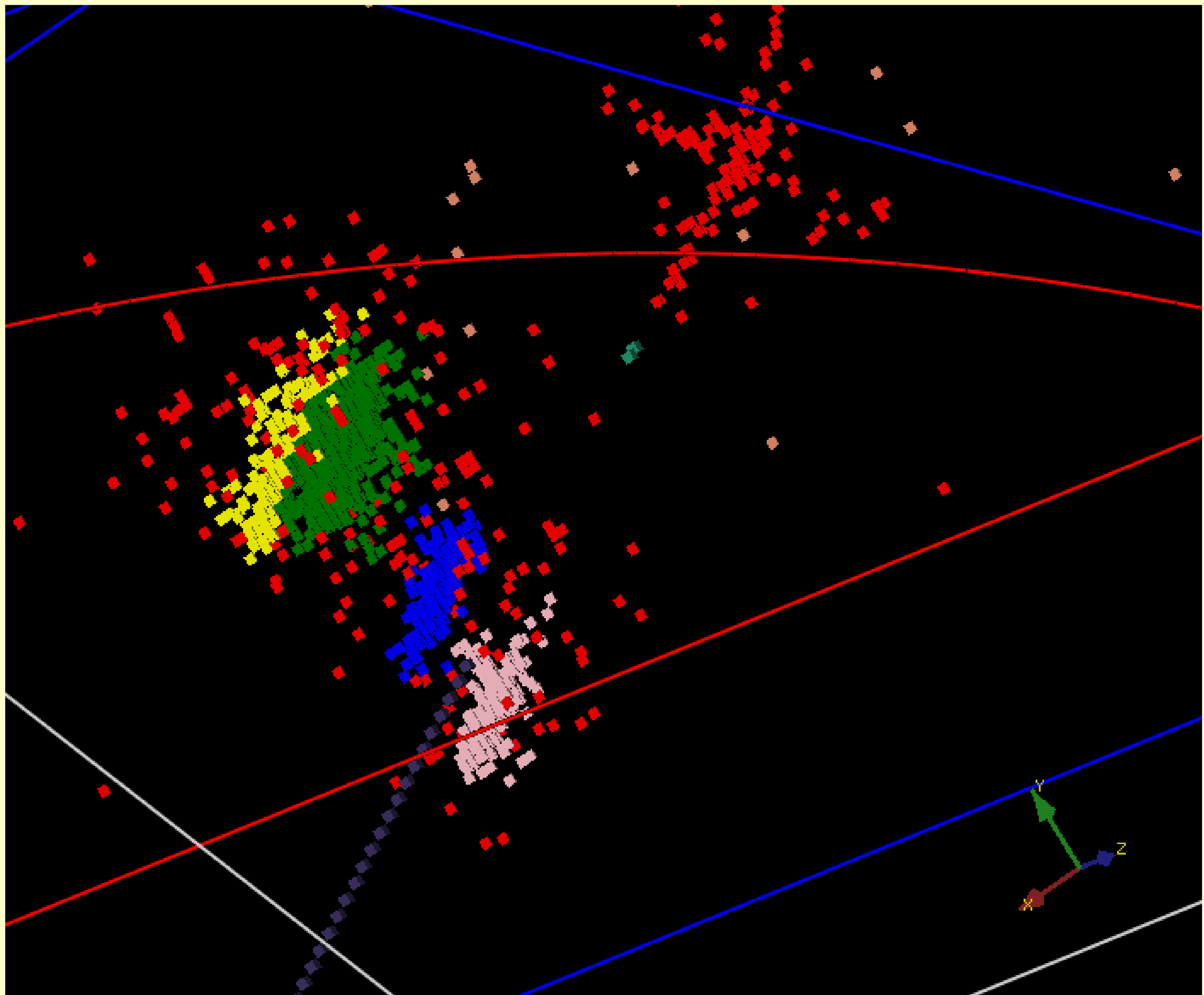

**PCB: 1200 µm (with FE embedded)**

**wafer: 325 µm**

**glue: 75 µm**

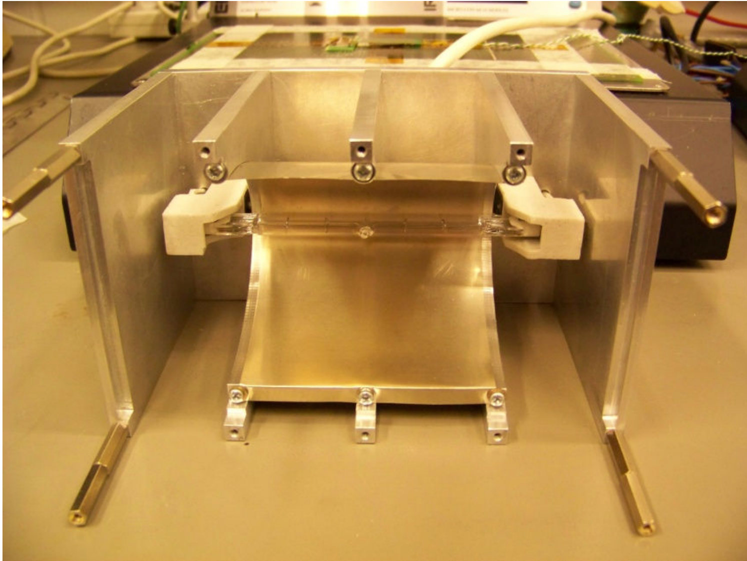
**HV Kapton® film: 100 µm**

# Granularity is beautiful

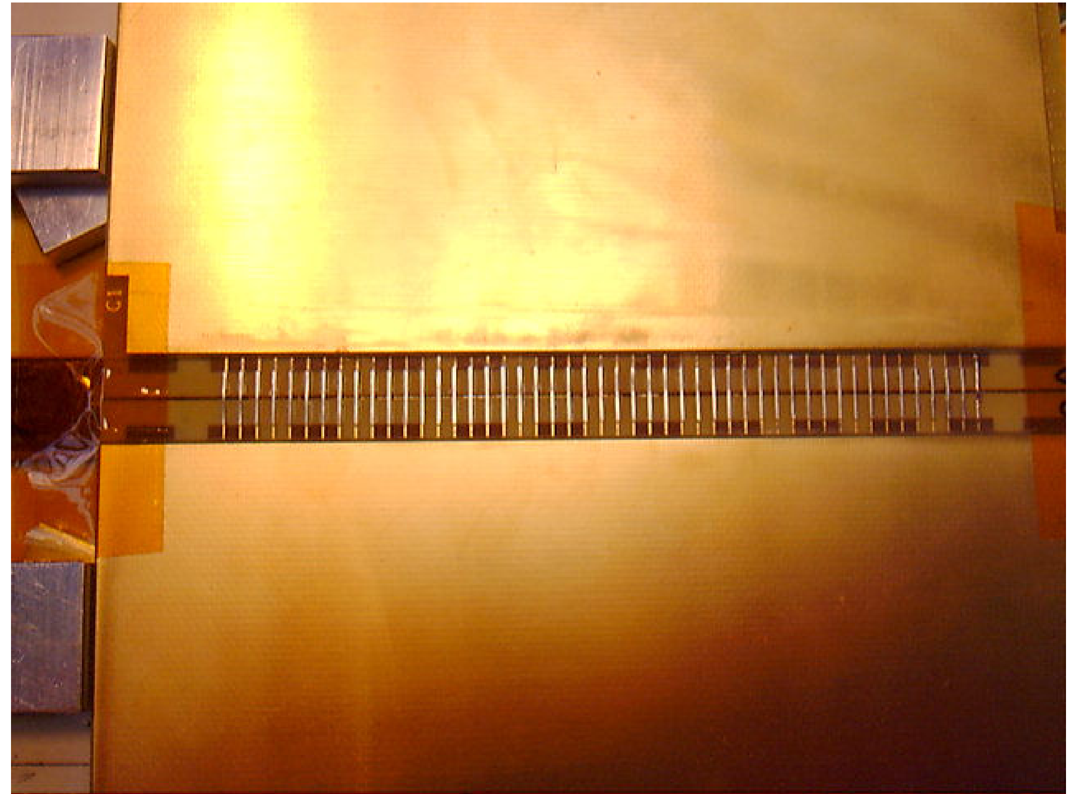


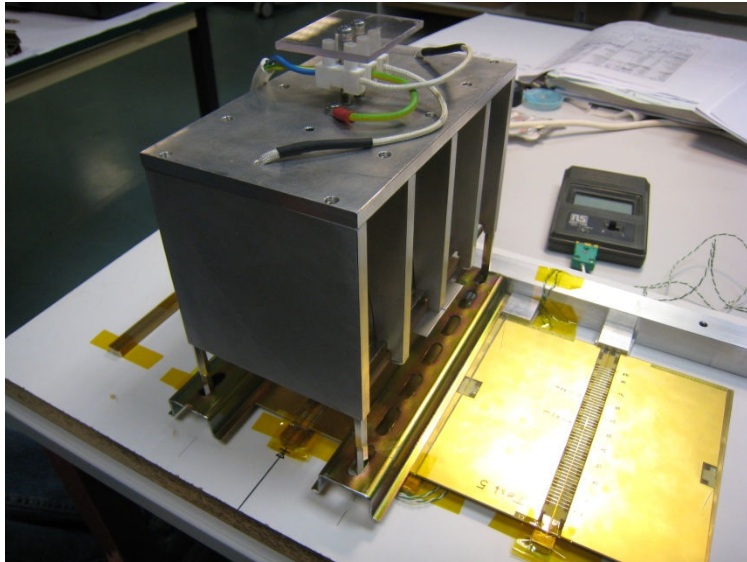
# SPARES

# ASUs to SLAB



The joint between two boards





- Joint by halogen lamp heating up tin-bismuth soldering paste (Method developed by U. Cambridge)

- Heating Temperature ~200º C

Delicate Process for Demonstrator – Easier for EUDET Module