Recent & future developments in the DAQ2 integration

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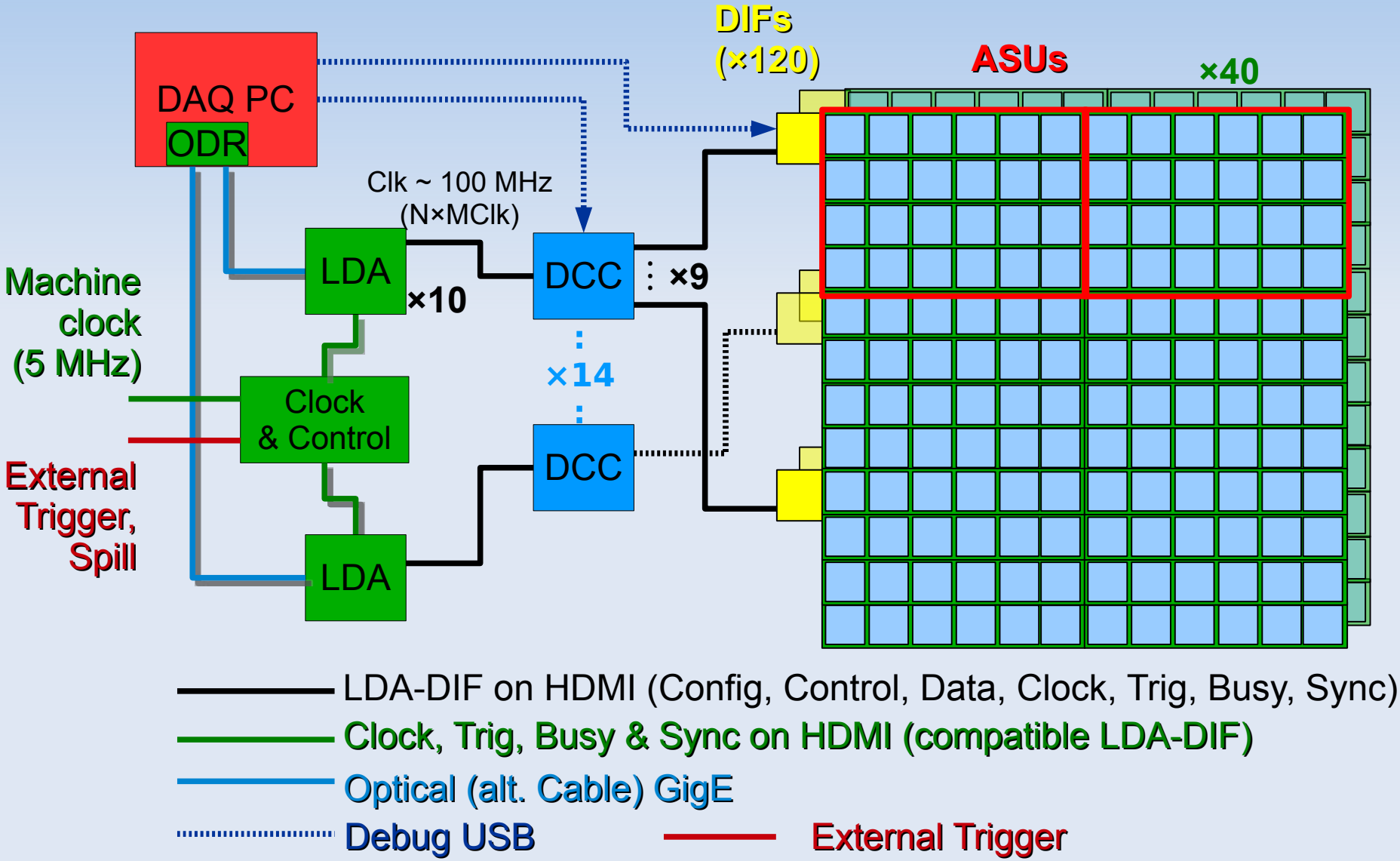
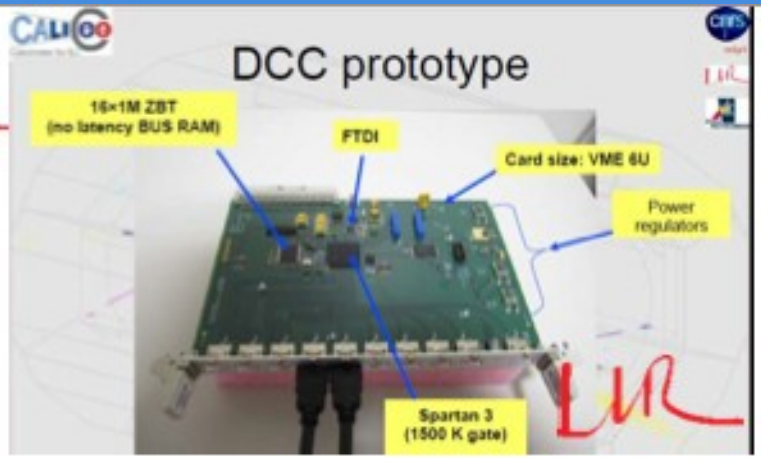
Forewords

- Imprecise view → needs sharping up
  - Un-even view
  - Reschuffling due to stepping down of UK
  - New actors ? AIDA ?
- Key dates
  - AHCAL
    - Now (LabView + USB)
    - TB end of 2010 / 2011
  - SDHCAL
    - TB 3×m² Mai—Fall 2010
      - USB + CCC (+ DCC) → DAQ-II
    - Cosmics tests : Summer—Fall check of 40 planes
      - probably on USB (rates ~ 100 Hz)
    - M3 → Spring 2011
  - ECAL
    - Cosmic in Summer
      - FEV COB ; 1 chip; 1 Wafer
      - Lecture DIF USB then USB+DCC+DIF
    - Some short Slabs in Spring 2011
    - Full set-up end 2011 ?

EUDET DAQ2 (for the DHCAL)





LDA

- The LDA (from Enterpoint) consists of :
  - Mulldonoch2 baseboard;
  - add-on HDMI board to connect to 10 DIFs;
  - an add-on ethernet board to connect to an ODR.
- Firmware development :
  - DIF <=> LDA link running;
  - new code soon to be posted to svn;
  - same format as ODR in svn repository.

Gig Eth validated

DCC and LDA are essentially similar to an ethernet switch but using a low level protocol

They both fan-out/in fast isochronous signals on a dedicated path and commands on the 8b/10b serial link

LDA has a fast link : Gb ethernet to the upper level = ODR, and can connect to 10 DIFs or DCC with the 8b/10b serial link

DCC can connect to 1 LDA and 9 DIFs using the 8b/10b serial link, data from DIF are buffered and sent to the LDA

CCC

- Overall status unchanged for a while.
- Fans out clocks, fast commands and control signals.
- Fans in busy.
- Full complement of 10 boards with power supplies tested.
- One in LLR and one in LAPP.
- CCC link to LDA still needs to be done :
  - Board designed and firmware developed for testing;
  - Soon to produce enough boards for all LDAs.

⚠ Big effort done ⚠

ODR

- Receive data on 4x fibre (RX),
- Write to disk FAST (>150MB)
- Send data up fibre (TX)
- Controlled from Linux driver
- DOOCs Interface

Documentation / repository

- All components *should* have extensive documentation on twiki : it is being updated and as components are basically done, can soon be finalised.
- Twiki main :

  https://twiki.cern.ch/twiki/bin/view/CALICE/CALICEDAQ
- Also list of hardware availability /status started.

  https://twiki.cern.ch/twiki/bin/view/CALICE/HardwareList

HW status (DIFs)

- DIF ECAL OK
  - A few (~15 [⊃ 6 in LLR]) for tests
  - Material for 40 more available in total
- DIF AHCAL
- DIF DHCAL
  - 20 protos available
    - 1-2 defects
    - Tests of µMegas & Dirac
    - 1 DAQ test (LLR)
    - 5 (soon 9) for 3 RPCs m^2
  - “Emergency” prod of 20
  - Additionnal prod of 150 cards (prod by LAPP funded ANR DHCAL +LLR)
    - See Julie's talk

Tests with DHCAL DIF

Two weeks ago, Guillaume went to LLR, to make the first tests with the LAPP DIF and the DCC

We passed the tests successfully :

Send Fast commands from DCC.

Send Block Transfer command from DCC.

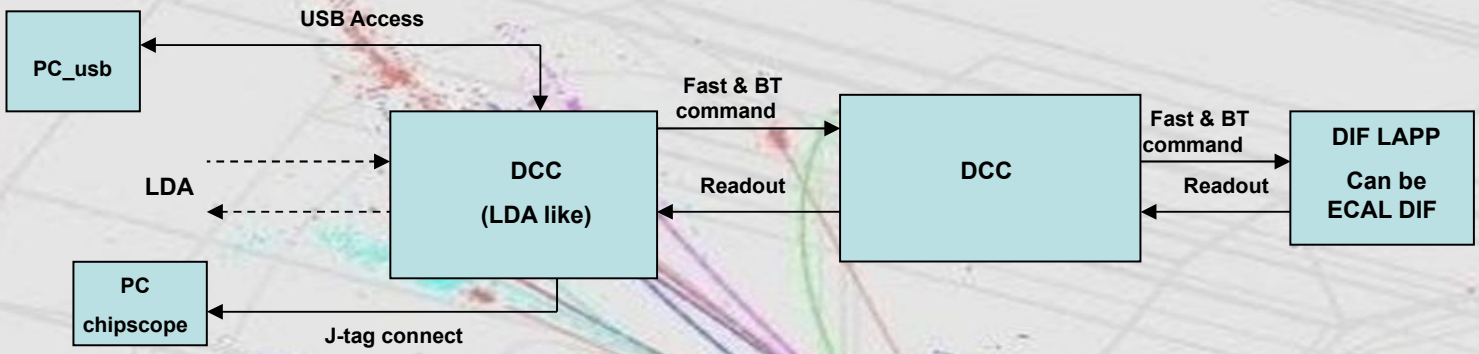
Received an “acknowledge” from the DIF on DCC after sending the commands above.

Remarks :

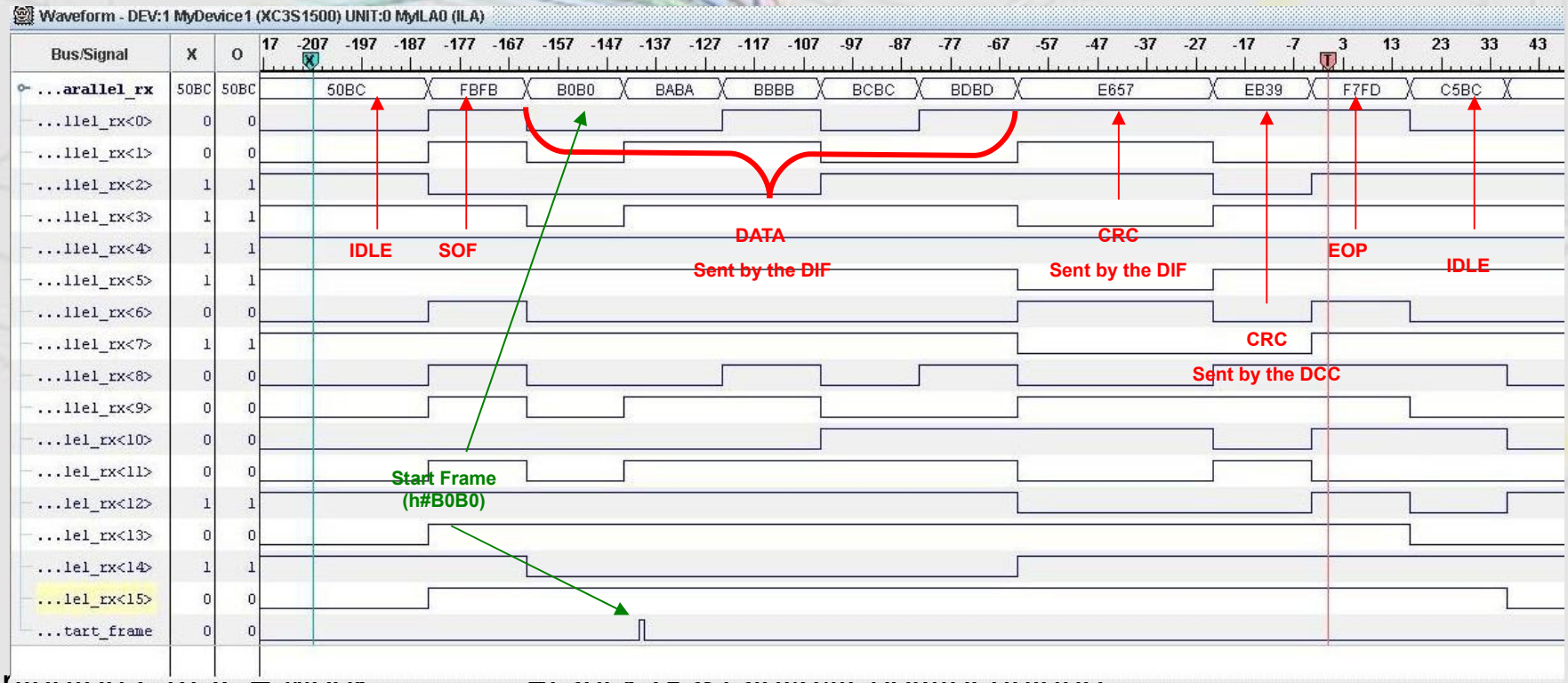
All commands were sent through the USB connection on the DCC

The received data (acknowledge) were checked by Chipscope (Xilinx logic analyzer).

DCC — DHCAL DIF comm test



Result seen on Chipscope



Summary

- Firmware :
  - USB : Some bugs for the readout are under investigation and will be solved in a few days.
  - HDMI link : the link is locked when the DCC is connected with the DIF or the LDA. About LDA, only the connection have been tested.
  - Next step of tests with LDA : command & readout.
  - Some improvements are needed on main firmware to work with a full DCC
- DCC card :
  - Improvements on routing are made before the launch of the production

HW Status (DCC)

- 2 protos + 1 proto0 available
- Prod of 20 cards (funded ANR DHCAL +LLR)
  - Proto ~ OK.
  - → End of March
    - Components schuffling (improvement of routing)
    - Bigger (and cheaper) FPGA
    - Launch of prod → April-May
  - until June
    - Improvement of firmware and tests with DIF and LDA
  - June-July
    - Complete stress tests
  - avail in Sept 2010 for TB

FW status

- SVN repositories @ CAM, Lyon, CCIN2P3, Cambridge, CERN → listed on Calice DAQ pages *(to be updated)*
- DIF task force (RC (LLR), JP (LAPP), BH (CAM), MR (DESY)
  - Definition of DIF φ connection LDA ←→ DIF ←→ ASU/HBU
    - Reference document
    - Some specification forgotten (value of VCC on one pair)
  - Definition of DIF link protocol done
    - Needs reference document
  - Cooperation on blocs in FW
    - See Rémi's Talk
    - DIF task force Meeting end of March

- ASIC interface:
  - ECAL → link to Spiroc/Skiroc
  - AHCAL: Exists
  - DHCAL: JP, GV working with USB
- Comm. bus (RC)
  - Now “Hardwired comm.” → end of March
  - Bus for re—usability & usable dev^{t}
- USB “standard” (FTDI chip)
- HDMI interface (bloc from M. Kelly :left in nov.)
  - Adapt ECAL ✔ (RC, FG) → AHCAL
  - Adapt DHCAL (Xilinks) on going (JP, GV)

FW status (DCC)

- same blocs as LDA & DIF
  - Good way to learn & integrate code of MK
  - Now @ 50 MHz
- Connection 1 ch. USB→DCC→DCC→DIF (Physical test)
  - OK data readout
  - OK fast commands
  - OK config commands
- Connection many channels
  - Simulated: 4 channels ✔
    - Space limitation removed → OK for 9 channels
- USB will be used for first test
  - DHCAL TB in Mai ? (Aggressive)

FW Status (LDA)

- Code taken over by BH & MW
  - First test OK (see Rémi's talk)
- Complete review / hand over on the 17th of Match → UCL
  - Link LDA_DIF
  - DIF = DIF module + pattern gen.
  - ODR ou GEth ?
  - LDA code
    - Checking of IP licences
    - Discussion on maintenance / needed completion
      - Good experience from FG on this code
      - Devt @ LLR on G-Eth

FW status (CCC)

- Working CCC code
  - MW follows the code & ready to adapt
    - trigger logic
    - Busy logic etc.
- Shipping of 3 cards
  - 1 LLR for test bench
  - 1 LAPP, 1 IPNL for sync of many DIF
- direct connections CCC-DIF
  - clock & trigger distribution
  - Sync commands (Sync, Reset)
    - FW by LAPP ←→ MW
    - for TB in May...
- *Could be also used for AHCAL TB as asap.*
  - *needs DIF FW adapt (clock, trigger)*

Next actions

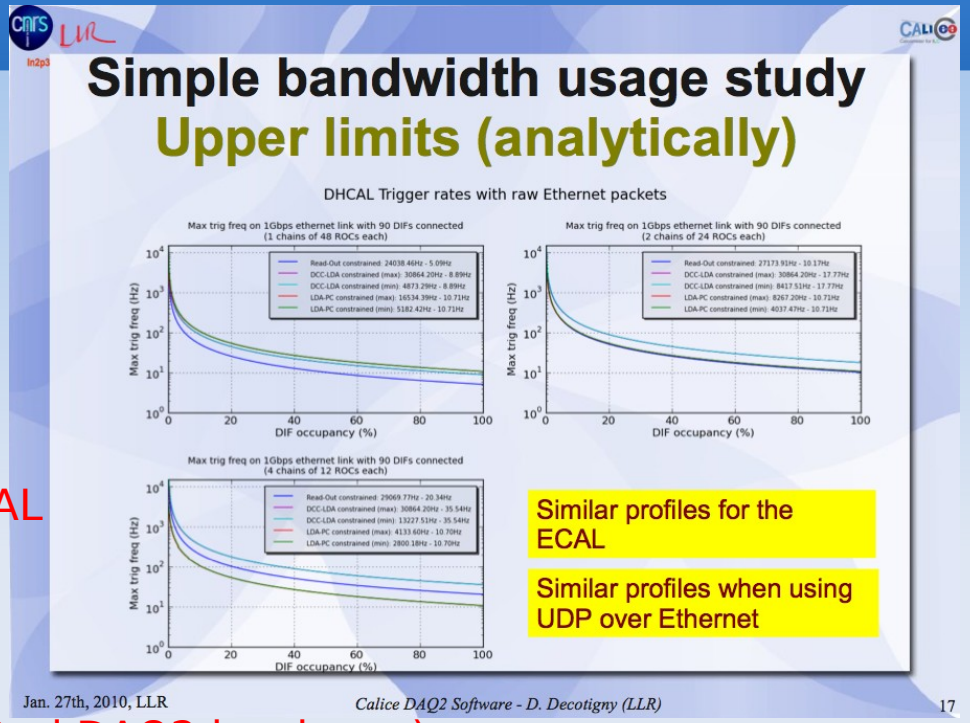
- "Validation of complete chain" with support for intermediate steps
- Feb.
  - Inclusion CCC-Dhcal DIF (on going)
    - synch.
- March
  - Code DIF ⊃ 8b10b ✔
  - Launch of DHCAL DIF prod ✔
  - DIF Common framework (on going)
- End of spring
  - Validate first setup with DCC+CCC controlling a m² over USB → TB ?
- May
  - System test
- June
  - Geth+LDA+DCC+DIF (Done)
  - Stress tests

Next activities (2)

- Fall
  - DIF FW complete
  - integrate the LDA In parallel
    - R/O by Ethernet
- End of 2010:
  - Integrated the ODR
- Jan 2011
  - Ready for 1 m^3
    - 2 LDA
    - 14 DCC
    - 120 DHCAL DIFs
- Pending
  - Stress tests
  - 50 MHz
    - 80-100 MHz for 2011

Software status (General)

- Dev^{t} in DOOCS on hold (since departure of TW, VB)
  - DD has collected the code & experience
  - Mainly ODR driver & config Database
- “Small works”
  - Simulation of DAQ data flow SDHCAL, ECAL
    - System C
  - Evaluation of reassembly & stability
  - Evaluate LCIO storage on real PC (simulated DAQ2 hardware)



- Fall 2010: Topology-aware slow-control config database + tools to generate the SC blocks
- Fall 2010: Abstract SW layer to indifferently drive LDA/Ethernet or DCC/USB
  - Xdaq + DOOCS + Tango
- Data format
  - Identifier & Headers formalized
  - incl for LCIO

Possible integration of all detectors there *ROC, DIRAC, DCAL's

RAW data proposal (suitable for ROCs)

V. Boudry, R. Cornat, D. Decotigny

LCIO format (source):
https://svn.in2p3.fr/calice/online-sw/trunk/daq/reassembler/lcio_dump.hpp?view=markup

Physical address (⊃ redundancy)

Event Counter/Tagging

Event Timing

Compacity vs Redundancy (debugging)

```
* Event:
*  - DetectorName <- runHdr::DetectorName
*  - RunNumber    <- runHdr::RunNumber
*  - EventNumber  <- ROEventId::toUnsigned()
*  - TimeStamp: default
*  - Weight: default
*  - LCCollection "rawdata_DIF:str(DIF_id)":
*         + param "id_ODR" (unsigned): from raw event
*         + param "id_LDA" (u32b)
*         + param "id_LDA_diflink" (unsigned)
*         + param "id_DIF" (unsigned)
*         + param "TrainNumber" (unsigned)      // since DAQ start
*         + param "BC_DIF" (unsigned)           // since RUN start
*         + param "DeltaCounter" (unsigned)     // 40 MHz counter
*         + param optional extra DIF info (type, temp, adc) ???
*         + elt[0]: LCGenericObject
*              + int[0]: id_roc_chain
*              + int[1]: id_roc
*              + int[2]: index_in_dif_dump (starts at 0)
*              + int[3]: chipType
*              + int[4]: acqMode
*              + For HR2 chips:
*                 + int[5]: nframes (< 128)
*                 + int[6 + i*5]: bcid for frame i (i in [0, nframes])
*                 + int[7 and 8 + i*5]: t0 vector (msb 7=t0_63, lsb 8=t0_0)
*                 + int[9 and 10 + i*5]: t1 vector (msb 9=t0_63, lsb 10=t0_0)
*                 + int[11 + i *5...]: additional data ??
*        + elt[1]: other LCGenericObject (ROC event)
*           ...
*  - other LCCollection "rawdata_DIF:str(DIF_id)":
*    ....
```

```
namespace IO
{
  class LCWriter;
};
/**
 *
 * Run Header:
 *   - RunNumber: user-specified
 *   - DetectorName: user-specified
 *   - Description: user-specified
 *   - ActiveSubdetectors: [ "DIF_rawdata" ]
 *
```

RAW Data ”in the tubes” format:
https://svn.in2p3.fr/calice/online-sw/trunk/daq/calice_packets/calice_raw_formats.h?view=markup

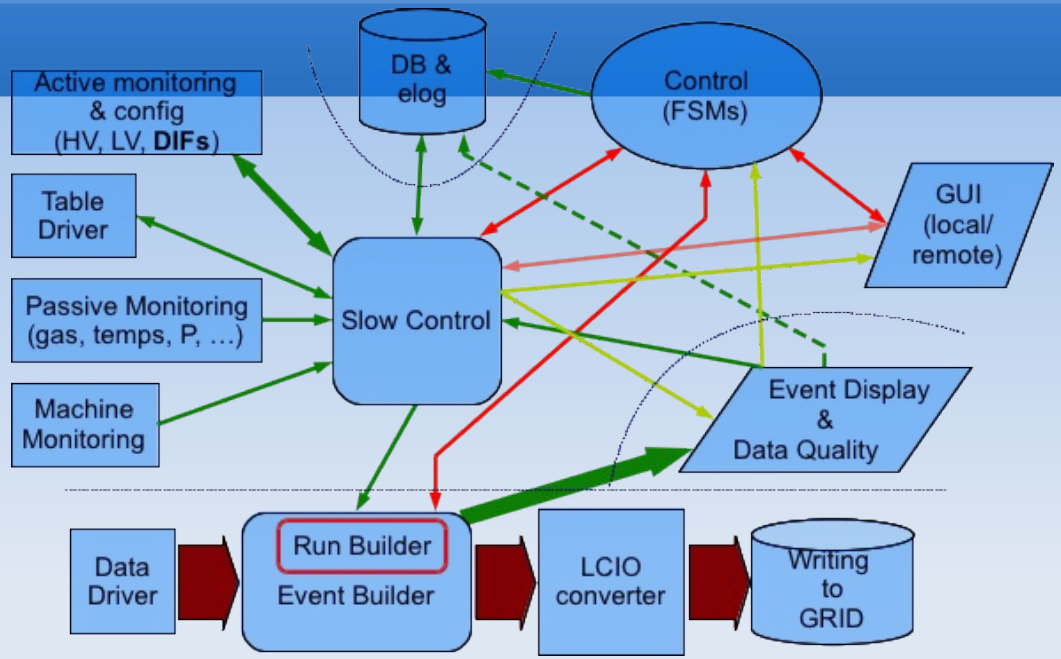
LCIO format for reconstructed DHCAL Calorimeter hits (proposal v0.01)

ILD and TB compatible

```
EVENT::RawCalorimeterHit
{
    int  _cellID0;          // Chan (64 ==> 6b)
                            // + Asic (max 420 ==> 9-10b)
                            // + Dif_Id (48-144 ==> 7-8b)
                            // + Module_Id (40 Barrel + 24 Endcap ==> 6b)
                            // == 28-30b (remain 2-4b)  [6+6+7 == 19b in TB]
     int _cellID1;          // Time2Previous (in BC) ==> 24b (remain 8b) (CHBIT_ID1 must be set)
    int  _amplitude;        // 3 Thr ==> 2b (remains 30)
    int  _timeStamp;        // Rec Time on 32b wrt (Spill start | Ext. Trigger)
}


EVENT::CalorimeterHit
// Recontructed Hits
{
    int  _cellID0;           // Idem RAW
    int  _cellID1;           // Idem RAW (CHBIT_ID1 must be set)
    float    _energy;       // Rec Energy
    float    _time;         // time from ref (in ns).(LCIO::RCHBIT_TIME must be set)
    (float   _position [3]);   // Position (unit not fixed) (LCIO.CHBIT_LONG must be set)
    int  _type;              // Deposit type (mip, EM, noise, ...)
    EVENT::LCObject *  _rawHit; // Link to RAW hit
}

One also needs the mapping functions:    int[3] GetIJK(cellID);
                                         float[3] GetXYZ(cellID);

Error on Energy => to be recalculated, or integrated to energy.
```

SW status (XDAQ)

- XDAQ (see Christophe's talk)
  - Very well advanced for DHCAL
    - TB at CERN
    - Cosmics test
  - Very Strong support from L. Mirabito
    - Wrote CMS tracking DAQ
    - Participated to dev^{t} of the FrameWork
  - Natural candidate for Data stream
    - ~all outside DB, SC, Display (rootbased)
  - Interest at ILD // DAQ session from other R&D collaboration/projects
    - for combined TB



Conclusions

- slow Pull-out of UK but
  - HW is OK (last part GigE of LDA ✔)
  - FW → LDA critical pt
    - Will see in march
    - should be OK with synergy with DCC
- Manpower
  - “Not too bad”
    - too French ?
      - AIDA might help (RHUL, Bristol part of AIDA)
    - Sharing ok BUT needs coordination
    - Thanks to various delais (esp. ECAL)
- Slowly converging
  - In time for large TB
  - ILC-like tests will require additionnal HW : Beam InterFace (BIF) card

AIDA sub package 8.6.2 (!)

- Development of combined beam tests and common DAQ
  - Merge the EUDAQ and CALICE DAQ software framework providing the base for a common DAQ, including access to the test beam facility information (LLR, UNIGE, LAPP, RHUL, UNIBRIS);
  - Develop the hardware part of the common DAQ to allow the synchronisation of all the systems and to permit the work in ILC like mode (post-readout of bunch trains) (LLR, UNIGE, LAPP, RHUL, UNIBRIS);
  - Develop System Interfaces to existing LC detector subsystems (LUND, ULB, LPNHE, TAU, IFJPAN);
  - Extend the readout for high fluxes (LUND, ULB, RHUL)
    (TPC specific; µTCA testing)

• EUDET TLU
• our CCC
• new BIF card

- 400k€ requested
- All ILC Detector R&D involced (CALICE, TPC, VTX, SiTr, FwdCal)
  - Critical for EUDET telescope
- First “pre-AIDA” meeting in Palaiseau before ILD meeting
  http://ilcagenda.linearcollider.org/conferenceDisplay.py?confId=4333

Who's who

- *MK* = Mark Kelly – formʸ CAM (since Oct 09 in private cie)
- BH = Bart Hommels – CAM
- MW = Matt Warren – UCL
- *VB* = Valeria Bartsch – formʸ UCL (since June 09 at Bristol)
- *TW* = Tao Wu – fromʸ UCL (left since march 09)
- FK = Frantisek Krivan – DESY
- MR = Matthias Reinecke – DESY
- GV = Guillaume Vouters – LAPP
- JP = Julie Prast – LAPP
- CC = Christophe Combaret – IPNL
- LM = Laurent Mirabito – IPNL
- RDN = Rodolphe Della Negra - IPNL
- RC = Rémi Cornat – LLR
- FG = Franck Gastaldi – LLR
- DD = David Decotigny – LLR