SKIROC2 unveiled !!

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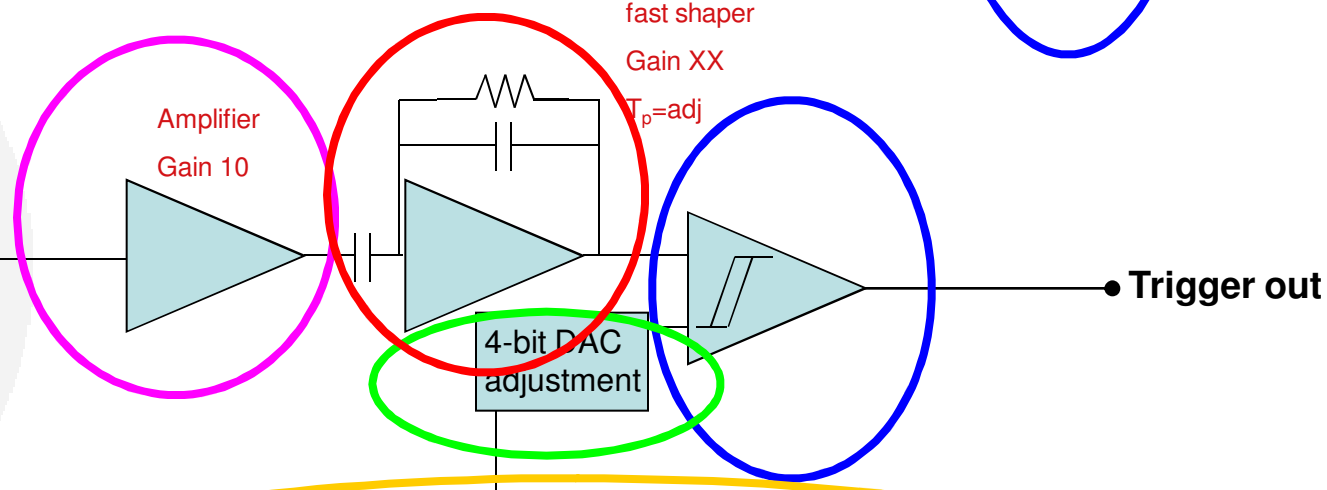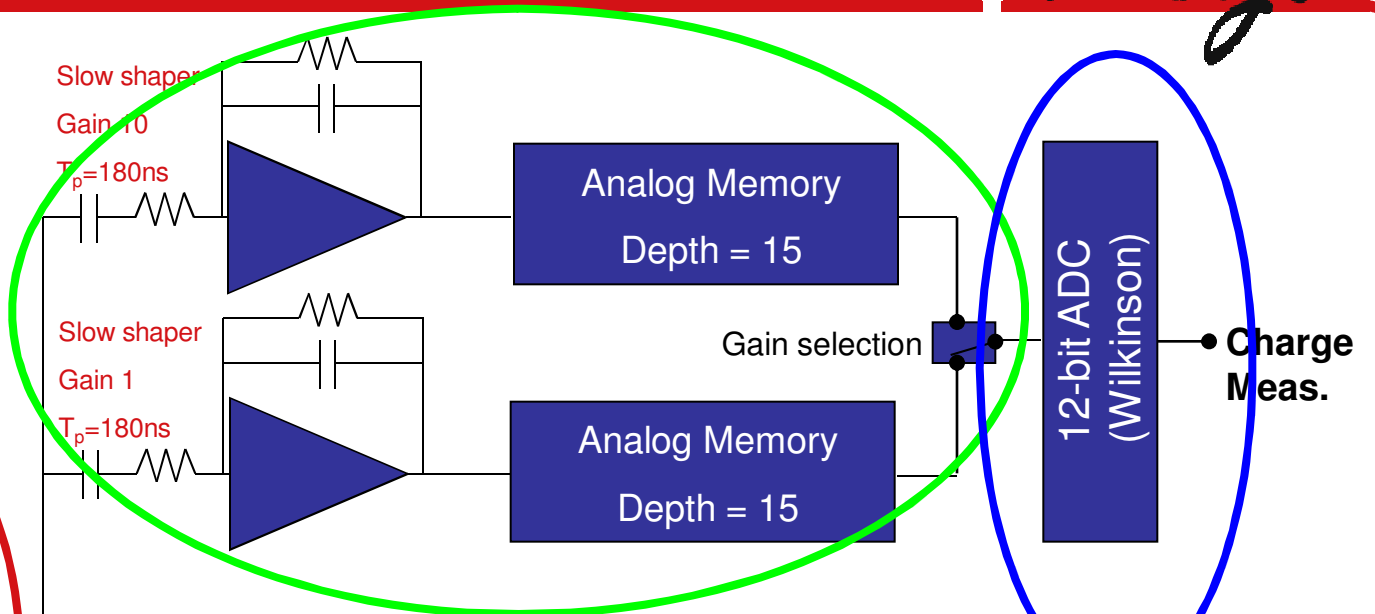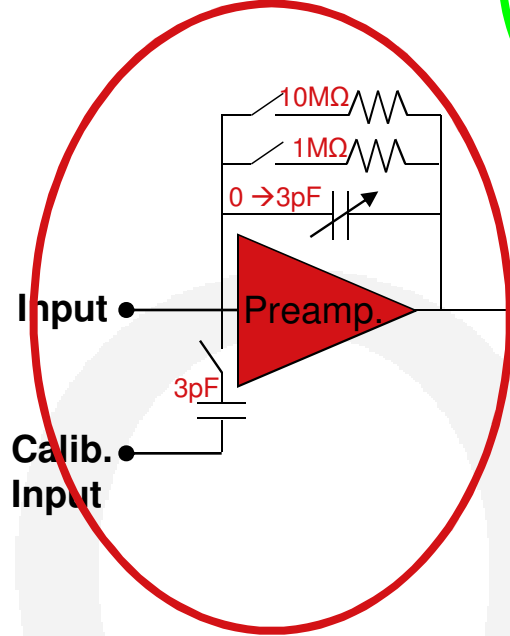CSNSM

IN2P3

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Orsay MicroElectronics Group Associated

SKIROC2 One channel block scheme

Omega

- **SPIROC**
- **SKIROC**
- **HARDROC**
- **PARISROC**

Slow shaper
Gain 10
T_p=180ns

Slow shaper
Gain 1
T_p=180ns

Analog Memory
Depth = 15

Analog Memory
Depth = 15

Gain selection

12-bit ADC (Wilkinson)

Charge Meas.

$10M\Omega$

$1M\Omega$

$0 \rightarrow 3pF$

Preamp.

Input

$3pF$

Calib. Input

Amplifier
Gain 10

fast shaper
Gain XX
T_p=adj

4-bit DAC adjustment

Trigger out

- New…

10-bit dual DAC – common to 64 channels

SKIROC 2 main features

- Cdetector estimated : 20pF
  - PIN Diode 9pF
  - PCB 10pF

- Full power pulsing capability

- Dynamic Range : from ½ MIP up to 2500 MIP
  - Using the same gain !

- PIN diode leakage current swallow capability (up to 10nA)

- Die size : 7229 µm x 8650 µm   (62,53 mm²)
  -> too expensive in a MPW (cost : 62 500 € for 25 samples !)

- 64 Channels

- Vss separated :
  - Inputs
  - Analogue part
  - Mixed part
  - Digital part

- 250 pads
  - 3 NC
  - 17 for test purpose only

- Die size
  - 7229 µm x 8650 µm

SKIROC 2 analogue features
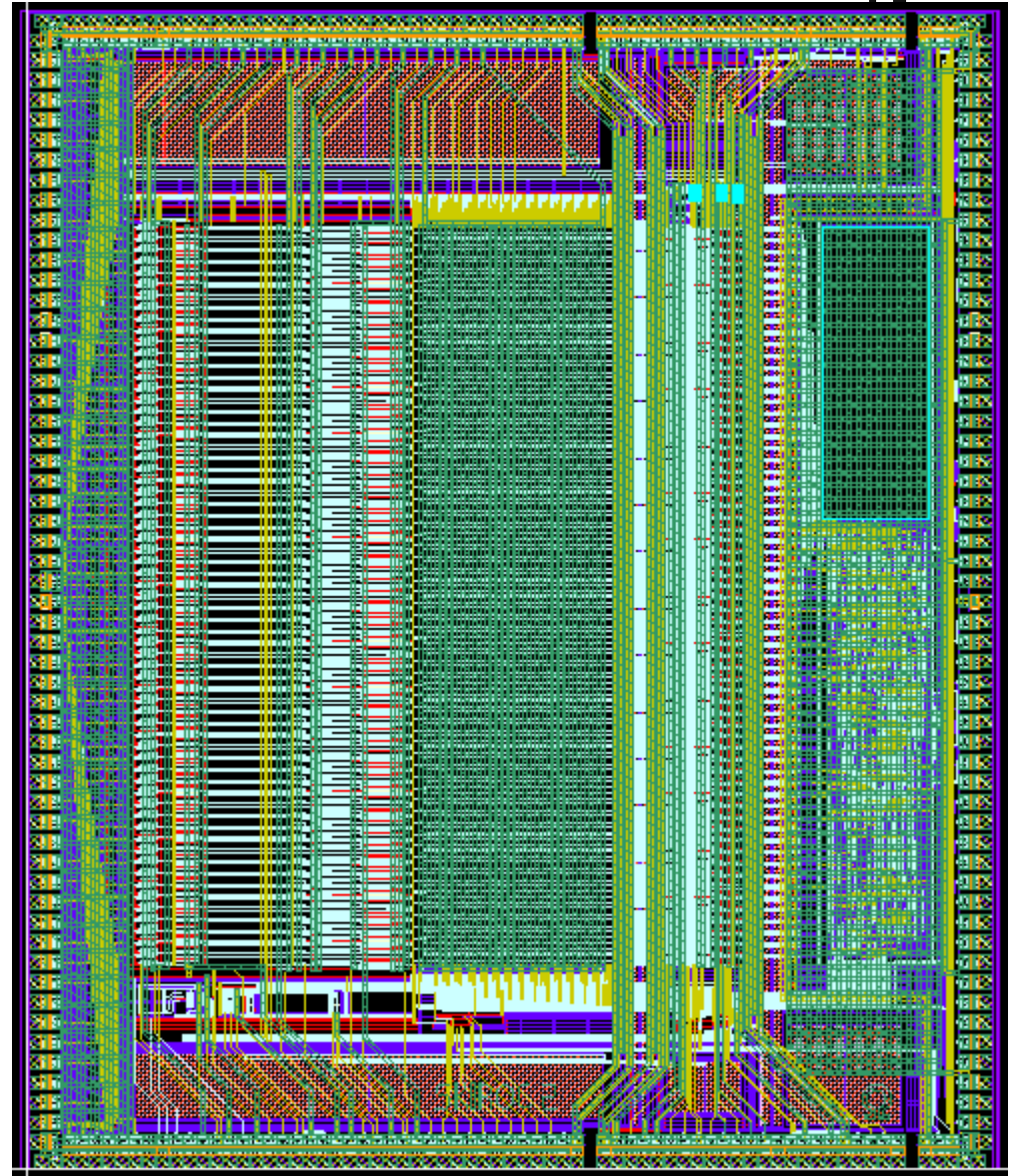
- Bandgap (reference voltage from HardRoc2b)

- Analogue channel muting capability (PA can be shut down)
  - Common 4-bit adjustable gain

- 180ns shaping time Slow Shapers for charge measurement
  - To optimize S/N
  - Antisaturation system in Gain 10 slow Shaper

- Analogue signal-to-noise ratio : 17 (1500 e$^-$ noise for 1 MIP)

- 2-bit shaping time adjustable Fast Shaper (50 to 100ns)
  - Antisaturation system in Fast Shaper

- Analogue Memory depth : 15 events can be stored
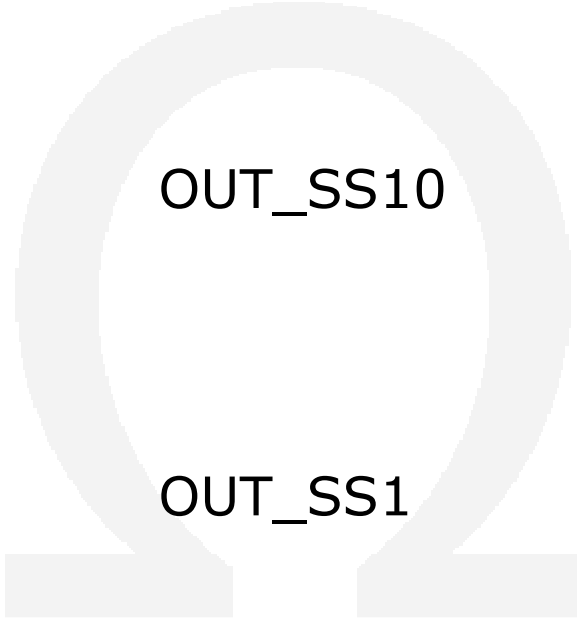
SKIROC 2 analogue simulations

Q inj	Out_PA	Out_SS1	Out_SS10
1 MIP	639.6 µV	623.7µV	6.65 mV
10	6.32 mV	6.236mV	66.47 mV
100	63.2 mV	62.33 mV	664.1 mV
200	126.4mV	124.7 mV	1317 mV
500	315.9 mV	311.5 mV	Saturation to 1.5V
1000	631.6 mV	622.4 mV	
2000	1252 mV	1234 mV	
2500	1465 mV	1437 mV	

SKIROC 2 analogue simulations

OUT_PA

OUT_FS

OUT_SS10

OUT_SS1

Transient Response

VT("/I///out_to_fs") - VDC("/I///out_to_fs")
M0(178.2ns, -6.318mV)

VT("/out_fs") - VDC("/out_fs")
M2(111ns, 556.6mV)

VT("/out_ss10") - VDC("/out_ss10")
M3(226.7ns, 59.37mV)
M5(58.77ns, 25.61uV)

VT("/out_ss1") - VDC("/out_ss1")
M4(239.7ns, 6.23mV)

SKIROC 2 mixed features
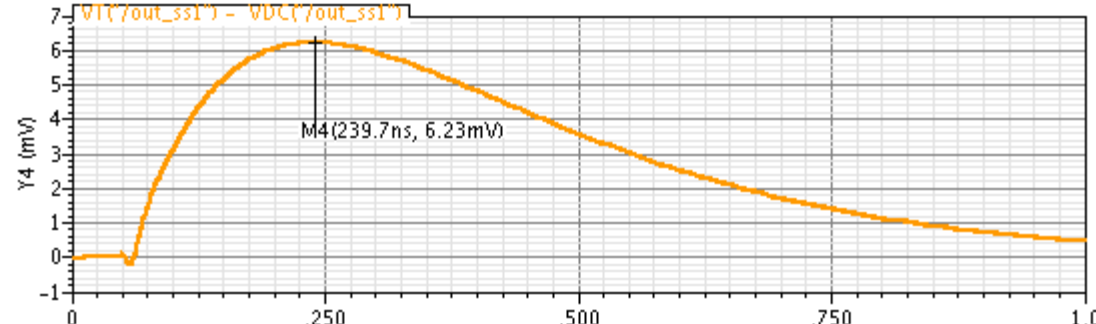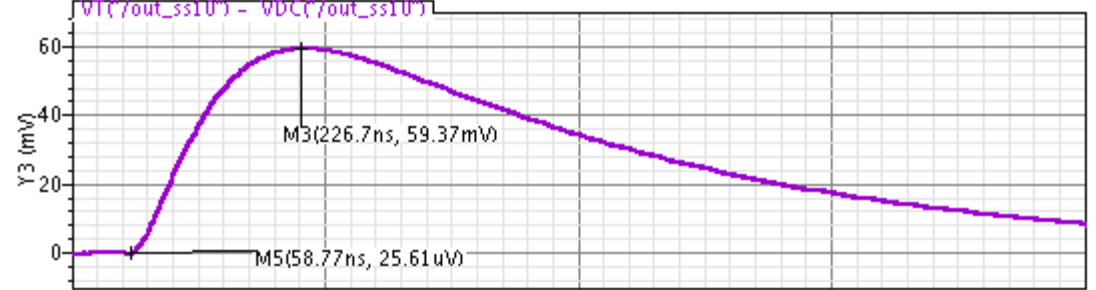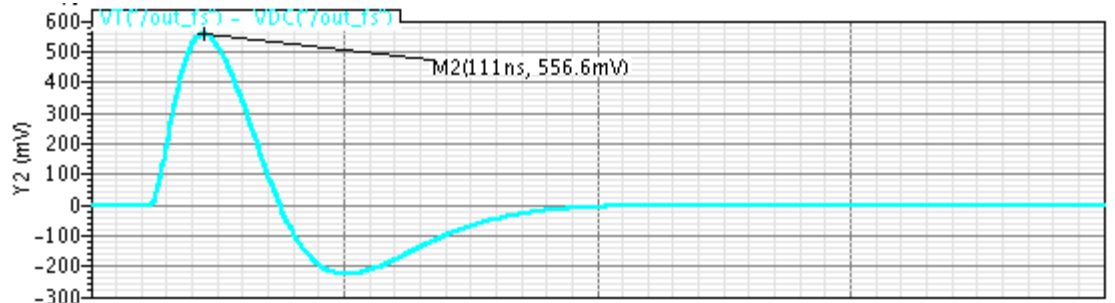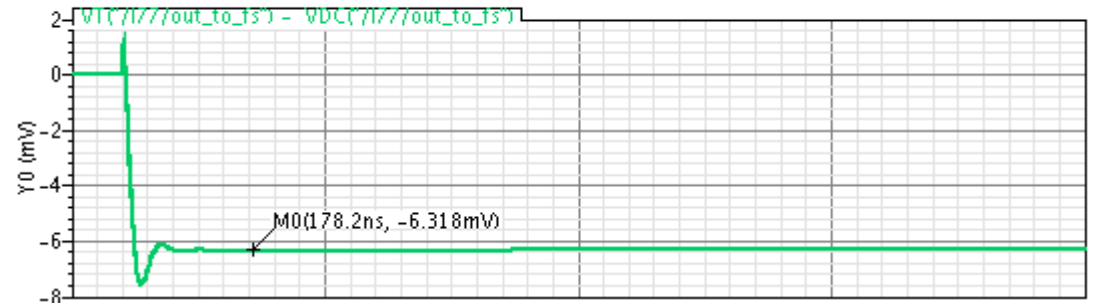
- 10-bit DAC for discriminator threshold
  - With improved 4-bit adjustment on each channel

- Trigger Discriminator from Parisroc
  - Better performance
  - Mask on each channel

- External Triggers now follow same path as internal ones

- 8-bit adjustable delay for peaking maximum signal

- (10 or 12-bit) ADC Discriminator from Parisroc
  - Better performance

- Digitization of either time and charge or of both charge

SKIROC 2 digital features

- Common features with hardroc & spiroc :
  - Multiplexed Slow Control & Probe
  - Redundancy on Data Out & Transmit On signal lines
  - 2 switchable StartReadOut & EndReadOut (prevent chip failure)

- Improved Slow Control/Probe

- New Digital Part :
  - new layout (easier interconnections with analogue part)
  - minor modifications concerning some timings (allowing more latency to analogue signal during conversion)

SKIROC 2 extra features

- 1 ns TDC capability
- TDC facility to operate in ILC mode or in test beam mode
  - 200ns for ILC / 5µs for test beam

- Power consumption optimized
  - POD included for lvds receivers
  - Each stage can be totally disabled

- Analogue and Digital probe system

- Tri-state multiplexed Analogue output

- Test purpose : few pads required, single ended 40MHz needed, default slow control configuration, "only" Acquisition/Conversion/ReadOut Command necessary

Summary

- Thanks to our engineering run, we should have 1250 samples
    - Few samples packaged in xQFP240 for complete characterization on test board
    - Others have to be quickly tested on a probe station

- Then, SKIROC2 will be integrated in FEV8 boards
    - 16 chips on each board to read out 1024 channels