AHCAL electronics.

Status and Outlook

Peter Göttlicher
for the AHCAL developers
CALICE meeting
UT Arlington, March 11th, 2010

HELMHOLTZ GEMEINSCHAFT

CALICE Calorimeter for ILC

EUDET

DESY

Outline

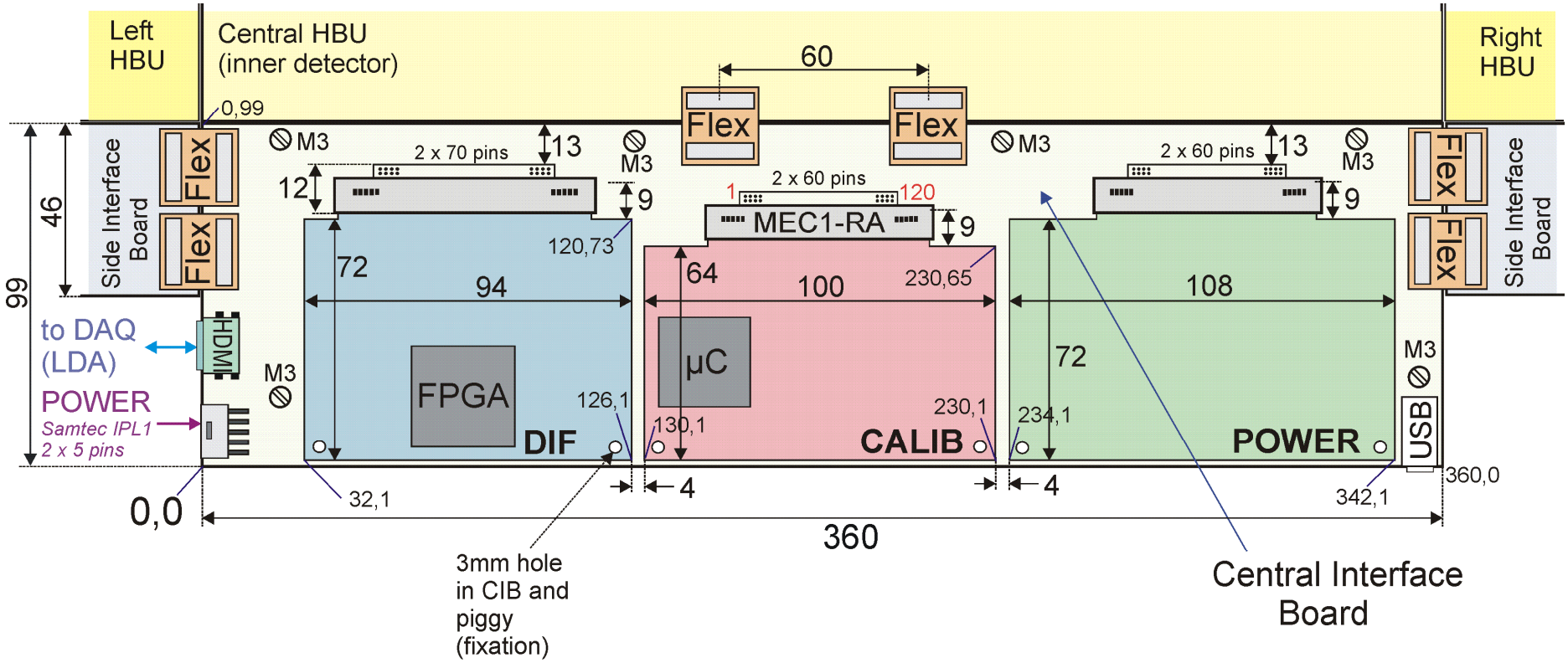
- Status AHCAL DAQ (Labview and USB)
- DIF development
- First preliminary results with HBU_II
- Testbeam timing issues
- Conclusions and Outlook

DIF development

- Labview-USB interface to AHCAL DIF done! In operation.
- DIF task force meetings: Nov. 27th, 2009 @LLR,
  next meeting March 31st, 2010


- Remi: proposal for general FPGA firmware block structure.
  Block definition during next meeting.
- AHCAL code can be adapted to this scheme with minor changes
  (mainly adding some extensions to existing structures).

DIF development (+ CALIB and POWER)



- Board Dimensions fixed.
- Redesigns about to start.

DIF development – Connectors to Base Module CIB

DIF: 2x70 pins

DIF Connector			
Pin	Column 1	Column 2	Pin
2	GND	GND	1
4	Analog_0	Analog_1	3
6	GND	GND	5
8	SC_SRIN	SC_SRIN_BYP	7
10	SC_SROUT1	SC_SROUT_BYP	9
12	SC_Reset	SC_SROUT2	11
14	SC_Load	SC_SROUT3	13
16	SC_Select	SC_CLK1	15
18	SC_CLK2	SC_CLK3	17
20	GND	GND	19
22	SCA_Sat	Start_Acqt	21
24	Start_Readout	Start_Conv_DAQb	23
26	GND	GND	25
28	Start_Readout_BYP	TransmitOn1	27
30	Dout1	TransmitOn2	29
32	Dout2	TransmitOn3	31
34	Dout3	TransmitOn4	33
36	Dout4	TransmitOn5	35
38	Dout5	TransmitOn6	37
40	Dout6	GND	39
42	End_Readout4	End_Readout1	41
44	End_Readout5	End_Readout2	43
46	End_Readout6	End_Readout3	45
48	GND	GND	47
50	resetn	reset_BCID	49
52	reset_read_probe	pwr_analog	51
54	polariz.	polariz.	53
56	pwr_digital	pwr_adc	55
58	pwr_sca	pwr_dac	57
60	GND	GND	59
62	NOTBOOT	NOTRESIN	61
64	Trig_Ext_P (IN)	noTrig/RazChn_P	63
66	Trig_Ext_N (IN)	noTrig/RazChn_N	65
68	Clk_5MHz_0_P	Clk_5MHz_1_P	67
70	Clk_5MHz_0_N	Clk_5MHz_1_N	69
72	Clk_40MHz_0_P	Clk_40MHz_1_P	71
74	Clk_40MHz_0_N	Clk_40MHz_1_N	73
76	GND	GND	75
78	Val_Evt_P	CALIB_spare	77
80	Val_Evt_N	UART_Tx	79
82	Clk_40MHz_2_P	UART_Rx	81
84	Clk_40MHz_2_N	SCL_I2C	83
86	Clk_5MHz_2_P	SDA_I2C	85
88	Clk_5MHz_2_N	POWER_spare	87
90	GND	GND	89
92	srout_read	uC_clk+	91
94	srin_read	uC_clk-	93
96	clk_probe	clk_read	95
98	digital_probe1	srin_probe	97
100	digital_probe2	srout_probe	99
102	GND	GND	101
104	USB_D+	VBUS_USB	103
106	USB_D-	Enable_DIF_DIF	105
108	GND	GND	107
110	GND	Toggle_PWR_1d5V	109
112	SCK0	VDIF_5V	111
114	MISO0	VDIF_5V	113
116	polariz.	polariz.	115
118	MOSI0	GND	117
120	SSEL	VDD_3d3V_2	119
122	GND	VDD_3d3V_2	121
124	SPL2D+	VDD_3d3V_2	123
126	SPL2D-	VDD_3d3V_2	125
128	SPD2L+	GND	127
130	SPD2L-	GND	129
132	DD2L+	GND	131
134	DD2L-	GND	133
136	DL2D+	HDMI_CLK+	135
138	DL2D-	HDMI_CLK-	137
140	GND	GND	139

CALIB: 2x60 pins

CALIB Connector			
Pin	Column 1	Column 2	Pin
2	GND	GND	1
4	TCALIB1_1+	TCALIB1_2+	3
6	TCALIB1_1-	TCALIB1_2-	5
8	GND	GND	7
10	TCALIB1_3+	TCALIB2_1+	9
12	TCALIB1_3-	TCALIB2_1-	11
14	GND	GND	13
16	TCALIB2_2+	TCALIB2_3+	15
18	TCALIB2_2-	TCALIB2_3-	17
20	GND	GND	19
22	Trig_Ext1+	Trig_Ext2+	21
24	Trig_Ext1-	Trig_Ext2-	23
26	GND	GND	25
28	Trig_Ext3+	VCALIB1	27
30	Trig_Ext3-	VCALIB1	29
32	polariz.	polariz.	31
34	VCALIB2	GND	33
36	VCALIB2	GND	35
38	GND	GND	37
40		not connected	39
42	not connected	GND	41
44	GND	GND	43
46	GND	not connected	45
48	Temp1	Temp4	47
50	Temp2	Temp5	49
52	not connected	not connected	51
54	Temp3	Temp6	53
56	VREF_+4V5	Temp_DIF	55
58	VDAC_+5V	GND	57
60	VDDA	VADREF	59
62	GND	GND	61
64	polariz.	polariz.	63
66	GND	GND	65
68	Trig_Ext_P (IN)	HOLD_Ext+	67
70	Trig_Ext_N (IN)	HOLD_Ext-	69
72	GND	SCL_I2C	71
74	PWR_Enable_GR1	CALIB_POW_spare	73
76	PWR_Enable_GR2	SDA_I2C	75
78	HV_Level_10V_50V	NOTCONVST_ADC	77
80	GND	GND	79
82	SCK0	CALIB_spare	81
84	MISO0	GND	83
86	MOSI0	NOTRESIN	85
88	SSEL	NOTBOOT	87
90	GND	GND	89
92	UART_Tx	uC_clk+	91
94	UART_Rx	uC_clk-	93
96	pwr_calib_led	GND	95
98	pwr_calib_led	pwr_calib_charge	97
100	pwr_calib_led	pwr_calib_charge	99
102	GND	GND	101
104	GND	GND	103
106	VCC_+11V	VCC_+11V	105
108	VCC_+11V	VCC_+11V	107
110	GND	GND	109
112	VDD_3d3V_1	VDD_3d3V_1	111
114	VDD_3d3V_1	VDD_3d3V_1	113
116	VDD_3d3V_1	VDD_3d3V_1	115
118	GND	GND	117
120	GND	GND	119

POWER: 2x60 pins

POWER Connector			
Pin	Column 1	Column 2	Pin
2	GND	GND	1
4	VDDA	VDDA	3
6	VDDA	VDDA	5
8	GND	GND	7
10	VDDA	VDDA	9
12	VDDA	VDDA	11
14	VDDA	GND	13
16	GND	GND	15
18	GND	GND	17
20	GND	VDDD	19
22	VDDD	VDDD	21
24	VDDD	VDDD	23
26	GND	GND	25
28	VREF_+4V5	VDAC_+5V	27
30	VREF_+4V5	VDAC_+5V	29
32	polariz.	polariz.	31
34	GND	GND	33
36	GND	VADREF	35
38	GND	GND	37
40	GND	not connected	39
42	not connected	HV3	41
44	HV1	HV3	43
46	HV1	not connected	45
48	HV2	HV_Input	47
50	HV2	HV_Input	49
52	not connected	not connected	51
54	GND	GND	53
56	GND	GND	55
58	GND	GND	57
60	V+6V_IN	V+12V_IN	59
62	V+6V_IN	V+12V_IN	61
64	polariz.	polariz.	63
66	V+6V_IN	V+12V_IN	65
68	V+6V_IN	V+12V_IN	67
70	GND	GND	69
72	V+6V_IN	GND	71
74	V+6V_IN	GND	73
76	GND	GND	75
78	GND	GND	77
80	PWR_Enable_GR1	SCL_I2C	79
82	PWR_Enable_GR2	CALIB_POW_spare	81
84	HV_Level_10V_50V	SDA_I2C	83
86	POWER_spare	NOTCONVST_ADC	85
88	GND	GND	87
90	GND	GND	89
92	GND	GND	91
94	VDIF_5V	GND	93
96	VDIF_5V	VDD_3d3V_2	95
98	GND	VDD_3d3V_2	97
100	GND	VDD_3d3V_2	99
102	GND	VDD_3d3V_2	101
104	GND	GND	103
106	VCC_+11V	VCC_+11V	105
108	VCC_+11V	VCC_+11V	107
110	Toggle_PWR_1d5V	GND	109
112	VDD_3d3V_1	VDD_3d3V_1	111
114	VDD_3d3V_1	VDD_3d3V_1	113
116	VDD_3d3V_1	VDD_3d3V_1	115
118	GND	GND	117
120	GND	GND	119

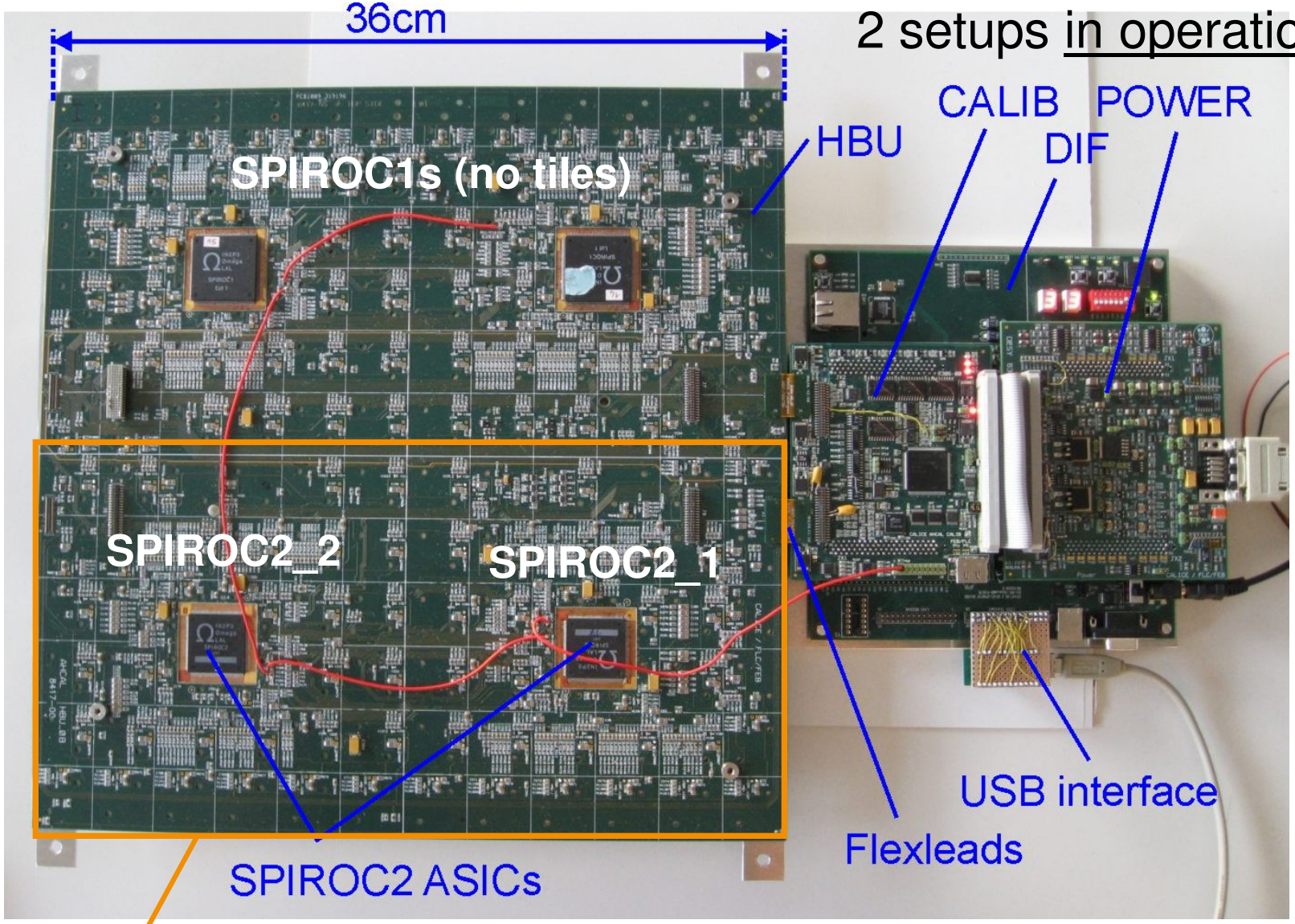
HDMI Interface
SPI (DIF to CALIB)
Analog
User Single Ended
Controls Single Ended
Digital Readout
Power pulsing controls
LVDS signals
Slow controls signals
POWER pins
USB Bus
GND
Ext. Voltage Input

Version 0.5
19.02.2010
Preliminary

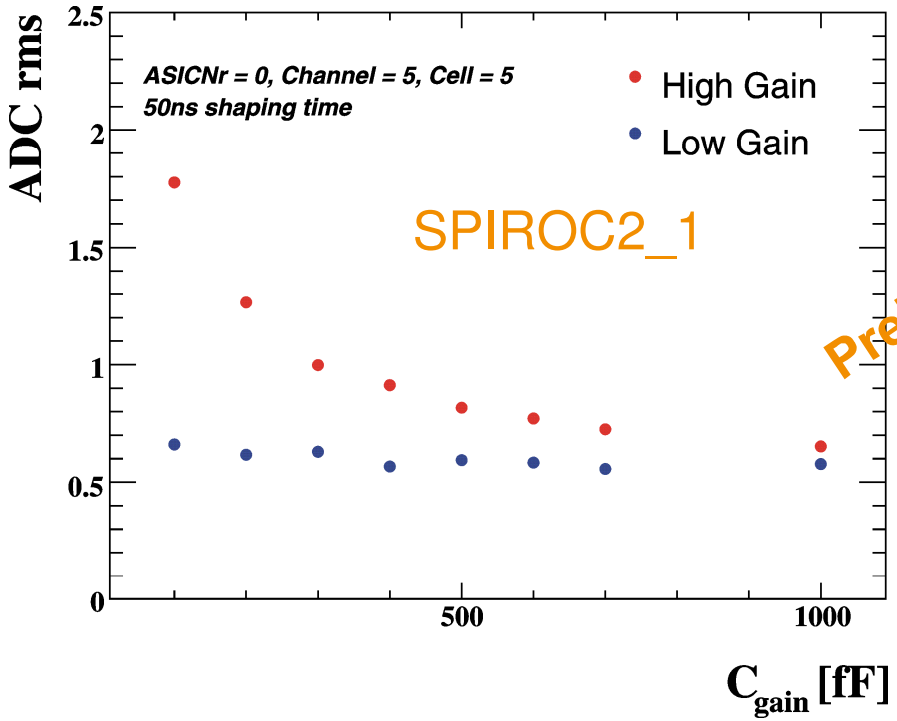
DIF Connector had to be modified – AHCAL DIF is really **'detector specific'**, (more pins needed).

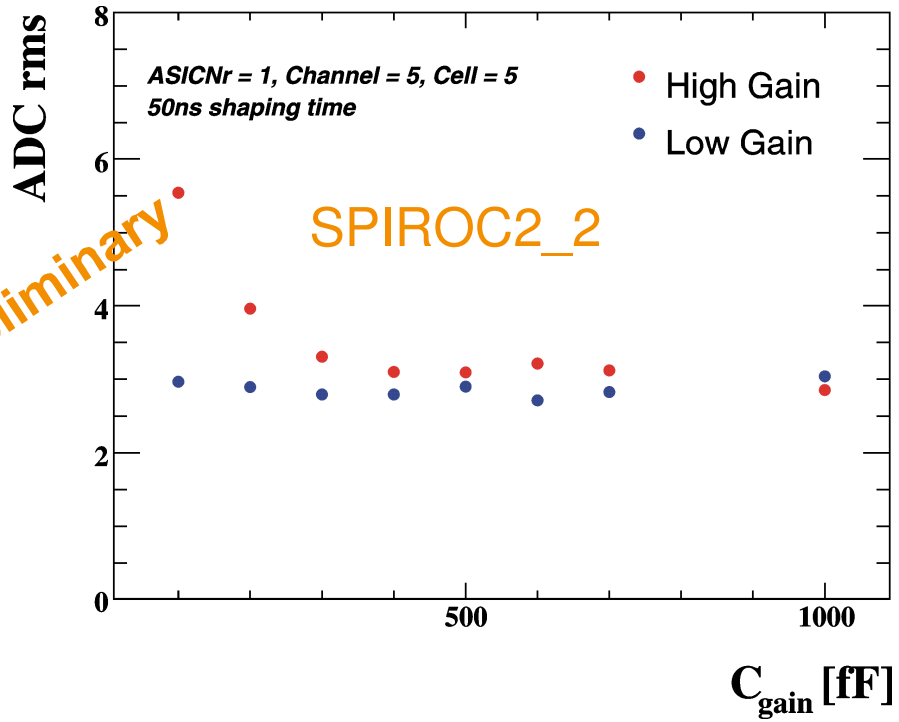
DESY

First Measurements – What is where!



First Results: RMS Noise for one channel

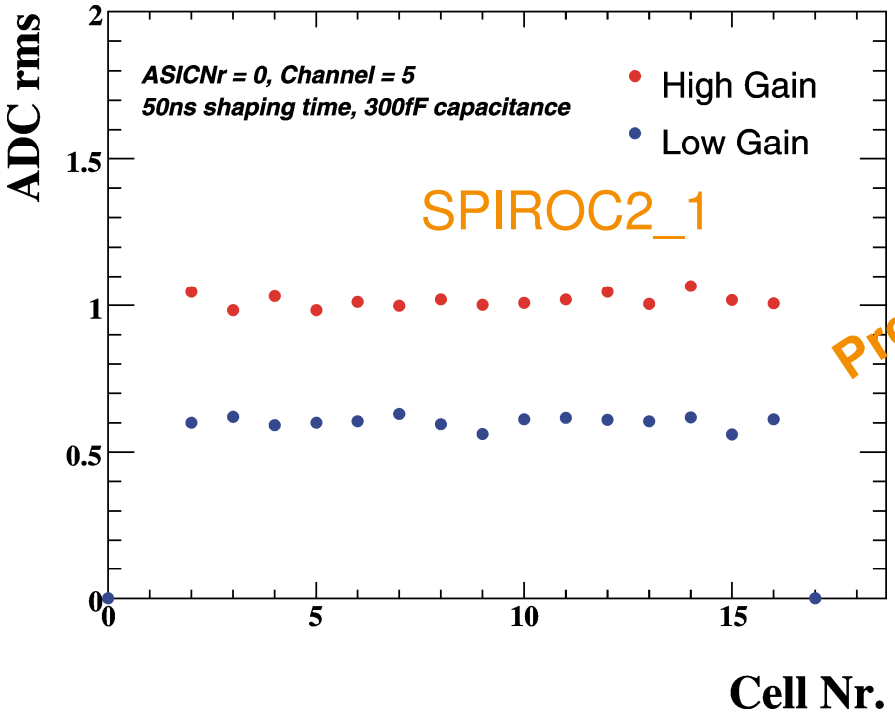


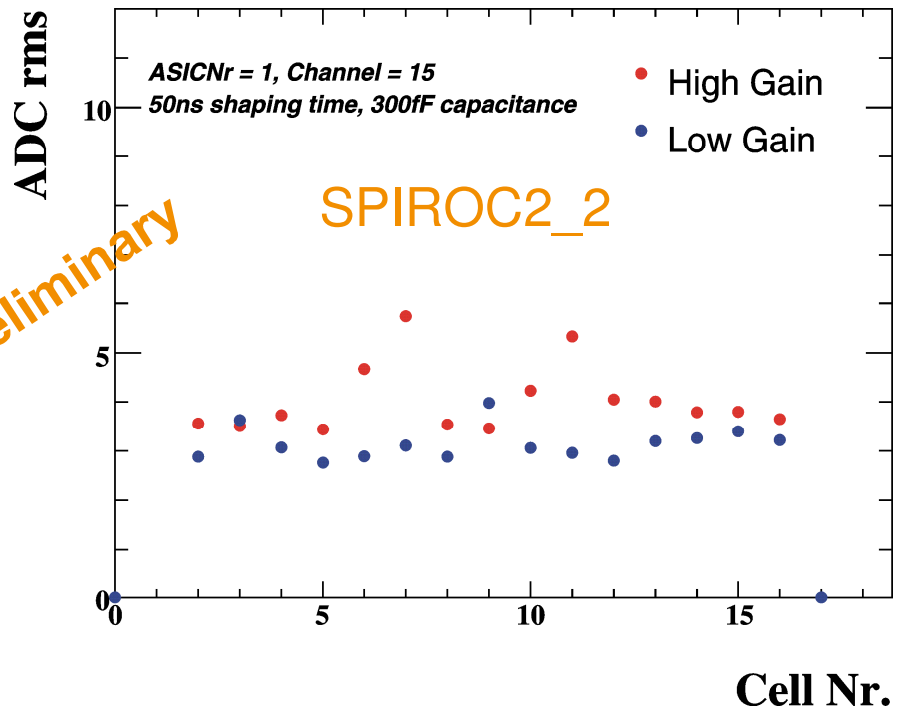


SPIROC2 ADC: 2958 ADC_chns/V => 2 ADC-counts RMS = 0.68mV
Overall characteristic is ok, but much higher noise on ASIC1.

To be done: Convert to charge!
Analyze SPIROC2_2 high-noise reason

First Results: RMS Noise over analogue memory cells

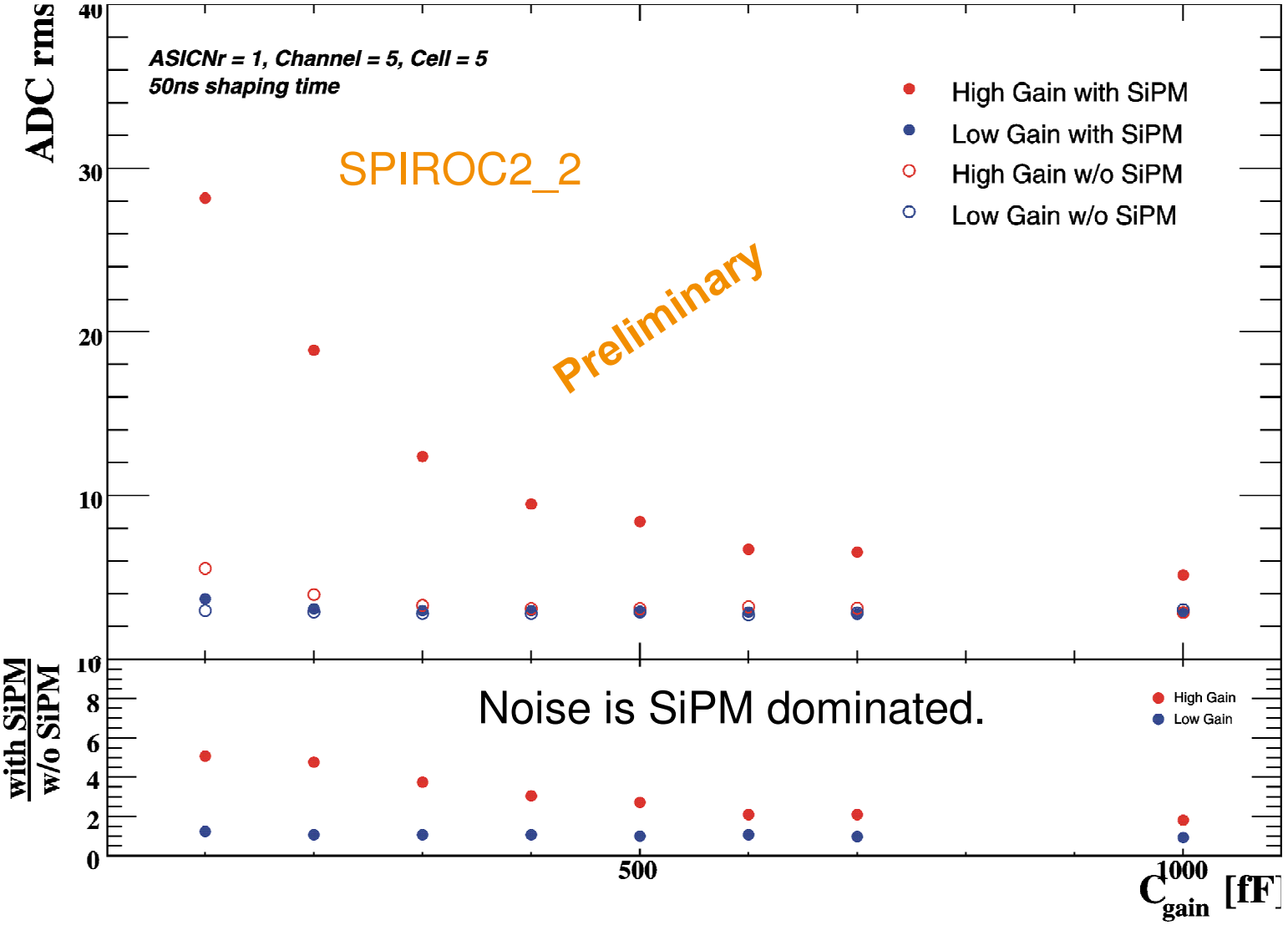




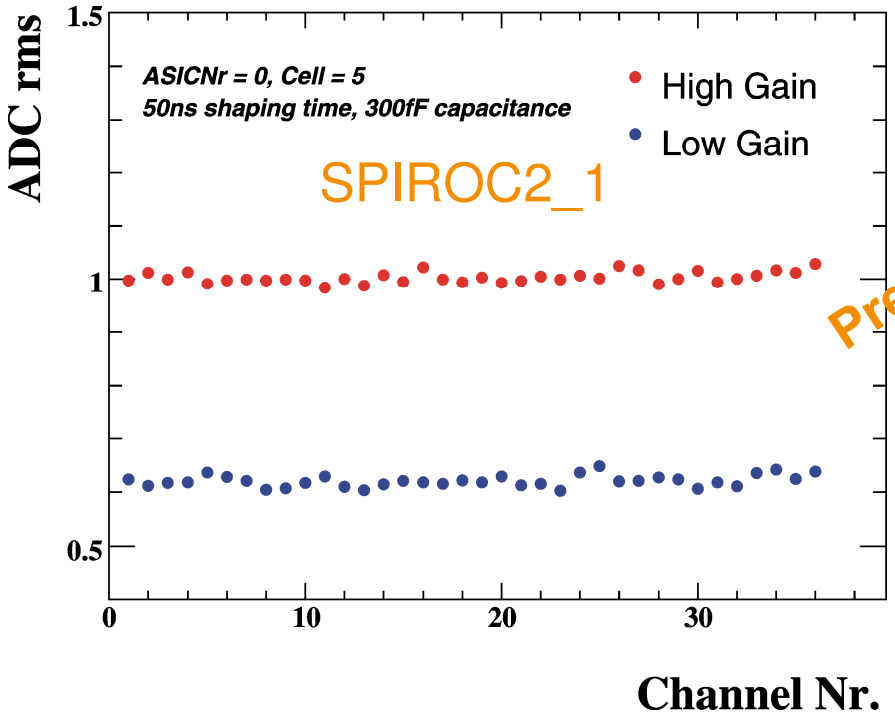
Preliminary

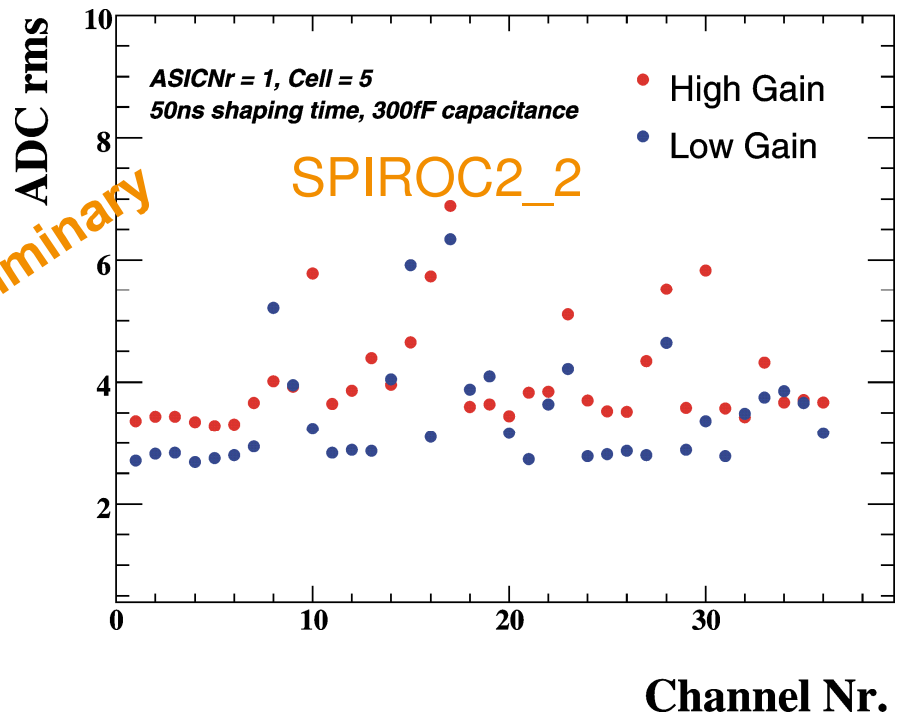
SPIROC2_2: Higher noise and not equal for the 16 analogue memory cells.

First Results: RMS noise with and without SiPM



First Results: RMS noise for all channels



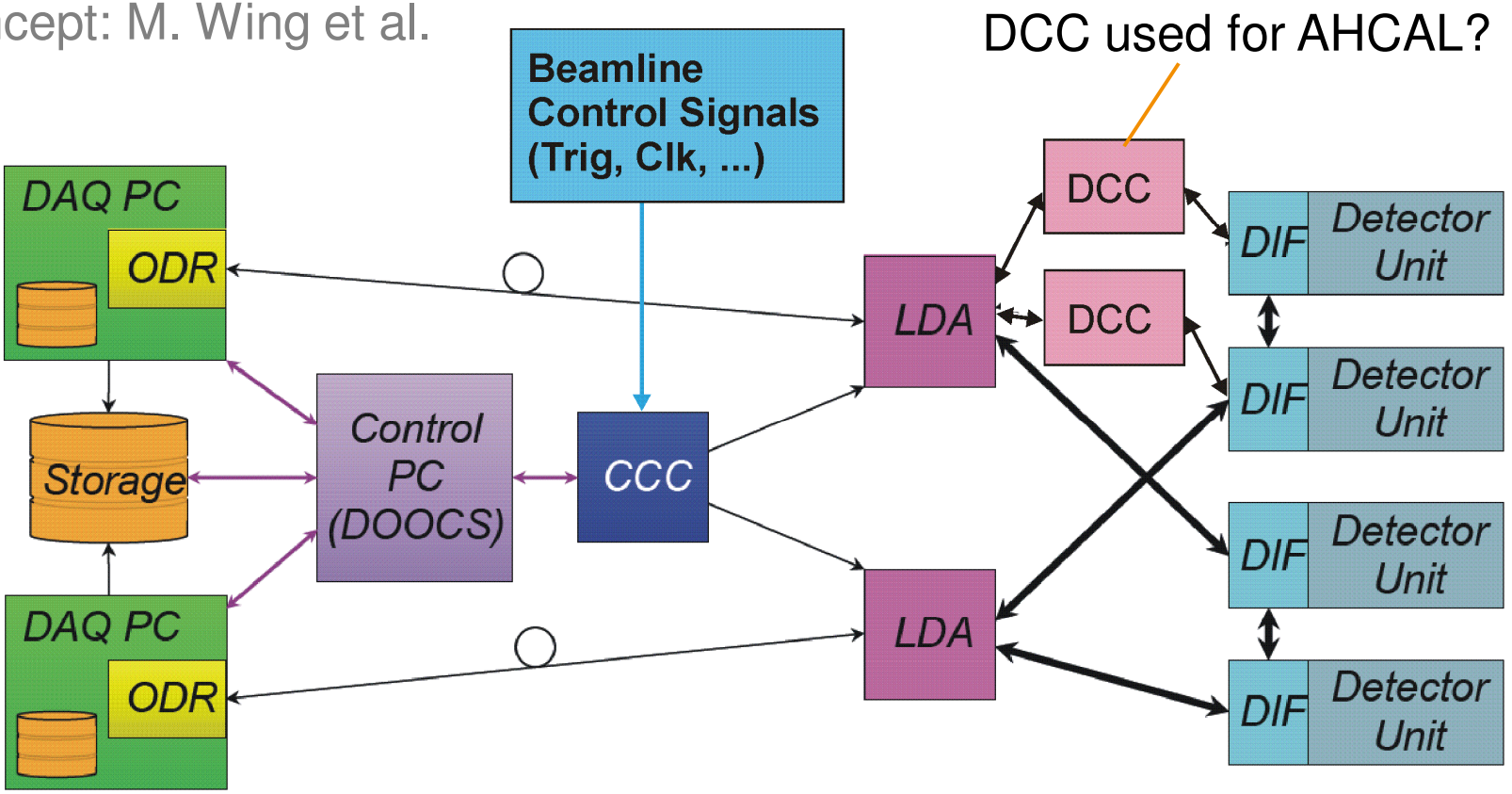


Preliminary

SPIROC2_2: Higher noise and
not constant for the 36 channels.

Testbeam Synchronization (CALICE DAQ setup)

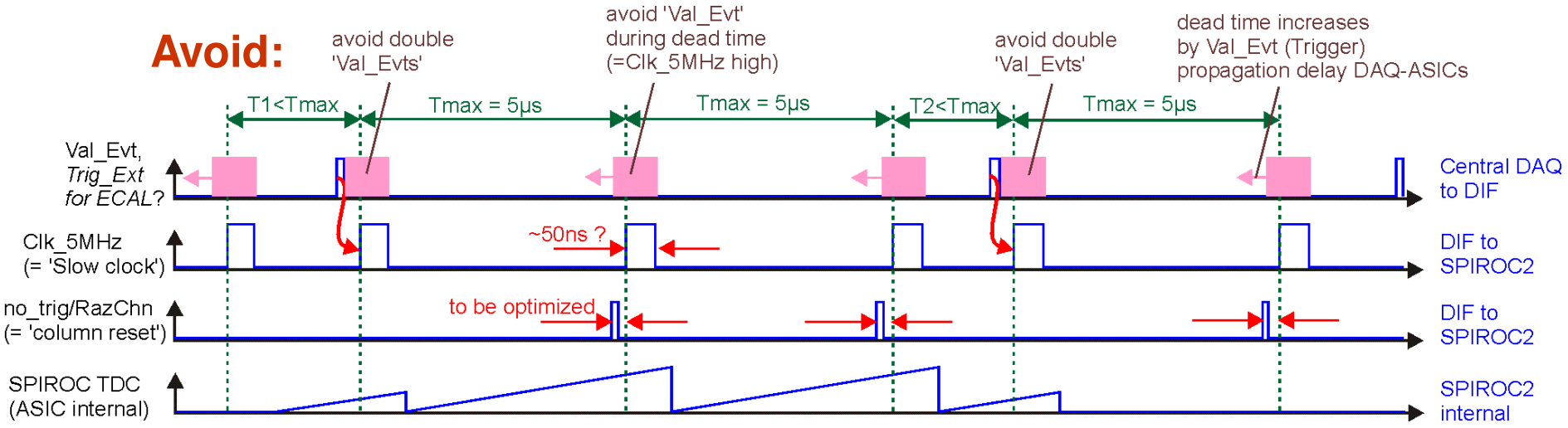
Concept: M. Wing et al.



- All timing critical signals are distributed from central DAQ (via CCC).
- All detector units (+DIFs) run synchronously.

Testbeam: Internal Trigger in Validation Mode

AHCAL timing scheme for common CALICE testbeam

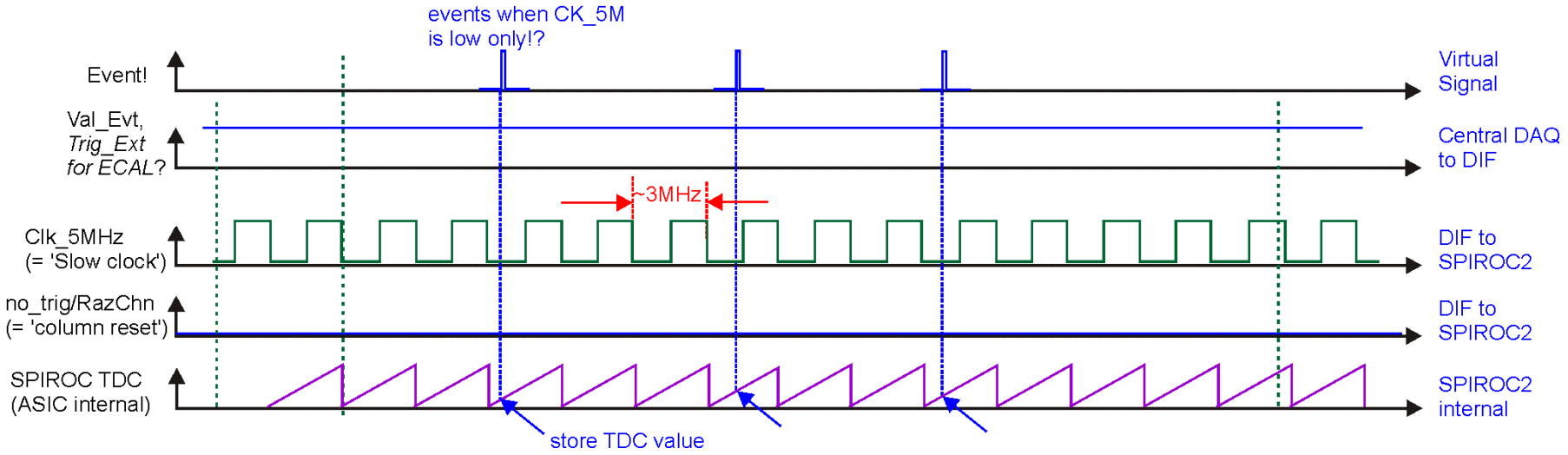


- Internal Trigger with “Validate_Event”. **Pink boxes: deadtime!**
- ECAL (DHCAL as well?): Continuous CK_5M (3-5MHz?)
- CALICE DAQ: Synchronize Val_Evt on global clock (multi-DIF synchron.).
- Event time information: Store in DAQ: Validation time points (AHCAL), ECAL: has a (continuous) clock counter.

This scheme: Mode for high statistics.

Testbeam: Internal Trigger in ILC Mode

AHCAL timing scheme for common CALICE testbeam

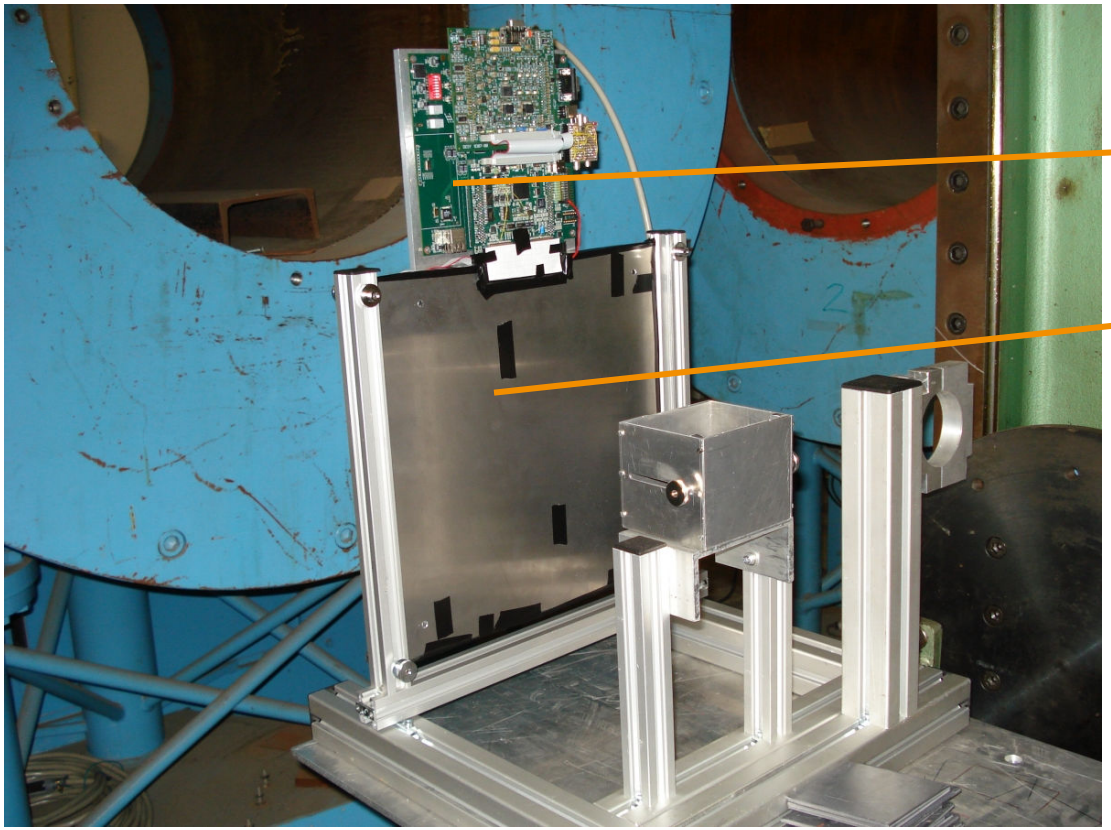


- AHCAL stores every event above threshold (events and noise), no validation. SPIROC is filled after 16 triggers.
- Overall deadtime is readout-dominated => not most efficient for AHCAL (many noise hits due to SiPM's dark rate > 0.5MIP).
- Setup is the same for ECAL and DHCAL.

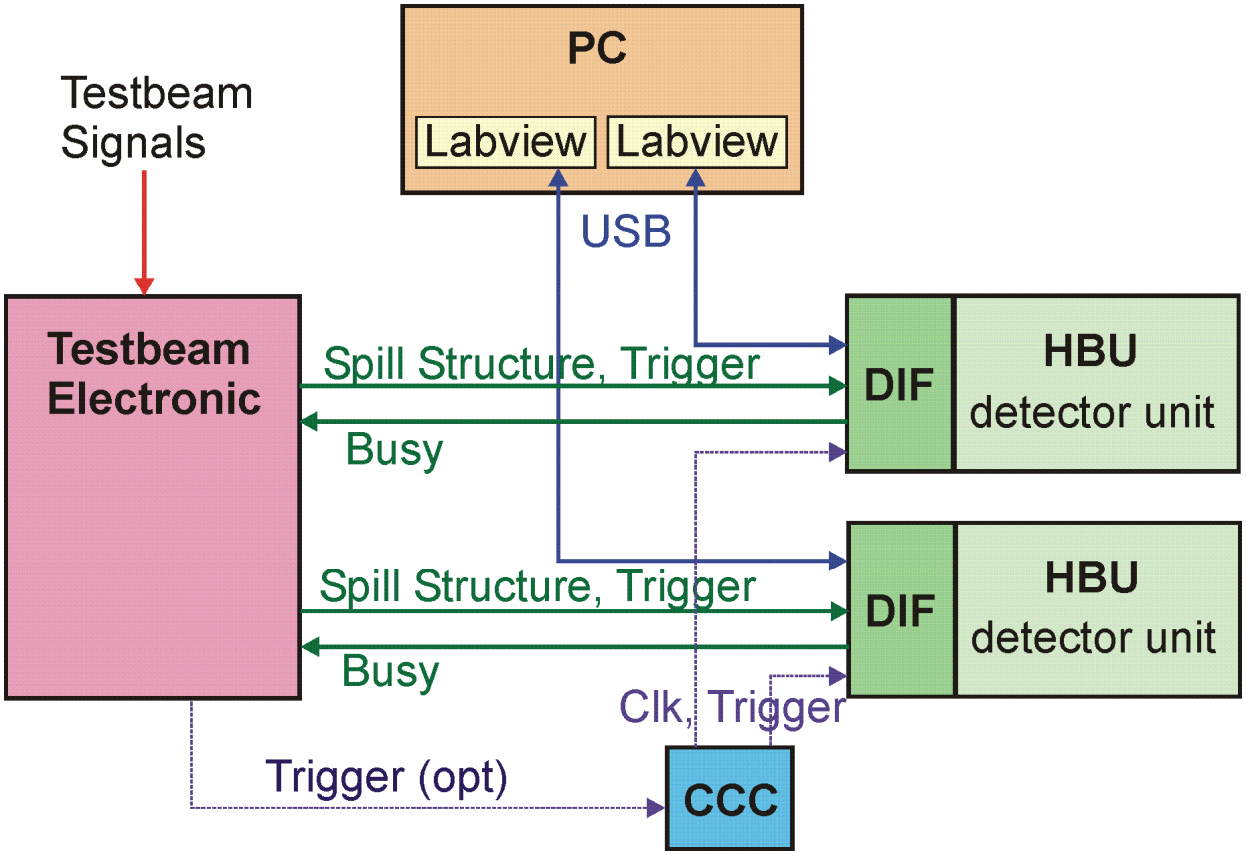
This scheme: Mode for ILC-behaviour test.

DESY testbeam (HBUII)

- First module has arrived at DESY testbeam.
  Operation still with Labview-USB DAQ.
- Still a few Control-Software functions needed (e.g. automatic HOLD Scan)



DESY Testbeam Synchronization (Labview setup)



- Synchronization done by temporary hardware signals to/from DIF.
- First: Only one DIF/HBU used. With two HBUs the CCC is needed.
- Readout Speed limited due to USB/Serial Interface.

Conclusions and Outlook

- AHCAL: 2 setups in operation!
- DIF generalization is prepared / has to be coordinated with testbeam firmware developments.
- Timing issues for common testbeam should be discussed now!
- Before module's redesigns, tests needed for:
  - Power cycling / Removal of blocking caps => Coherent Noise?
  - Identify source of high noise for SPIROC2_2