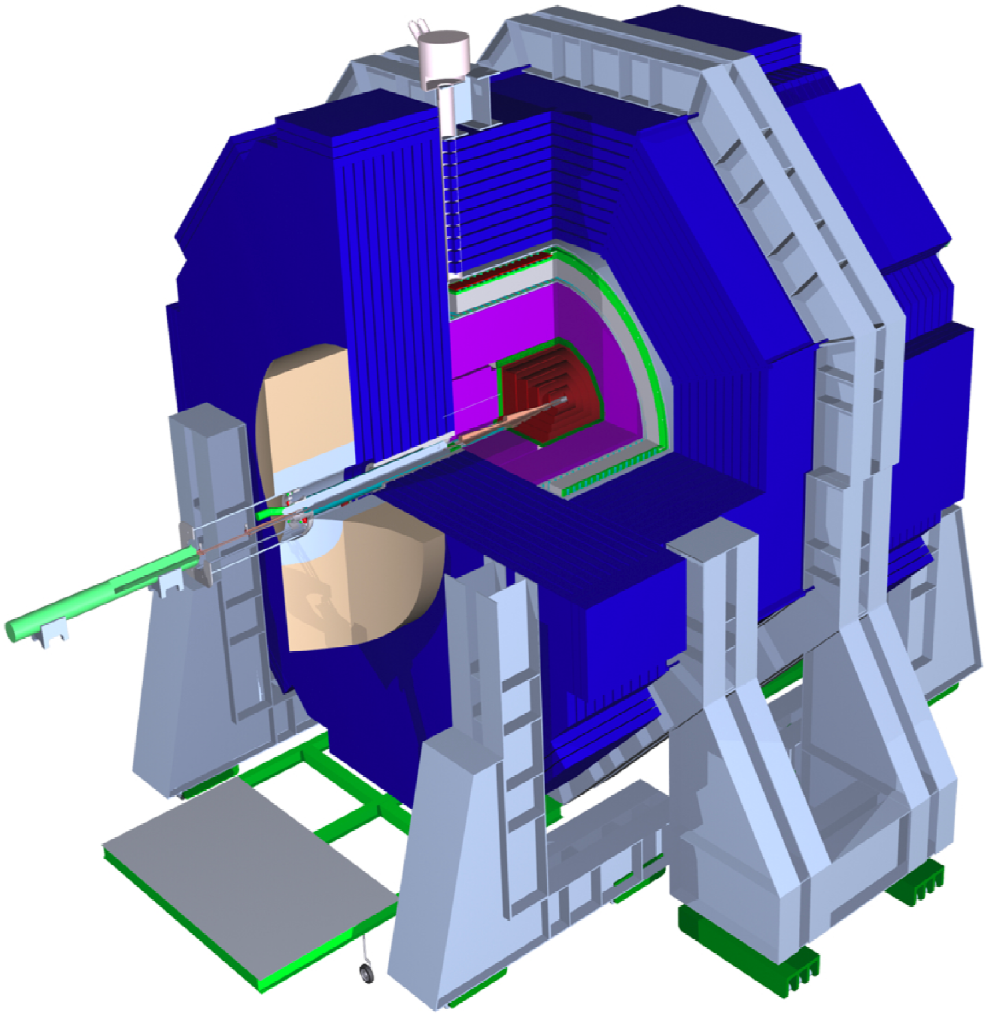
The SiD Detector Concept

On behalf of the SiD Concept Group

Andy White

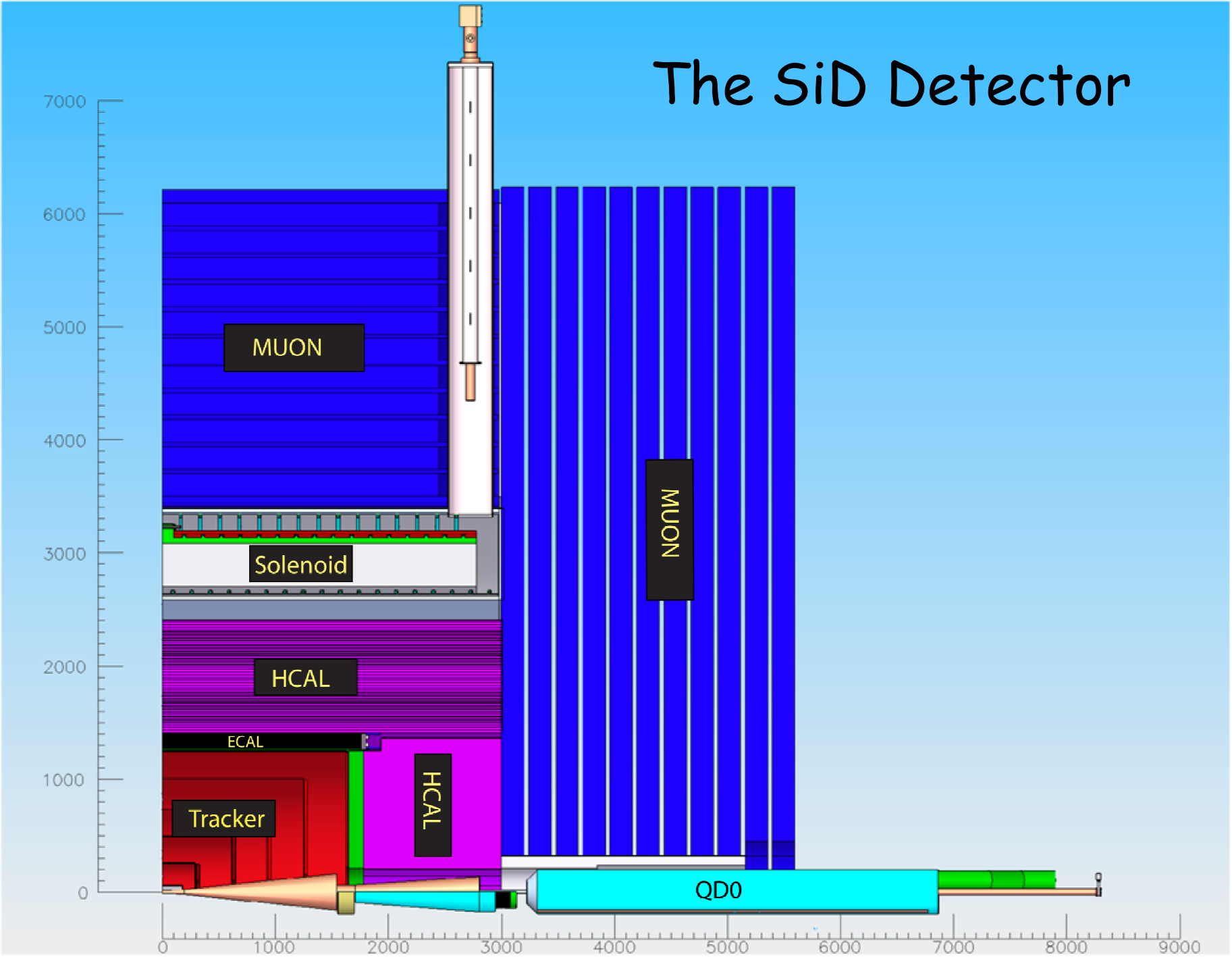
University of Texas at Arlington



Contents

- The SiD Detector – an overview.
- SiD Organization.
- Developments in subsystems R&D.
- Critical areas of R&D for SiD.
- The SiD Work Plan and the Path to 2012.

The SiD Detector

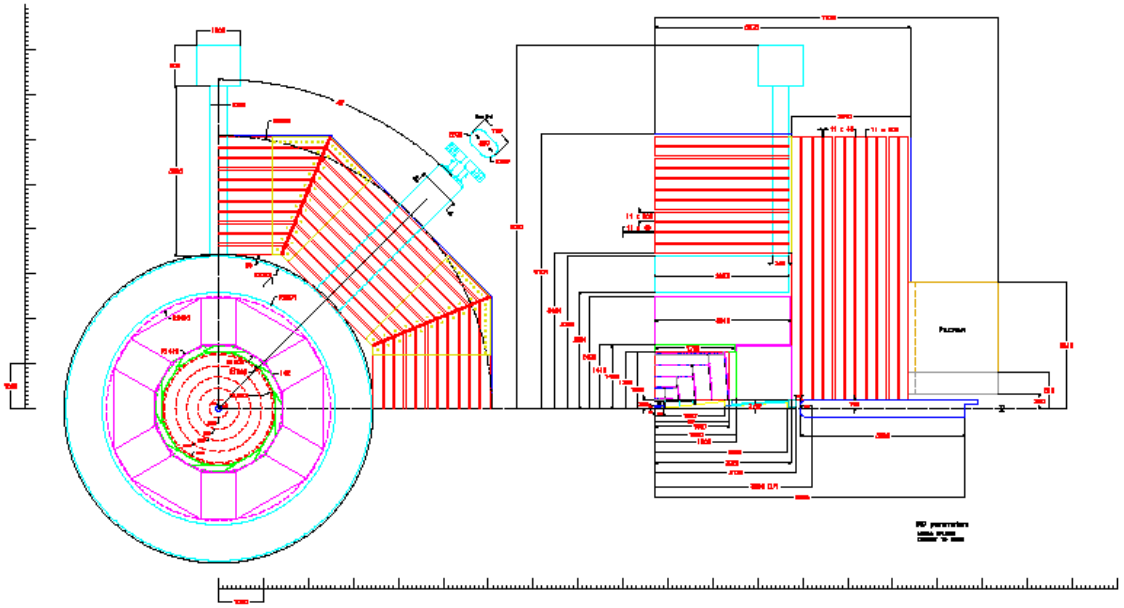


The SiD Design

A compact, cost-contained detector designed to make precision measurements and be sensitive to a wide range of new phenomena.

-> Compact design with 5T field.
-> Robust silicon vertexing and tracking system – excellent momentum resolution, live for single bunch crossing.
-> Calorimetry optimized for jet energy resolution, based on a Particle Flow approach, "tracking calorimeters", compact showers in ECal, highly segmented (longitudinally and transversely) ECal and HCal.
-> Iron flux return/muon identifier – component of SiD self-shielding.
-> Detector is designed for rapid push-pull operation.

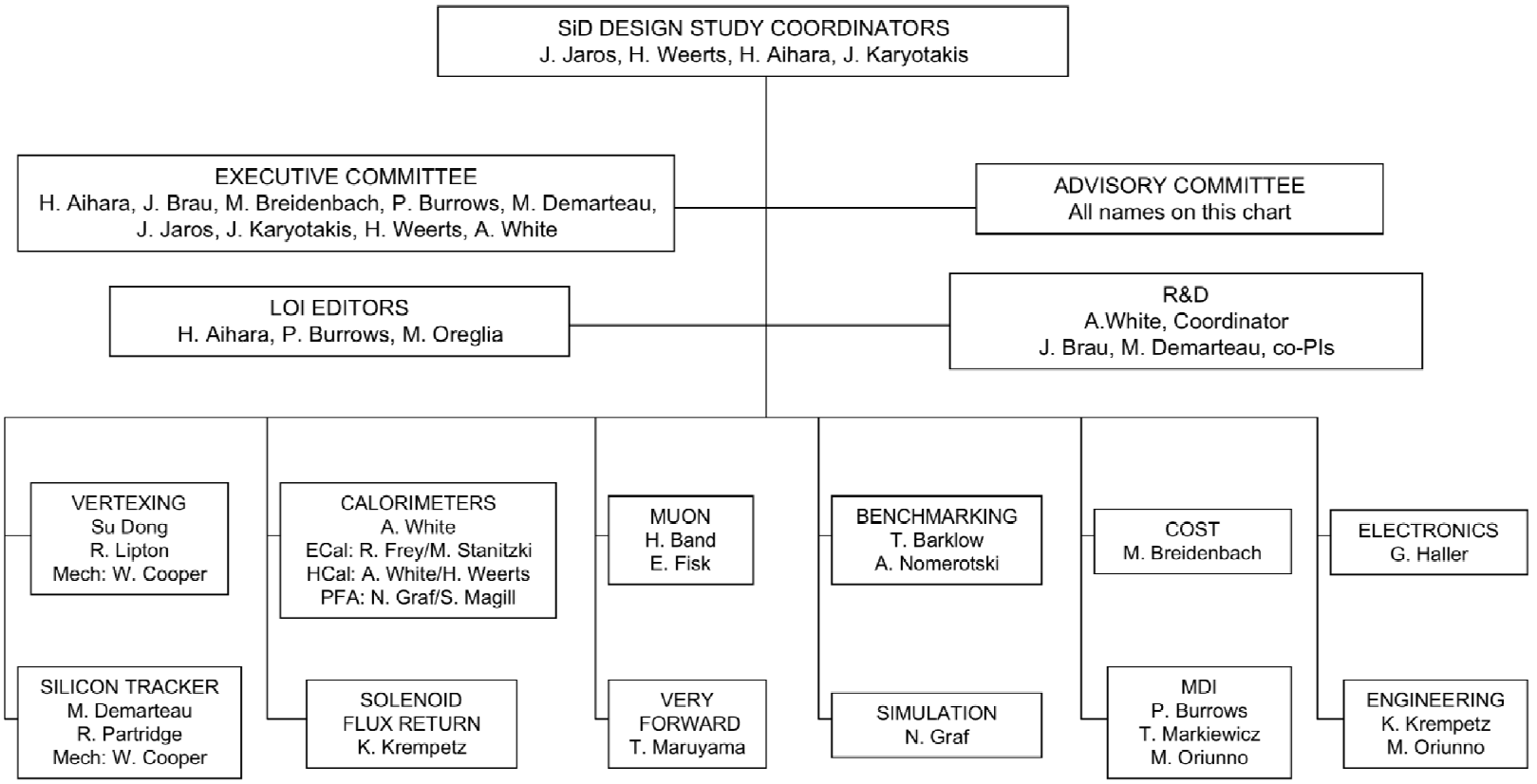
SiD Global Parameters (LOI)



Detector	Radius (m)		Axial (z) (m)	
	Min	Max	Min	Max
Vertex Detector	0.014	0.060	0.000	0.180
Central Tracking	0.206	1.250	0.000	1.607
Barrel Ecal	1.265	1.409	0.00	1.765
Endcap Ecal	0.206	1.250	1.657	1.800
Barrel Hcal	1.419	2.493	0.000	3.018
Endcap Hcal	0.206	1.404	1.806	3.028
Coil	2.591	3.392	0.000	3.028
Barrel Iron	3.442	6.082	0.000	3.033
Endcap Iron	0.206	6.082	3.033	5.673

Kurt Krempetz

SiD Organization



-> Alternating weekly SiD Executive Committee and SiD Advisory Board meetings.

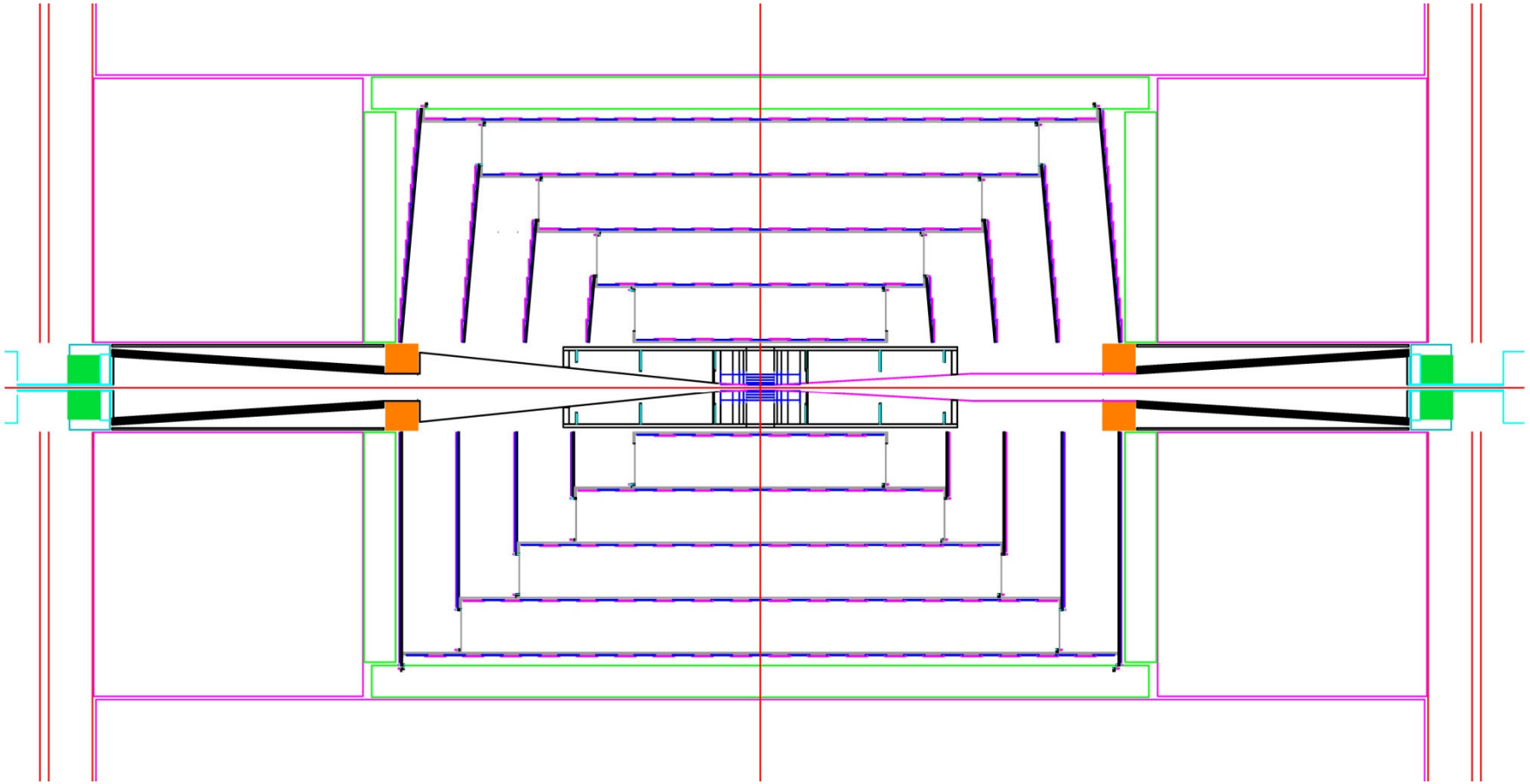
-> Current focus on PFA and Calorimeter subsystem meetings.

-> Next SiD Workshop: June 3-5, 2010 at Argonne National Laboratory

Progress on SiD Detector Subsystems

Recent R&D Results and Plans

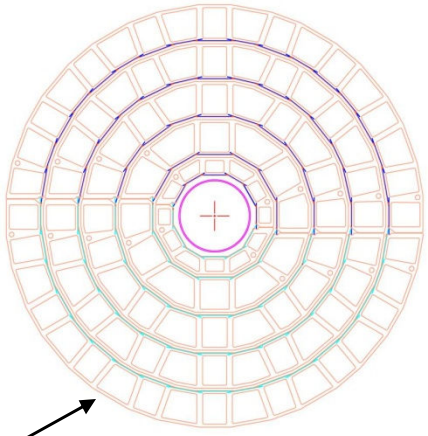
SiD Beam Pipe and Tracking system

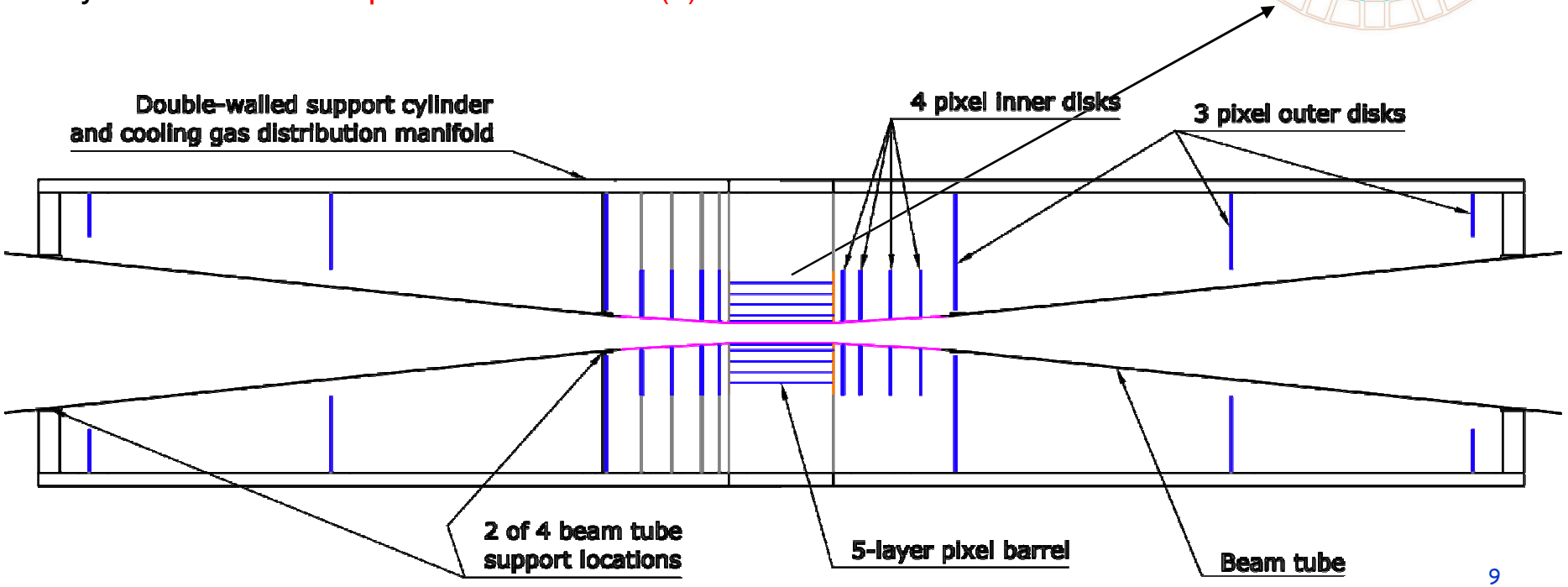


Vertex Detector

- Gas cooled (Barrel 20Watts)
- Power pulsed (Barrel:100:1 duty factor, 2000Watt peak load =1.5Vx1333A)=> a serial powering/DC-DC(HV->LV) conversion
- low mass system (0.1% X_0 / layer)
- Sensor technology : SiD directly working on 3D, Chronopix, and DEPFET sensors. Chronopix and 3D options have full single bunch crossing time stamping capability.
- Support structure: Sensors themselves form a support structure; sensors of each barrel layer are glued along their edges to form a cylinder. How to replace it if a sensor(s) failed ?

Rin=14mm
Rout=60mm

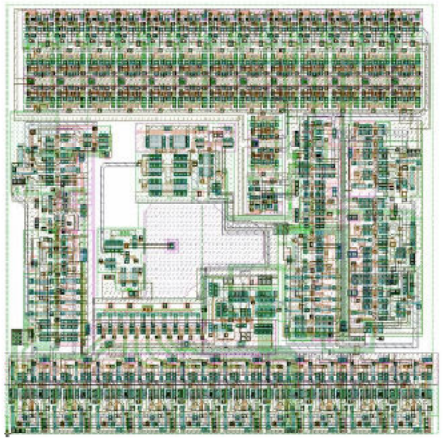


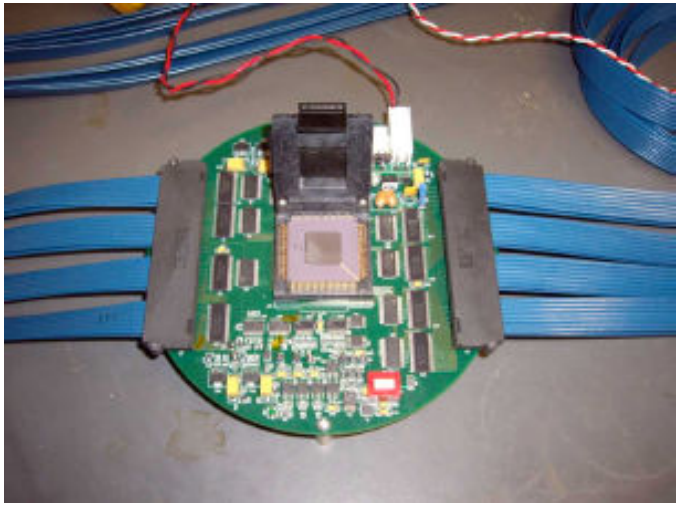


SiD VTX Example: Chronopix

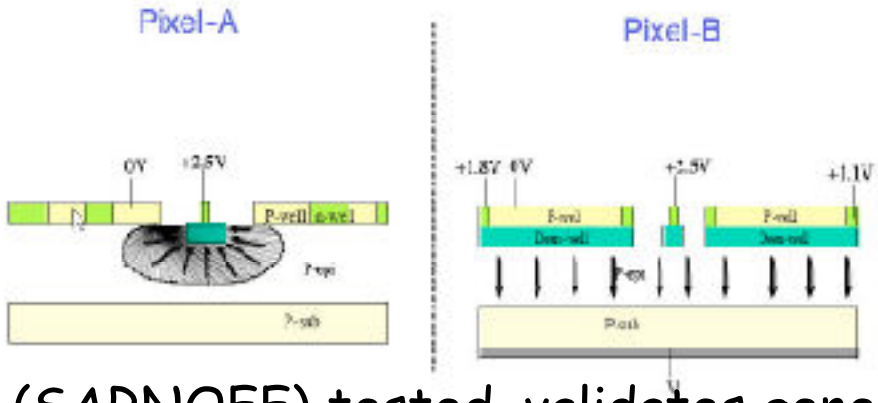
Specifications:

Detector sensitivity
10 μV/e (eq. to 16 fF)
Detector noise
25 electrons
Comparator accuracy
0.2 mV rms (cal in each pixel)
Memory/pixel
2 x 14 (will be 4 x 14)
Designed for scalability
eg. No caps in signal paths
Provisionally use limited pixel active area
use processes without deep-p well





Two sensor options
used for first prototype



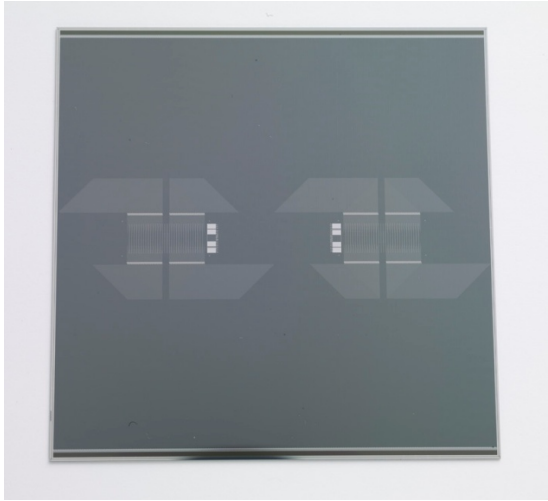
Status: First prototype (SARNOFF) tested, validates general concept, but improvements needed.

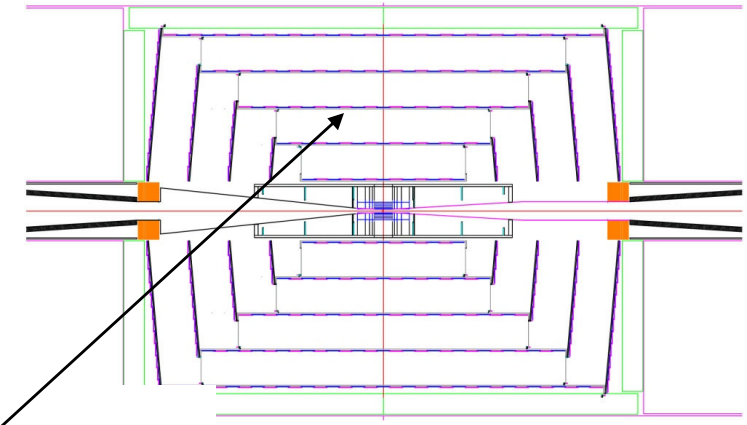
Second prototype: Fall 2010 after more design evolution and simulation.

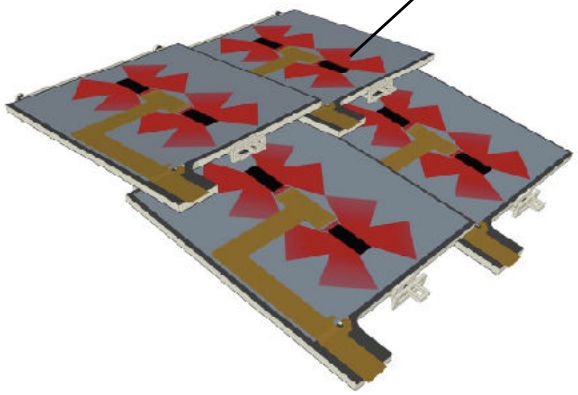
SiD is also working on 3-D and DEPFET solutions.

SiD Tracking – Silicon strips

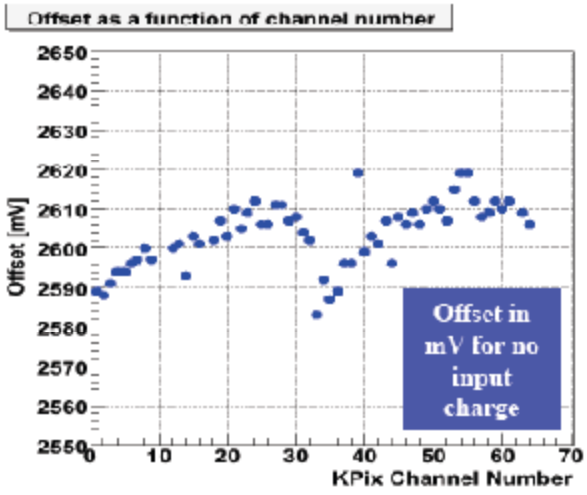
- SiD has an all-Silicon Tracker
- 5 barrel + 7 disk pixel inner vertex detector
- 5 barrel (axial strip) + 4 disk (stereo strip) outer detector. ~10 precision hits per track.







Tiling of tracking layer with Si sensors and on-board KPiX chips



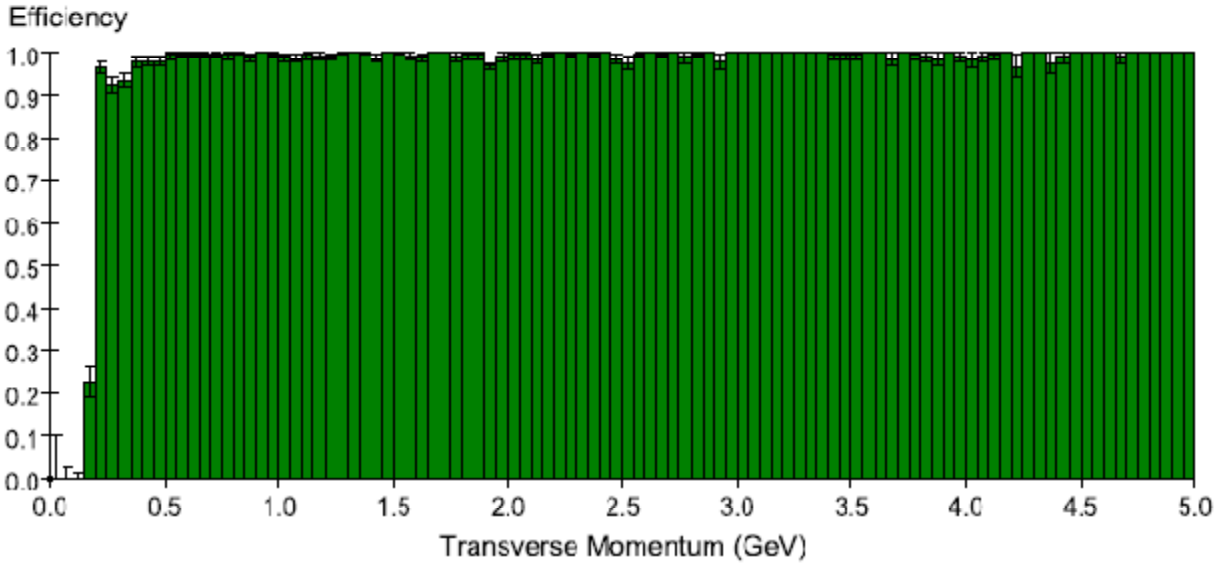
Sensor testing: UCSC/SLAC

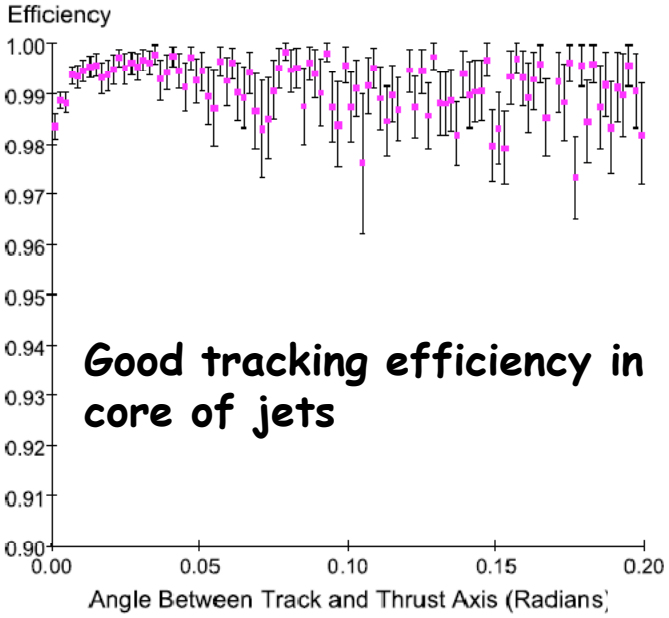
Tracking system performance

Generally find high tracking efficiency for tracks with:

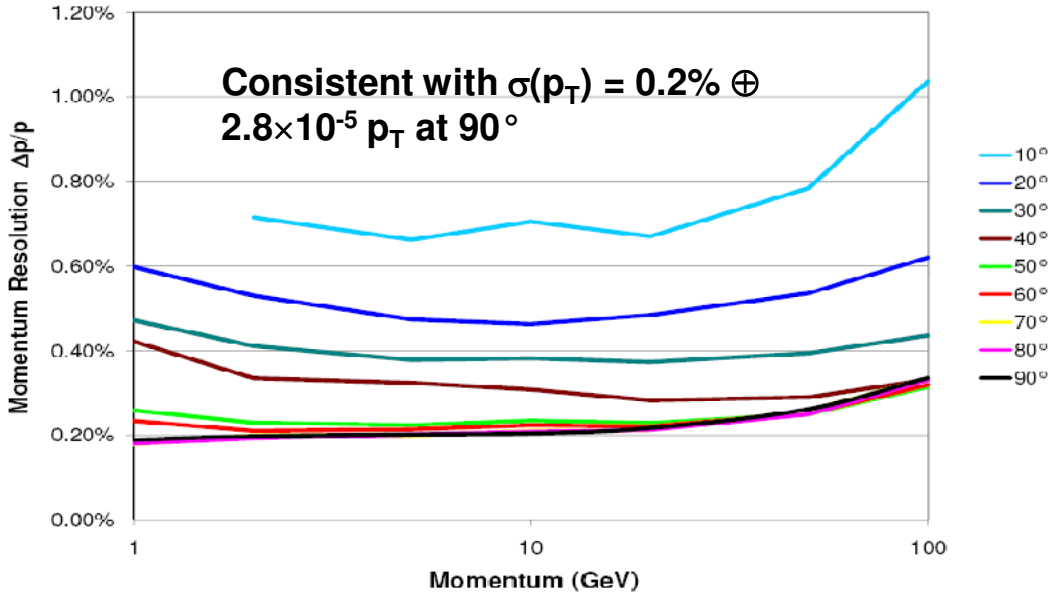
pT > 0.2 GeV

$|\cos(\theta)| < 0.99$

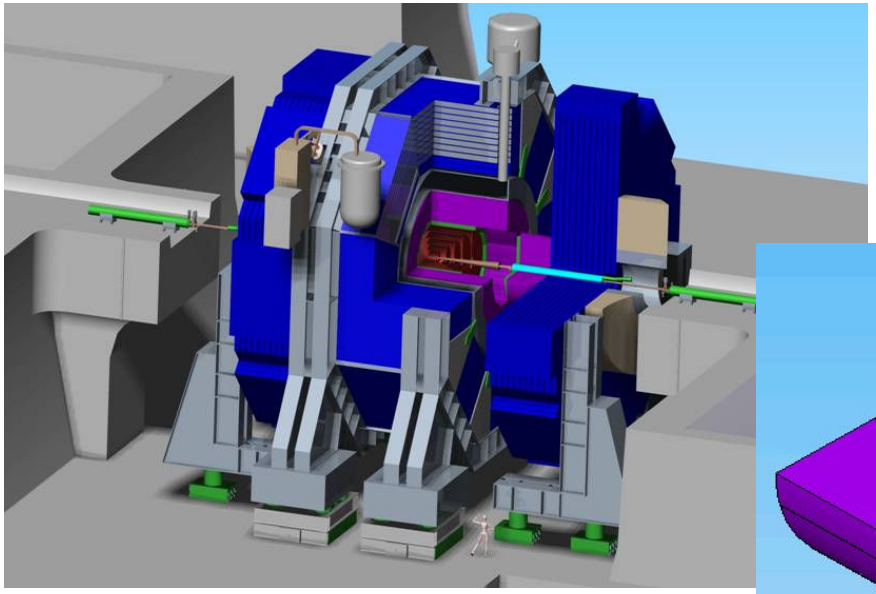


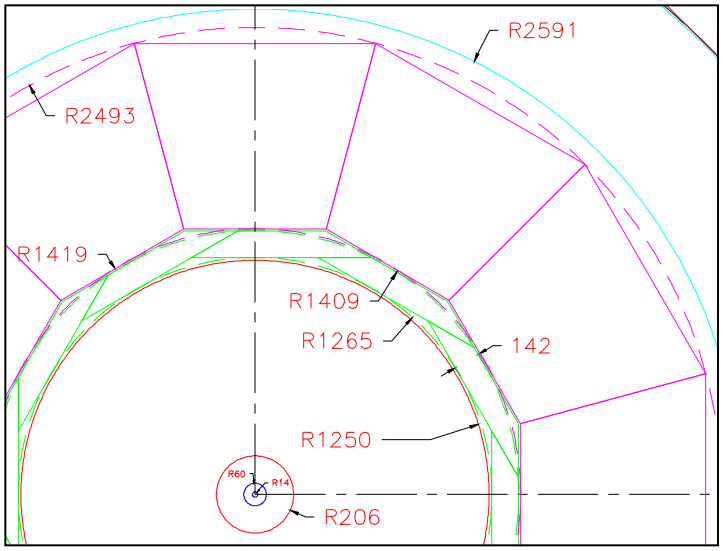


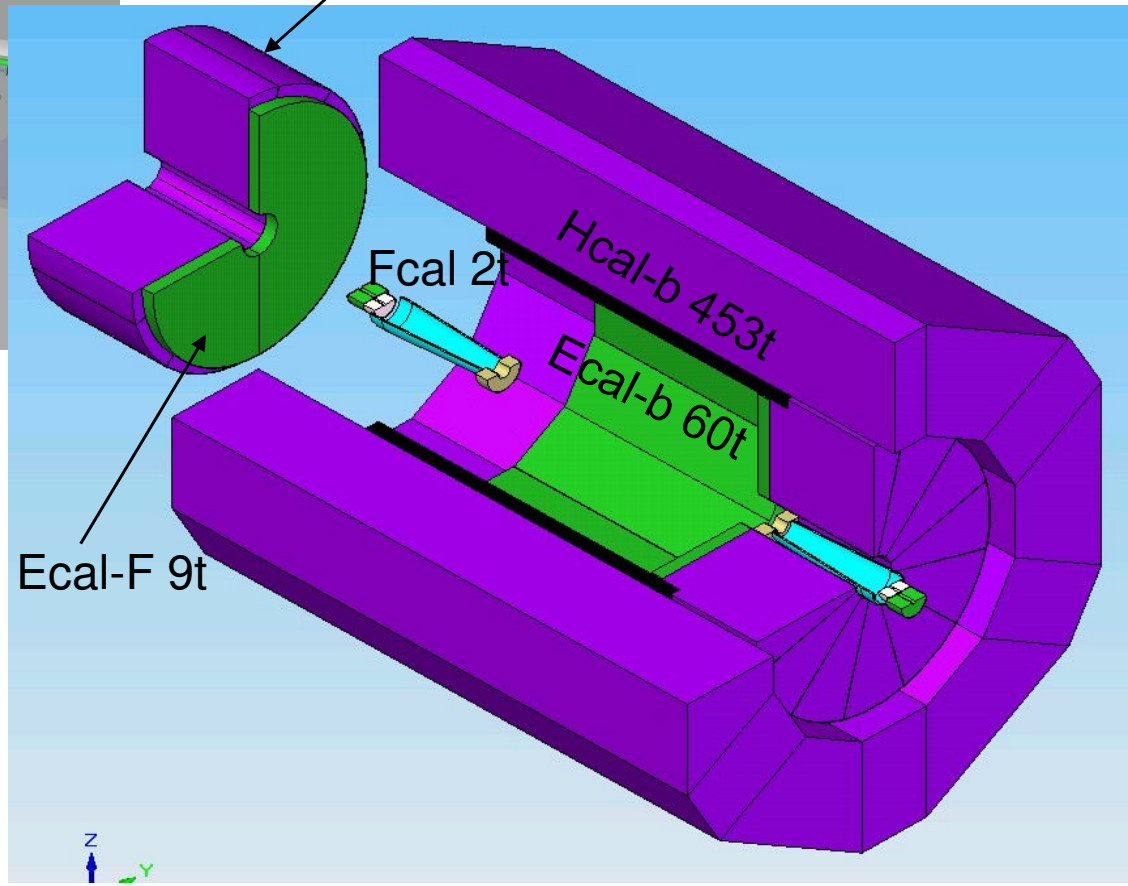
Good tracking efficiency in core of jets



SiD Calorimeter System



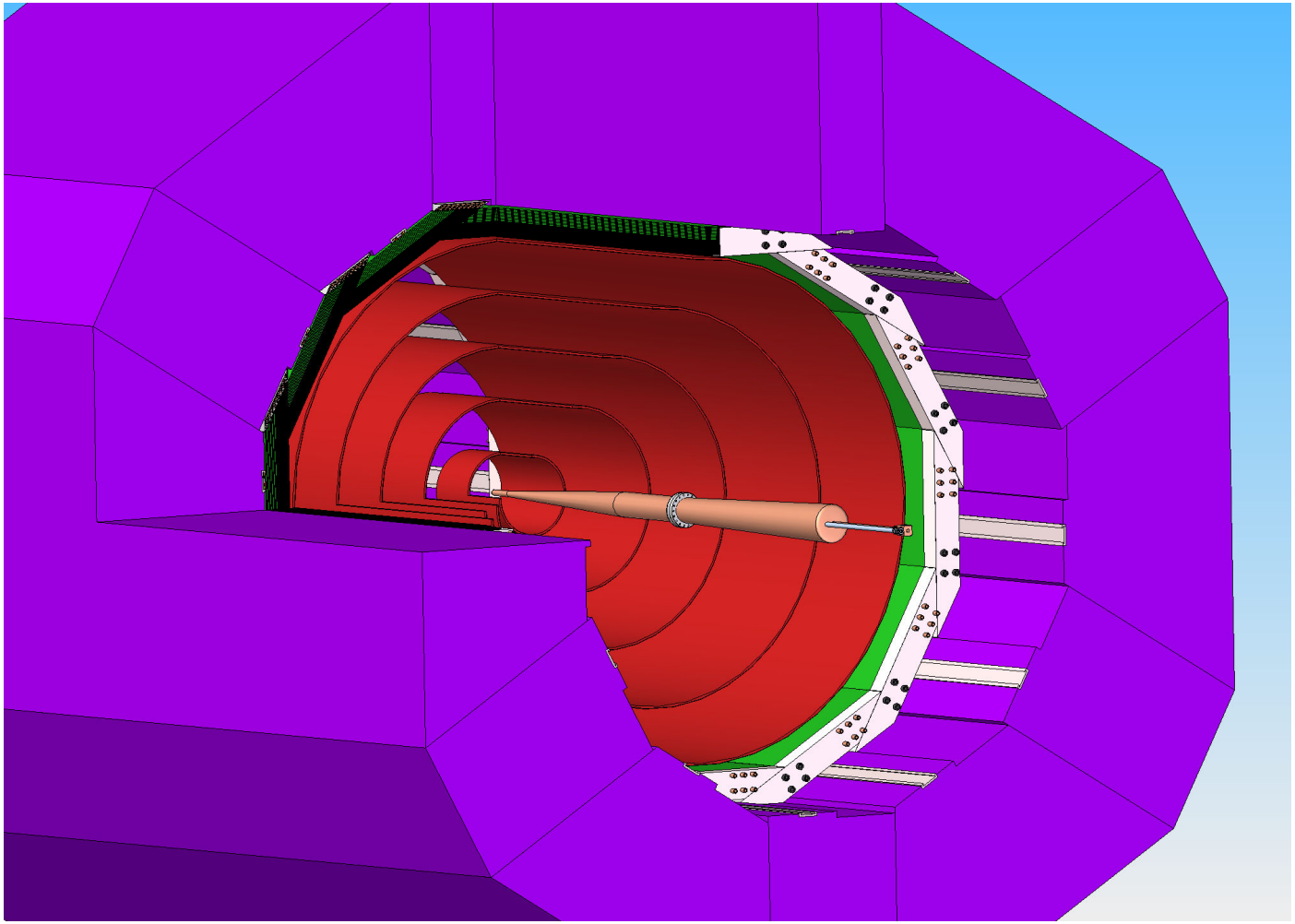




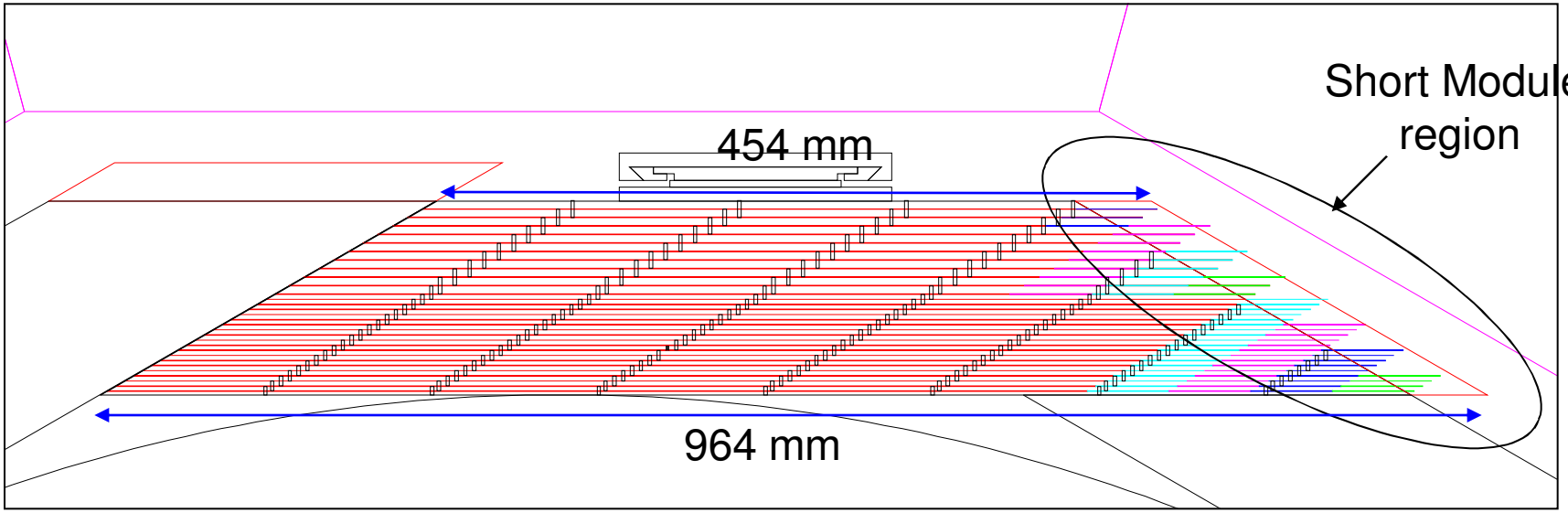
SiD Critical R&D

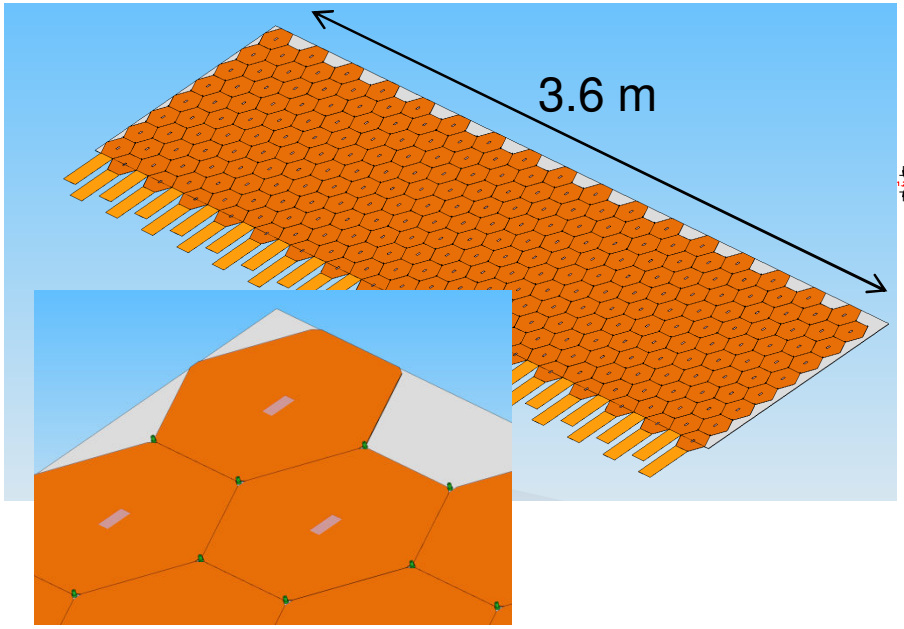
4) Electromagnetic Calorimetry.
For the baseline silicon-tungsten Ecal design, the operability of a fully integrated active layer inside the projected 1.25mm gap between absorber plates must be demonstrated. Sufficient S/N, successful signal extraction, pulse powering, and adequate cooling must be shown as well. Mechanical prototypes with steel rather than tungsten will first be built, followed by a full depth tower appropriate for beam tests. For the alternative MAPS technology being investigated in the U.K., a key need is production of large sensors with sufficient yield.

Si-W sampling/imaging ECAL



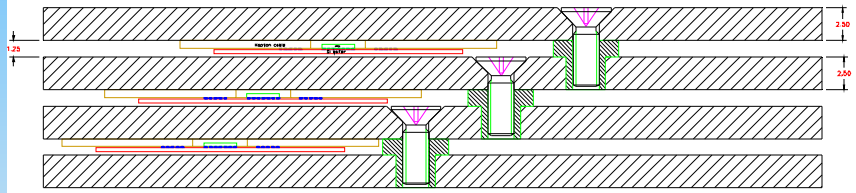
SiD Electromagnetic Calorimeter

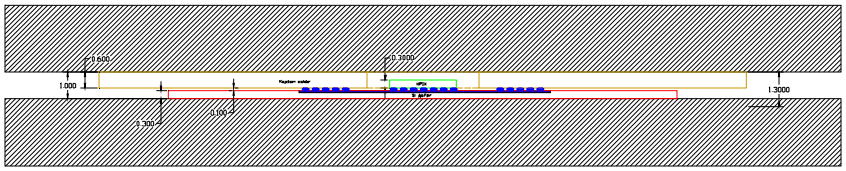




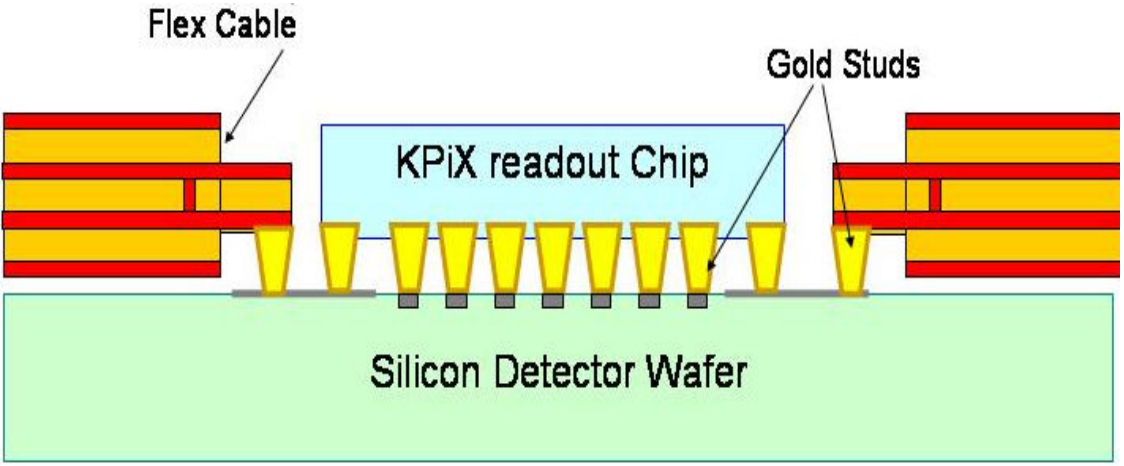
Staggered layout

Only 2 masks for the wafer and 8 for the kapton

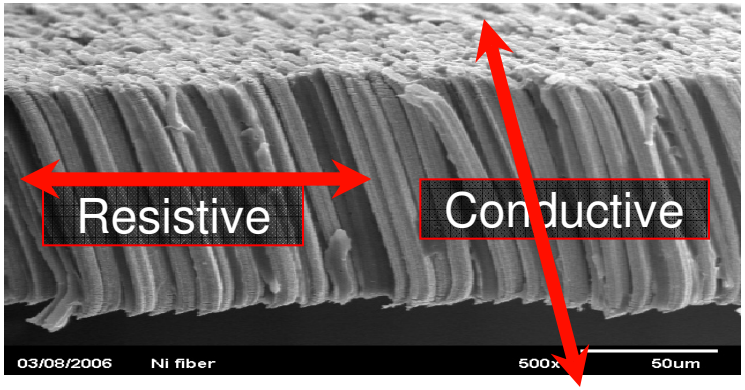


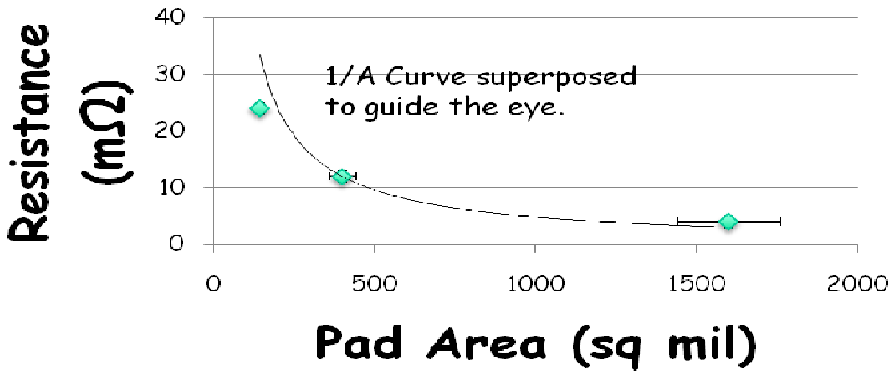


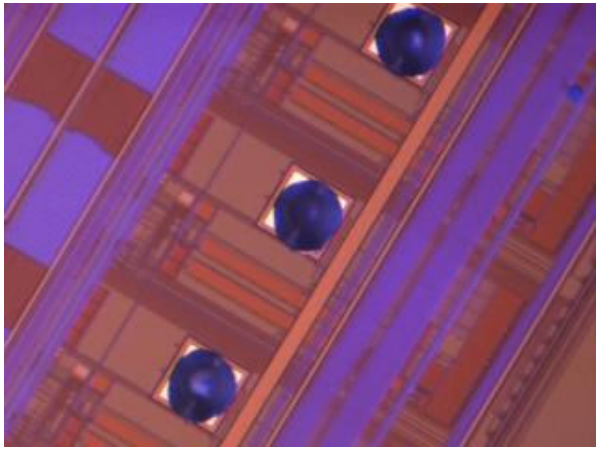
SiD Electromagnetic Calorimeter



Anisotropic Conducting Film







Initial results are promising. Goal for Flex Cable pads (100 sq mil) is ~100 mΩ, which is achievable.

Beyond the first year

Calorimetry: ECal

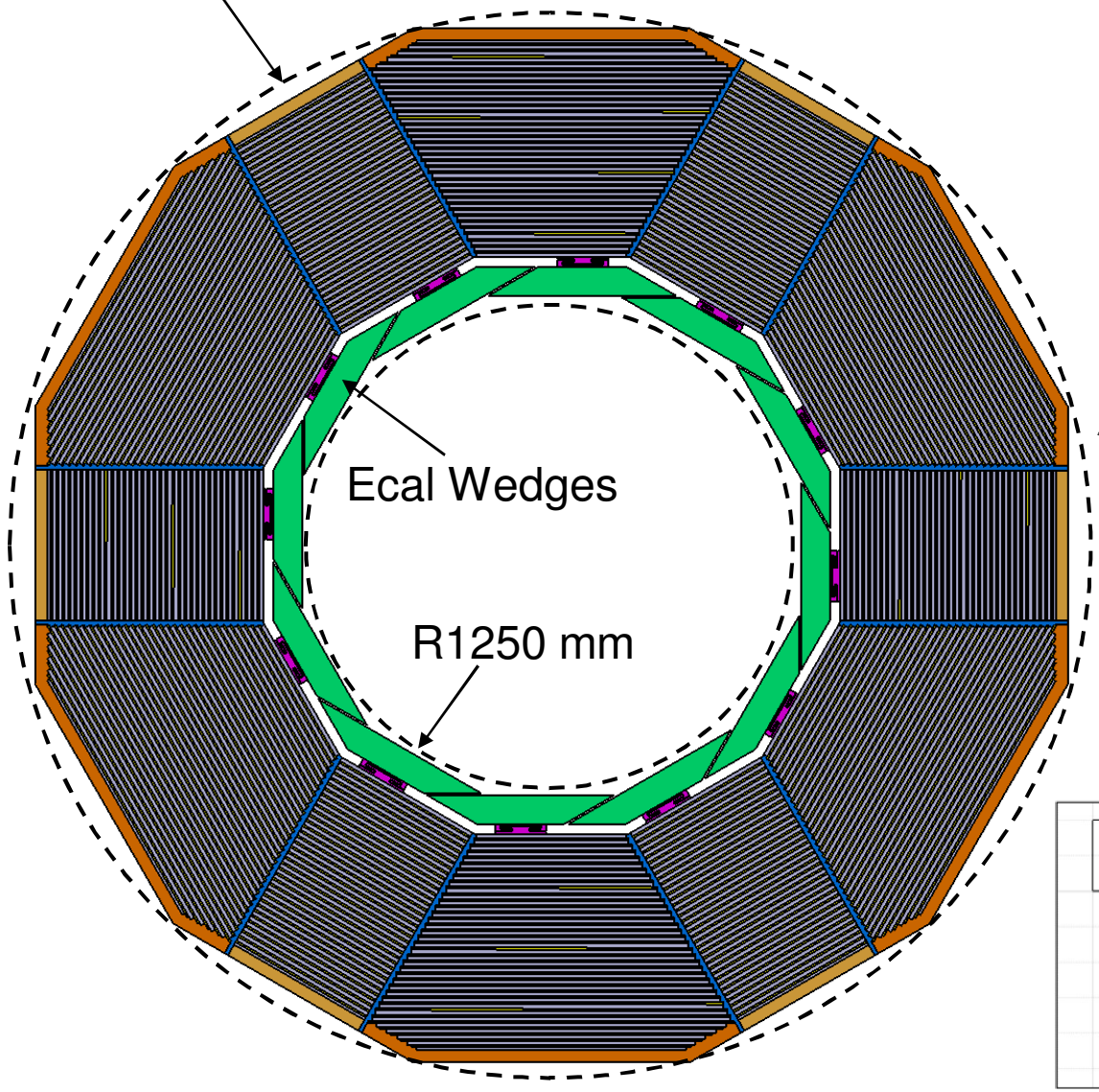
- Si-W ECal: anticipate that the test-beam related data taking and analysis will continue well into 2011.

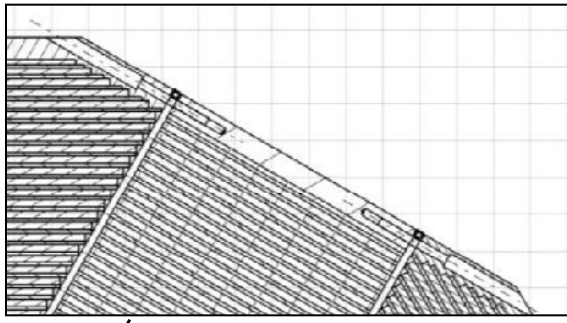
- First the module will be tested in an electron beam (possibly at SLAC), followed later by a beam test with hadrons.

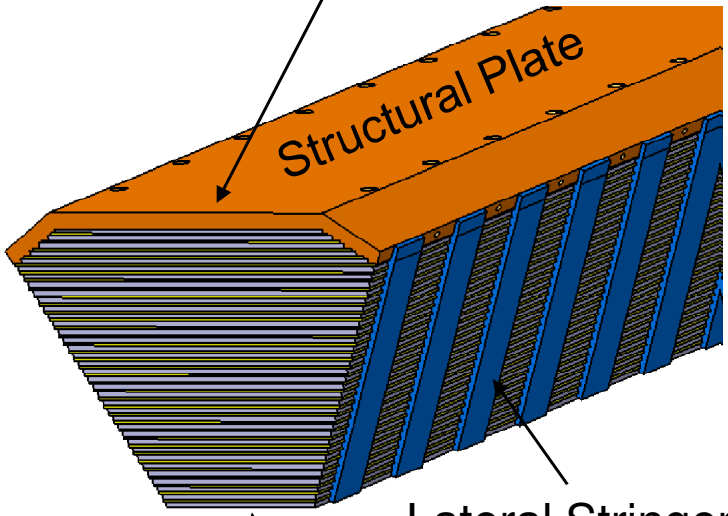
- Completion of this R&D is expected by 2012.

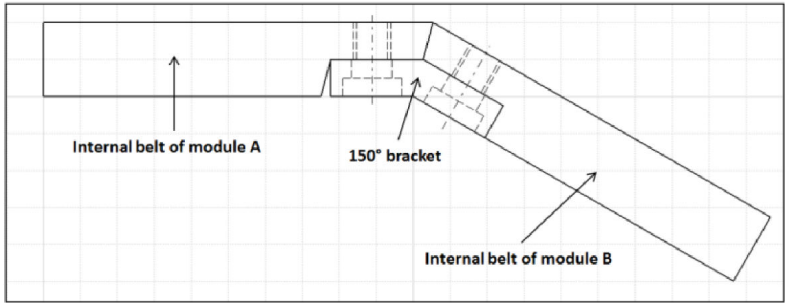
- MAPS ECal: the goal is to make a second generation chip which is sufficiently large to make a ECAL stack to study digital electromagnetic calorimetry in detail.

SiD HCal – a design









Nicolas Geoffroy - LAPP

SiD Critical R&D: HCal

5) Hadronic Calorimetry.
The priority for hadronic calorimetry is to demonstrate the feasibility of assembling a fully integrated, full-size active layer within a ~8mm gap between absorber plates. Several technologies are being investigated: RPC's, GEM's, Micromegas, and scintillating tiles/SiPM's. All of this work is being carried in conjunction with the CALICE Collaboration, and the results will form a critical component of SiD's future technology selection. An alternative approach, using homogeneous crystal calorimetry with dual readout, is also being studied. This effort needs to demonstrate good hadronic energy linearity and resolution in a test beam, to develop suitable crystals, to produce a realistic conceptual design, and to simulate physics performance.

RPC DHCAL

Argonne NATIONAL LABORATORY

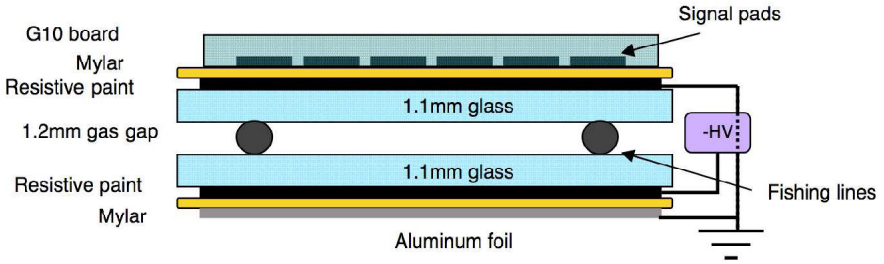
The University of Iowa

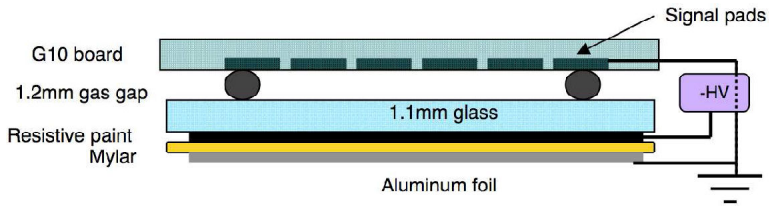
Boston University

CALICE Calorimeter for ILC

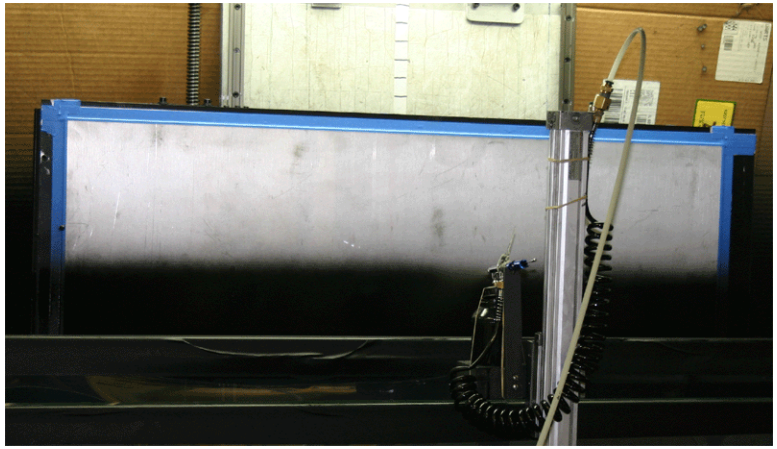
Construction of 1m^3 prototype RPC stack:

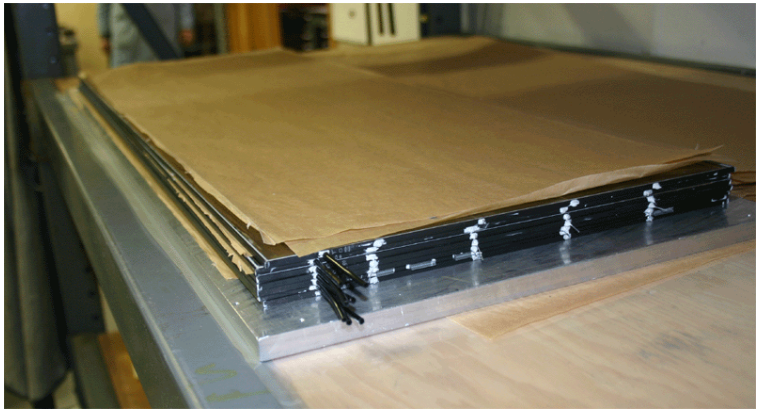
- 114 chambers + spares
- Essentially all materials in hand
- 2 man-days/chamber
- 3 assembly lines
- Start tests at Fermilab in September (after shutdown)

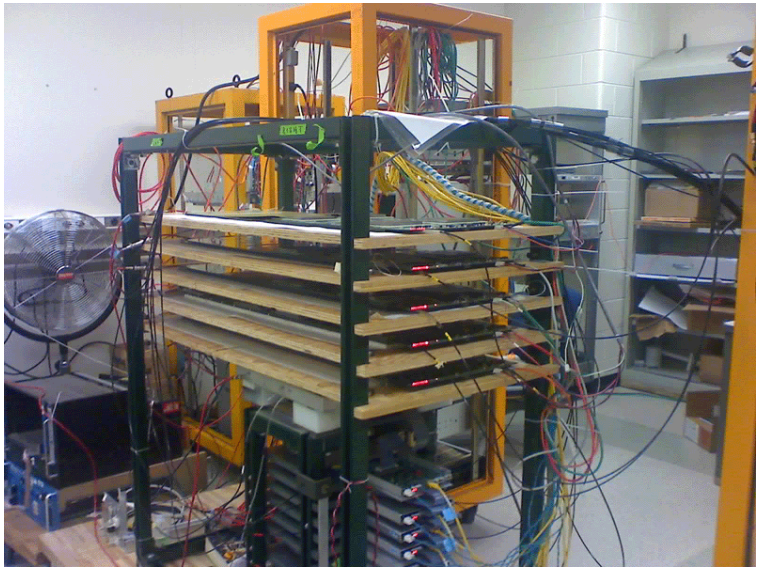




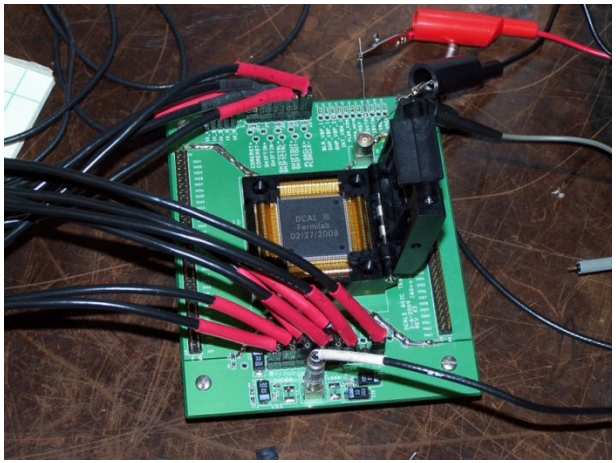
RPC chamber construction for 1m^3 stack

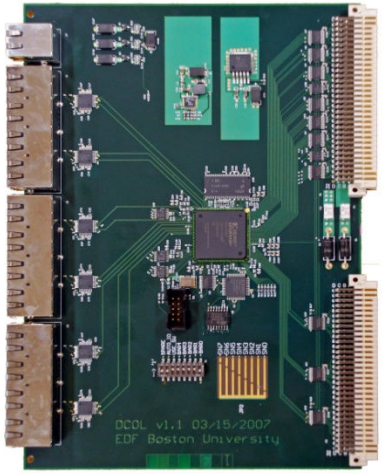


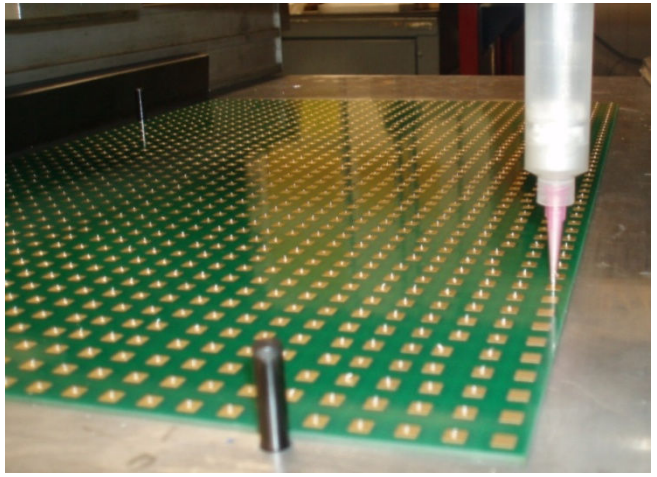


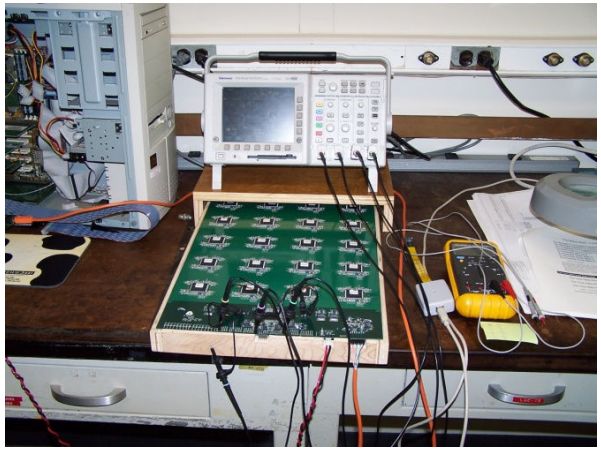


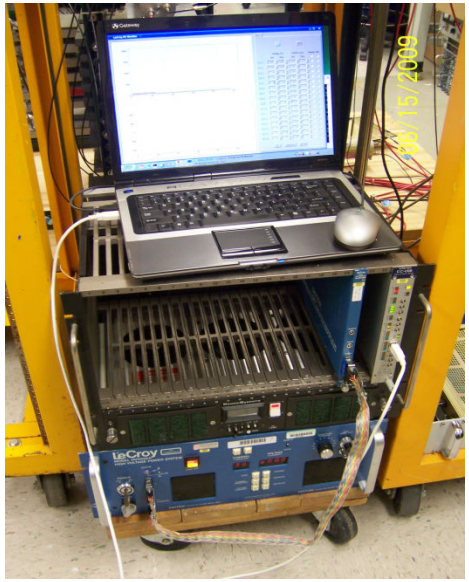
RPC-DHCAL – DCAL chip, Data collector, FEB, Gas, HV







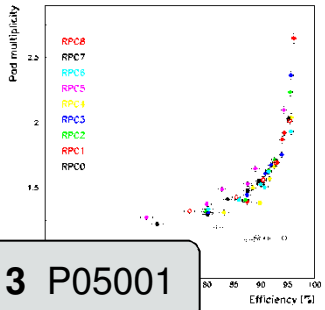




Analysis of Vertical Slice Test Data

Calibration of a Digital Hadron Calorimeter with Muons

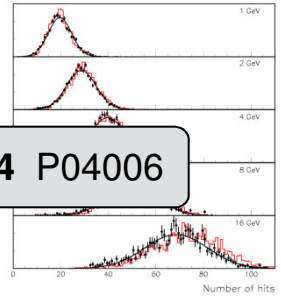
Measurement of the noise rate
Measurement of the efficiency and pad multiplicity under different operating conditions



B.Bilki et al., 2008 JINST **3** P05001

Measurement of Positron Showers with a Digital Hadron Calorimeter

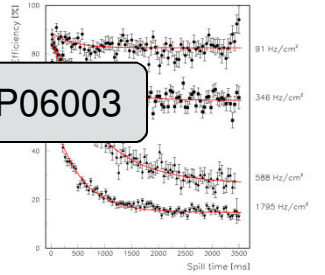
Measurement of positron showers (response and shape)
Tuned simulation to reproduce measurement



B.Bilki et al., 2009 JINST **4** P04006

Measurement of the Rate Capability of Resistive Plate Chambers

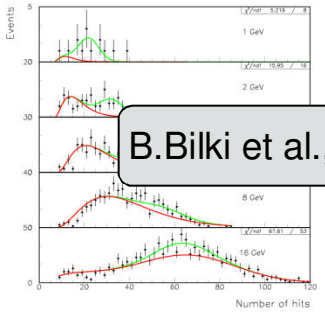
Measurement of short term effect (not observed)
Measurement of rate dependence
New model to calculate RPC response
(contribution to understanding of RPCs)



B.Bilki et al., 2009 JINST **4** P06003

Hadron Showers in a Digital Hadron Calorimeter

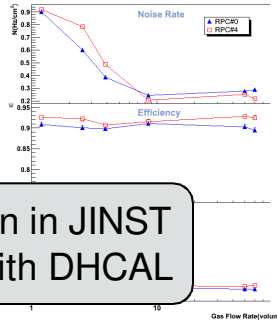
Measurements with very small calorimeter (leakage)
Absolute prediction from simulation (no tuning!)
Including simulation of response of 1 m³ prototype



B.Bilki et al., 2009 JINST **4** P10008

Environmental Dependence of the Performance…

Measurement of efficiency, pad multiplicity and noise rate as function of air pressure, ambient temperature, air humidity and gas flow

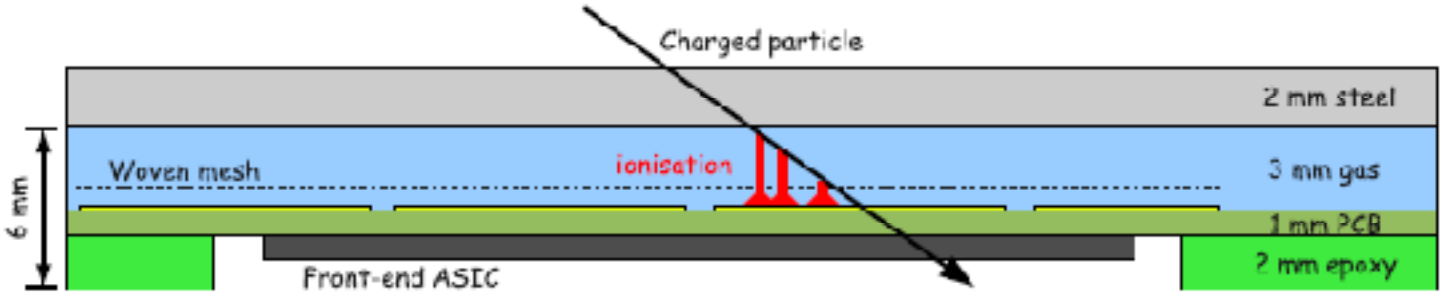


Now published!

Paper accepted for publication in JINST
First completed PhD thesis with DHCAL

Many results from Vertical Slice Test !

Micromegas-DHCAL

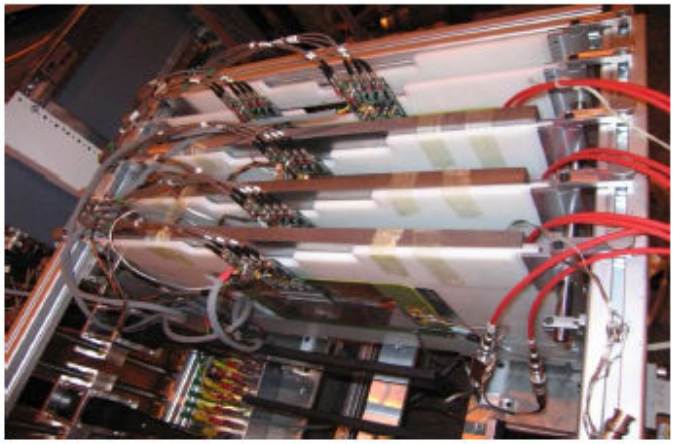


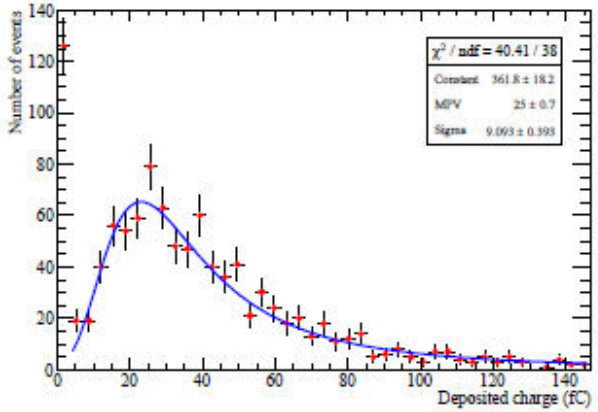
- MICROMEGAS for a DHCAL:
  - fast, radiation hard, good aging properties, robust, large area, high gas gain, spark proof, standard gas mixture (Ar, iC_4H_{10}, CO_2)
  - small avalanche charge $\rightarrow$ sensitive front-end electronics

Micromegas-DHCAL

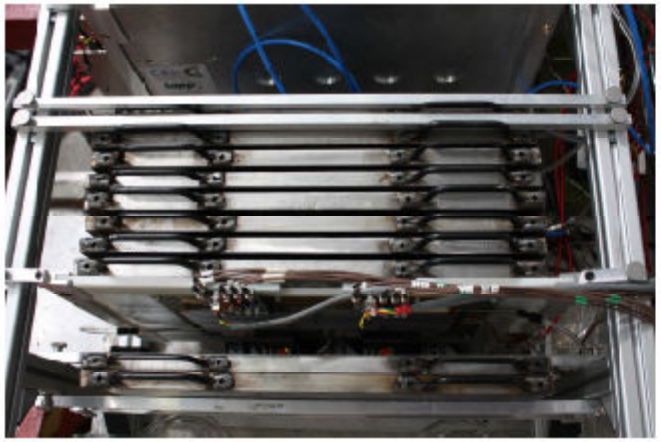
Test beam results

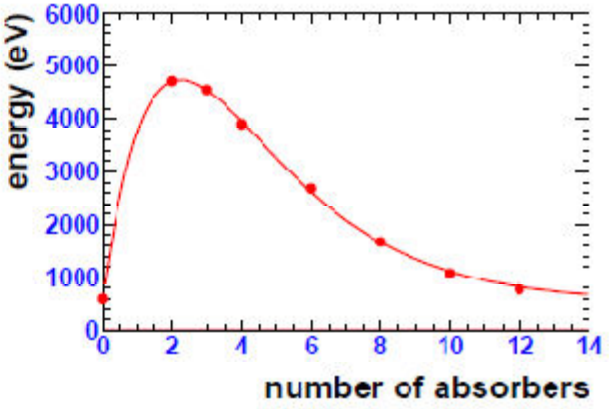
2008





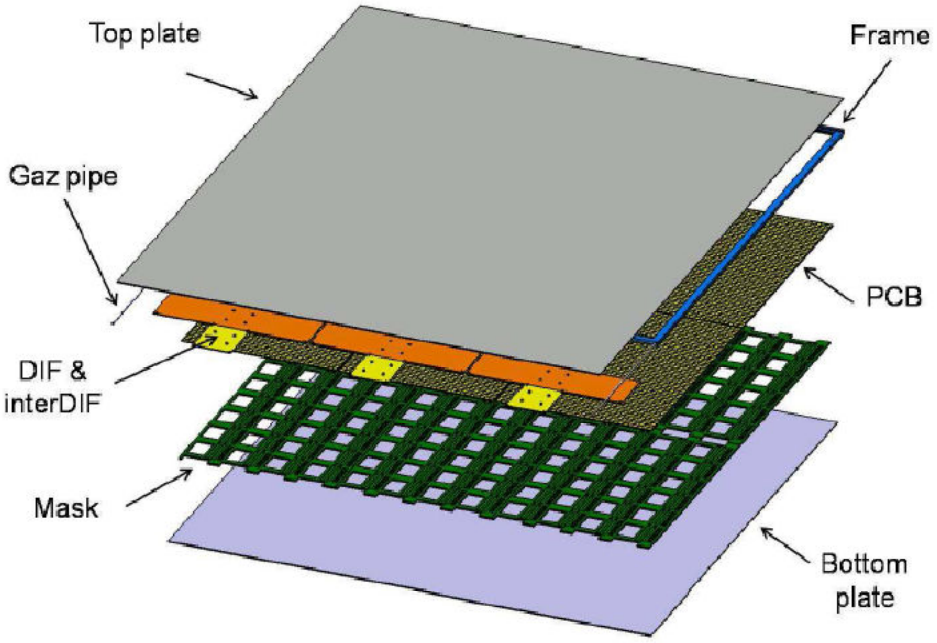
2009





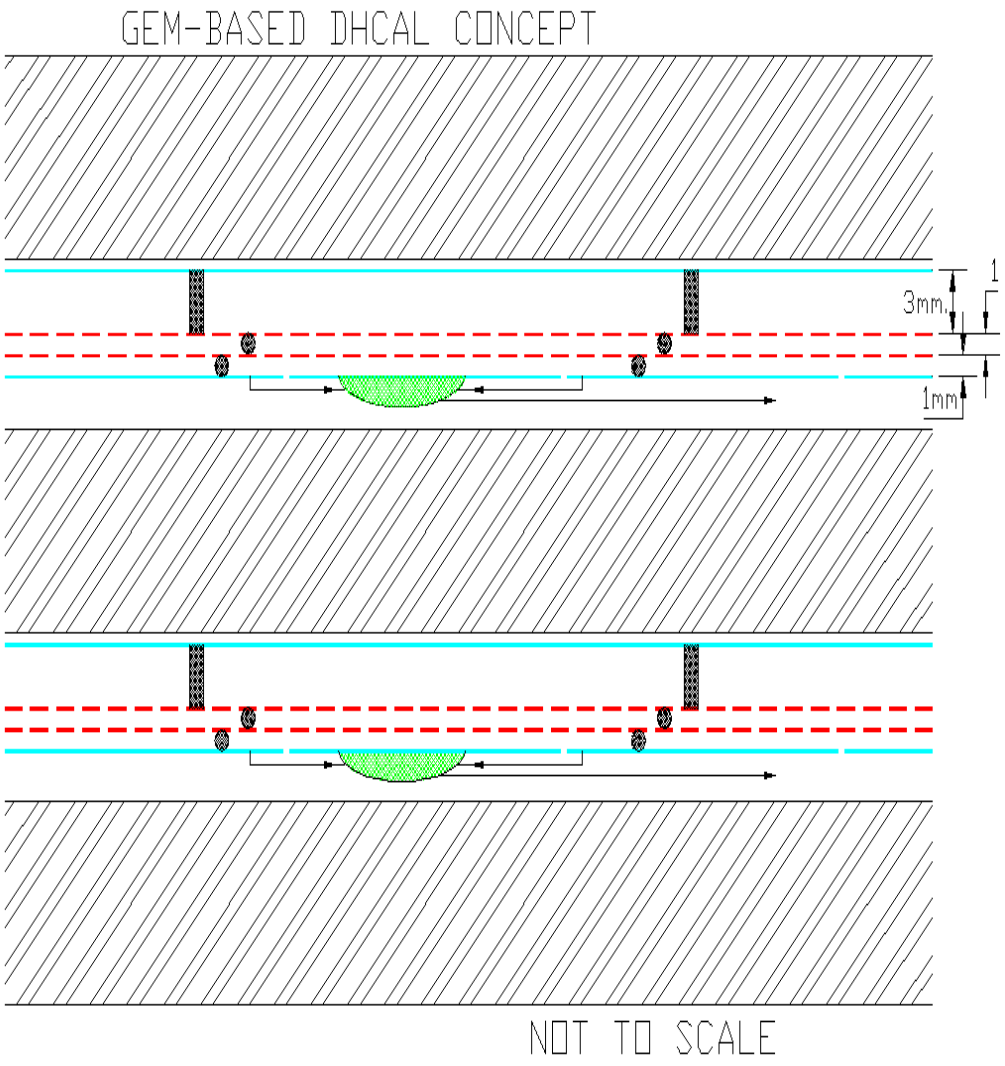
Micromegas-DHCAL

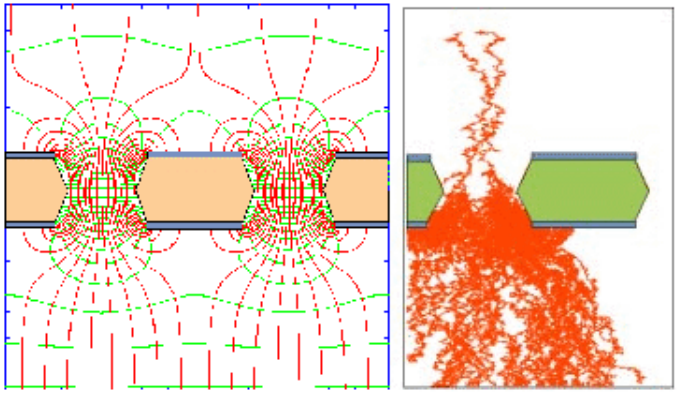
Design for 1m^2



Good progress towards 1m^3 technological prototype

GEM/DHCAL active layer concept





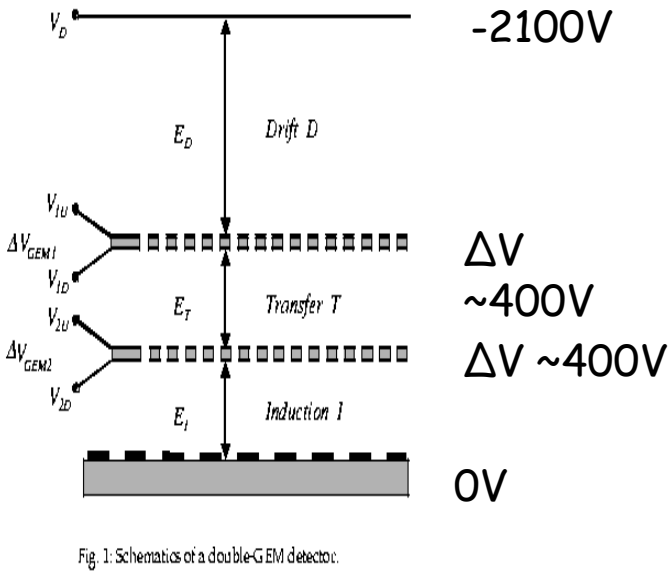
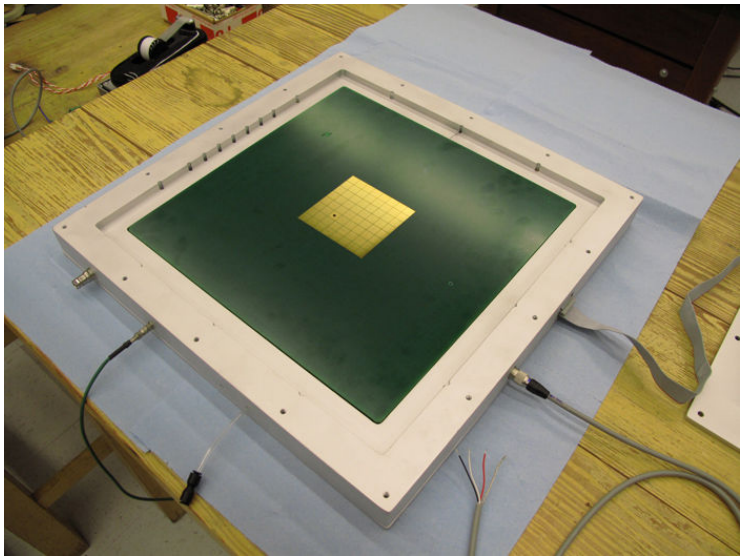
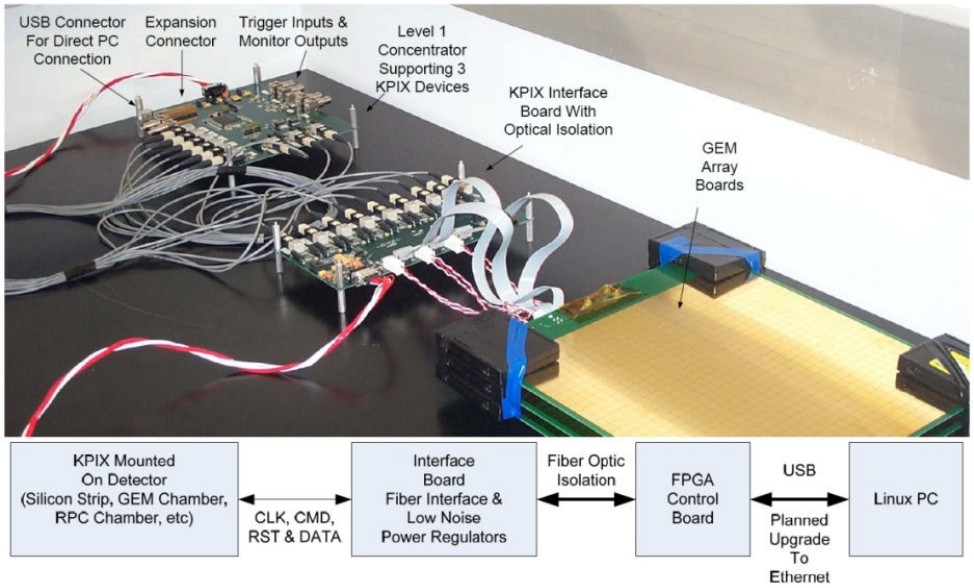
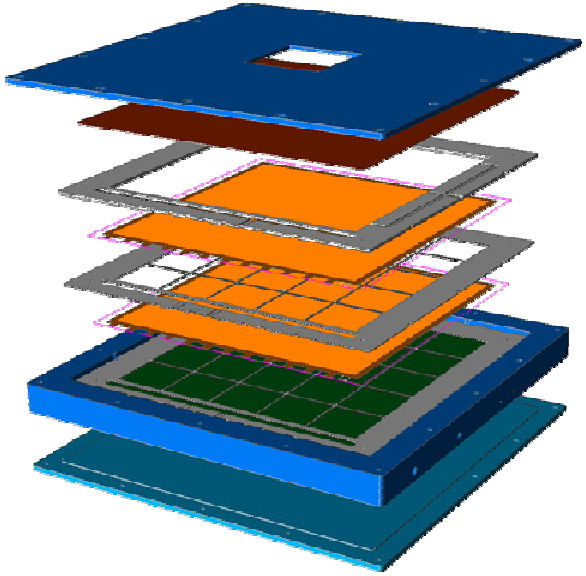


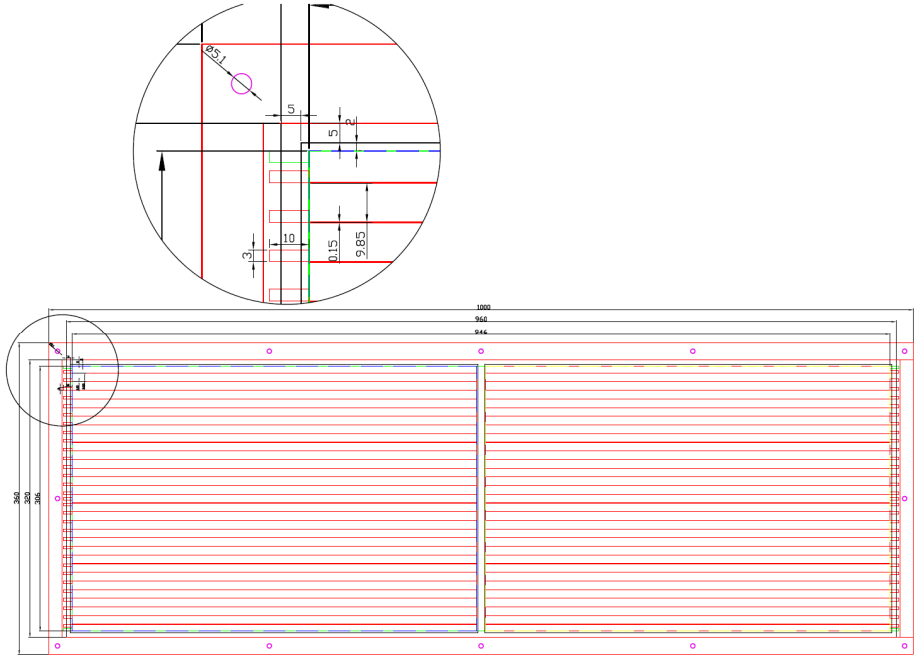
Fig. 1: Schematics of a double-GEM detector.

SiD GEM-DHCAL



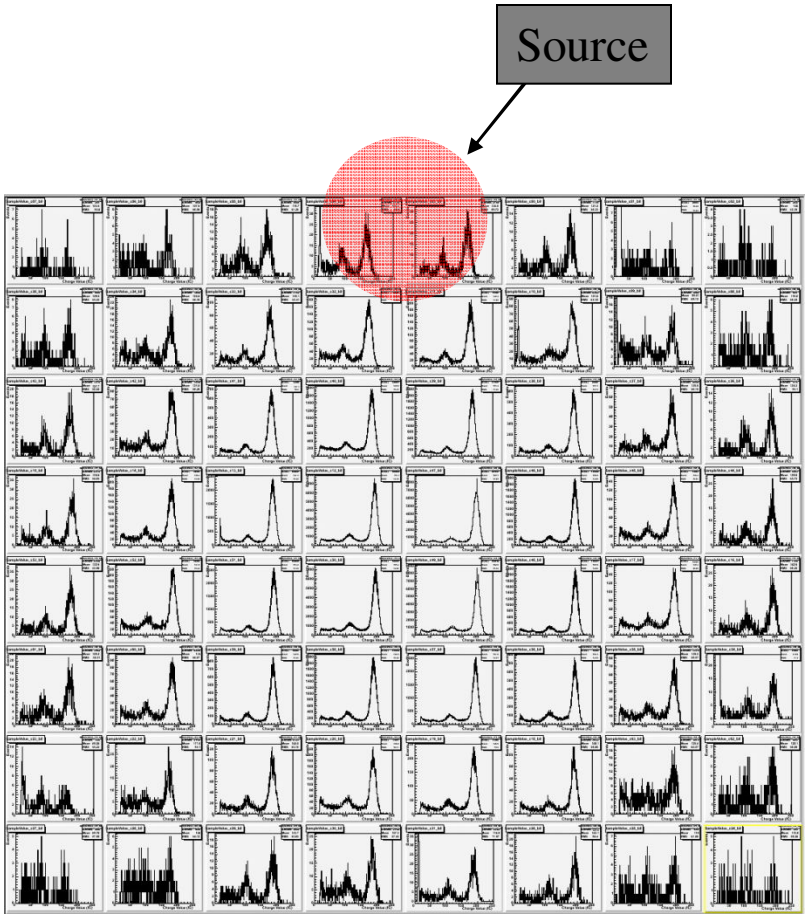


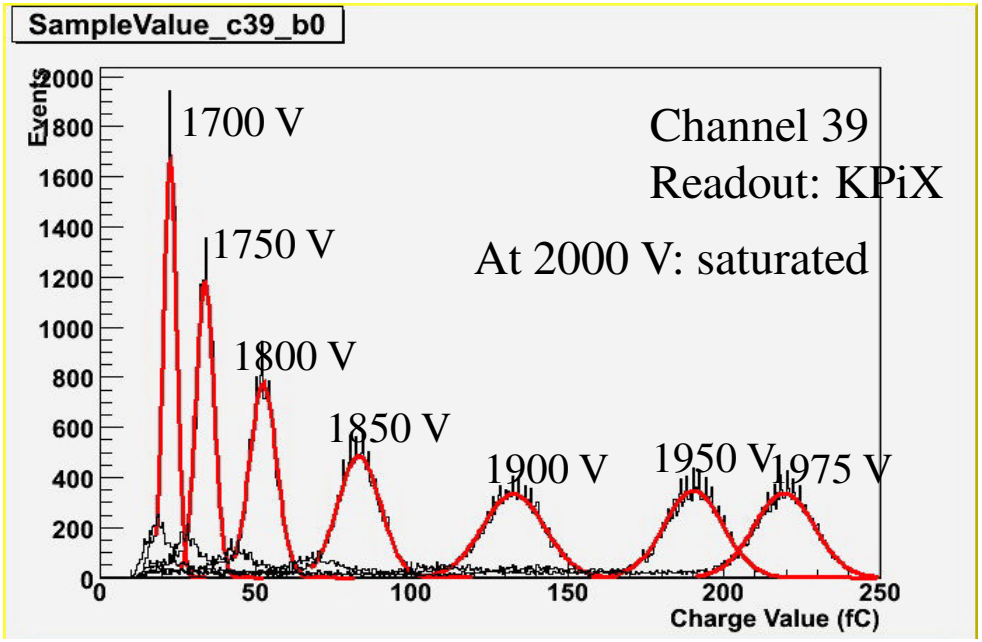


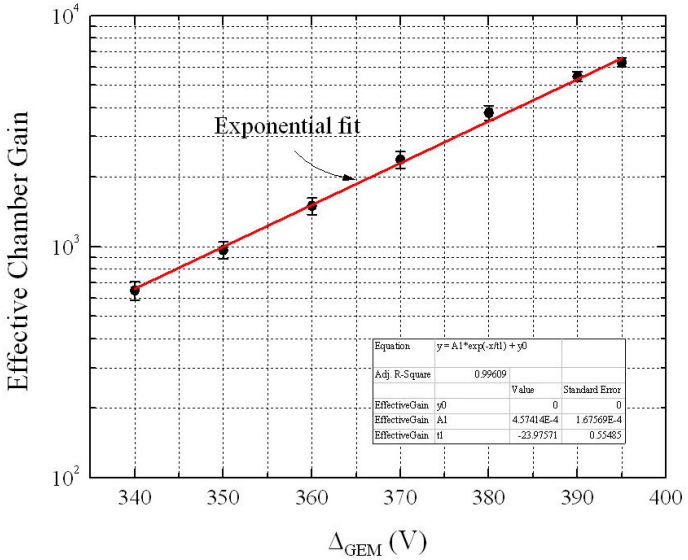


SiD GEM-DHCAL

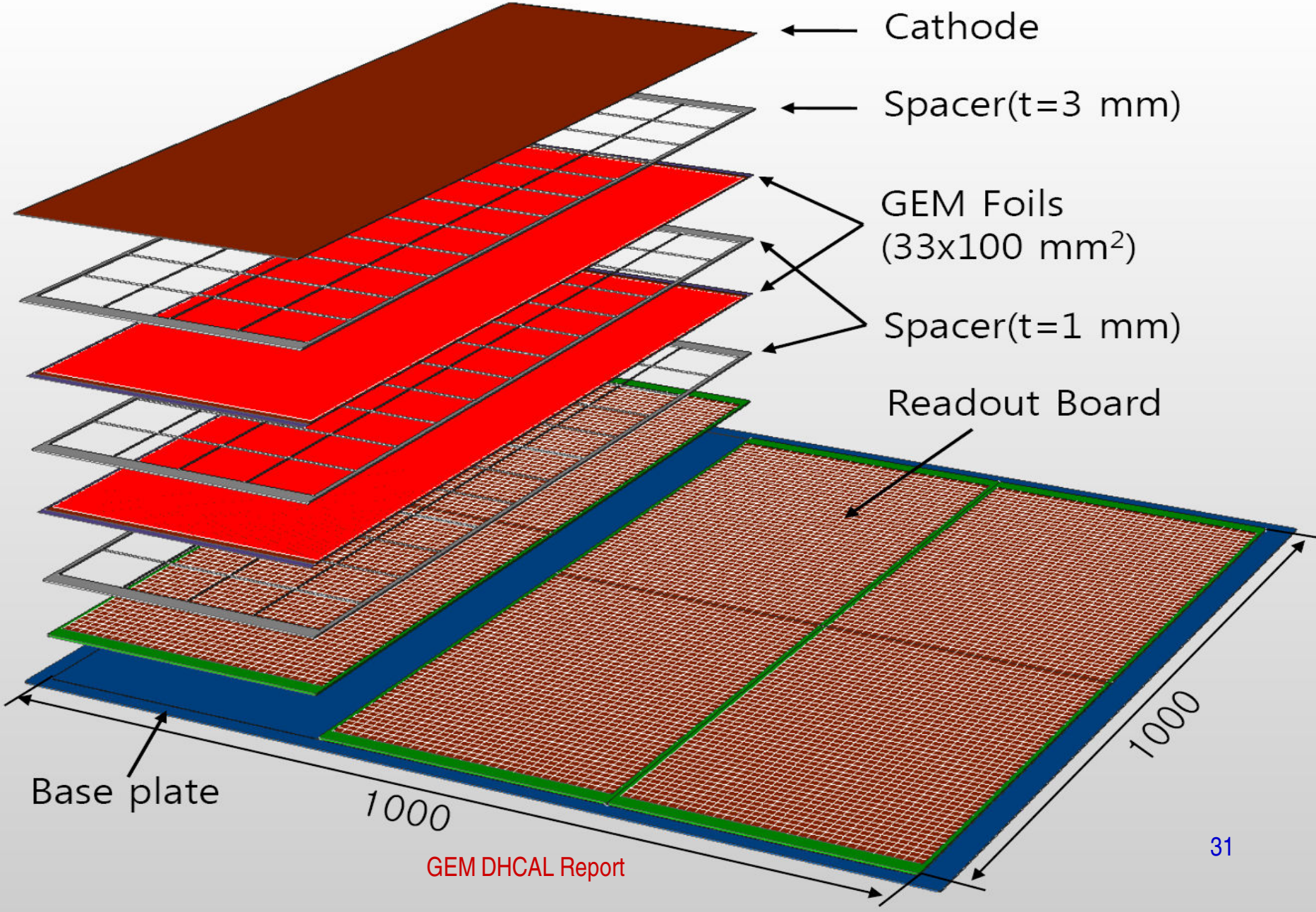
Histogram Map for Fe^{55} GEM+KPiX7







UTA's 100cm x 100cm Digital Hadron Calorimeter Plane



GEM DHCAL Beam Test Plans

- Phase I ➔ Completion of 30cm x 30cm characterization
  - Mid 2010: using one to two planes of 30cm x 30cm double GEM chamber with 64 channel KPiX7
- Phase II ➔ 33cm x 100cm unit chamber characterization
  - Mid 2010 – mid 2011 at MTBF: Using available KPiX chips and DCAL chips
- Phase III ➔ 100cm x 100cm plane GEM DHCAL performances in the CALICE stack
  - Early 2011 – Late 2011 at Fermilab's MTBF *or CERN*
  - Five 100cm x 100cm planes inserted into existing CALICE calorimeter stack and run with either Si/W or Sci/W ECALs, and RPC planes in the remaining HCAL

Beyond the first year

Calorimetry: HCal

- RPC option -> continue with testing the $1m^3$ stack. beyond the first year. Calorimeter will be exposed to muons and pions and positrons of various energies. The response and energy resolution will be measured together with characteristics of hadronic showers, for Particle Flow Algorithms. R&D for Technical Prototype – 2010-2012.

- GEM option will test its $1m^2$ layers as part of the CALICE hadron calorimeter prototype (2010-2011), and will design and build a complete, integrated layer with minimal thickness and full services. Thick GEM prototypes will also be assembled and tested as large sections of thick GEMs become available. Gas studies for thick GEMs will also continue.

Beyond the first year

- **Calorimetry: HCal**

-Micromegas option -> continued testing of, and analysis of results from, the $1m^3$ stack 2010-2011

- Scintillator/SiPM option -> insertion of the integrated readout layer planes fabricated with the CALICE/EUDET electronics into the CALICE absorber stack. This installation will be followed by the commissioning and exposure of this prototype to a test beam. 2010-2011?

- Homogeneous dual-readout calorimetry -> development of suitable crystals, photodetectors, and associated readout electronics, all in preparation for a demonstration of linearity and energy resolution for hadrons in a test beam, while developing a conceptual design for inclusion of this technology into SiD. 2010-2012?

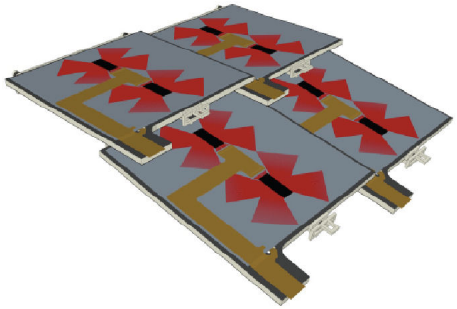
SiD Critical R&D: Electronics

6) Electronics.
One critical item on electronics is a demonstration of the operation of 1024 channel version of the baseline KPiX chip. Another is to develop power distribution schemes for the vertex detector and tracker with DC-DC conversion or serial powering. Adapting and testing KPiX readout to the tracker, calorimeters, and muon systems must also be continued and perfected.

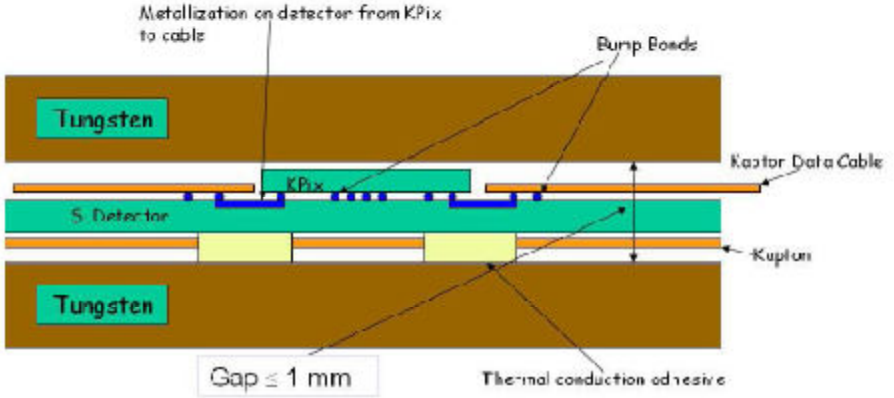
SiD Electronics - KPiX

KPiX readout for all SiD subsystems except VTX and FCal

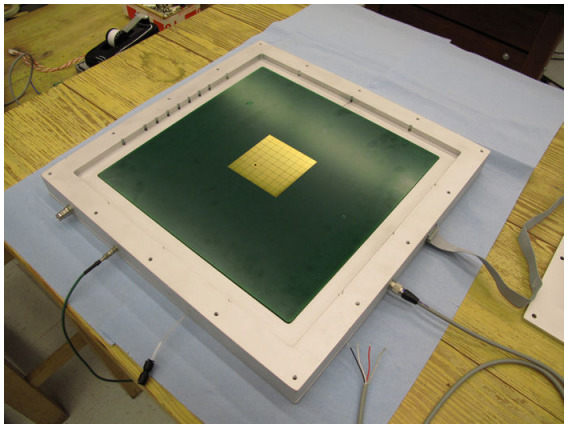
Tracker



ECal



HCal

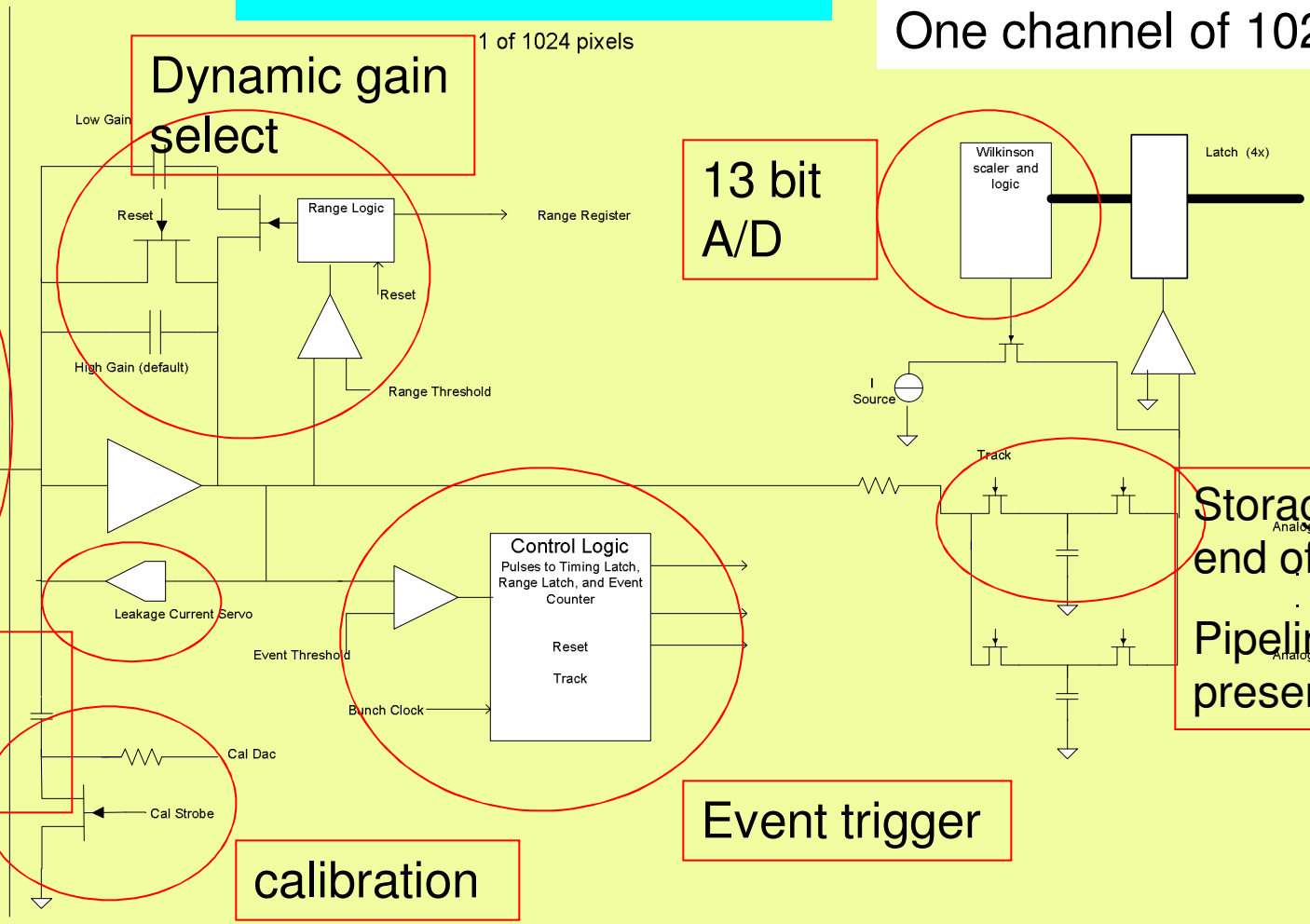


...and Muon!

KPiX/GEM/DHCAL

KPiX chip

One channel of 1024



Simplified Timing:

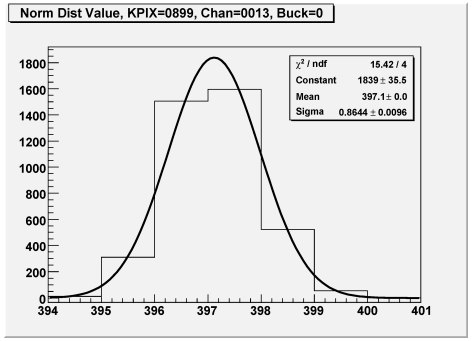
There are ~ 3000 bunches separated by ~300 ns in a train, and trains are separated by ~200 ms.

Say a signal above event threshold happens at bunch n and time T0.
The Event discriminator triggers in ~100 ns and removes resets and strobes the Timing Latch (12 bit), range latch (1 bit) and Event Counter (5 bits).
The Range discriminator triggers in ~100 ns if the signal exceeds the Range Threshold.
When the glitch from the Range switch has had time to settle, Track connects the sample capacitor to the amplifier output. (~150 ns)
The Track signal opens the switch isolating the sample capacitor at T0 + 1 micro s. At this time, the amplitude of the signal at T0 is held on the Sample Capacitor .
Reset is asserted (synched to the bunch clock) . Note that the second capacitor is reset at startup and following an event, while the high gain (small) capacitor is reset each bunch crossing (except while processing an event)
The system is ready for another signal in ~1.2 microsec.
After the bunch train, the capacitor charge is measured by a Wilkinson converter.

SiD Electronics - KPiX

- Some problems (lock-up) with KPiX 7 (64-channel), and KPiX 8 (256-channel).

-> Noise measurement

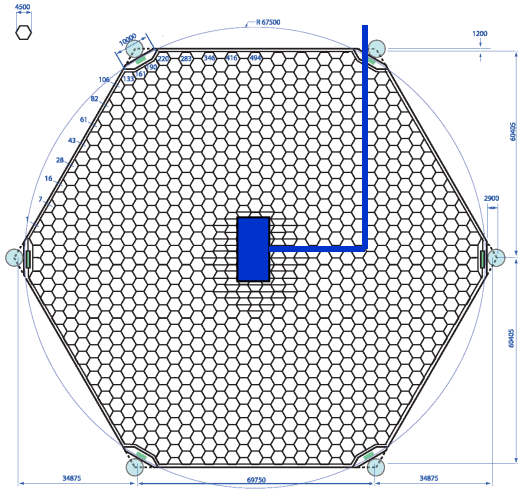


1300 e rms

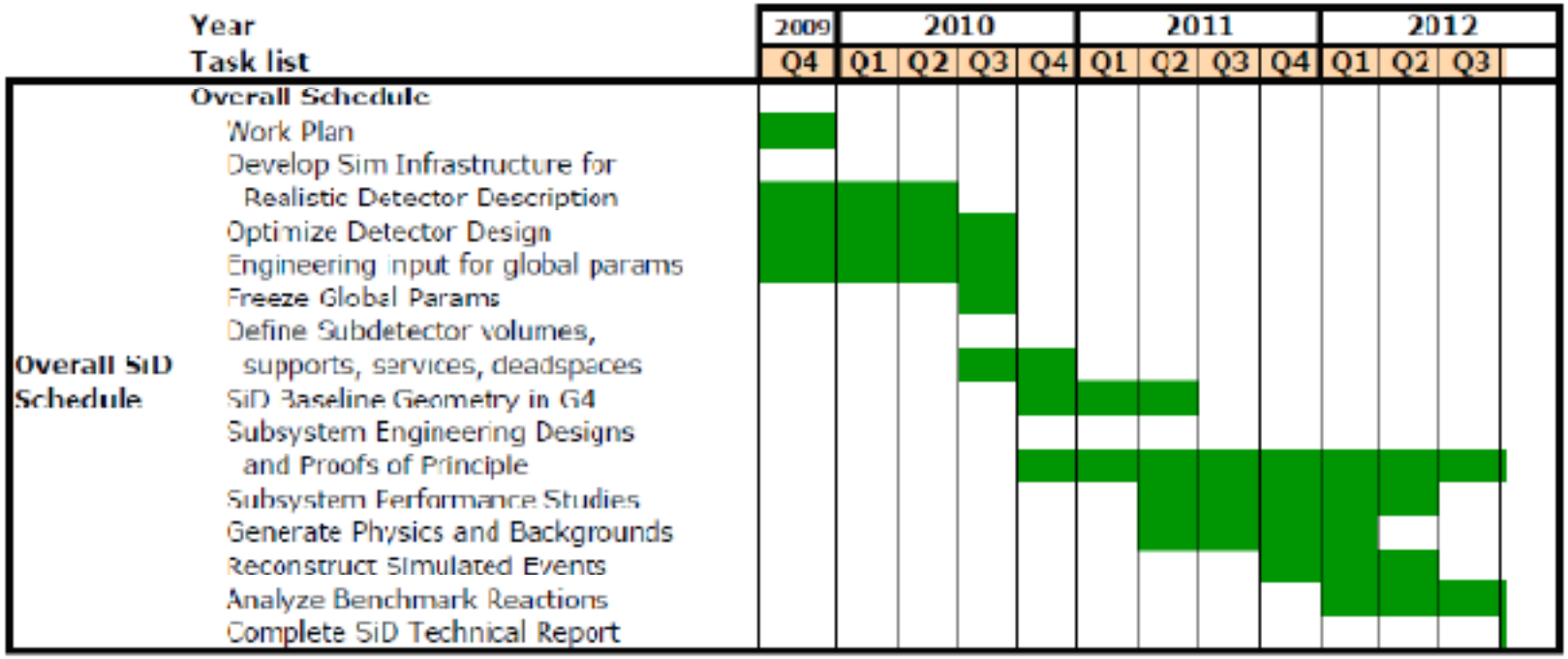
- Version 9 submitted: 512 channels – back in few weeks.

With a 512-channel KPiX-9 bump-bonded to a sensor, can get noise measurements for the full range of input capacitances and resistances. Goal for ~ Spring.

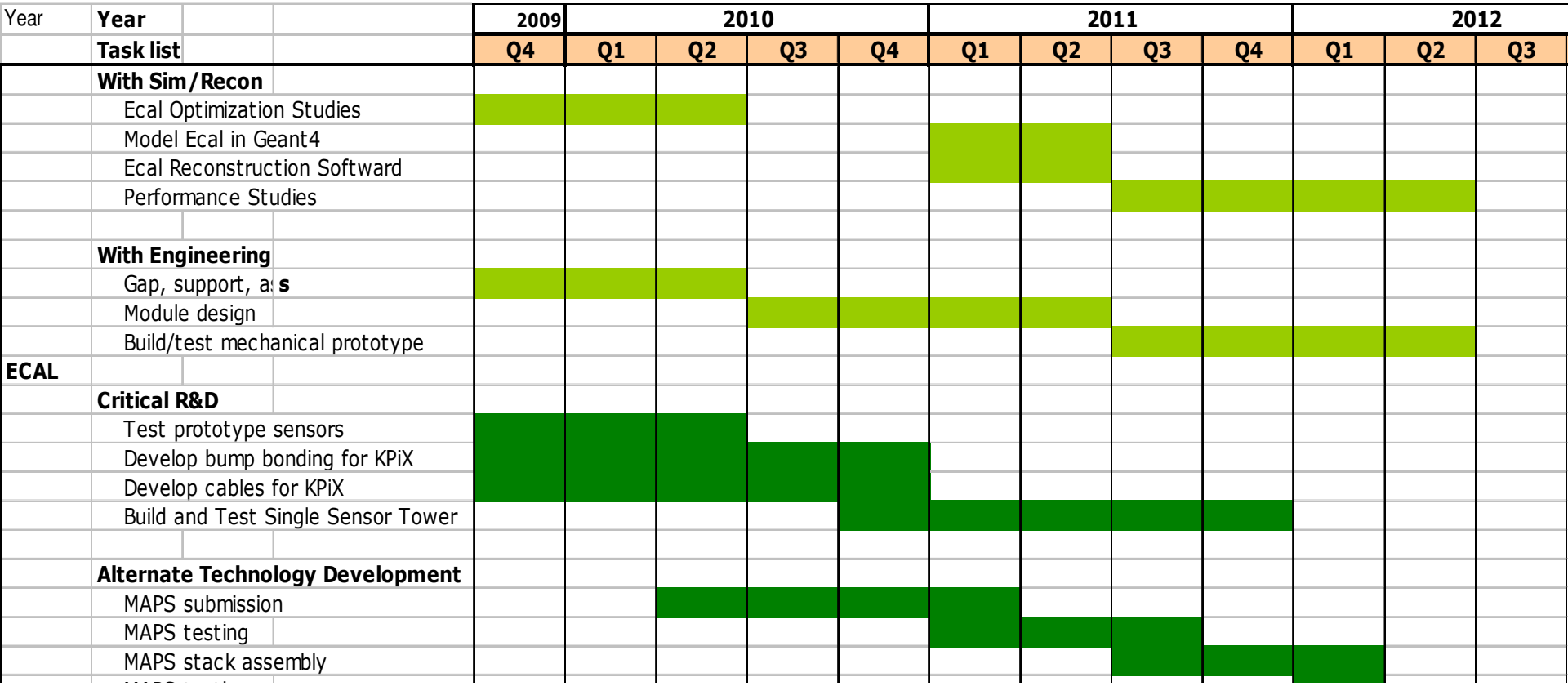
1024-channel KPiX by Summer



The Path to 2012: SiD Work Plan



Subsystem Planning: ECal example



Complete Work Plan for SiD and all subsystems completed and submitted to Research Director, Oct 09