

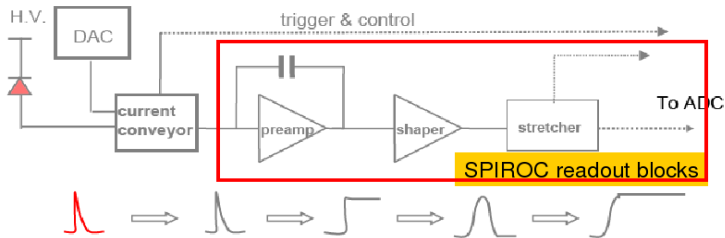
Update report on SiPM Charge Readout Chip (KLauS) in Heidleberg

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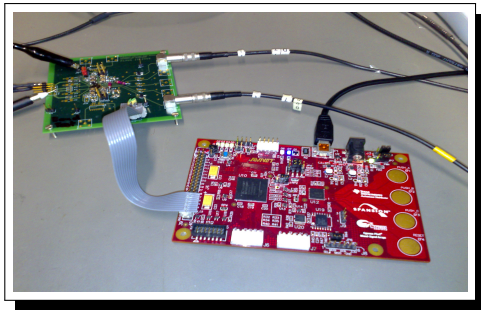
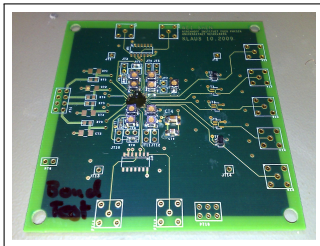
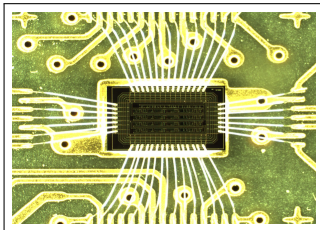
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Diagram of KLauS



- AMS $0.35\mu m$ CMOS technology , 4 channels
- shaping 25ns,50ns, 100ns ; scale factor 1,10,50
- SPI interface, 30 bits slow control

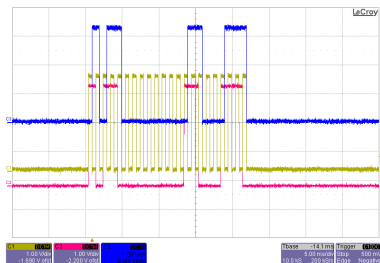
Wire-bonded KLauS & test PCB



- FPGA connect via USB with PC
- slow control controlled by commands in Linux
- SPI to FPGA , normal 6 pins connector

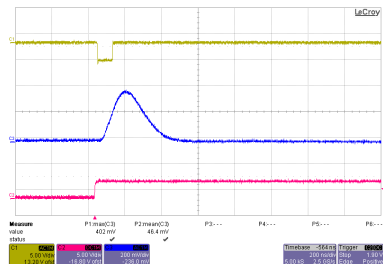
Slow control & function test

SPI configured with FPGA



- Xilinx SPARTAN 3
- SPI data in = data out

function test via charge injection

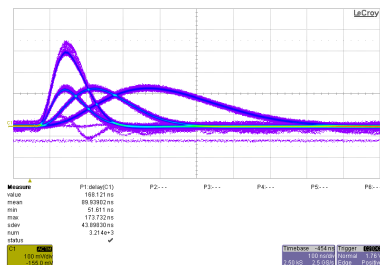


- reponse after the shaper
- TTL trigger from CVY unit

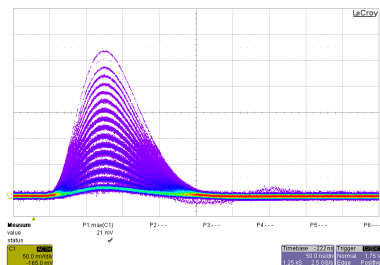
Shaping, scaling & charge injection test

current scaling factor 1

shaping time & gain switch



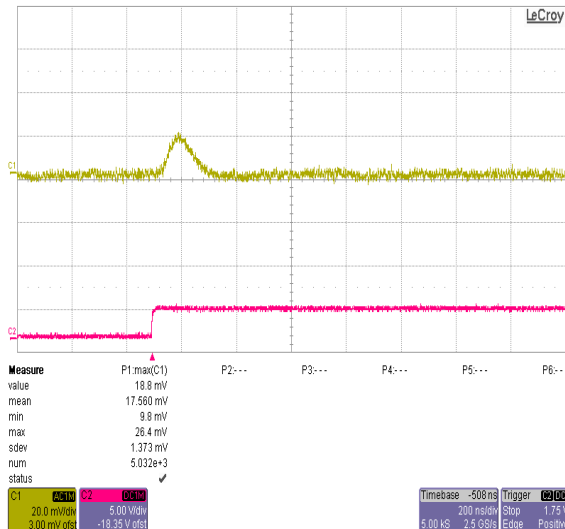
charge injection test @ 40 fC



- 3 sets of wfms, 25ns,50ns,100ns
- shaper gain : factor 2

- assume gain $2.5 \cdot 10^5$
- 1 pxl to 20 pxls

Signal to Noise Ratio - current scaling factor 1



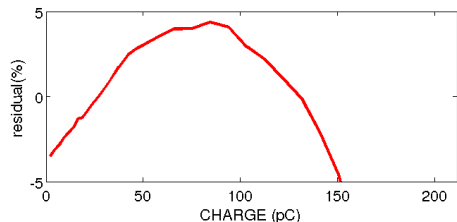
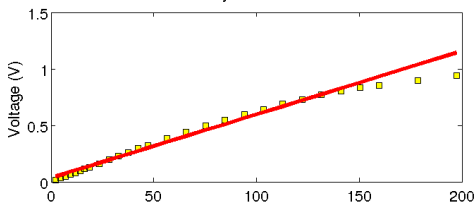
- charge injection
47pF
- input voltage
1mV, $Q = 47\text{pC}$
- peak = 17.6 mV
- RMS = 1.4 mV
- SNR for $2.5 \cdot 10^5$

$$\frac{17.6\text{mV} \cdot 40\text{pC}}{1.4\text{mV} \cdot 47\text{pC}} > 10$$

Dynamic range & linearity

current scaling factor 50

linearity scan of KLauS



- dynamic range is related to linearity
- charge injected via 470pF
- dynamic range up to 150pC ($\pm 5\%$ residual)
- total range is 12 ~ 13 bits

$5 \cdot 10^5$ gain
1600 pxls
charge 128 pC

Trigger quality & SiPM bias tune

first tests on trigger walk and jitter

- THRD @ 0.5 pixel (20 fC)
- time walk 4.5 ns from 1 pxl to 20 pxls (40 fC/pxl)
- time jitter ~ 700 ps

SiPM bias tune

- 0.8 V to 2.8 V range (3.3 V power supply)
- in the whole range, peak variation $< 1.5\%$

Summary and Outlook

Summary

- Charge Readout Scheme is implemented and first results are positive
- SNR > 10 for gain $2.5 \cdot 10^5$
- dynamic range goes up to 150 pC (linearity $\leq 5\%$)
- trigger walk $\sim 5ns$, jitter $< 1ns$, delay $< 5ns$
- SiPM bias tune range of 2V

Outlook

- more measurements in the near future
- SiPM will be connected to the chip