

Japan



- Our hearts go out to our Japanese colleagues who suffered three major disasters simultaneously
 - Earthquake
 - Tsunami
 - Nuclear Catastrophe



Thus in silence in dreams' projections, Returning, resuming, I thread my way through the hospitals; The hurt and wounded I pacify with soothing hand, I sit by the restless all dark night - some are so young; Some suffer so much - I recall the experience sad...

Walt Whitman, from Leaves of Grass, 1876

Outline



- The physics drivers
- Status of R&D
- Reflections



Physics Goals

- The LHC has brought us to the threshold of discovery for new physics, and we expect to cross it, momentarily ?
- If the new physics is within the ILC center of mass reach, it will let us unravel the structure of that physics
 - Electroweak Symmetry Breaking
 - Higgs sector(s)
 - Extra symmetries, dimensions, ...
- If no new physics is uncovered at the LHC, precision allows unprecedented probe of SM
 - Uncover cracks in SM
 - Channels missed at the LHC (trigger or signature)







Physics Environments





Design Challenges

Physics

 Unambiguous identification of multi-jet decays of Z's, W's, top, H's, χ's,

ZHH

• Higgs recoil mass and SUSY decay endpoint measurements

 $ZH \rightarrow \ell^+ \ell^- X$

• Full flavor identification and quark charge determination for heavy quarks

 $ZH, H \rightarrow c\bar{c}, b\bar{b}, \dots$

• Full hermiticity to identify and measure missing energy and eliminate SM backgrounds to SUSY

 $\widetilde{\mu}$ decay

• The unexpected



 $\tilde{\mu}$ decay

The unexpected

Demands unprecedented jet energy resolution

$$\sigma_{E_{jet}} / E_{jet} = 3\%$$

Pushes tracker momentum resolution

$$\sigma(1/p_T) = 5 \times 10^{-5} (GeV^{-1})$$

Detector

Demands superb impact parameter resolution

 $\sigma_{r\phi} \approx \sigma_{rz} \approx 5 \oplus 10/(p \sin^{3/2} \vartheta)$

Instrumented forward region

 $\Omega = 4\pi$

Smarts

Design Challenges

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Full flavor identification and guark charge determination for heavy quarks $ZH, H \rightarrow cc. bb, ...$

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Detector Concepts

<u>ilc</u>

• Two validated detector concepts for the ILC



ALCPG 2011, Eugene, March 19-23, 2011 -- M. Demarteau



Detector Concepts plus Siblings



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Detector R&D Organization



- The matrix of detector R&D is quite convoluted
 - R&D for ILD mainly carried out within horizontal R&D collaborations
 - R&D for SiD mainly carried out by the concept



• Control held by R&D collaborations, but even that is very limited

Detector R&D Organization

• R&D based in many regions, many funding sources, many oversight bodies





Detector R&D Organization



• R&D based in many regions, many funding sources, many oversight bodies It works !





Vertex Detectors

ALCPG 2011, Eugene, March 19-23, 2011 -- M. Demarteau

Research Thrusts



- Precision vertexing/tracking/imaging ideally requires detectors that have
 - zero mass: transparency of $\sim 0.1\% X_0$
 - zero power: allow for air cooling (< 50 W)
 - zero dead zones
 - zero dead time
 - zero effective occupancy: integration over few bunches
 - zero noise susceptibility: EMI immune
 - 1/zero precision: spacepoint < 5μm, impact parameter 5μm \oplus 10μm/(p sin^{3/2} θ))
 - 1/zero pattern recognition capability: many layers close to IP
 - Modest radiation hardness
- These aggressive set of goals and the physics need, has led to a wide range of R&D based on established and emerging technologies
- No technology has established itself yet. It is expected that the experiments will choose the best technology that will meet their needs at the time of the technical design

Detector Design Options

- Long Barrel Configuration (ILD)
 - Single geometry for all layers
 - Large charge sharing at small angles and larger occupancies
 - More mass on trajectories at small angle
 - Limited number of space points on particle trajectory at forward angles
- Barrel and Disk Configuration (SiD)
 - No precedent for disk geometry for pixel planes and associated services
 - Uniform angular coverage and response
- Ongoing studies on low-mass support
 - PLUME: Pixelated Ladder with Ultralow









CCD Technology



- R&D is focused on fine pixel CCD sensors (FPCCD) and readout ASICs
- Goal:
 - Pixel size : 5µm× 5µm
 - Total # modules: 6080
 - 20,000×128 pixels/module \rightarrow 10¹⁰ pixels
 - Full depleted, 15 µm thickness
 - Readout speed > 10Mpix/s
 - Readout noise < 50 e⁻, Power < 100 W
- Currently produced: FPCCD #3
 - Pixel size: 12 6 μm
 - Sensitive thickness: 15 μm
- Tests being carried out:
 - Pixel size: 12µm×12µm
 - 4 frames with 512×128 pix/frame
- Status









MAPS CMOS



- sensors Strategy for ILC (ILD)
 - Layer 1: spatial resolution
 - Pixel pitch 16x16 μm², binary output
 - $\sigma \leq 3 \,\mu\text{m}$, integration time $\leq 50 \,\mu\text{s}$

Layer 2: time resolution

- Pixel pitch 16x64-80 μm², binary output
- $\sigma \sim O(5) \mu m$, integration time $\leq 10 \mu s$

Outer Layers: low power

- Pixel pitch 35x35 μm², 4-bits ADC output
- 4 cm² of sensitive area
- $\sigma \sim 4 \,\mu\text{m}$, integration time $\leq 100 \,\mu\text{s}$
- **Proof of principle: Mimosa 26**
 - **Used in EUDET telescope**
 - Pixel array: 1152 x 576, 18.4 µm pitch
 - 10 k images/s _
 - Also used in STAR VXD upgrade and for CBM MVD





Chronopixel



- Chronopixel design provides for single bunch-crossing time stamping
 - When signal exceeds threshold, time stamp provided by 14 bit bus is recorded into pixel memory, and memory pointer is advanced
 - Comparator threshold adjusted for all pixels
- Current design
 - 50x50 μm² pixels
 - Two pixel architectures
 - Regular p/n-well design (A)
 - Deep n-well design (B)
- Tests show that general concept works
 - Good sensitivity (µV/e⁻) as designed
 - Sensors timestamp max. recording speed (7.27 MHz) is adequate
 - Noise figure meets specifications





Vertical Integrated Circuits – 3D



- Vertical integration of thinned and bonded silicon tiers with vertical interconnects between the IC layers
- Technology driven by industry; offers potential for transformational new detectors



VIP Chip

- Fermilab designed Vertical Integrated Pixel (VIP) chip for ILC pixel detector, through MIT-LL process
- First chip was functional and a redesign was submitted VIP-2A, MIT-LL
 - Pixel array 48x48, 28x28 μ m² pixels; design for 1000 x 1000 array
 - Provides analog and binary readout information
 - 7-bit Time stamping of pixel hit
 - Token passing readout scheme
 - Sparse readout
- Chip divided into 3 tiers
 - $\sim 7 \ \mu m$ / tier









Fermilab 3D Multi-Project Run





- Fermilab formed a 3D consortium and hosted a 3D multi project run with Tezzaron
 - Two layers of electronics fabricated in the Chartered 130 nm process, useful reticule size is 16x24 mm
 - Wafers will be bonded face to face
 - Submission closed September 2009
- Frame divided into 12 sub-reticules for consortium members
- More than 25 two-tier designs (circuits and test devices)
- Unfortunately there have been a lot of growing pains with this process
- But, 2D wafers have been obtained and test well
- Full expectation that 3D bonded wafers will be available this year and testing can begin with sensor integration with 3D ICs.

MAPS in 3D



• INFN has pilot project with Fermilab 3D Tezzaron project for 3D MAPS



- Tier 1: sensor + analog FE + part of the discriminator
- Tier 2: part of the discriminator, digital front-end and peripheral readout electronics
- Extend to CMOS FE integrated with high resistivity sensor







Tracking

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Research Thrusts

- Precision tracking to enable high resolution calorimetric measurements
 - Low mass
 - Unprecedented momentum resolution: $\sigma(1/p_T) = 5 \times 10^{-5} (GeV^{-1})$
 - Good double track separation: \sim 150 μ m
 - Hermetic, uniform coverage
 - Excellent pattern recognition capability



TPC R&D





TPC R&D

•

TPC R&D

MicroMegas

• GEM

B=1 T $\sigma_0 = 61.3 \pm 1.9 \,\mu m$

Resolution of 80 µm at 2m drift in B=3.5 T obtained!

- Read out based on T2K AFTER electronics (Saclay)
 - April/May: new AFTER electronics
 - Late 2011 (B=0): 7 Micromegas modules with new AFTER electronics
- Read out based on ALTRO electronics (EUDET, Lund, CERN)
 - New ALTRO electronics developed

TPC Readout

- S-Altro 16 chip: a 16 channel front-end chip; each channel comprises :
 - Low-noise progrmble pre-amp, shaper, ADC,
 - Digital Signal Processor
 - Max sampling frequency: 40MHz
 - Max readout frequency: 80MHz
 - IBM 130nm CMOS
- ASIC currently being tested
- TimePix2 for pixelized TPC readout; matrix layout: 256x256 pixels (Pixel size 55x55 µm)
 - Low minimum detectable charge:
 - < 500 e- minimum threshold
 - Time stamp and TOT simultaneously
 - Fast time-stamp ~1.5ns
 - Slow time-stamp ~ 25ns
 - TOT 8-10 bit
 - Sparse Readout

GridPix

- Octopuce : 8 InGrids (integrated MicroMegas grids on TimePix chips) bonded on a LP panel
 - 65 000 digital pixels (55 μm x 55 μm)
 - Time and Time over Threshold (TOT) measurement
 - Tests started inside 1T magnet
- Activities:
 - Octopuce, maybe second Octopuce plane
 - DESY 3-GEM module beam test on LP
 - Asian 2-GEM module beam test
 - S-Altro16, new AFTER, TimePix2 chips
 - Continued engineering studies for new endplate (Cornell)
 - Preparation cooling and power pulsing tests
 - PCMAG upgrade in Aug'11-Jan'12
- Vibrant R&D program

Silicon Tracking

- Silicon Strip modules with hybrid-less design
 - Two ASICs directly mounted on a sensor with 2k strips
 - Double-metal trace routing
 - Power and clock routed over sensor
- Component test of:
 - kPix: 1k-channel ASIC
 - Low-mass cable
 - Low-mass ASIC bonding
 - Gold stud attachment using thermo-compression 300-350 C
 - 160 g/bump ok
 - Low-mass module design
 - Induced readout noise
 - Power pulsing and induced Lorentz force in B-field

Silicon Tracking

- A very broad R&D program carried out within the SILC collaboration
 - Investigating double-sided silicon detectors for the forward regions
 - Development of a 128-channel silicon tracker readout chip: SiTRK
 - Silicon strip sensors with integrated pitch adapters
 - Edgeless sensors

. . .

Trapezoidal sensor with test structures

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Calorimetry

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Research Thrust

- Calorimetry based on Particle Flow
 - Reduce the function of the calorimeter to measuring the energy of neutrals only
 - Key word is granularity !

Silicon-W ECAL

- Studies with the Si-W physics prototype nearly completed
- Development of Technological Prototype started:
 - Final detector-like mechanical structure
 - ~2/3 scale
 - Final detector-like powering and services
- Assembly:
 - Final mechanical assembly underway
 - ~40 silicon sensors purchased, ~10 ordered
 - Readout with SKIROC-2 ASIC; critical step to move forward
 - PCB interconnections possibly with anisotropic conductive film (3M)
- Schedule
 - Tests of first layer this year at DESY
 - Test with SKIROC2 chip, 2012
 - Multi-layer tests end 2012, 2013

Scintillator ECAL

- Design uses 5mm scintillator strips (x,y), 5mm wide with MPPC readout
- Current focus is on Layer Integration Wonderful demonstration of CALICE leverage
 - Uses EUDET absorber structure (French)
 - Uses AHCAL readout electronics (DESY)

- New Hamamatsu MPPC employed
 - 1600 pixels/1x1 mm² →
 2500 pixels/1x1mm²
 - Improve dynamic range and linearity
- Schedule:
 - Complete construction in 2011
 - Test beam in 2012

Analogue HCAL Analysis

- both CERN and Fermilab
 - **Publications coming up**
 - New results appearing
- **Electromagnetic response** measured; established detector modeling for hadronic analyses
 - **Detailed test of Geant 4 hadron** shower models, exploit fine granularity, capability to tag shower start point
- Scintillator planes now serving in W stack in CERN testbeam

Analogue HCAL: Next Prototype

- 2nd generation prototype has integrated readout ASICs and LED system and time measurement
- **Prototype roadmap:**
 - 2010: 1st HBU
 - 2011: full layer (2000 ch)
 - **2012: several options**
 - instrument part of ILD wedge
 - tungsten HCAL

10 cm

New full readout board

Digital HCAL: RPC

- Digital hadron calorimetry based on glass RPCs with 1x1 cm² readout pads
- Large scale prototype built
 - 350,000 channels DHCAL +
 120,000 channels for Tail Catcher
 - 10,000 DCAL III ASICs
 - 205 RPCs, 337 Readout boards
 - Low Voltage (384 channels)
 - High Voltage (64 channels)

- Currently still taking data at Fermilab
- Schedule
 - April 2011: Combined with the CALICE Silicon-W ECAL
 - Fall: DHCAL with W plates (?)

Digital HCAL: RPC

Semi-Digital HCAL: RPC

- A technological prototype is being built for the SDHCAL
 - 48 layers, 2 cm absorber and 0.6 cm thick glass RPC
 - Depth 6λ
 - 1x1 cm² pads, 442,368 channels
- Two cassettes tested in CERN testbeam with and without power pulsing

Digital HCAL

MicroMegas

- Design of 48x32cm² PCB equipped with ASIC, pads and mesh
- 1 m² chamber with dead zone < 2%
- Deploy new ASIC: MICROROC

GEM

Hits

200

100

0

0

- Design of 1m² GEM foils
- Readout with kPiX and DCAL ASIC

R~17%

Ar-escape(3 keV)

200

100

400

500

600

300

700

Forward Calorimetry

Forward Instrumentation

z ľx

Beamcal + pair monitor

B

Luminosity monitor

Beam test with 4 GeV electrons at DESY

FCAL Prototype

- Collaboration preparing for a prototype calorimeter, supported by EU through AIDA program
 - Flexible, high precision tungsten structure
 - Fast FE Readout ____
 - Innovative connectivity scheme
 - **Position control devices**
- **Read out employs kPix ASIC**
 - Adapted to FCAL with fast feedback system
 - 72 channels
- **Exploits common European infrastructure**
 - **Power pulsing**
 - **Data acquisition** ____
 - Tracking in front of the calorimeter

Muons

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Muon Detectors

• Double scintillator strip, read out with SiPM with integrated wave form digitizer (212 MHz) studied as muon detector in Fermilab test beam

Next steps: 16, 32, then 64 strips in four stations to test:

Show me !

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Benefits of ILC Detector Program The development of new technologies and the implementation in prototype

- detectors has been very beneficial to the community at large
 - 3D Silicon

INGRID technology

Benefits of ILC Detector Program

- Readout Chip for SiPM Analog Hadron Calorimeter: SPIROC

3000 chips deployed in PEBS balloon experiment

WVD, CBM

... and EUDET beam telescope and vertex detector for STAR

Mimosa Pixel Array

Pixel matrix: 1152 x 576 18.4 µm pitch, 10 k images/s

Benefits of ILC Detector Program

• Development of the DEPFET technology brought to full detector level stage within the ILC framework

- ILC material budget goal achieved by DEPFET
- If it had not been for the ILC detector R&D program, BELLE-II would not have had a viable vertex detector technology

Benefits of ILC Detector Program

Т2К ТРС

• Quote: "I can confirm that the ILC TPC R&D was essential for T2K near detector TPCs. In fact, without the ILC TPC R&D program, there would have been no T2K TPCs"

Dean Karlen, February 2011

Support

• Even though the fruits of the ILC detector development are clearly visible inside and outside of HEP, support is still diminishing

- US ILC support

- Universities (LCRD)
- Terminates in FY12
- EU support
 - EUDET, 2006-09 €21.5 M
 - AIDA, 2011-15 €27 M,
 - Funding geared towards infra-structure

- Some other observations:
 - US initiated new detector R&D program for collider detectors with overall funding of \$3M (shared with LHC)
 - Japanese funding as it exists will terminate this year
 - Individual country contributions to R&D collaborations can widely fluctuate from year to year (+/- 30%)
 - UK funding has been eliminated

Own Advocates

 We have to be our own advocates: to garner support, the burden is on us to inform and educate the agencies and community about the excellent work being carried out and its benefits!

- We hope to see many in June in Chicago !
 - http://conferences.fnal.gov/tipp11/
- Also workshop on power delivery and power pulsing, May 9-10, Orsay
 - http://ilcagenda.linearcollider.org/conferenceDisplay.py?confId=5010

In Search of the Radical Solution

• In the January 2011 issue of the magazine Scientific American there is an interview with a famous Indian scientist :

"In Search of the Radical Solution"

• The sentiment in that interview applies, I believe, equally well to detector development in our field

In Search of the Radical Solution

• In the January 2011 issue of the magazine Scientific American there is an interview with a famous Indian scientist :

"In Search of the Radical Solution"

- The sentiment in that interview applies, I believe, equally well to detector development in our field
- Reinvestment in other than incremental, non-scalable innovations technologies is needed
- "The greatest payoffs will come from fundamentally reinventing mainstream technologies"

-- Vinod Khosla co-founder SUN microsystems venture capitalist

http://www.scientificamerican.com/article.cfm?id=in-search-of-the-radical-solution http://ScientificAmerican.com/jan2011/khosla

Summary

- Excellent R&D being carried out in the framework of the ILC all over the world; apologies to all excellent efforts not mentioned !
- AIDA program in Europe provides badly needed continuity
- The spin-off of ILC originated detector development is significant
- The community, however, seems unable to leverage that significant accomplishment
- Open-ended R&D is, in the long-term, not sustainable. The biggest disadvantage for a continued viable detector R&D program is the fact that there is no construction timeline for the ILC