UC SANTA CRUZ

CERN

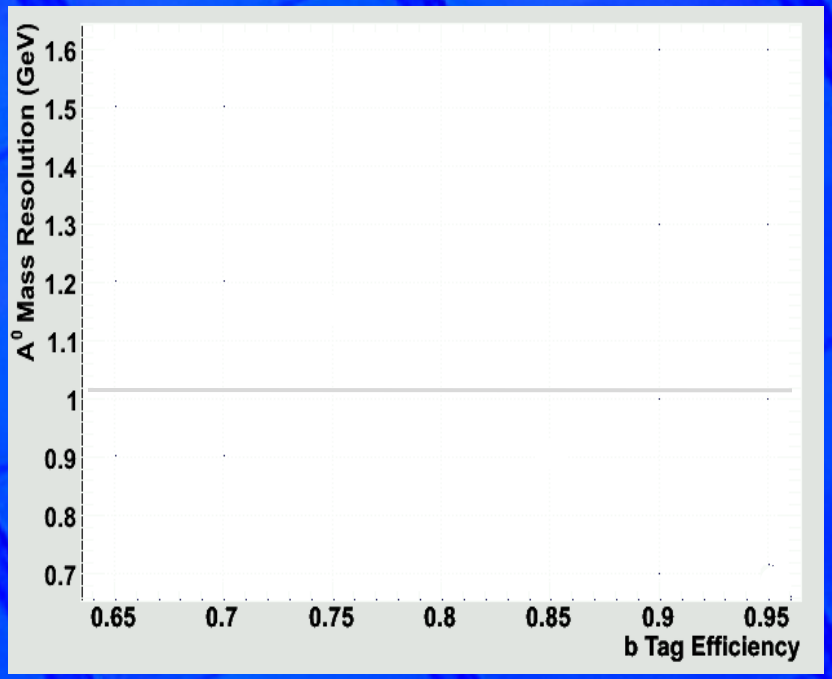
Vertex Detectors for Future Linear Colliders

Marco Battaglia
UCSC, LBNL and CERN

with contributions from L Andricek, Y Arai, R Lipton, N Sinev, W Snoeys, G Varner, S Zalusky

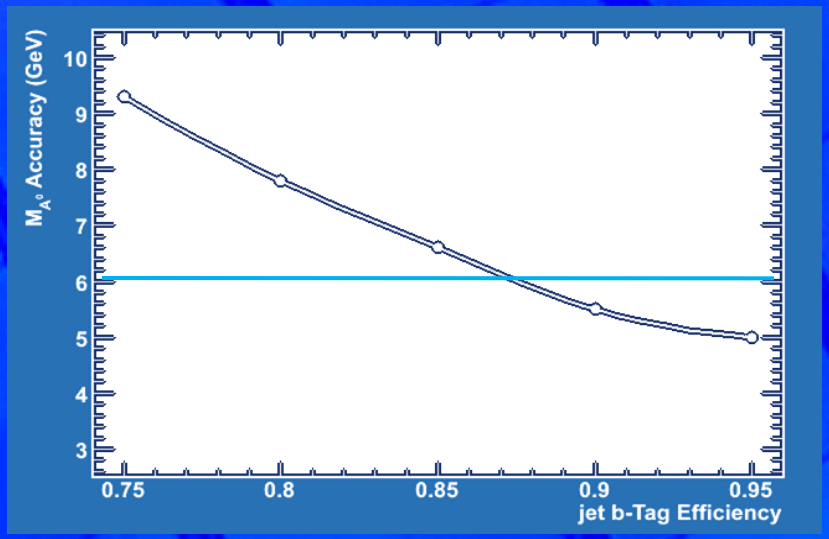
ALCPG2011
March 23, 2011 Oregon University, Eugene OR

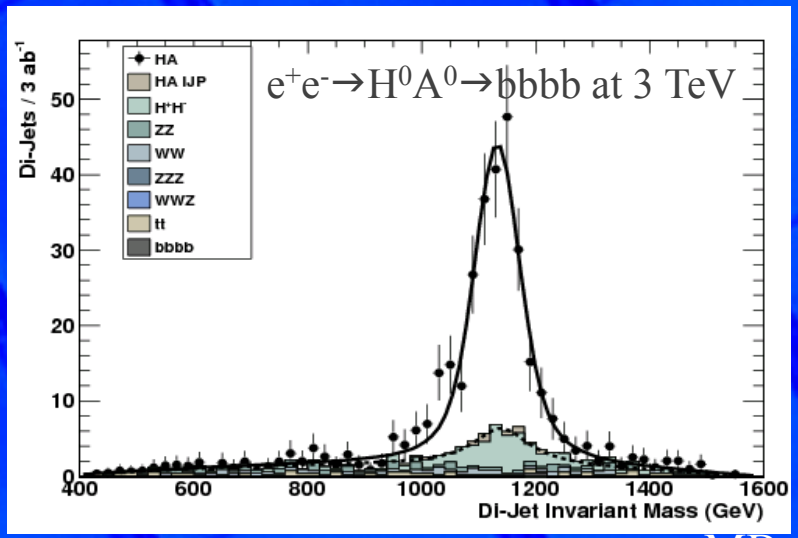
Multi-b Final States and Jet flavour tagging



MB et al. PRD78 (2008)

σ_{IP} (μm)	b Purity	ε_b
$5 \oplus 10 / p_t$	0.9	0.75
$12 \oplus 70 / p_t$	0.9	0.25

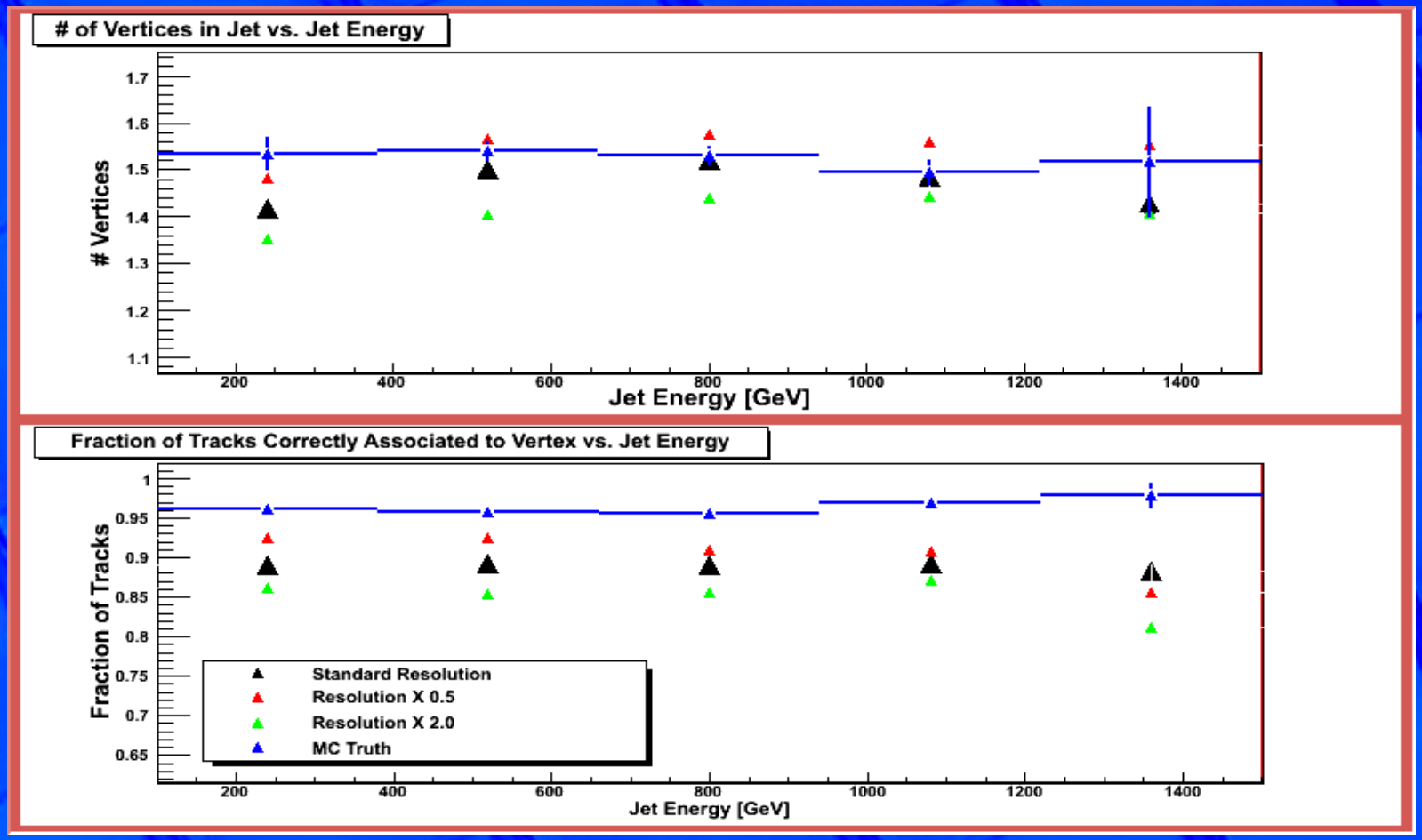




MB et al.
arXiV:1006.5659

Jet flavour tagging and Track Extrapolation Resolution

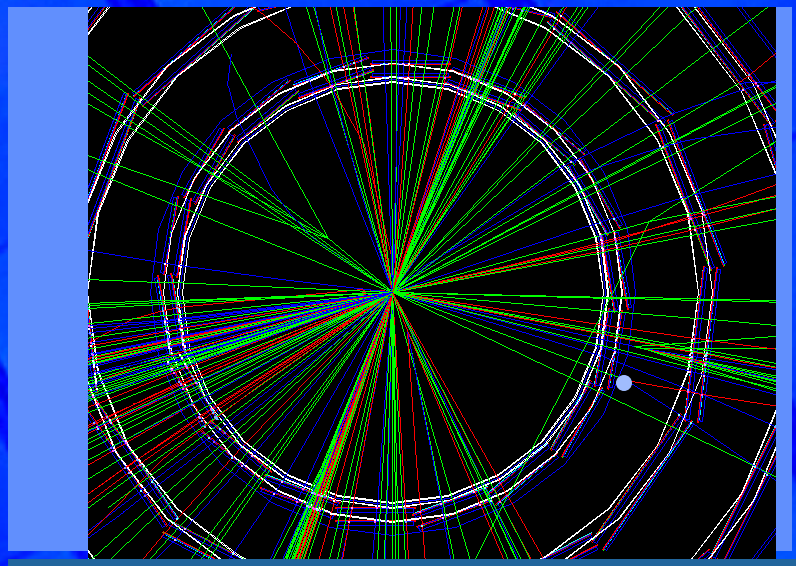
Performance of Jet Flavour Tagging at 3 TeV for std resolution $\sigma_{ip} = 3 \oplus 18 / p_t$ $\sigma_{ip}/2$, σ_{ip} x 2 and unsmeared track parameters vs. E_{jet}

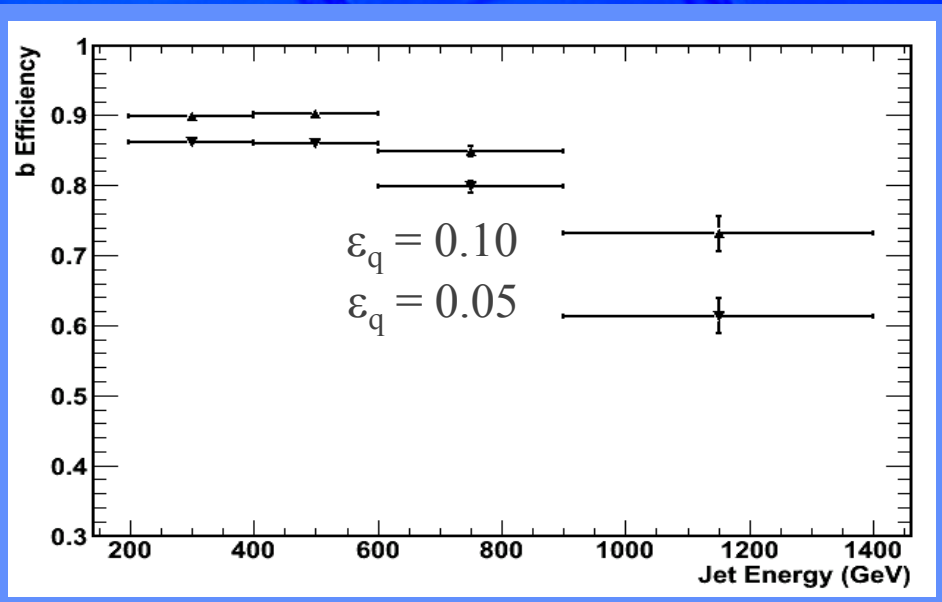


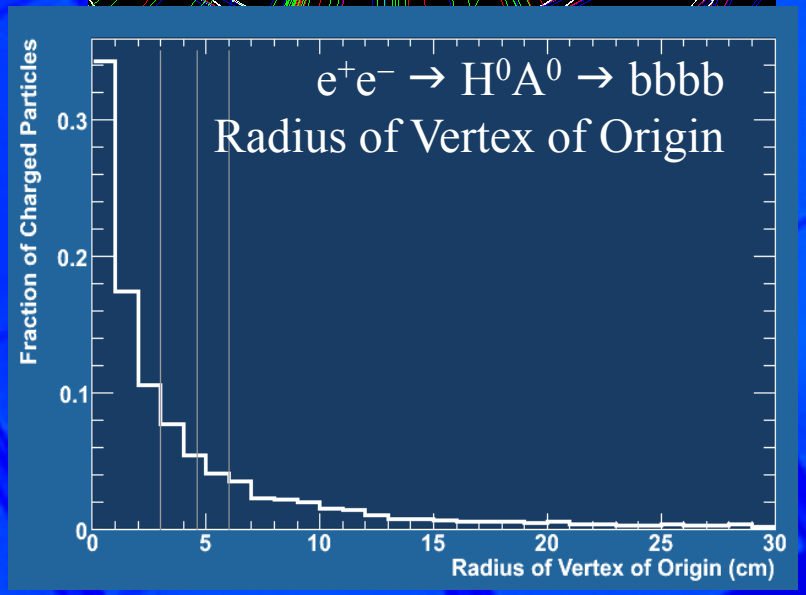
Jet flavour tagging and Track Extrapolation Resolution

Issues at large jet energies

Long B hadron decay distance past detector innermost layer(s) and reduced fraction of secondary particles in jet, limit performance of topological vertex search at TeV energies:



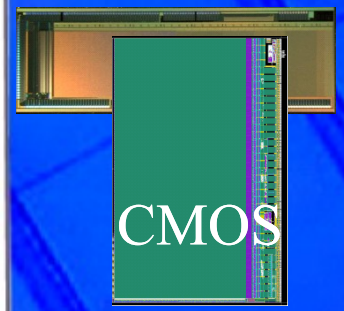


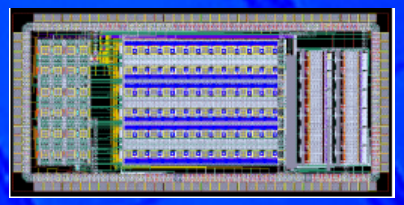


Linear Collider Pixel Sensor R&D

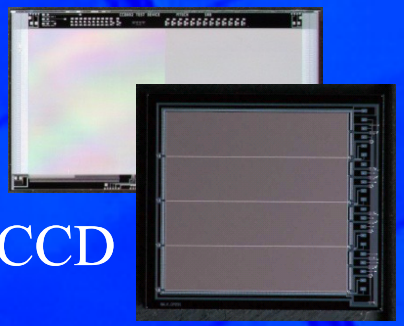
Requirements for the LC Vertex Tracker (~3 μm single point resolution, ~0.1%X_0 per active layer, power dissipation < 100 mW cm^{-2}, readout ~ 50 MHz [+ ~O(10ns) time stamping at CLIC], ~10-20 μm pixel pitch) require new generation of Si pixels:

Monolithic Si Pixel Technologies

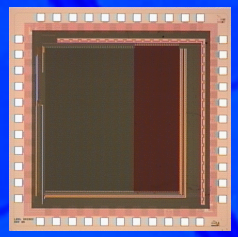




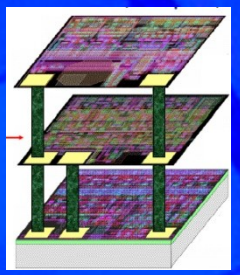
DEPFET



CCD



SOI

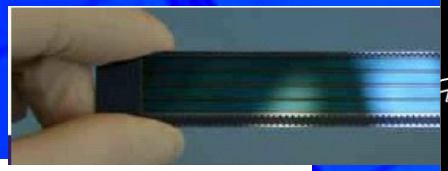


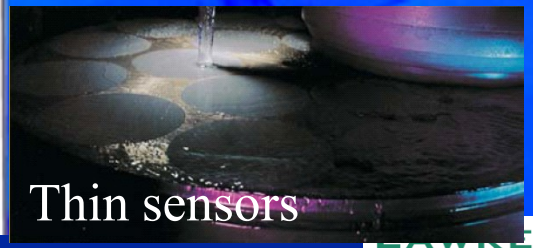
3D

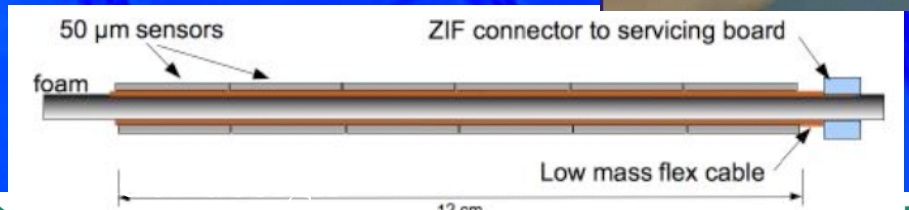
Vertical Integration

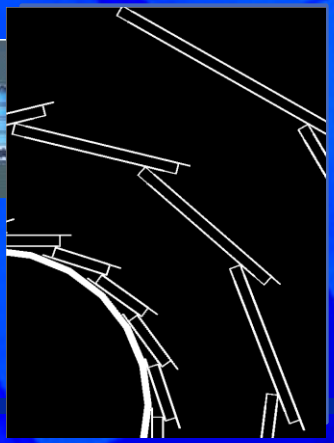
Architectures with advanced in-pixel and on-chip data processing

Innovative light-weight Ladders and Cooling



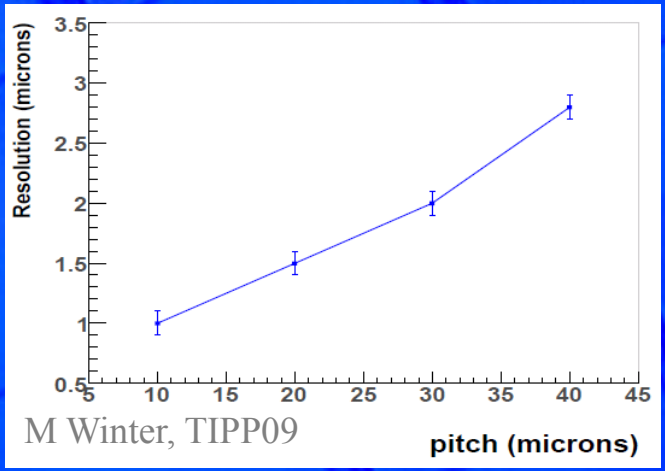






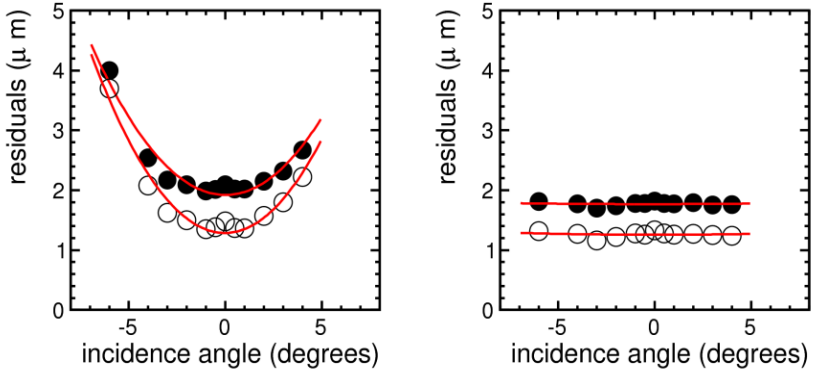
Single Point Resolution

σ_{point} vs pitch

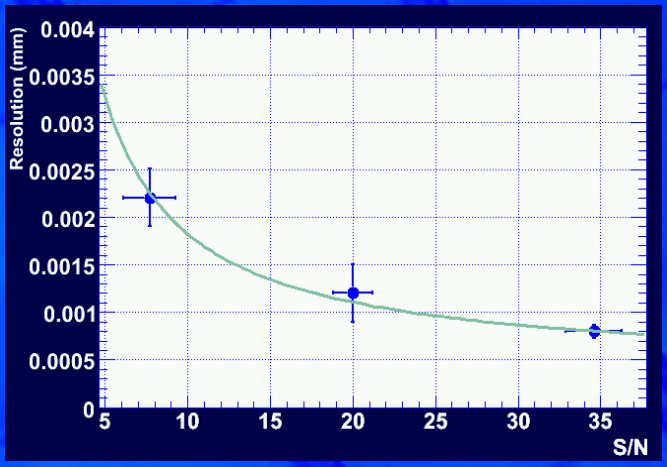


σ_{point} vs incidence angle

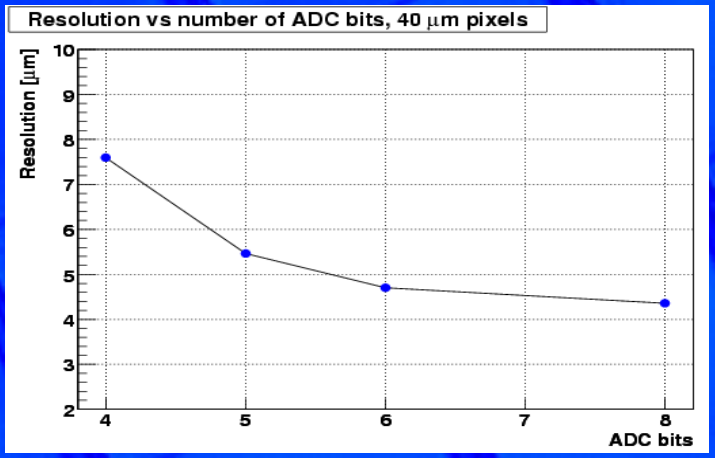
DEPFET TB2008, 120 GeV pions, 90°±5° , 24 x 24 μm^2 pixel



σ_{point} vs S/N

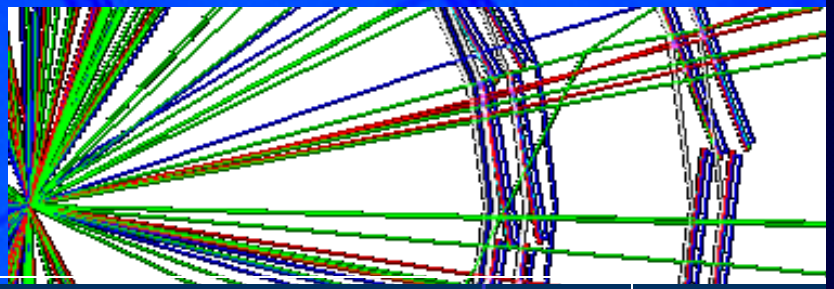


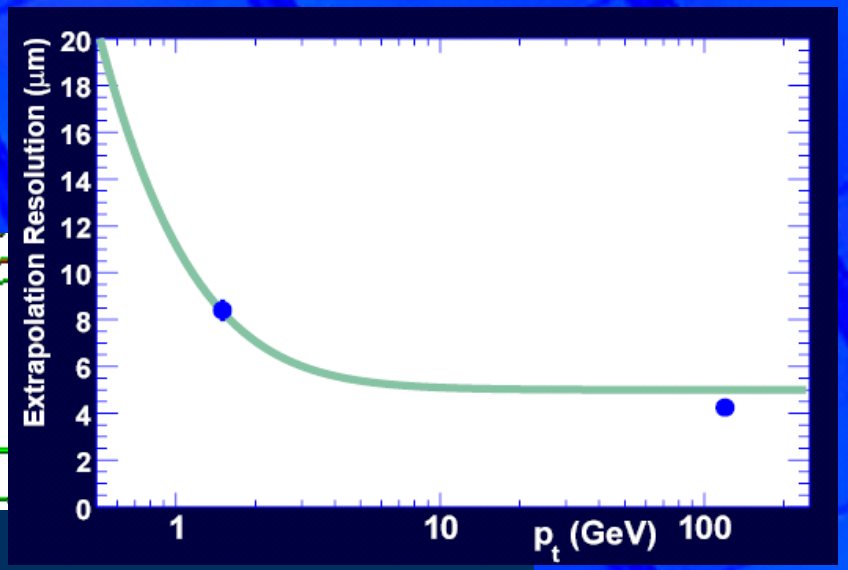
σ_{point} vs ADC accuracy



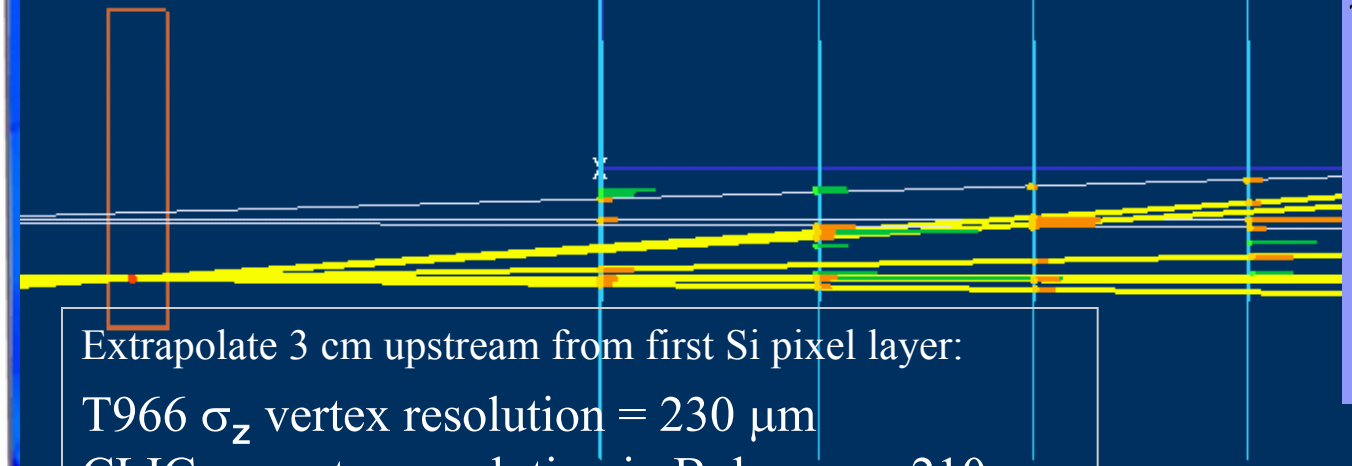
Track Extrapolation and Vertexing resolution

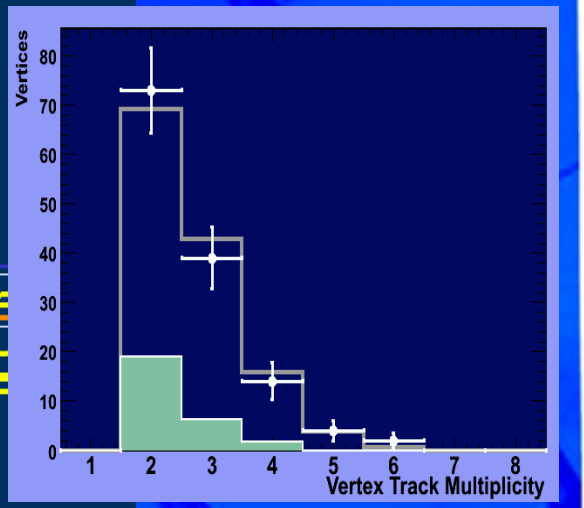
ILC/CLIC target track extrapolation accuracy demonstrate with small beam telescopes based on thin pixels:





FNAL MBTF T966 Data
120 GeV p on Cu target
LBNL Thin CMOS Pixel Telescope





Extrapolate 3 cm upstream from first Si pixel layer:

T966 σ_z vertex resolution = 230 μm

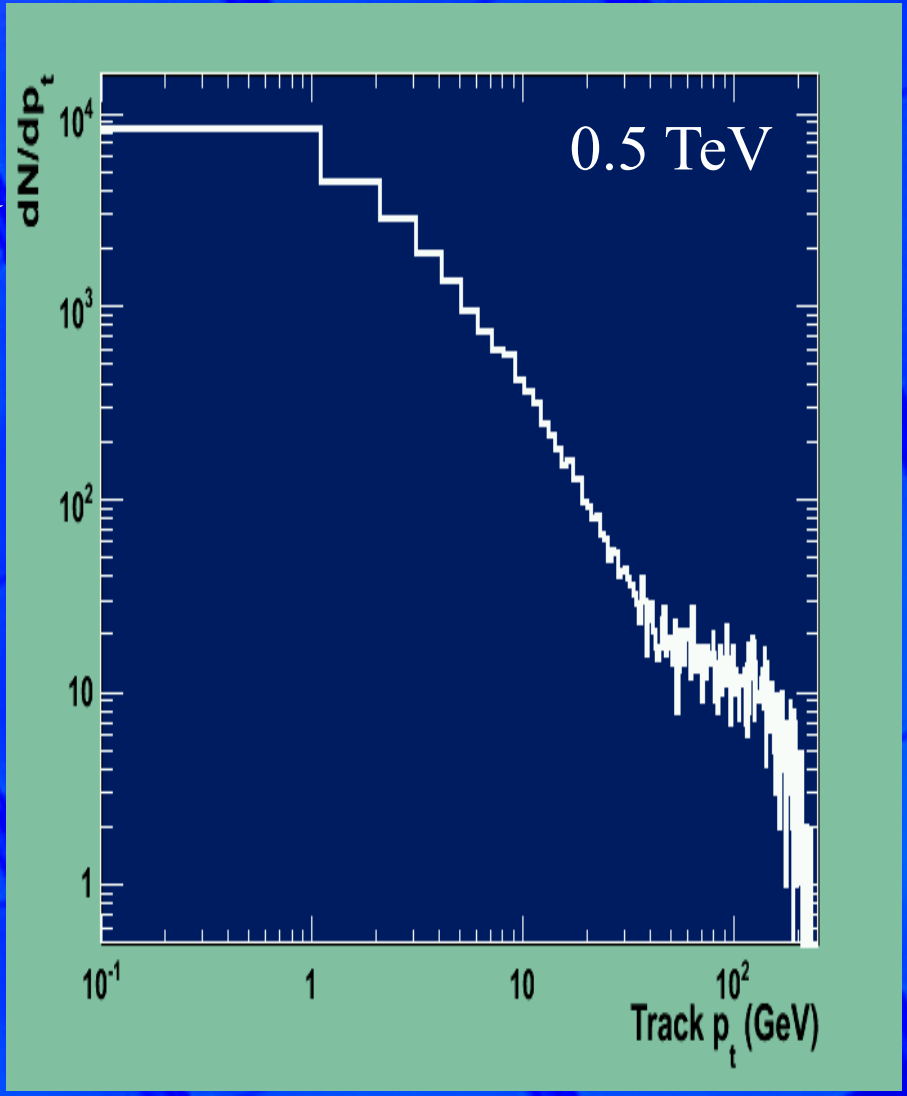
CLIC σ_z vertex resolution in B decays = 210 μm

MB et al., NIM A593 (2008)

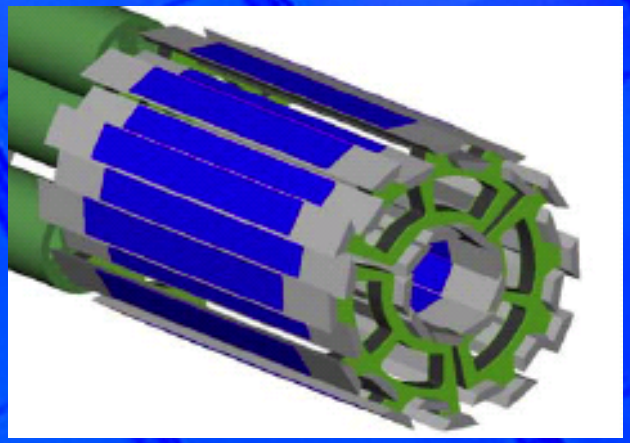
Despite large centre-of-mass energies, charged particles produced with moderate energies: interesting processes have large jet multiplicity (4 and 6 parton processes + hard gluon radiation) or large missing energies; Excellent track extrapolation at low momenta essential.

Impact Parameter resolution $a+b/p_t$ for ILC-like VTX with Si on 100 μm CFC

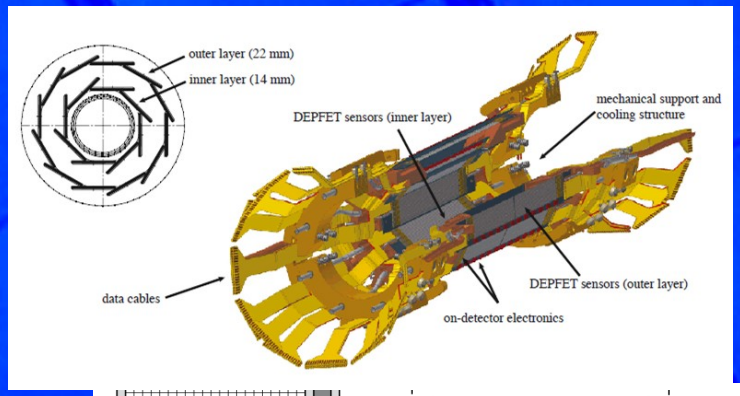
Si Thickness (μm)	a (μm)	b (μm)
25	3.5	8.9
50	3.7	9.6
125	3.8	11.7
300	4.0	17.5

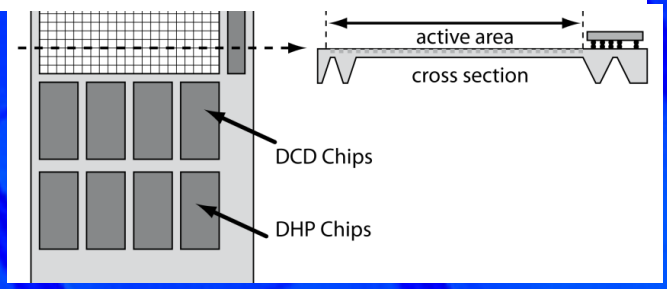


Ladder Thickness: Pioneer Experiments

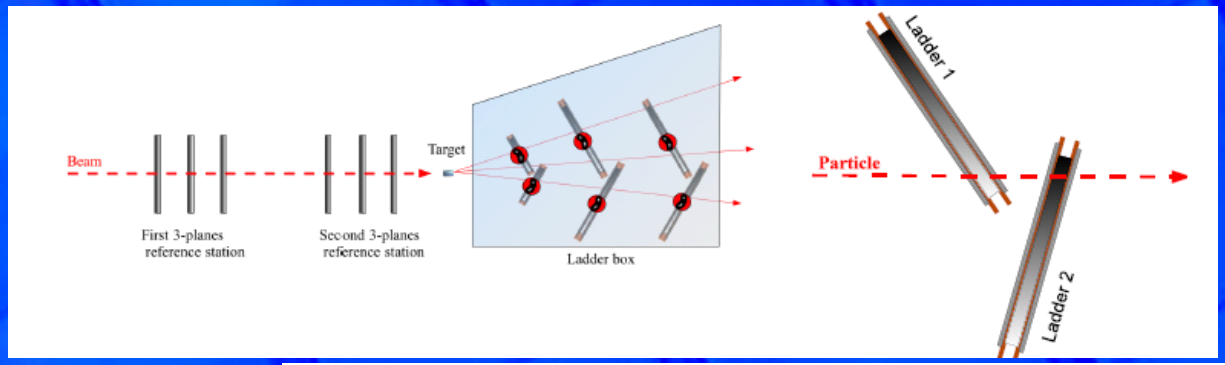


STAR 0.37% X_0



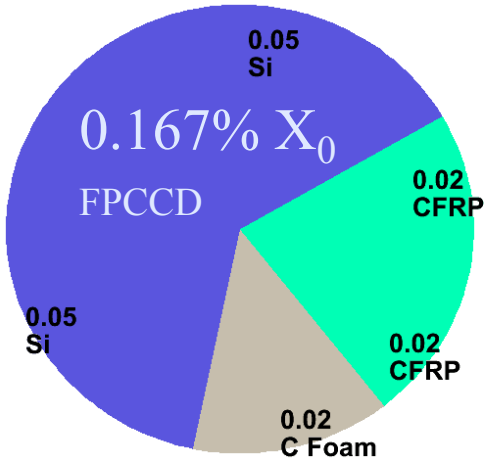


Belle-II 0.19% X_0

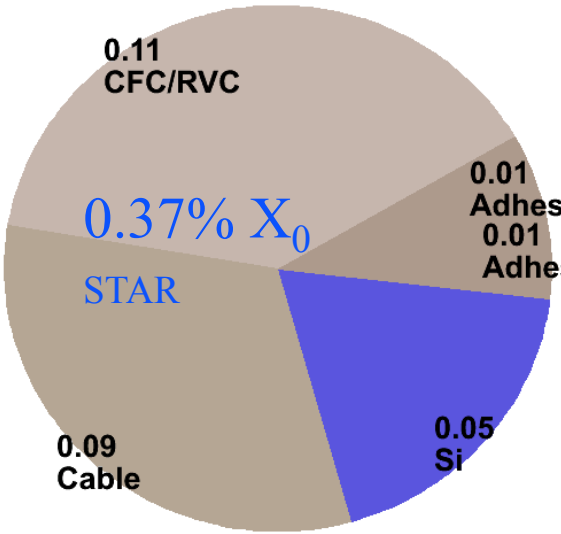


Monolithic Pixel-based Ladder Thickness

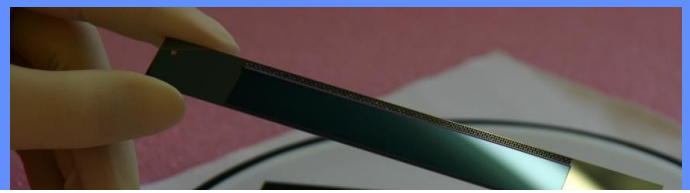
CCD

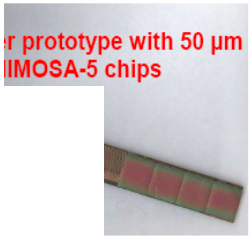


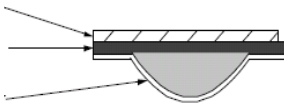
STAR HFT

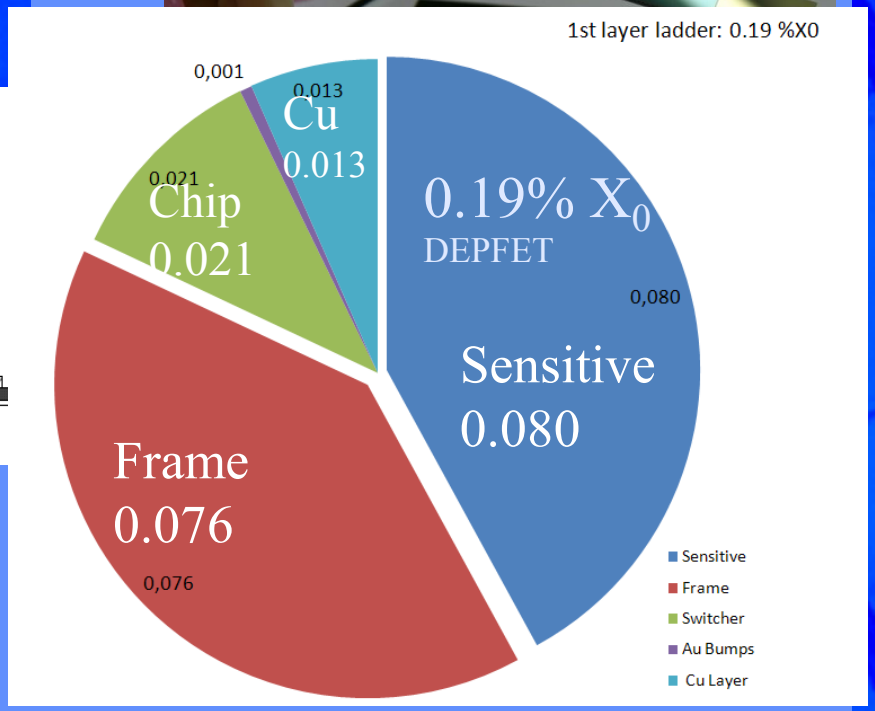


Material budget generally not dominated by sensor, all designs assume airflow cooling.







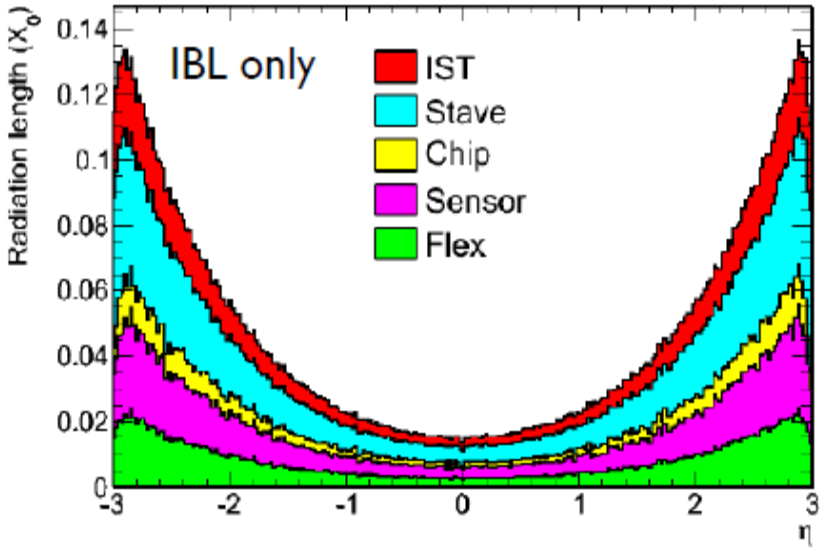


Ladder Material Budget: Experience from LHC and RHIC upgrades

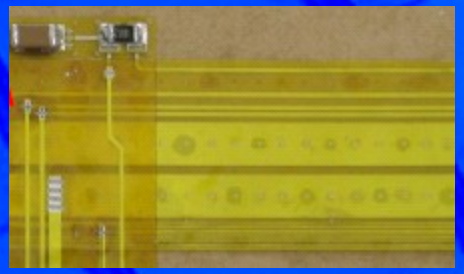
ATLAS current pixels 3.5% X0 / layer (1.47% stave, 0.92% services)

IBL 1.5% X0 (0.40% services)

SLHC upgrade target value <2% X0 / layer

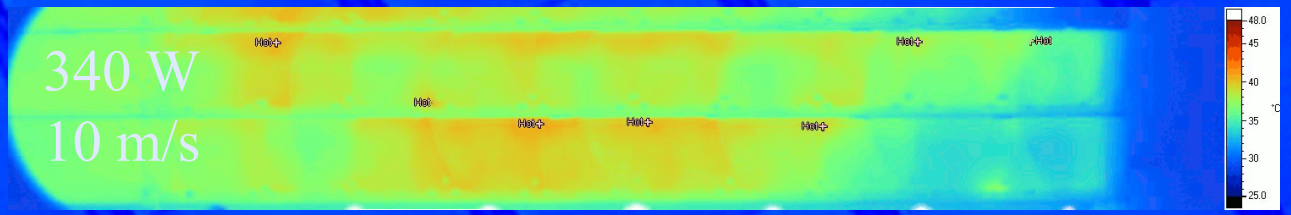


Flex cable material comparable (larger) than (thinned) sensor
STAR HFT and ATLAS IBL have flex with Al traces in active area + wire-bonds connections (STAR flex = 0.075% X_0 in active area).



Ladder Material Budget: Experience from LHC and RHIC upgrades

Tests at LBNL with STAR HFT mock-up show that airflow-based cooling can remove 170 mW/cm^2 with $\Delta T \sim 10^o$ above ambient with < 10m/s and ladder vibrations within 10 μm r.m.s.



L. Greiner

Power distribution: in-chip DC-DC converter or serial power ;

SP takes less material than DC-DC converter (ATLAS estimate SP/DC-DC ~ 0.25), ATLAS demonstrated its feasibility on half stave, integration into FE chip design.

Mechanics for the Vertex Tracker : Stability requirements

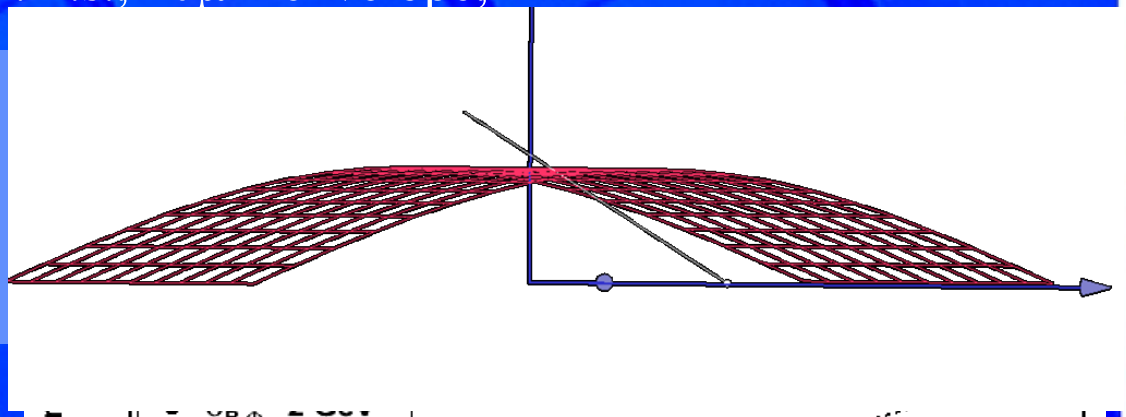
STAR stability requirement: 6μm r.m.s., 20μm envelope;

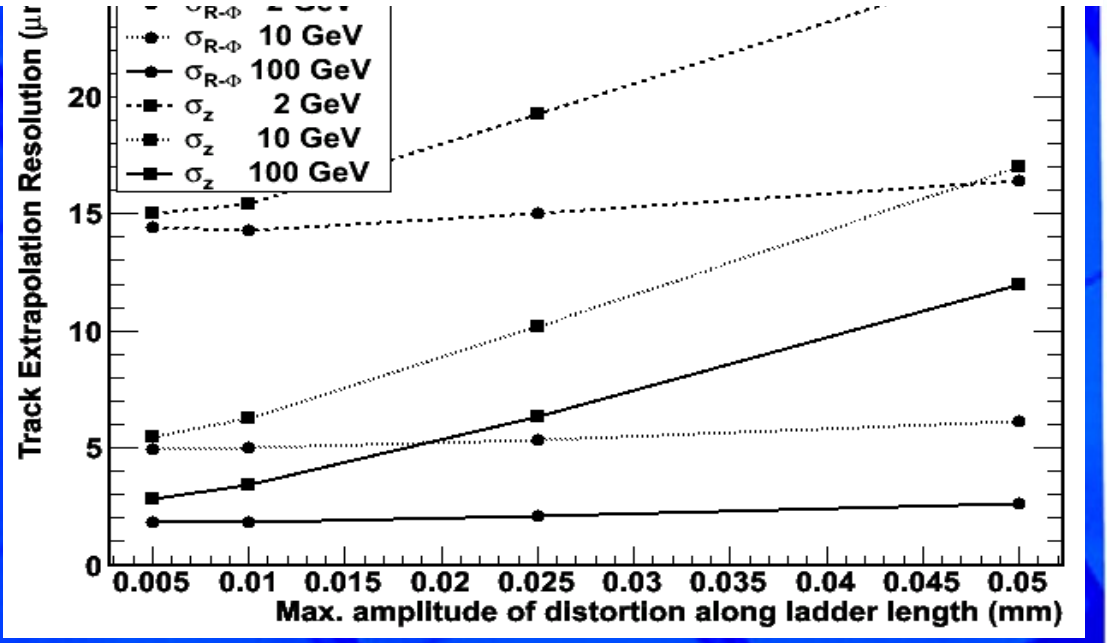
LC Vertex Tracker:

Study track extrapolation resolution in R-ϕ and z with amplitude of longitudinal and transverse ladder distortion;

Use new Marlin VTX digitiser under development for studies with the CLIC-ILD geometry;

Still need to propagate effect through ZVTOP b-tagging but appear that <10-15μm envelope will be required.

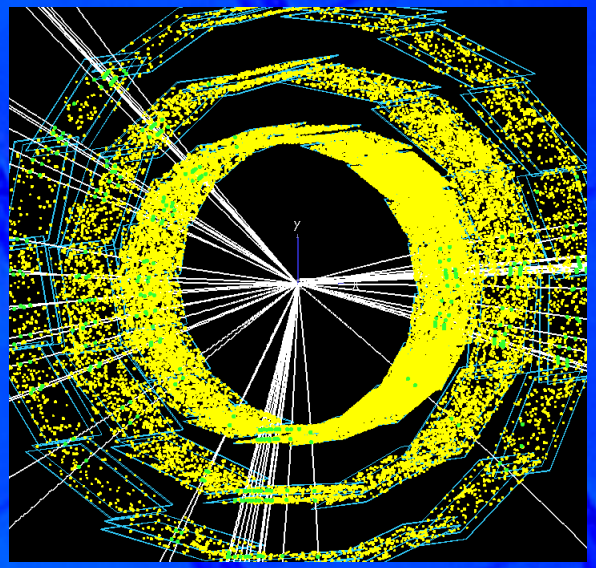


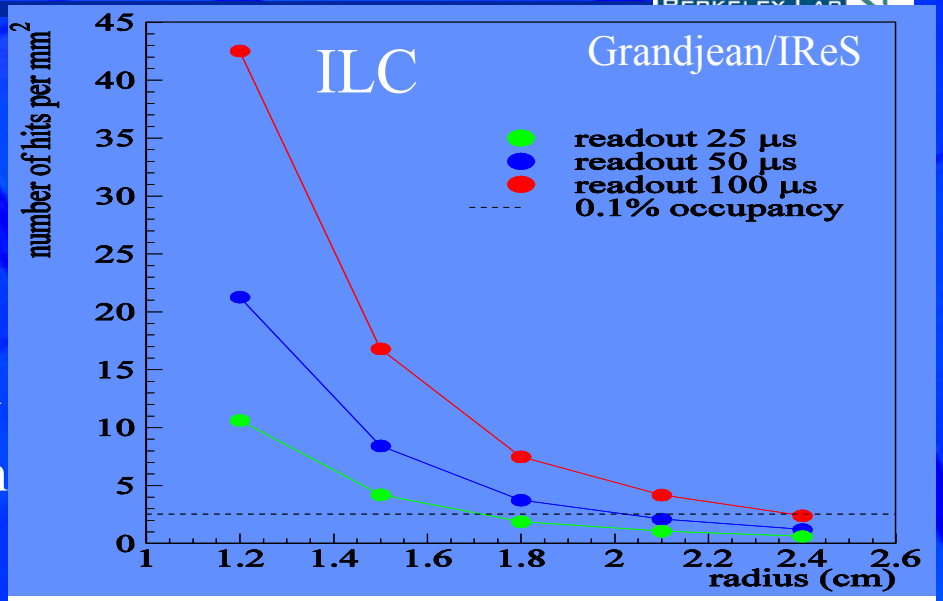


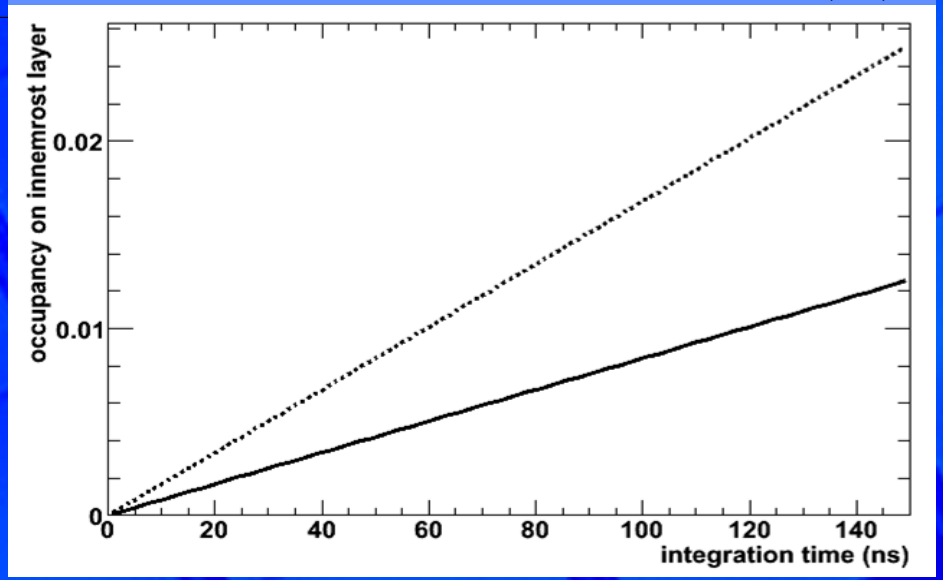
Space-Time Granularity and Occupancy

Simulation of pair backgrounds in VTX defines space-time granularity to keep local occupancy compatible with precision vertex tracking;

Requirements in terms of space granularity from occupancy and single point resolution appear to be comparable







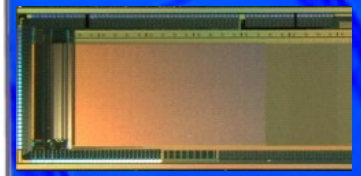
Read-out Speed and Occupancy

Most demanding requirement is mitigating occupancy:

ILC (2820 bunches w/ Δt_{bx}=337ns) r/o of first layers in 25-50 μs, time-stamping or 5μm pixels, at CLIC (312 bunches) Δt_{bx} = 0.5ns possibly 15-30 ns time-stamping

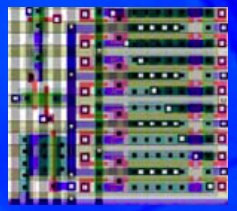
- Fast continuous readout architectures

CMOS APS



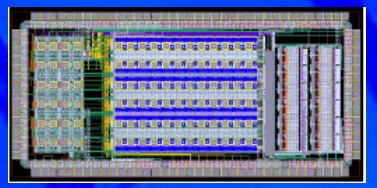
Double-sided col // binary r/o + 0 suppress, with 15 μm pixels

CMOS CAP Pixels



r/o 20 times during train data store on periphery

DEPFET Pixels

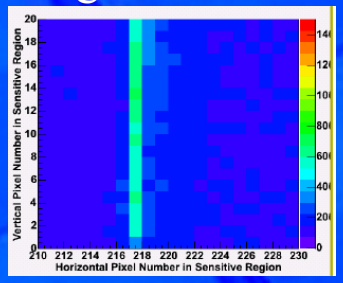


- In situ storage with high space-time granularity and r/o at end of train

Fine Pixel CCD

5μm pixels

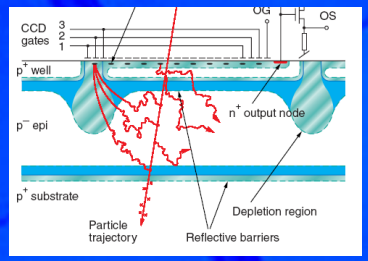
Reject bkg with cluster shape



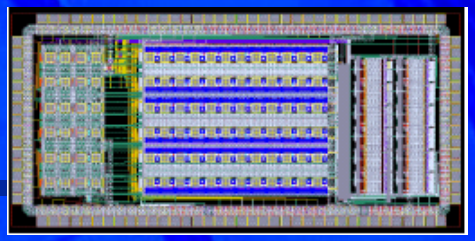
ChronoPixel

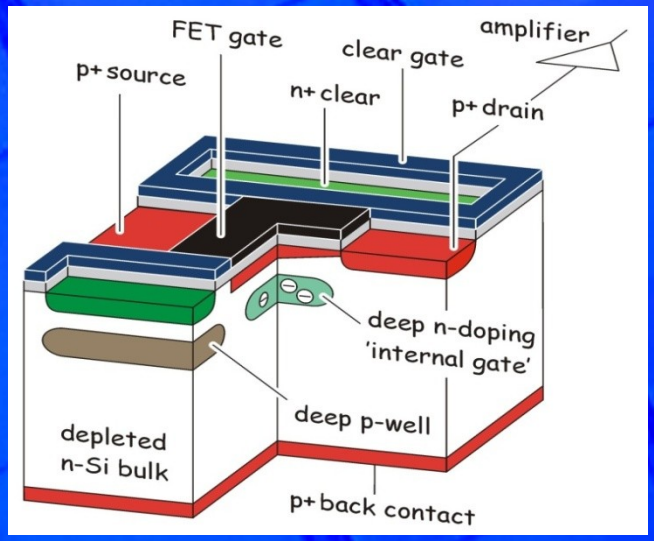
ISIS

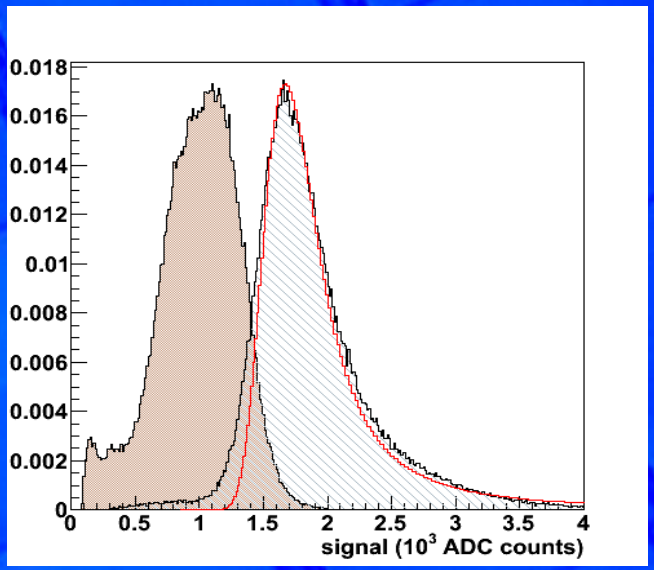
In-situ 20-cell charge storage



Technologies for the Vertex Tracker : DEPFET







Important experience with application at KEKB Belle-II upgrade.

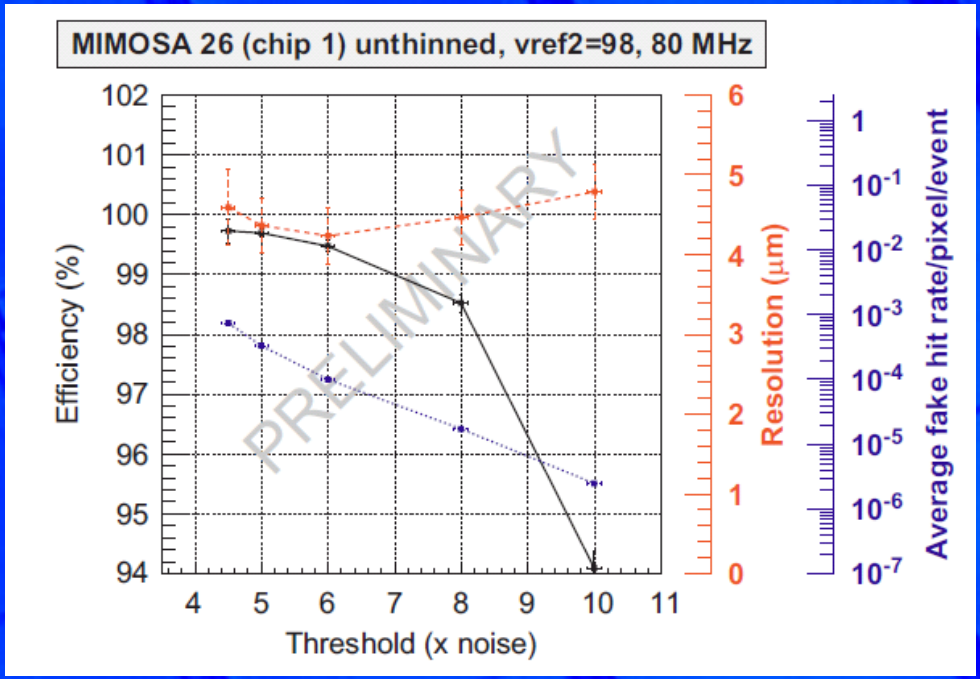
- fully depleted sensitive volume
  - fast signal rise time (~ns), small cluster size
- Fabrication at MPI HLL
  - Wafer scale devices possible
  - no stitching, 100% fill factor
- no charge transfer needed
  - faster read out
  - better radiation tolerance
- Charge collection in "off" state, read out on demand
  - potentially low power device
- internal amplification
  - charge-to-current conversion
  - large signal, even for thin devices
  - r/o cap. independent of sensor thickness

Technologies for the Vertex Tracker
CMOS Active Pixel Sensors

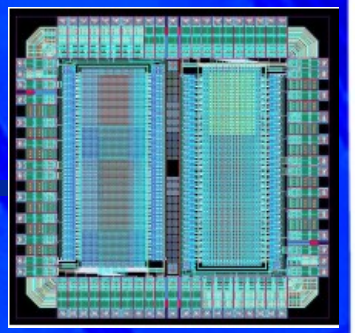
CMOS APS offers high granularity with thin sensitive layer, signal sensing and some processing in pixel, analog and/or digital processing in periphery, fast column parallel readout (rolling shutter);

R&D driven by ILC in the last decade, significant progress towards sensors ready for applications in real experiments (STAR, CBM)

S/N, speed and radiation tolerance motivate transition towards CMOS technology integrated with high resistivity sensitive layer.



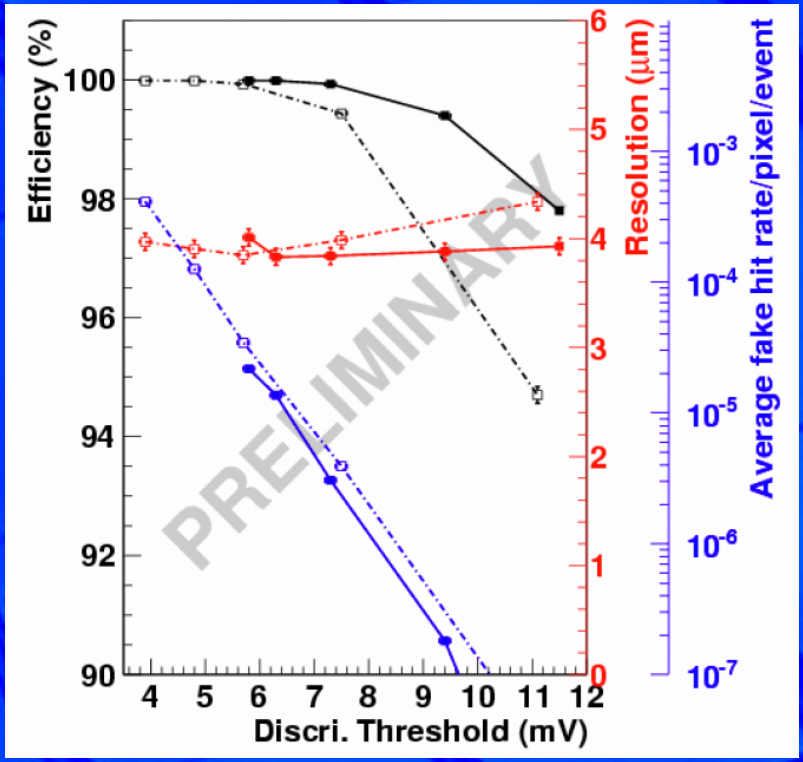
Technologies for the Vertex Tracker
CMOS w/ High-Res. Substrate



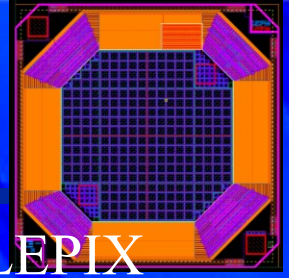
Port of std CMOS process on wafers with high resisitivity substrate offer higher charge yield, faster charge collection dominated by drift, improved radiation tolerance and faster r/o:

IPHC Mimosa 26 in 0.35AMS-OPTO with 400 Ω-cm epi layer, binary readout 80-115MHz (115-85μs integration time) M26 tested at SPS in EUDET telescope (10 and 15μm high-res epi layer):

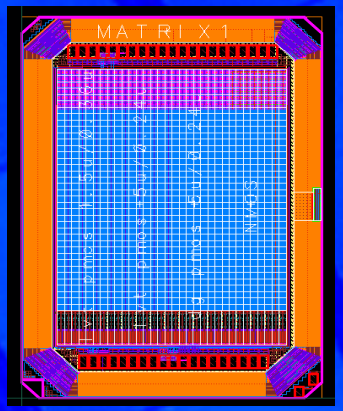
MIMOSA sensors with high-res epi-layer intended for application in STAR HFT (IReS, LBNL);



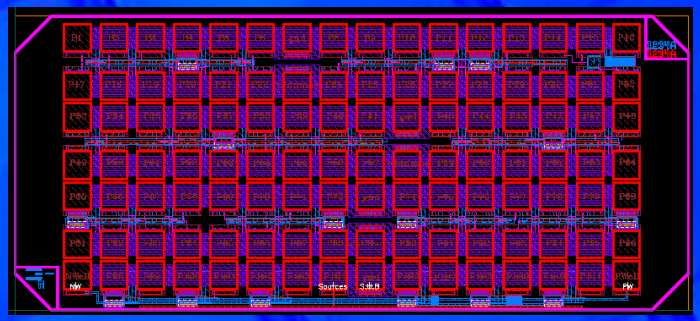
Technologies for the Vertex Tracker
CMOS w/ High-Res. Substrate

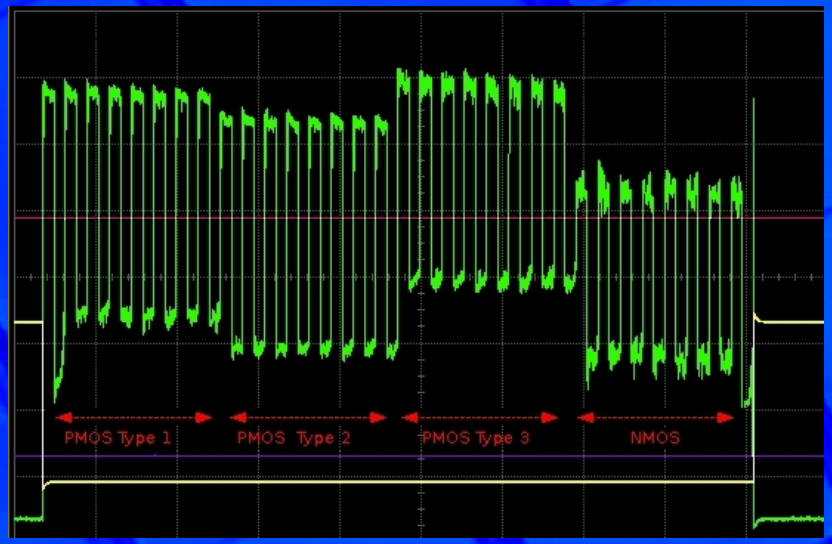


Port 90 nm CMOS process to high-res wafers developed by the LEPIX collaboration (CERN, INFN, IPHC, UCSC, Kosice, …) led by CERN:
expect good radiation hardness (charge collection by drift),
parallel pixel signal processing with 25ns time tagging,
low power consumption with low capacitance, …

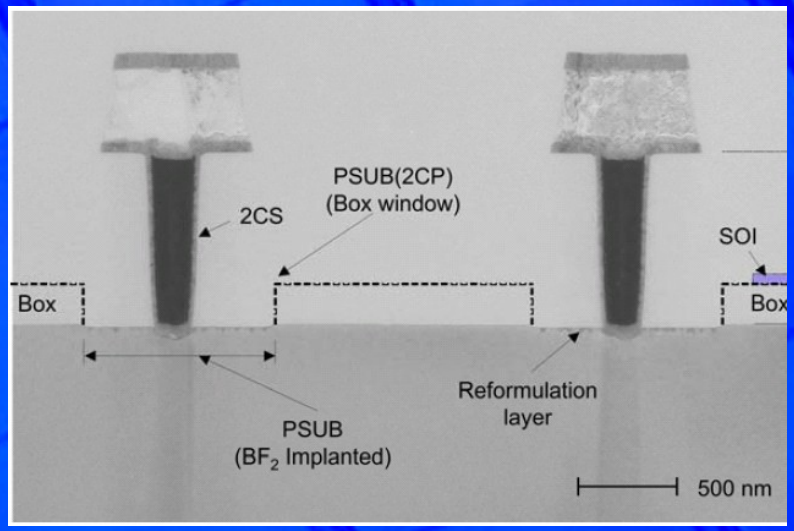


First structures produced and being tested at CERN:
- breakdown voltage > 30 V on std Si,
- expect to get depletion ~ 50 µm
  for a collection electrode capacitance
  of a few fF, or less.



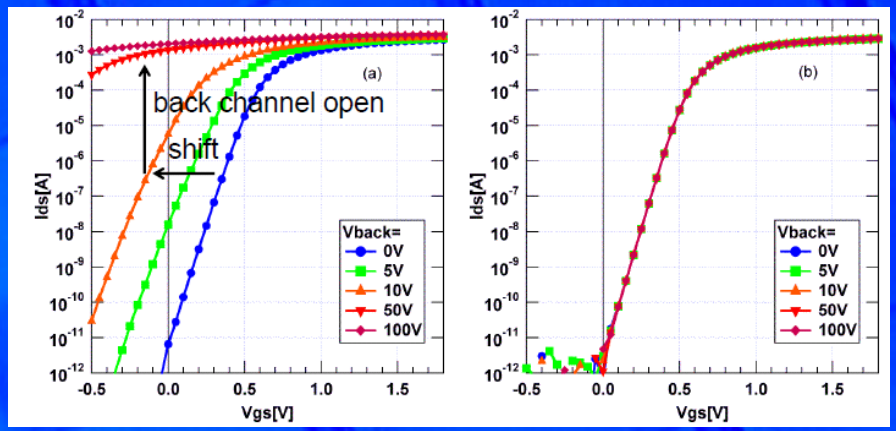


Technologies for the Vertex Tracker
CMOS w/ High-Res Substrate: Silicon-On-Insulator



SOI process offers appealing opportunity for monolithic pixel sensors, removing limitations of bulk CMOS processes;

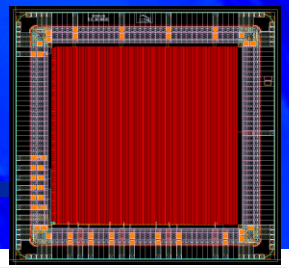
- High-res sensitivevolume → large signals;
- Deep submicron CMOS electronics;
- No interconnections;
- Low collection electrode capacitance;
- Potentially Rad-hard;
- Main challenges: transistor back-gating & charge trapping in BOX



Back-gating suppressed by adding buried p-well (KEK);
Nested well structure being tested (FNAL+KEK), double SOI layer wafer;
Successful sensor back-thinning to 50 & 110μm (LBNL, FNAL and KEK)

Y Arai et al.

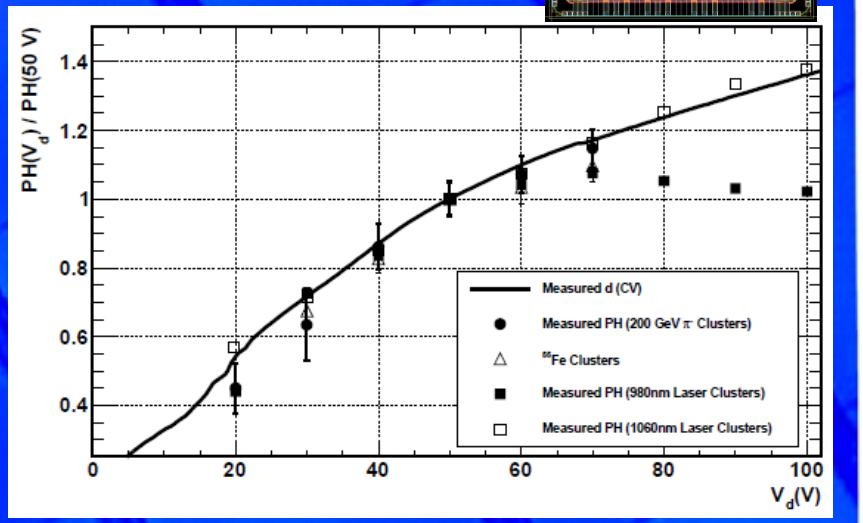
Technologies for the Vertex Tracker
CMOS w/ High-Res Substrate: Silicon-On-Insulator

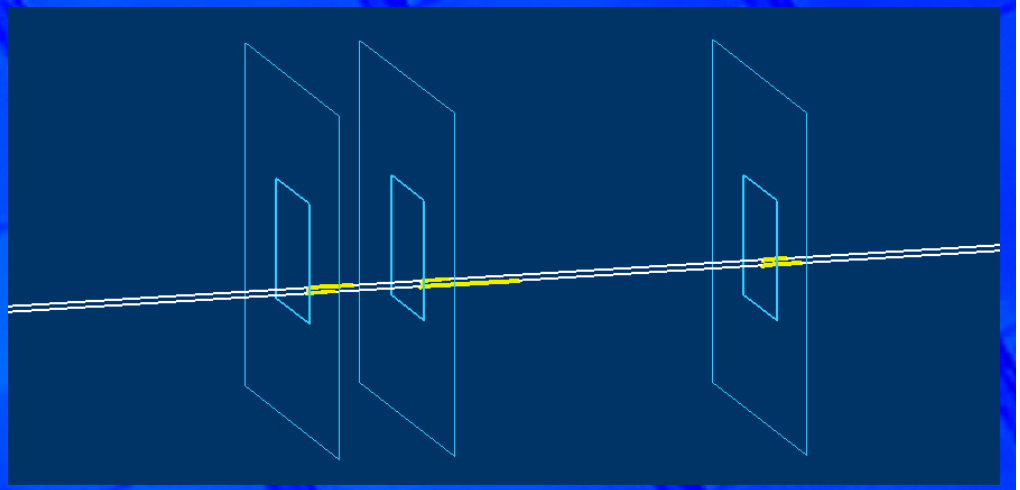


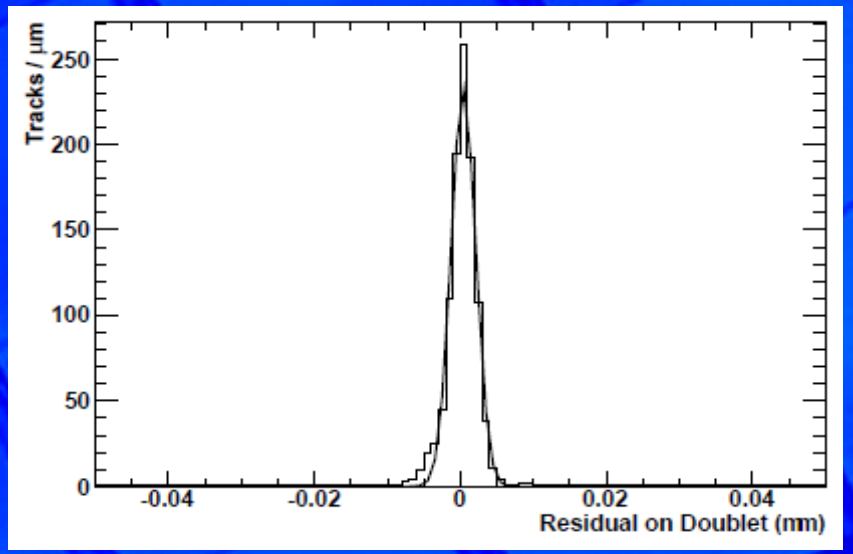
OKI-KEK MPW, 700 Ω-cm handle wafer: LBNL test chip w/ analog pixels on 15μm pitch and various designs

Prototypes with BPW operates up to 100V w/ depletion depth of ~150μm → S/N > 50; SPS beam test with 200 GeV π- shows

$\varepsilon = 0.99^{+0.01}_{-0.03}$ and $\sigma_{point} = (1.12 \pm 0.03)\ \mu m$



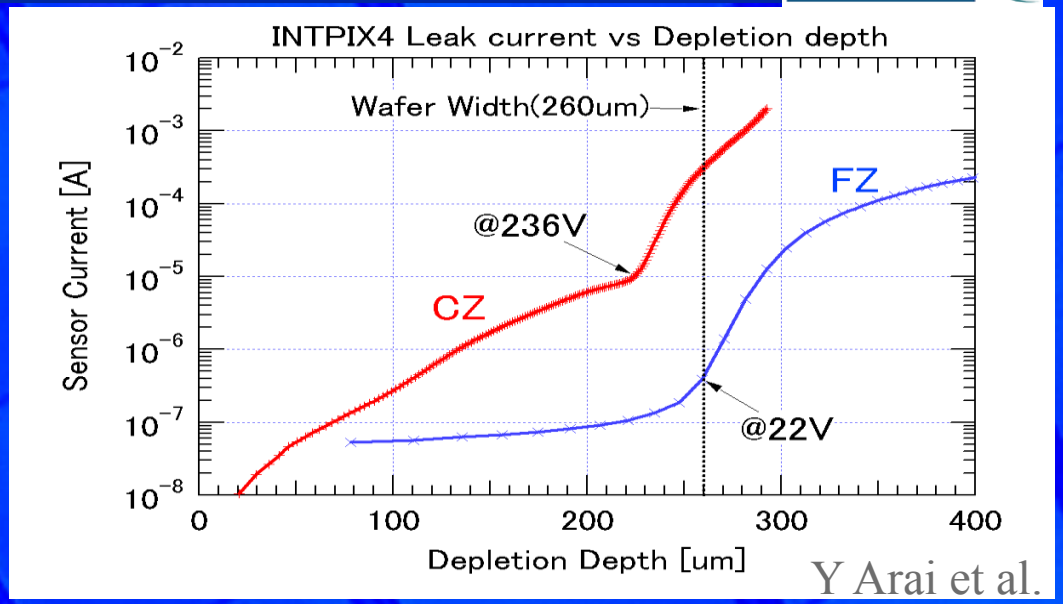




MB et al., arXiV:1103.088

Technologies for the Vertex Tracker
CMOS w/ High-Res Substrate: Silicon-On-Insulator

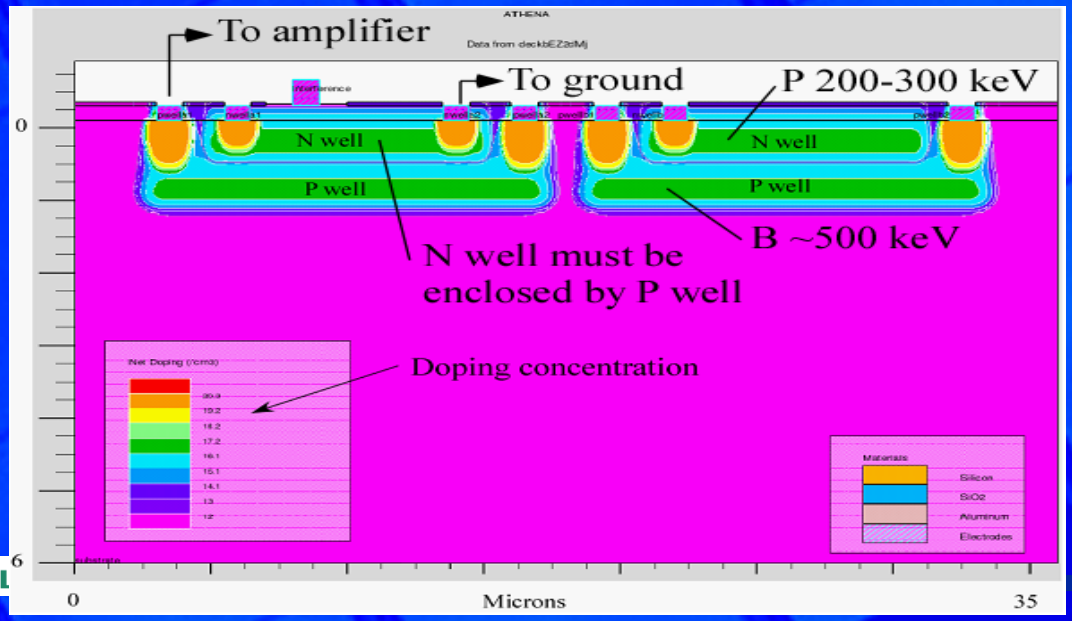
SOI with Float Zone Si gives encouraging results at KEK and FNAL, full depletion of 260µm thickness with 22 V (but higher leakage);



Y Arai et al.

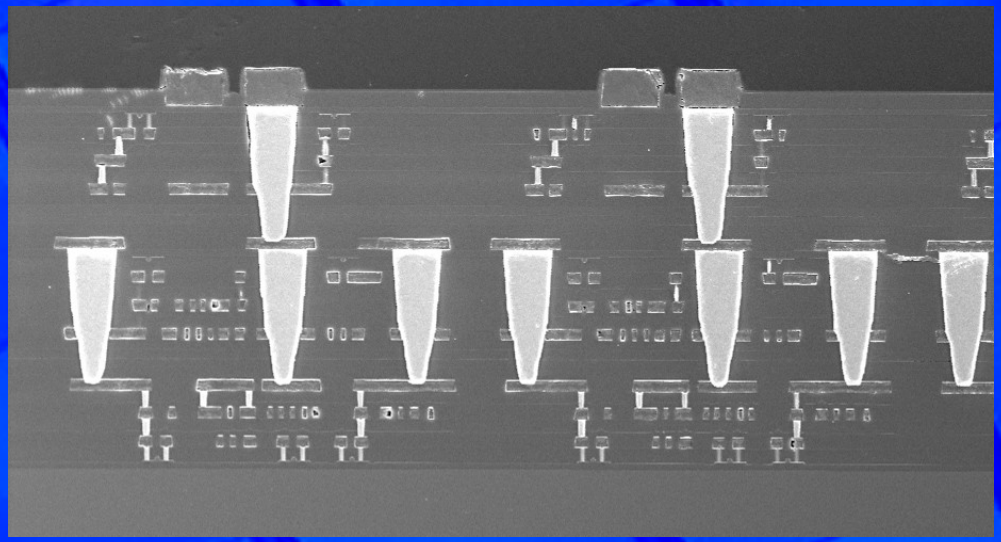
FNAL MAMBO chip exploring nested well design: deep p-well to collect charge and shallow n-well to shield electronics;

Complex architecture with large pixel size, will need to be revisited for LC application.

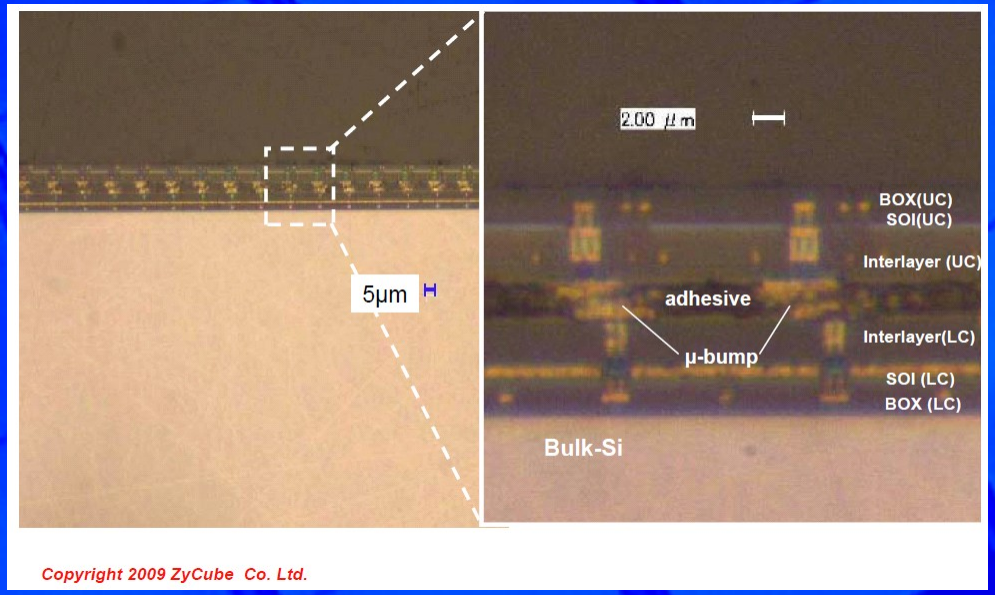


Technologies for the Vertex Tracker
3D Vertical integration

FNAL leading collaboration for sensor application of 3D technology at Chartered/Tezzaron

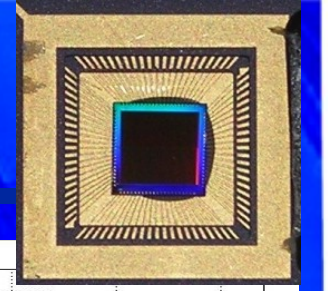


3D CMOS offers several advantages:
-heterogeneous tiers
-Isolation of electronics from sensor
- industrial standard
but progress very slow so far;



Test of 3D-SOI at T-Micro (KEK,LBNL,FNAL)

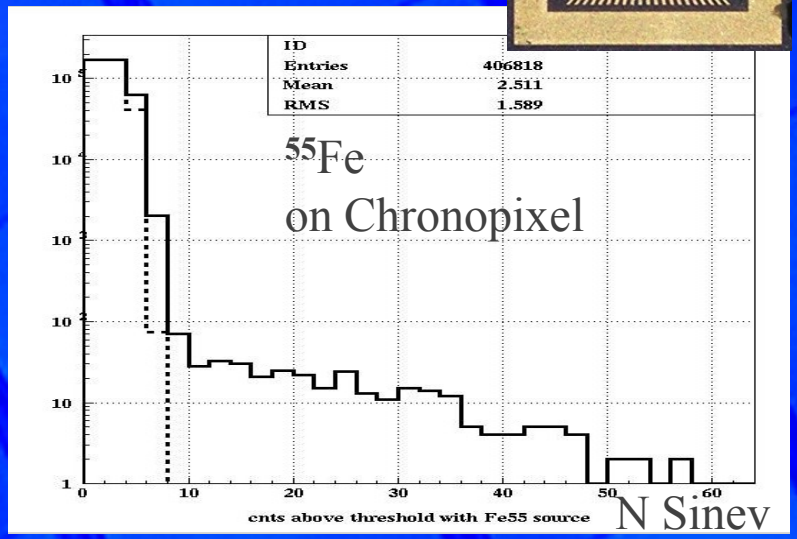
Architectures for the Vertex Tracker : Time stamping

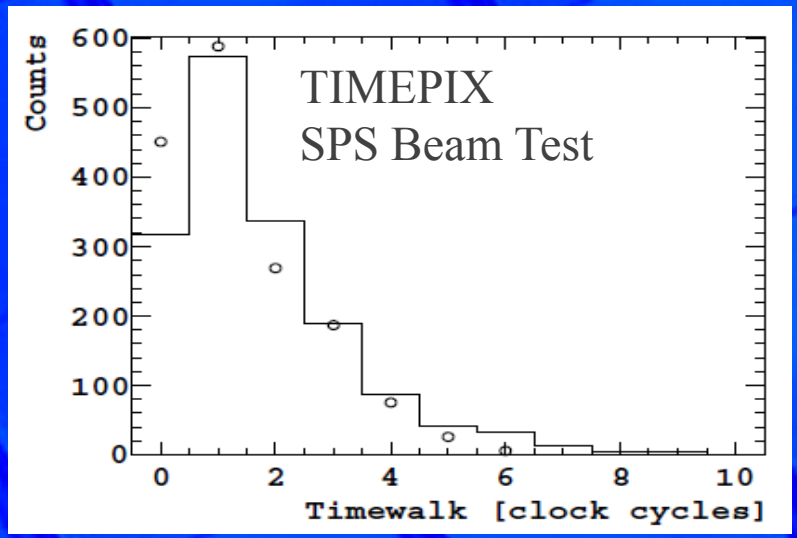


Chronopixel develop architecture w/ in-pixel time stamping, digital readout during inter-train period;
Current prototype in TSMC 180nm [45] CMOS, low-res 7μm [15] epi and no deep p-well: first test of architecture with 50μm pitch [10];

Pixel noise 25e- [24] using soft reset+feedback, Pixel capacitance ~ 3.5fF, gain 35.7μV/e- [10]
Comparator threshold spread 24.6mV [9];
Power dissipation 125mW/cm2 [15]; Time stamping at 7.27 MHz → 140ns resolution;
Faster time stamping (CLIC Δt=0.5ns) limited by charge collection time. [ ] ILC requirement

VELOPIX readout chip developed from TIMEPIX for LHCb upgrade may offer interesting approach to fast-time stamping.





Physics requirements at a future linear collider motivated significant R&D on monolithic pixel sensors to achieve small pixel cells with integrated charge sensing and some data processing, thin sensors with low power consumption and fast readout and/or high space-time granularity;

Contemplating energy increase from 0.5 TeV to multi-TeV implies new requirements on fast time stamping, which need to be addressed by dedicated R&D;

Technologies developed in ILC-motivated R&D have significant impact on other particle physics experiments as well as imaging and spectroscopy in other fields of science from electron microscopy to biology and astronomy.