

R&D on SOI and 3D Detectors and Electronics at Fermilab

Ronald Lipton



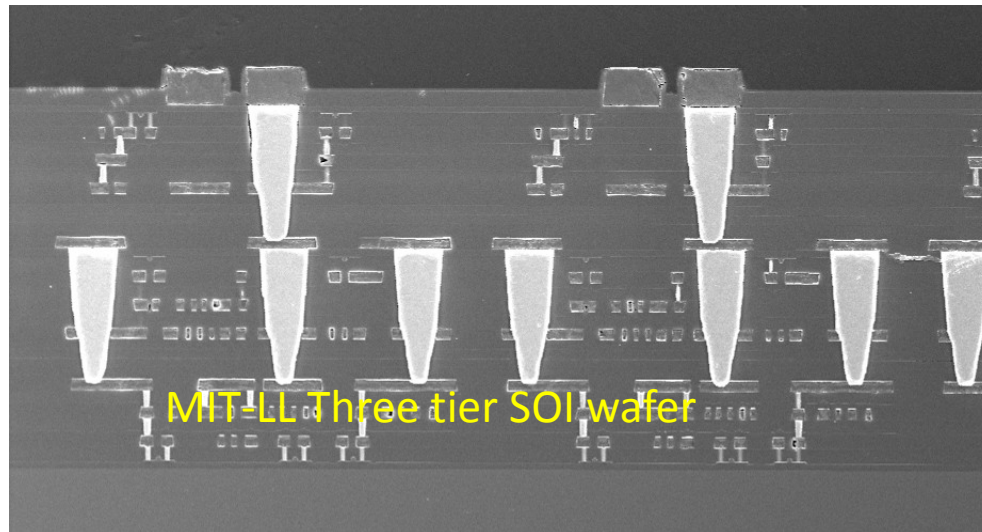
Fermilab has had a long program of development of new technologies for integrated detectors and electronics. I will discuss the status of this programs and prospects for the future.

- 3D Devices
 - VIP2a from MIT-LL
 - VIP2b from Global Foundries/Tezzaron
- SOI Devices
 - MAMBO4
 - 8" float zone integrated sensors
- Future Plans

A Bit of History

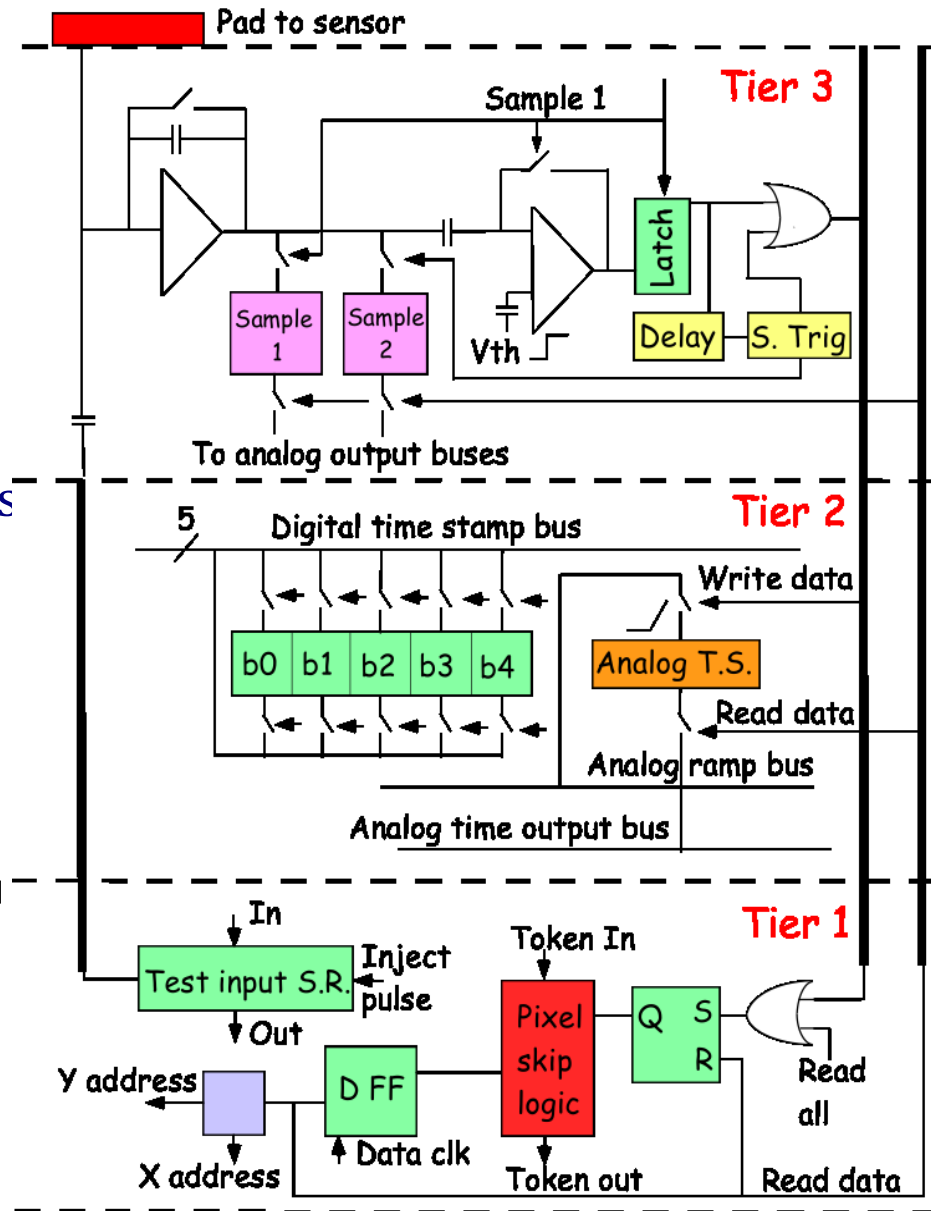
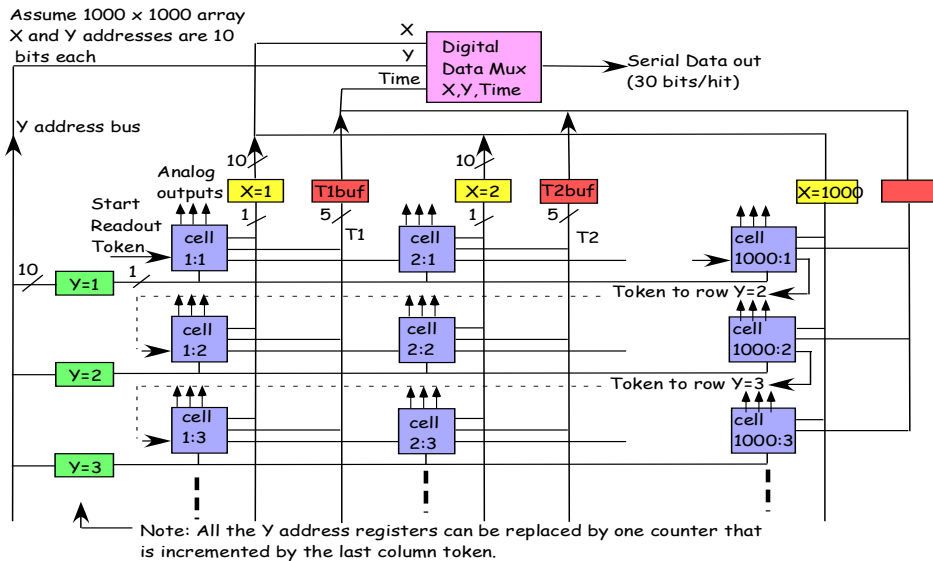


- We began working on 3D devices when it became clear that significant processing in small pixels would be necessary to meet the goals of:
 - >5 micron position resolution
 - Low mass $\sim 0.1\%$ RL
 - Time stamping to ~ 1 crossing if possible
 - Low power
- Other technologies have a difficult time integrating all of the needed functionality in a small pixel
- Multilayer 3D electronics solves this problem



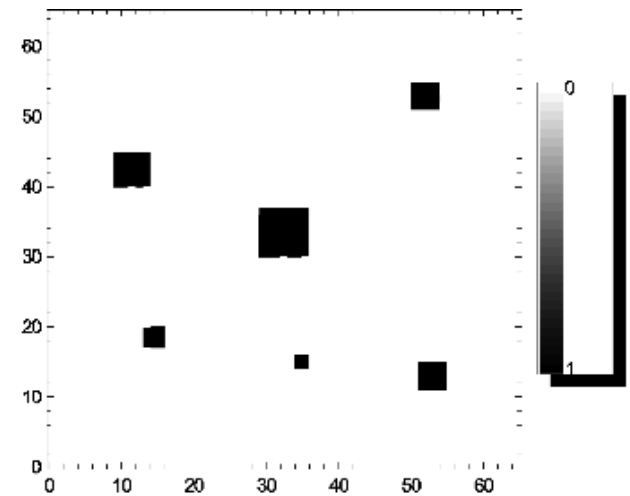
VIP Design

- Two (VIP2b) or three (VIP1,2a) tiers
 - Double correlated sampling
 - Analog and digital time stamp
- Can use analog as a vernier to provide single bunch resolution
- Minimal area lost to peripheral circuits

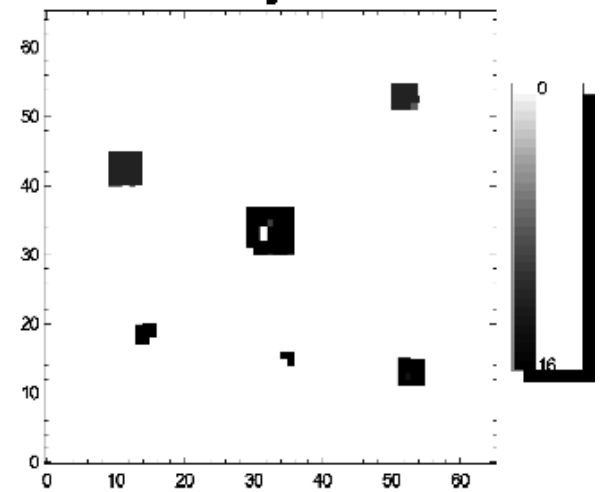


VIP1 - MITLL

- Basic functionality of the chip was demonstrated
 - Propagation of readout token
 - Threshold scan
 - Input test charge scan
 - Digital and analog time stamping
 - Fully sparsified data readout
- No problems could be found associated with the 3D vias between tiers. However:
 - Chip performance compromised by SOI issues:
 - Large leakage currents in transistors and diodes
 - Poor current mirror matching, V_{dd} sensitivity, low yield
 - Soft shorts between nodes



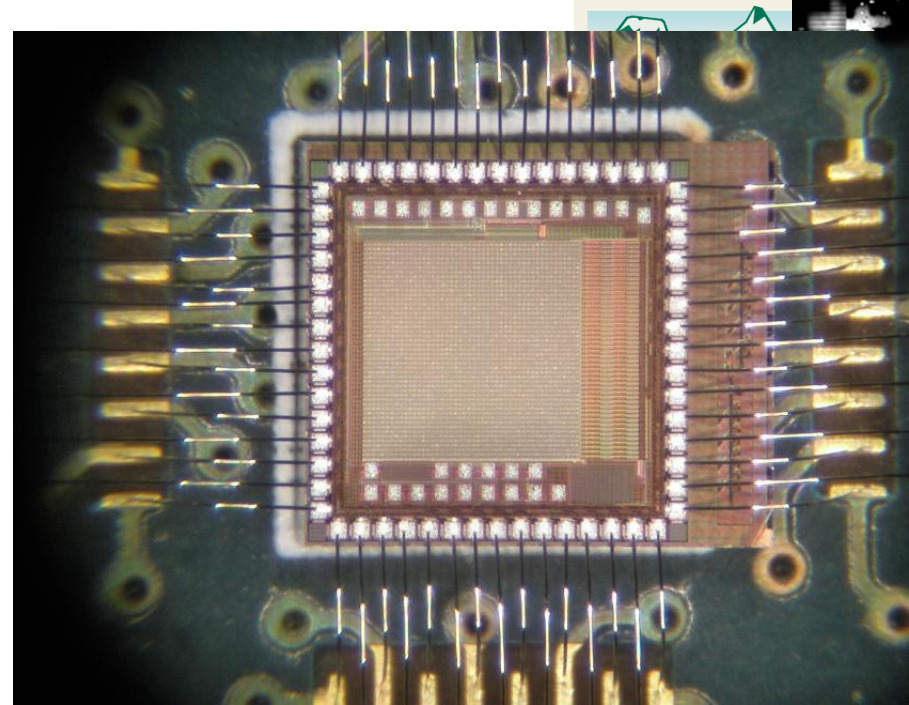
Preselected pattern of pixels for the injection of signal to the front-end amplifiers; pattern shifted into the matrix, then positive voltage step applied across the injection capacitance; threshold levels for the discriminator adjusted according to the amplitude of the injected signal



Pattern of pixels from the preselected injection pattern that after injection of tests charge reported as hit (grey level represents number of repetition - 8 times injection)

VIP2a Design

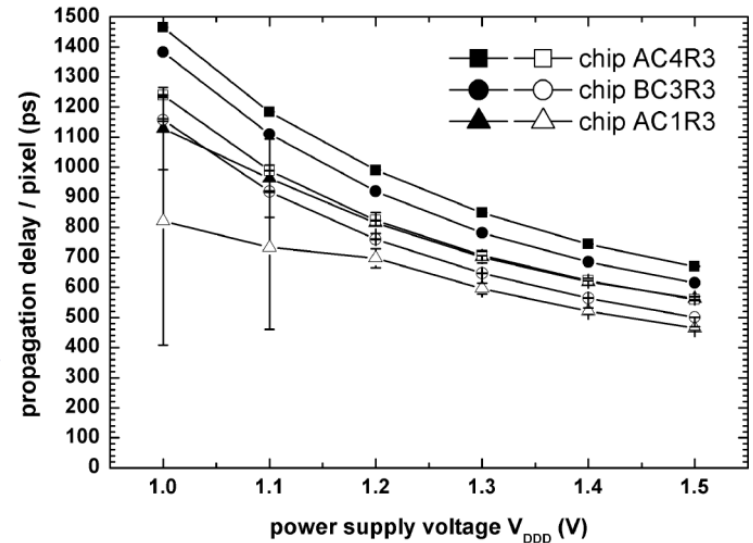
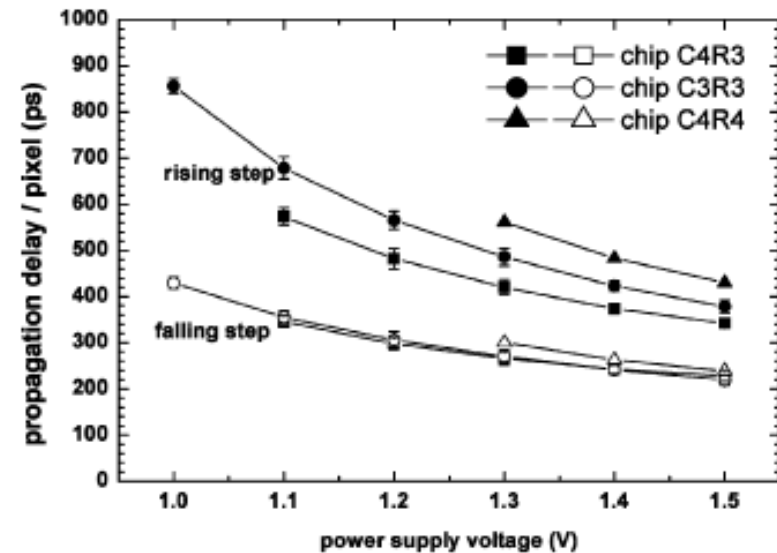
- Conservative design to avoid SOI issues:
 - Replace dynamic by static flip flops
 - Scale trace routing rules by 1.2
 - Increase transistor sizes (0.15 μm -> 0.3 μm)
 - Replace source followers by Op amps
 - Extensive power/ground mesh
 - >2x larger sample/hold capacitors
 - Redesigned current mirrors (use all separate devices instead of inter-digitated devices)
- Increased functionality and testability
 - 5->7 bit digital time stamp
 - Discriminator arming on digital tier (reduce coupling)
 - Switchable 20 fF load capacitor
 - 48 x 48 array of 28 x 28 μm pixels



VIP2a Test Results

The yield and performance are significantly improved in VIP2a.

- In VIP1 the analog time stamp did not work due to high leakage currents
- The analog time stamp, based on a voltage ramp and S&H, works well in VIP2a
 - Excellent linearity (no droop) from 10 μ s to 1 ms
 - Can be used in conjunction with digital time stamp to achieve equivalent 12 bit time resolution (less than 1 μ sec in 1 msec)
- Sparsification token propagation works over wider voltage range and on many more chips than on VIP1
- Token propagation time is higher in VIP2a due to larger transistor sizes
- Sparsification test mode works
- Protection diodes no longer leak

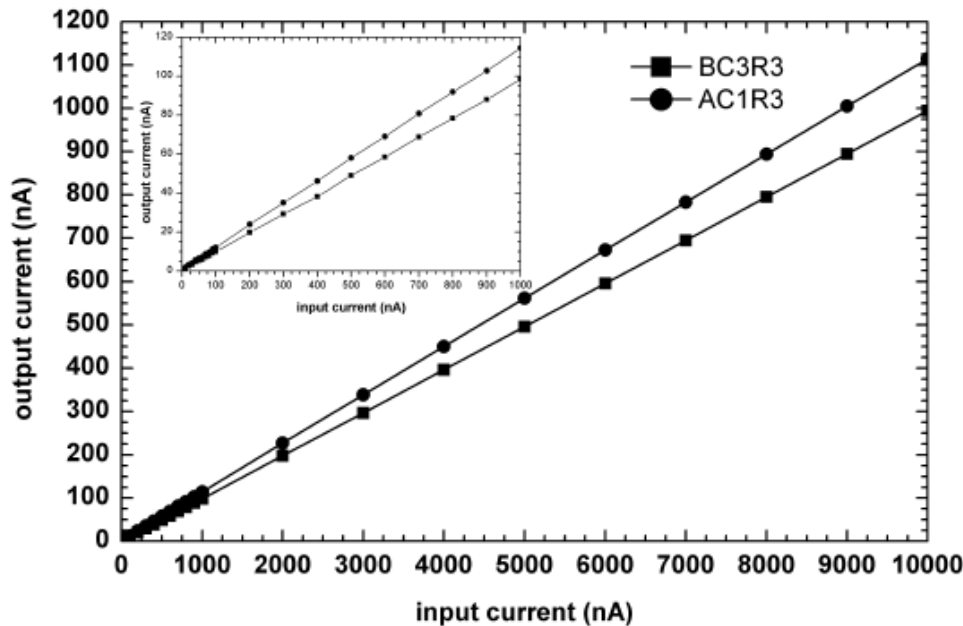
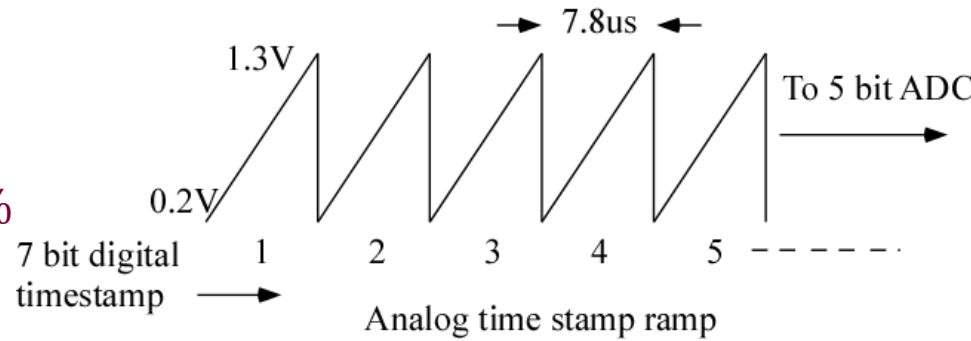


VIP2a Time Stamping

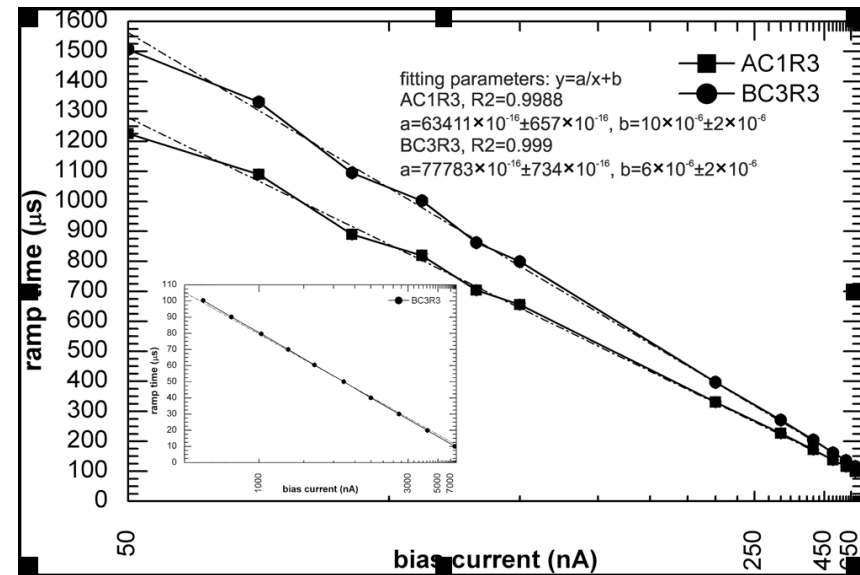


The current mirrors and time stamp ramp now function well

- Time jitter and linearity better than 1%
- Control over the full range to 1 ms



Current mirror linearity



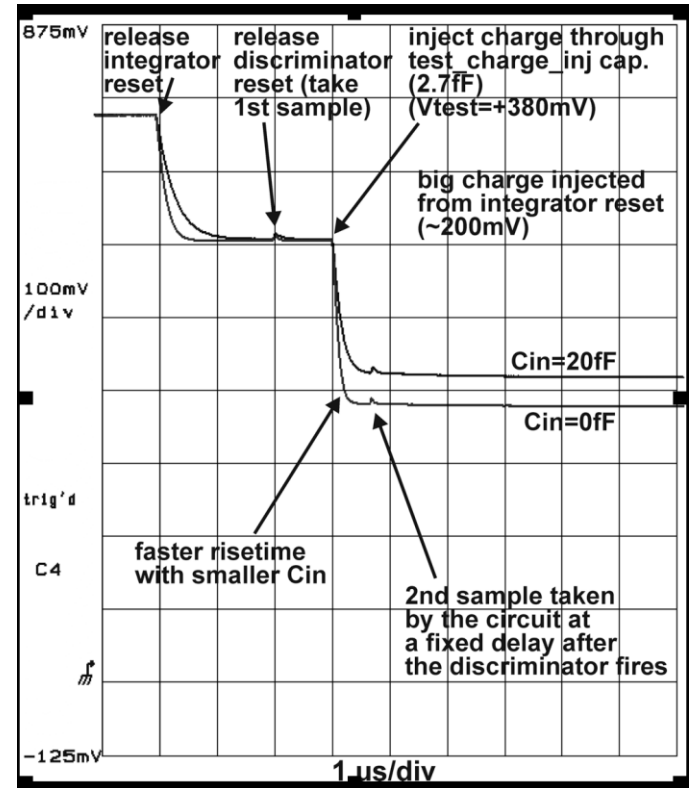
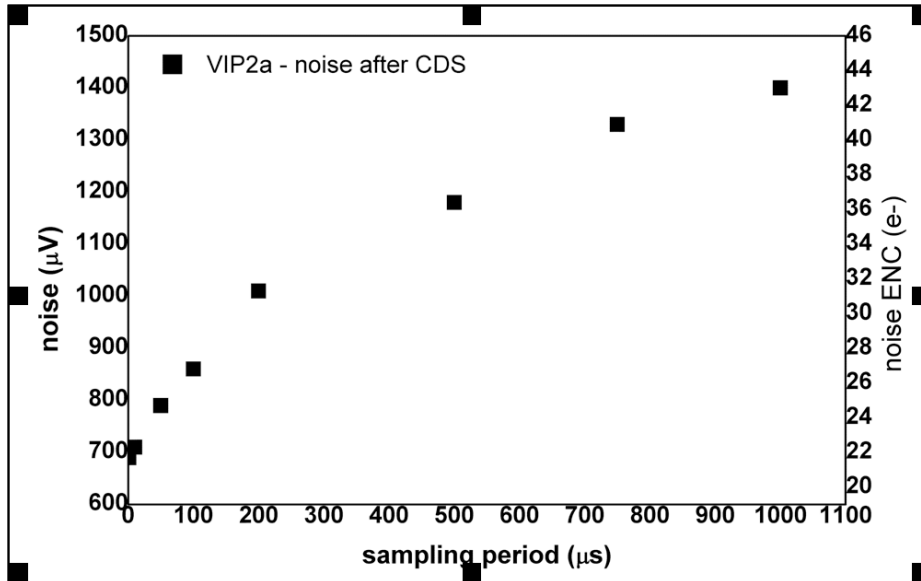
Analog Time Stamp ramp

Front End Results



Double correlated sampling (first sample at beginning of train)

- Good noise performance (20 fF simulated load, DCS with differential analog output, 1 μ s sample time, $T_r=120$ ns, $I_b=0.5\mu A$, $C_s=100fF$)
- Gain ~ 200 mV/fc at $C_L = 20$ fF



3D Multiproject Run



- HEP consortium for 3D circuit design formed in late 2008
 - 17 member groups from 6 countries (Italy, France, Germany, Poland, Canada, USA)
 - First Meeting Dec 2008
 - Began working on 3D MPW run to Chartered/Tezzaron -First MPW run for outside customers
 - Two tiers
 - Identical wafers with face to face bond
 - Single set of masks for both tiers
- HEP MPW run - more than 25 two tier designs (circuits and test devices)
 - CMS strips, ATLAS pixels
 - ILC pixels
 - B factory pixels
 - X-ray imaging
 - Test circuits
- Frame divided into 12 subreticules for each tier

Birth Pains



- Everyone did not use the same design kit provided by Tezzaron resulting in
 - Stream layer map errors
 - Misuse of top metal
 - Incorrect MiM cap rules
 - Unsupported design options
- Some design rules were interpreted incorrectly leading to various TSV design problems.
 - Dishing of wafers where a third layer was to be added
 - Metal 1 over lap on TSV which could cause contamination problems
- Initially some designs did not use a fill program resulting in fill problems later on
- The bond pad interface pattern must be uniform across a reticule. Repeated requests to route on the bond layer had to be denied.
- SRAM cells raised numerous questions.
- Tezzaron uses MicroMagic to assemble the frame for 3D submissions.
 - In the course of receiving designs, two separate software problems were found due to the nature of our designs
 - A rounding error caused off grid placement of bond interface pads only in some designs leading to unnecessary errors.
 - An ARM cell was used that had off grid vertices that created unnecessary errors
 - The problems have been fixed

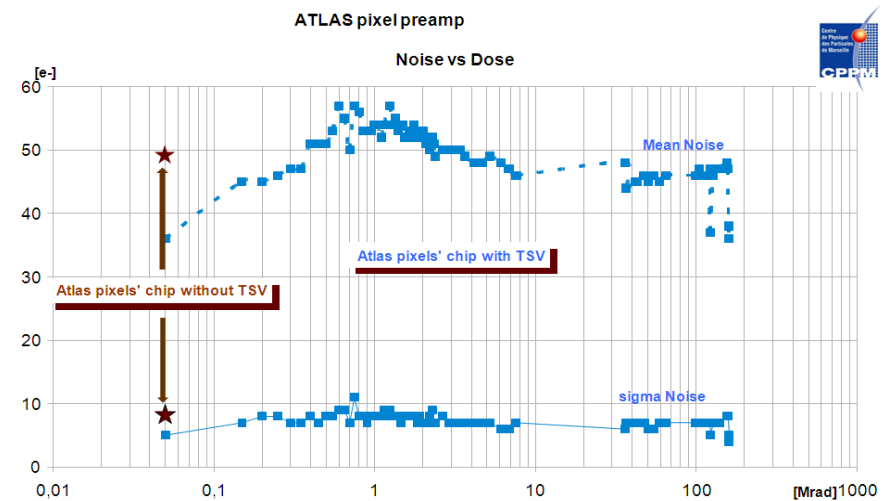
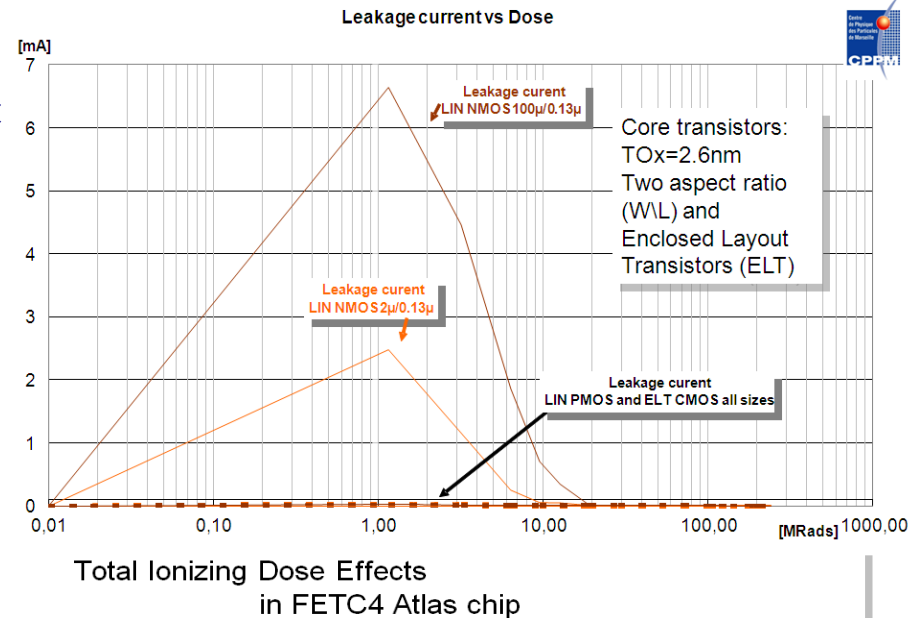
Submission Issues



- Chartered provided initial size of design area in the frame. After all designs were completed and used all the design space, Chartered requested additional street space. It took three submissions before Chartered would finally accept the frame.
- Some designs had labels outside the design area causing Chartered to reject submission and much rework.
- After designs received by mask house, individual blocks were incorrectly mirrored by the mask house which fortunately was caught by Tezzaron before the masks were made.
- Chartered would not accept some error waivers we thought were acceptable.
- Some designs were submitted with incorrect mirroring
- Global/Chartered did not properly place frames on wafers for 4 different lots of wafers being processed for Tezzaron. The wafers could not be aligned properly for 3D bonding.
 - Never happened before
 - HEP wafers had to be refabricated resulting in several months delay
- Due to delays in fabrication, the 3D wafer bonding facilities were not available when the wafers were ready.

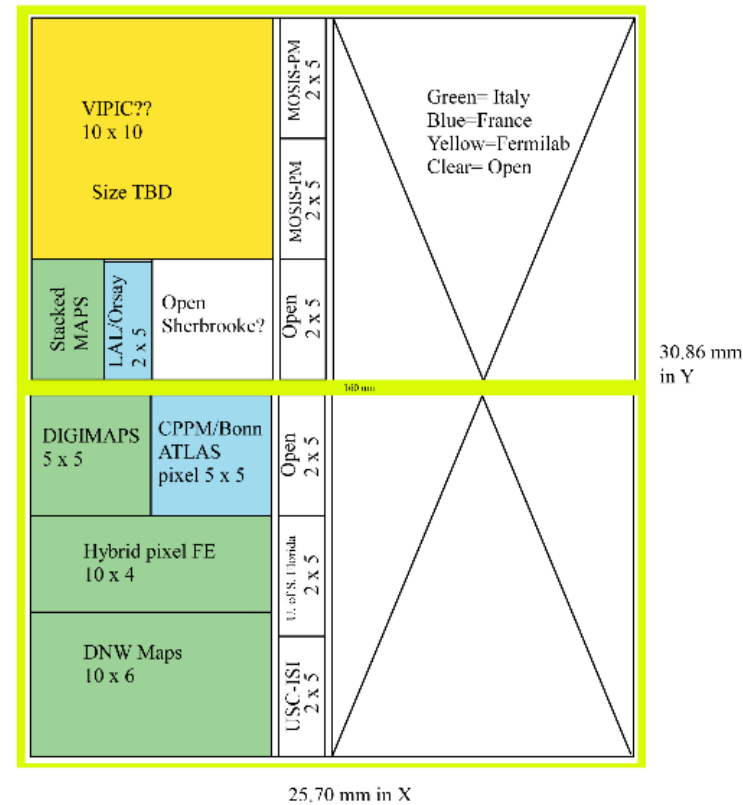
Radiation Test Results

- Testing of 2D wafer transistors and pixel circuits with TSVs in CERN's X-ray test lab at 3.2 Mrads/hour (Preliminary results)
 - NMOS leakage current shows peak around 1 Mrad – similar to other CERN results
 - Linear NMOS leakage may be a concern
 - Linear PMOS and ELT NMOS and PMOS are good
 - NMOS and PMOS V_t shifts are similar to CERN tests on other 130 nm processes, however Chartered NMOS V_t shift is positive instead of negative
 - Tests on ATLAS pixel preamp show only a small change in noise up to 160 Mrads
- Radiation tests thus far suggest that the Chartered 130 nm process is similar to other 130 nm processes tested at CERN
- Rad tests thus far validate moving the 3D circuit design activity from the MIT SOI process to commercial CMOS



Commercialization

- MOSIS/CMP/CMC (silicon brokers in US, France, and Canada)
 - Agreement with Tezzaron for commercialization
 - June 2010 - Announced plan to offer 3D services using Tezzaron
 - Working with Fermilab to make HEP 3D efforts available to the commercial world
 - Design platform is being developed by Kholdoun Torki at CMP and the first version is now available
 - MOSIS, CMP, and CMC will all receive designs
 - MOSIS will assemble designs into a reticule
 - Tezzaron will handle the final processing of the 3D frame (e.g. adding bond pad interface fill, etc.) and submit design to Chartered.



VIP2b

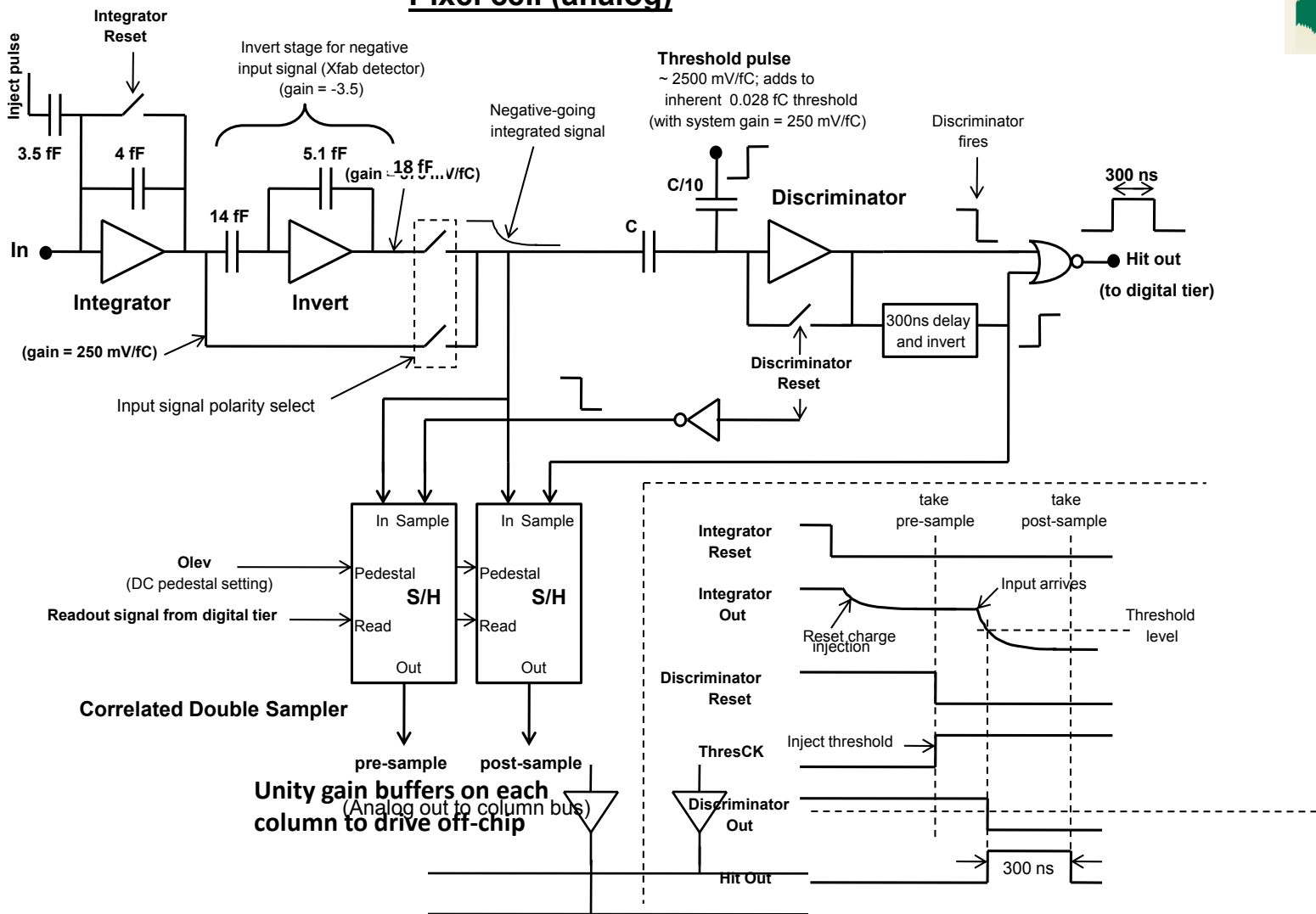
Functionally similar to VIP2a

- Part of 3D multiproject run
- 2 Tiers of 0.13 μm CMOS
- 24 μm pixel pitch
- Will be integrated with detector using oxide bonding process

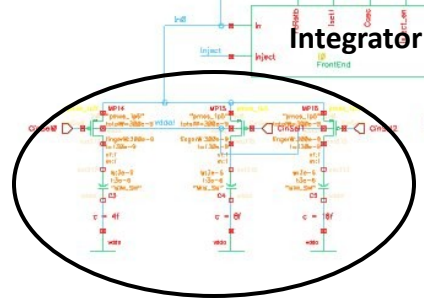
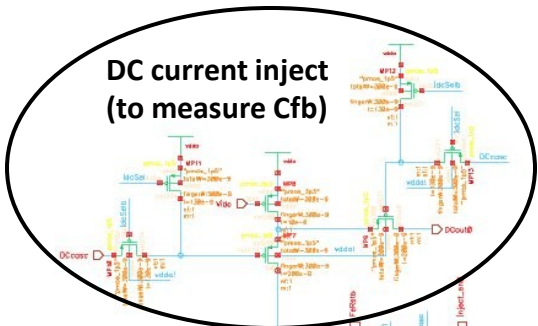




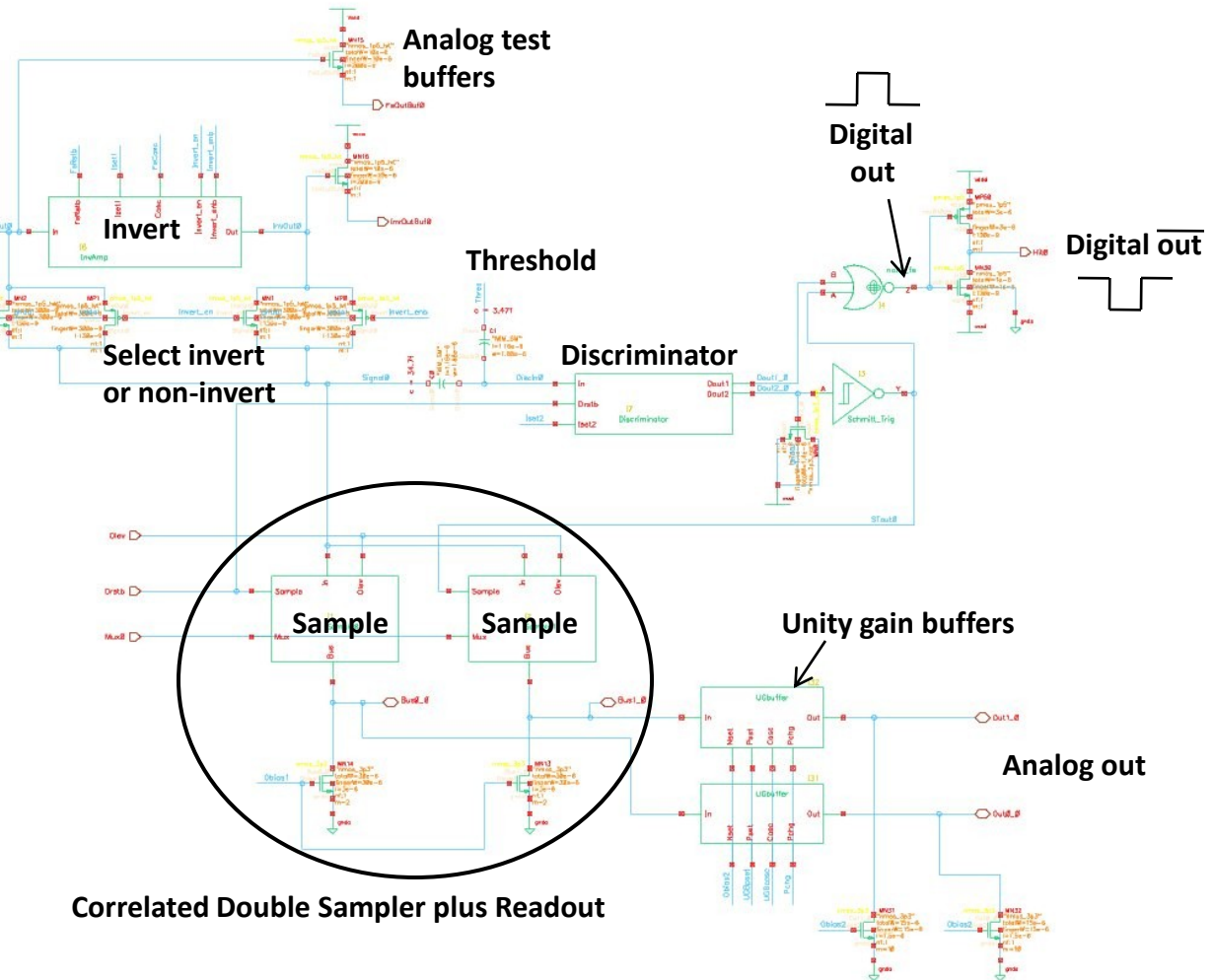
Pixel cell (analog)



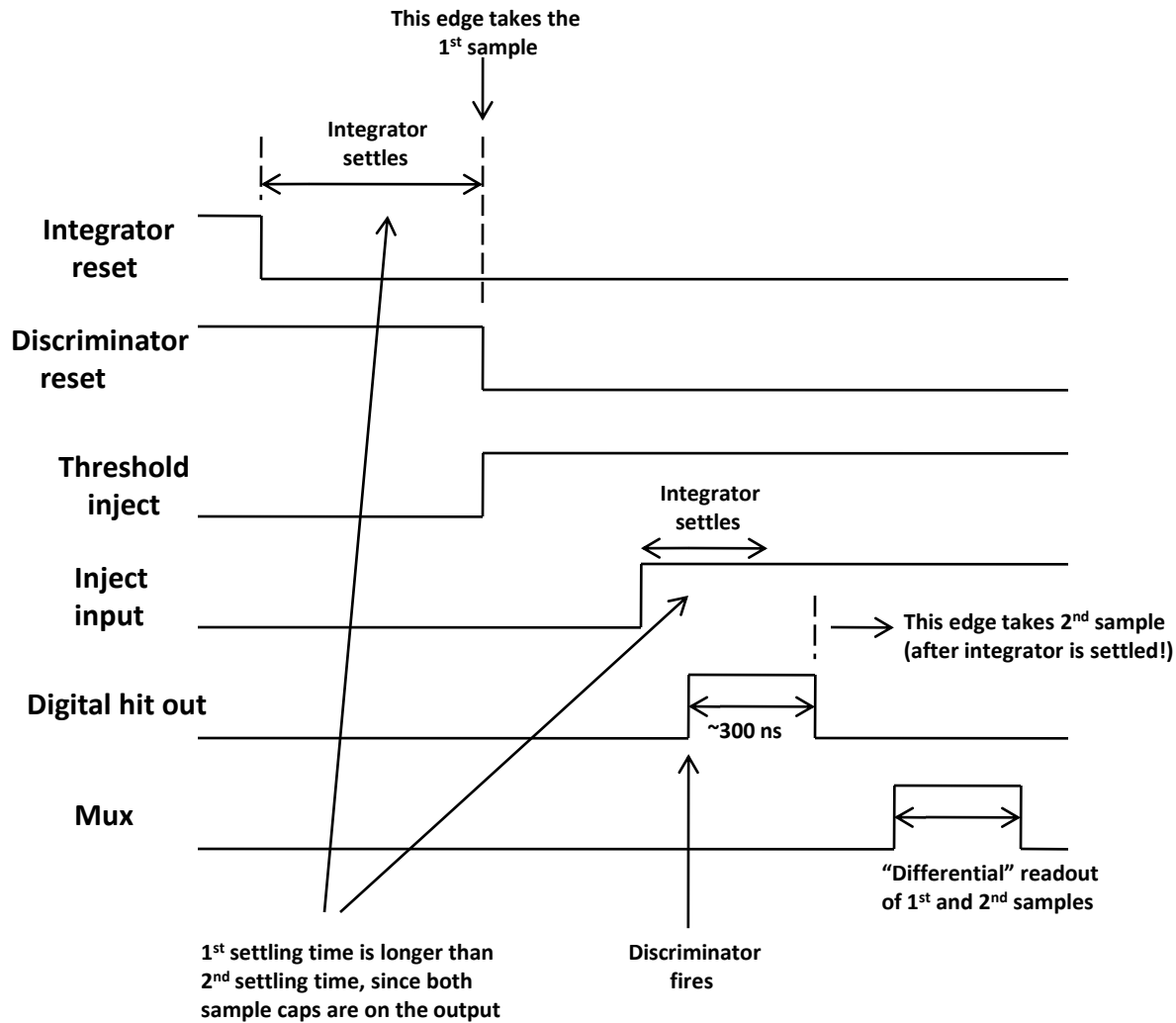
2D VIP Test Chip GF/Tezzaron



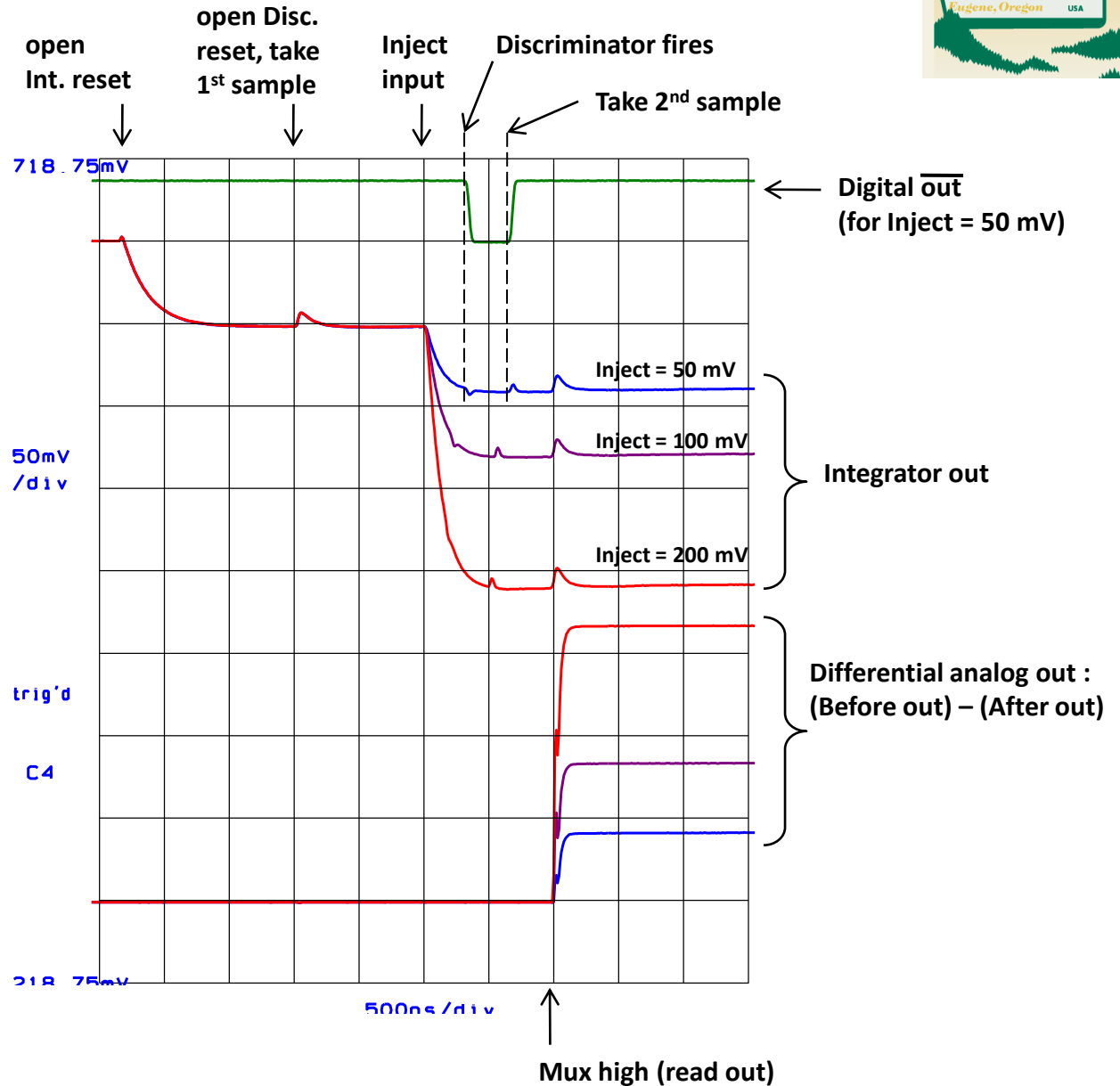
One channel of test circuit (Analog pixel circuitry)



Signals and Timing



Measured Response



Threshold and Linearity



Vthreshold	Vinject req'd to fire disc.	Integrator out
0	17 mV	-13 mV
98 mV	29	-22.5
198	42	-33
295	54	-43
384	65	-52
503	80	-64
606	94	-75

Threshold offset: 0.052fC (intentional; injected by discriminator reset opening)

Vthreshold sensitivity: 0.41 fC/V

Threshold/Integrator out = 9.8 (close to expected)

Vinject	Integrator out	UGbuffer out (diff.)
50 mV	-41 mV	42 mV
100	-82	86
150	-123	129
200	-164	173
250	-205	216
300	-246	259
350	-287	302
400	-328	345
500	-410	430
600	-491	510
700	-574	575
800	-655	619

Readout + UGbuffer gain ~ -1.06

← Readout very linear up to here

← Integrator very linear all the way

Measured Speed



(T = one RC time constant)

Csel	Cin added	Cin + Cinstray	Both sample caps on the output		One sample cap on the output	
			T _{before} Int. out	T _{after} Int. out	T _{before} Inv. out	T _{after} Inv. out
111	0	12.5 fF	115 ns	73 ns	135 ns	65 ns
000	28 fF	44 fF	215 ns	125 ns	140 ns	80 ns

At integrator out; speed varies due to varying C_{sample} and varying C_{in}.

At invert stage out; varying C_{in} has much less effect on bandwidth.

Noise with Double Corr. Sampling



Csel	Cin added	Cin + Cinstray	Noise at Inv. Out (mV)	Noise at Inv. Out (e)	Noise at Int. Out (mV)	Noise at Int. Out (e)
111	0	12.5 fF	2.26 mV	16 e	0.74 mV	19 e
110	4 fF	17 fF	2.58	18	0.79	20
101	8	21.5	2.84	20	0.82	21
100	12	26	3.11	22	0.87	22
011	16	30.5	3.38	24	0.93	23
000	28	44	4.09	29	1.04	26



Bandwidth not very sensitive to Cin



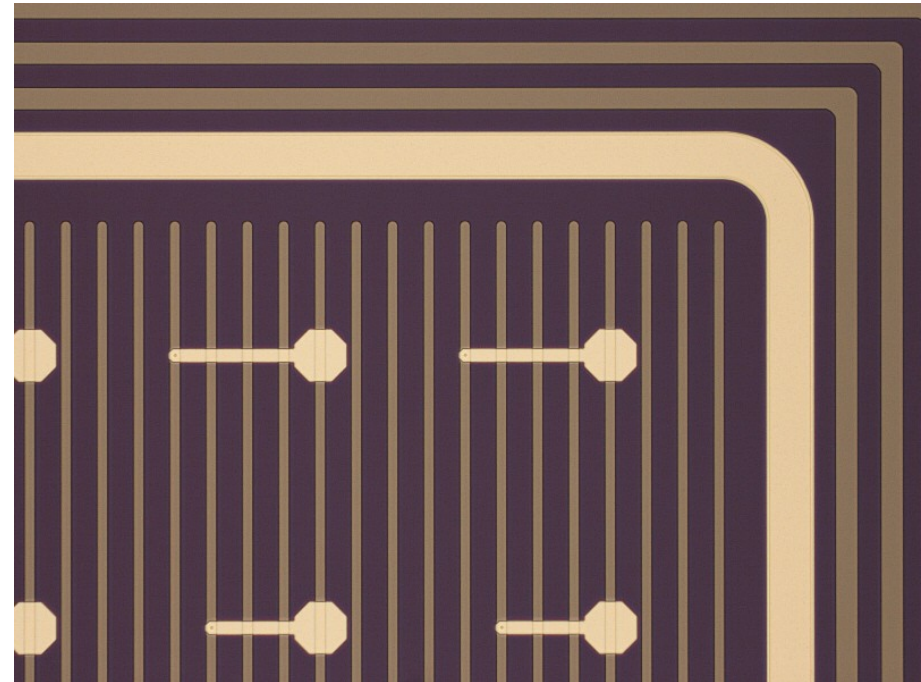
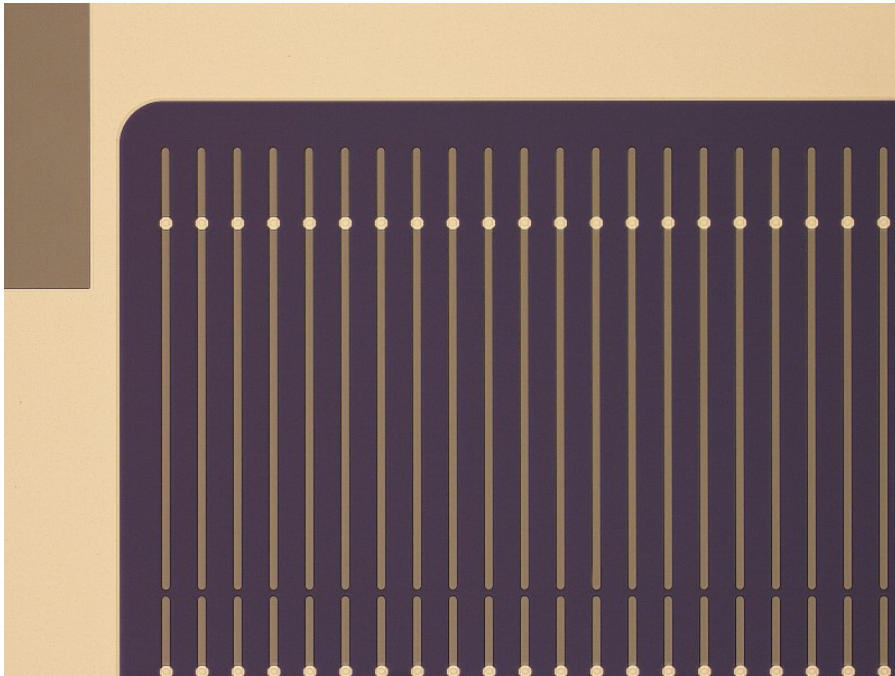
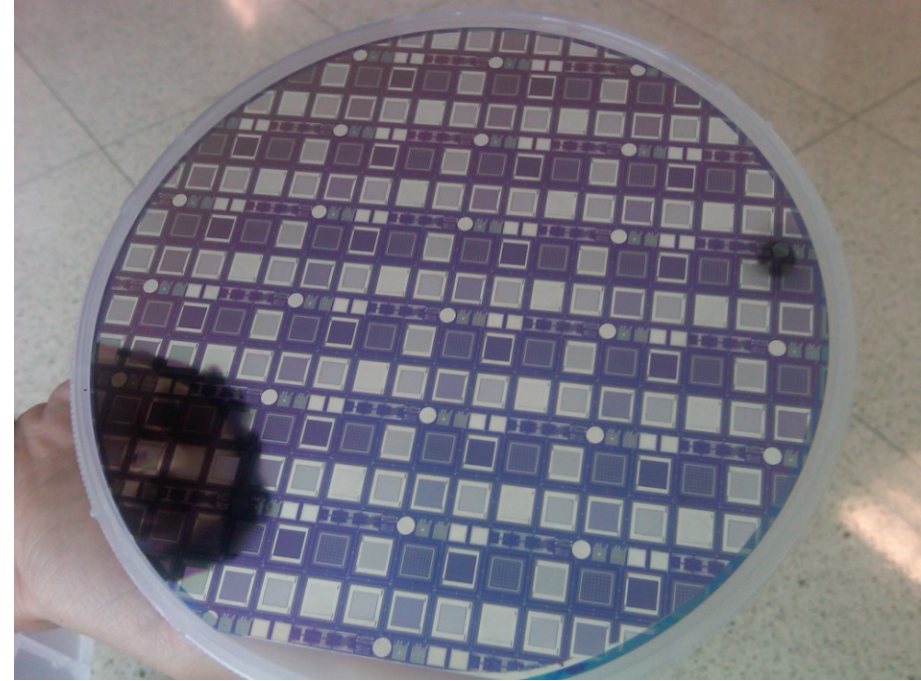
Bandwidth varies with Cin

↑
 $8e + 0.5 e/fF$

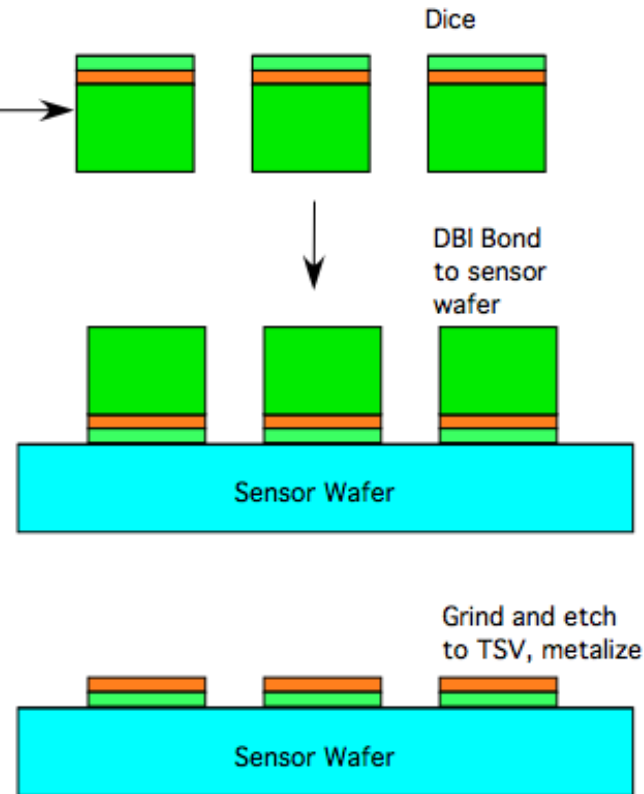
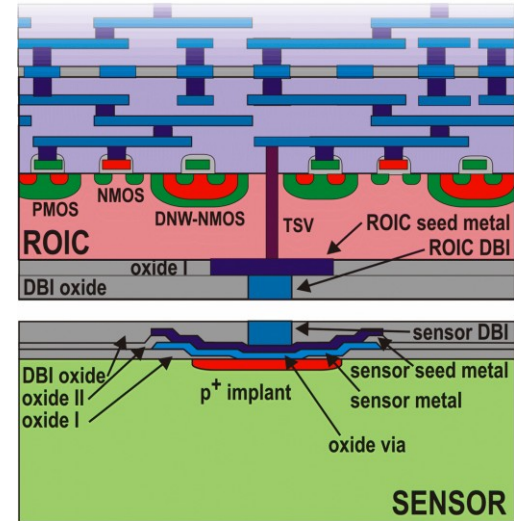
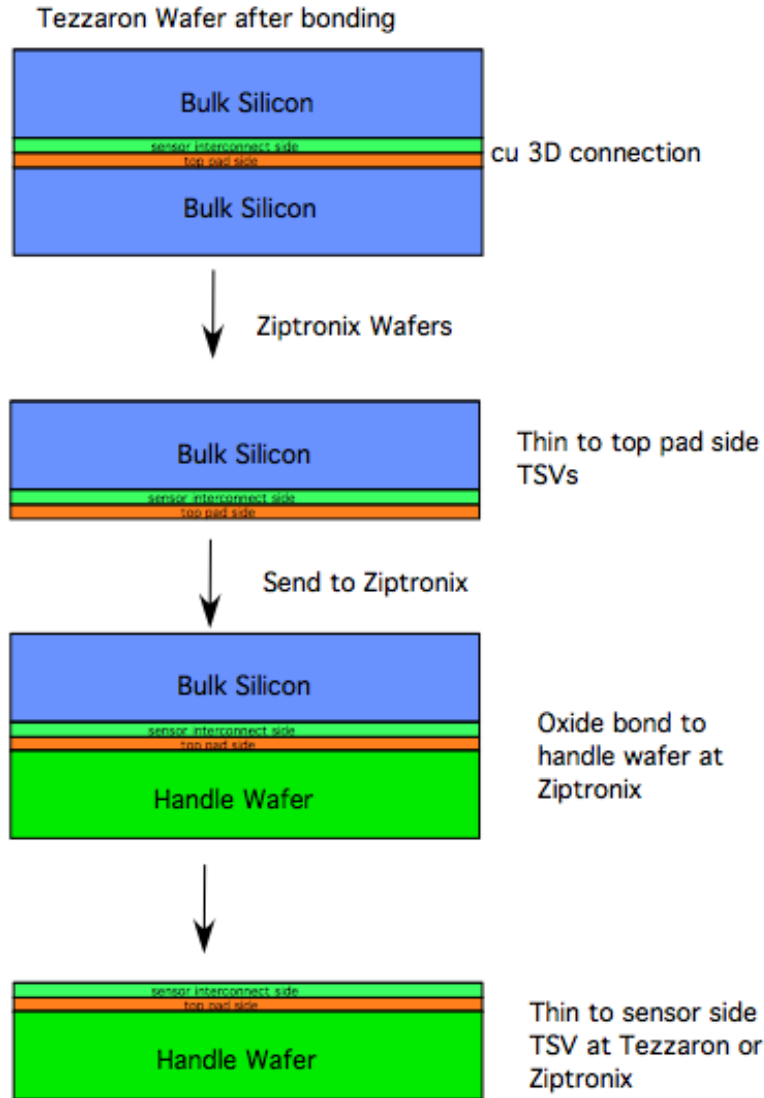
Detector Integration

The first, pre-series set of sensors have been fabricated at BNL

- CV, IV, topography look good
- One to FNAL for testing
 - $I_L < 3 \text{ na/cm}^2$
 - Bump bond tests



Detector Integration



Frame Layout



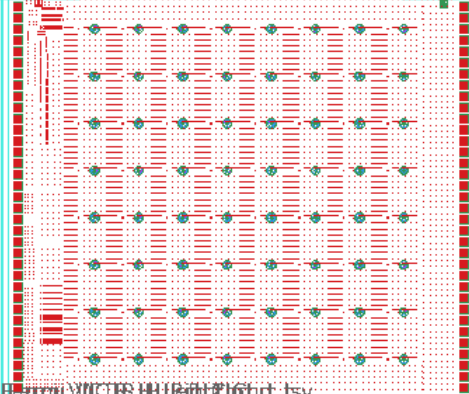
LHC short strip

LHC Long Strip

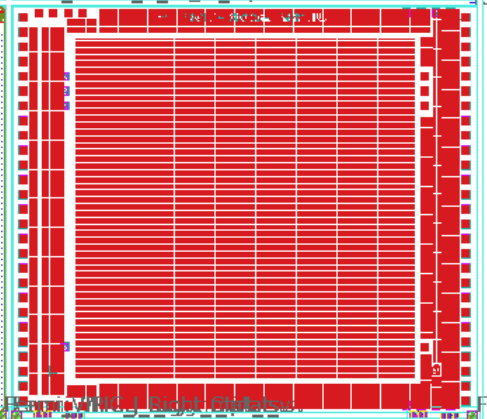
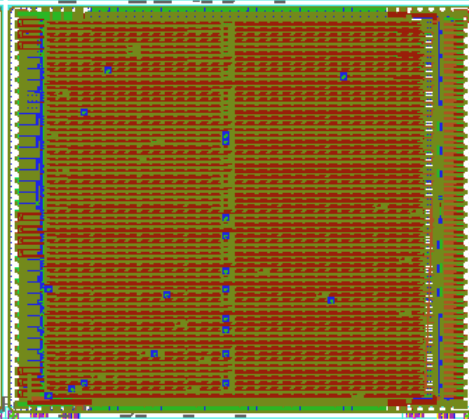
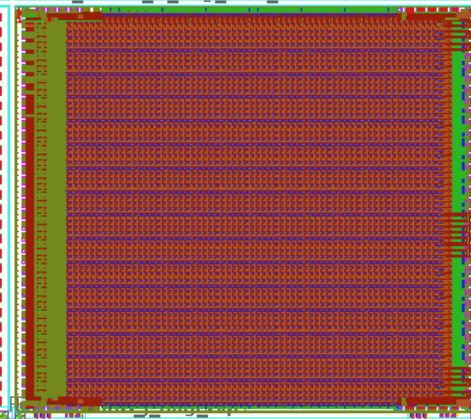
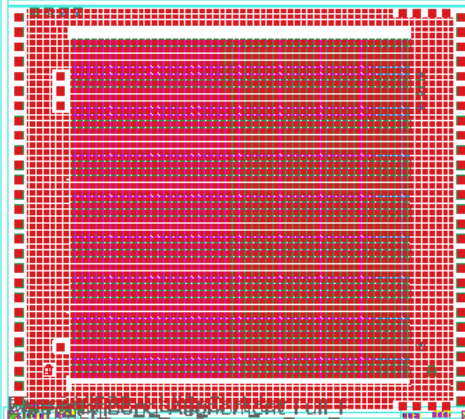
Ziptronix Stepper Alignment Fra



Ziptronix Stepper Alignment Fra



Ziptronix Stepper Alignment Fra



VIP2b sensor

X-ray imaging

X-ray imaging

VIP2b top

half_frame

SOI Work



SOI detectors utilize the “handle wafer” of an Silicon-on-Insulator device as a detector, with electronics mounted in the thin device layer on top of the “buried oxide”

- A truly monolithic device ... however:
 - The fields in the handle can act as a “back gate” to the topside transistors, shifting the characteristics and limiting the practical applied voltage.
 - The topside digital signals are in close proximity (200nm) to the sensor, causing unacceptable noise coupling.
- Possible solutions
 - Dual gated transistors with intrinsic shielding (American Semiconductor FLEXFET)
 - 3D assembly with minimal circuitry on sensor tier
 - Buried well structure to shield transistors and pixel

Mambo Chip – X ray Imaging

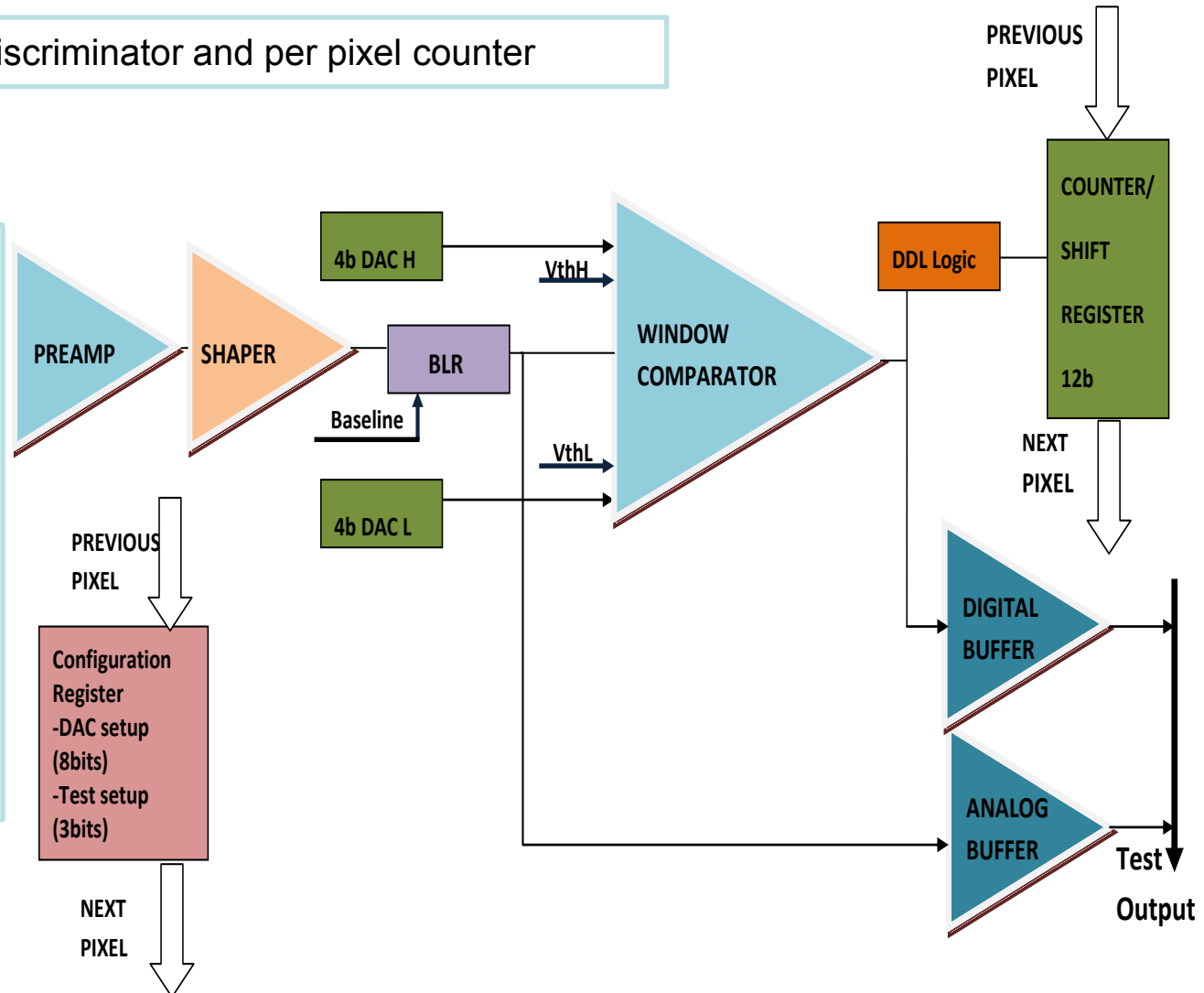
Test bed for SOI work – can be adapted to LC

MAMBO III and IV

pixel design with window discriminator and per pixel counter



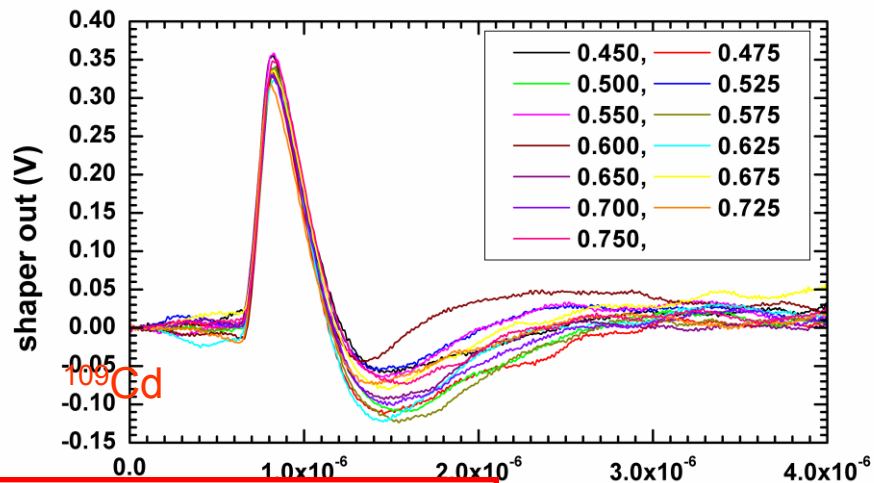
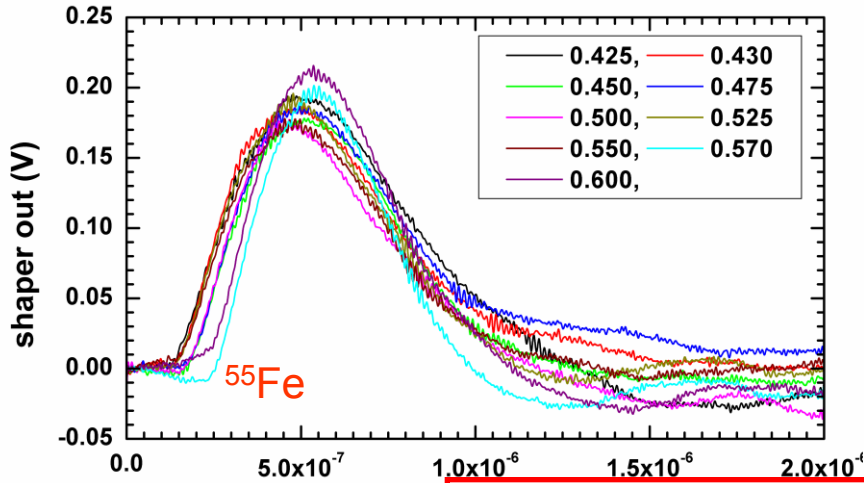
integrating CSA w/ p-z network, shaping filter CR-RC² with $\tau_p=200\text{ns}$; gain= $\sim 100 \mu\text{V}/e^-$, ripple counter reconfigurable into shift register, DACs for threshold adjustment, control logic for testability



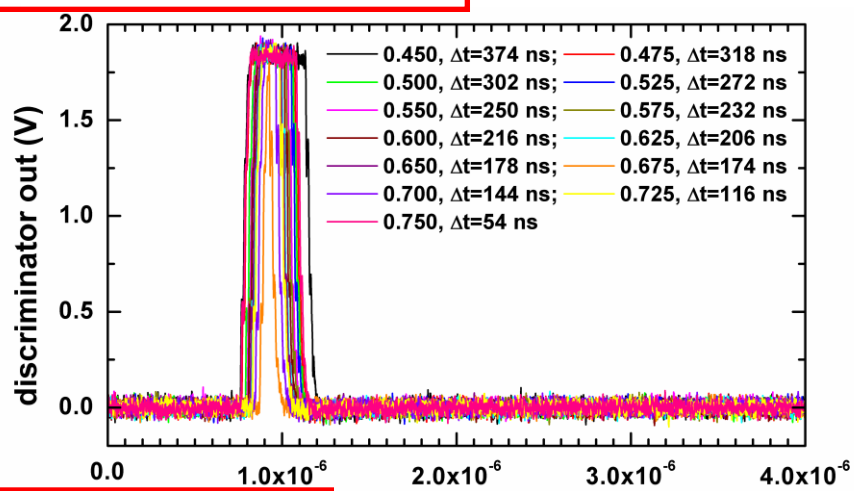
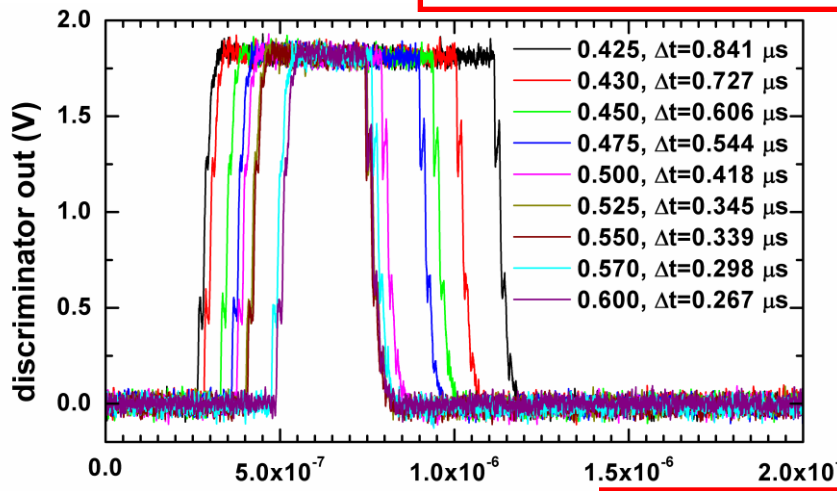
MAMBO II single pixel test



Monitoring of the shaper and discriminator outputs (transient signals)



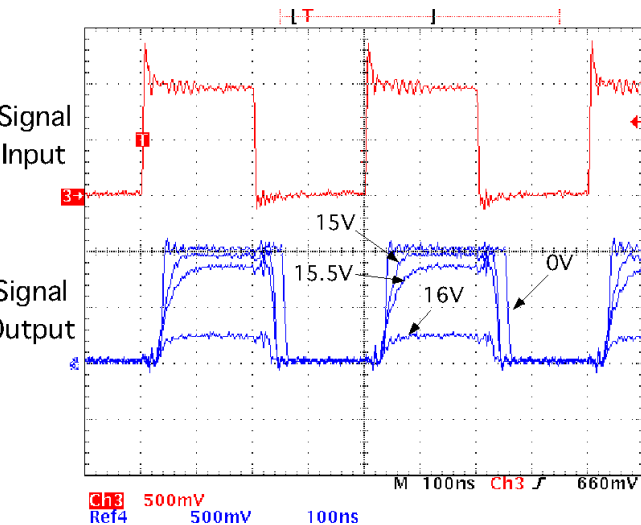
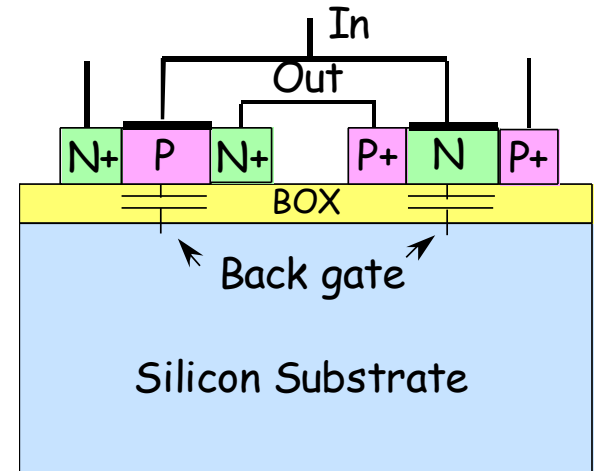
Discriminator at different thresholds



It seems to be OK but....

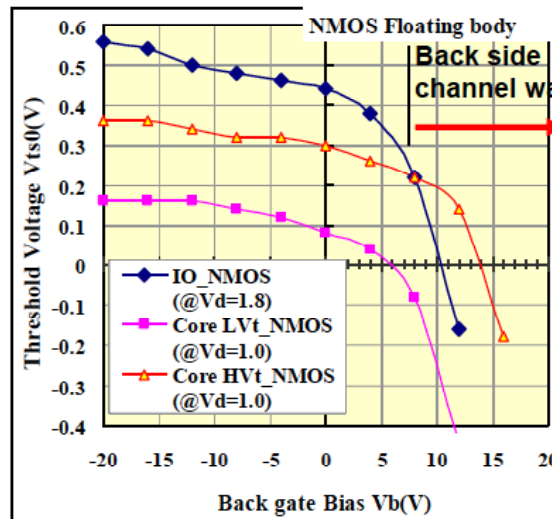
Backgate Effects

- Performance of SOI detectors is limited by:
 - mutual coupling between the electronics and the detector
 - charge injection due to swing of signals
 - shift of transistor characteristics due to detector bias and charge accumulation in BOX (radiation effects)

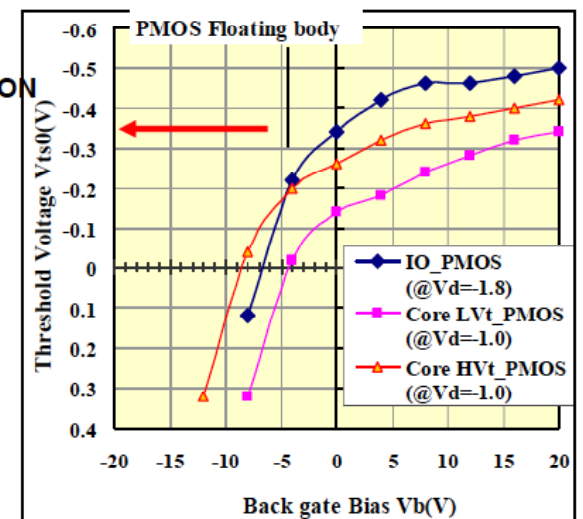


Signal disappears at $V_b \sim 16V$

NMOS transistor



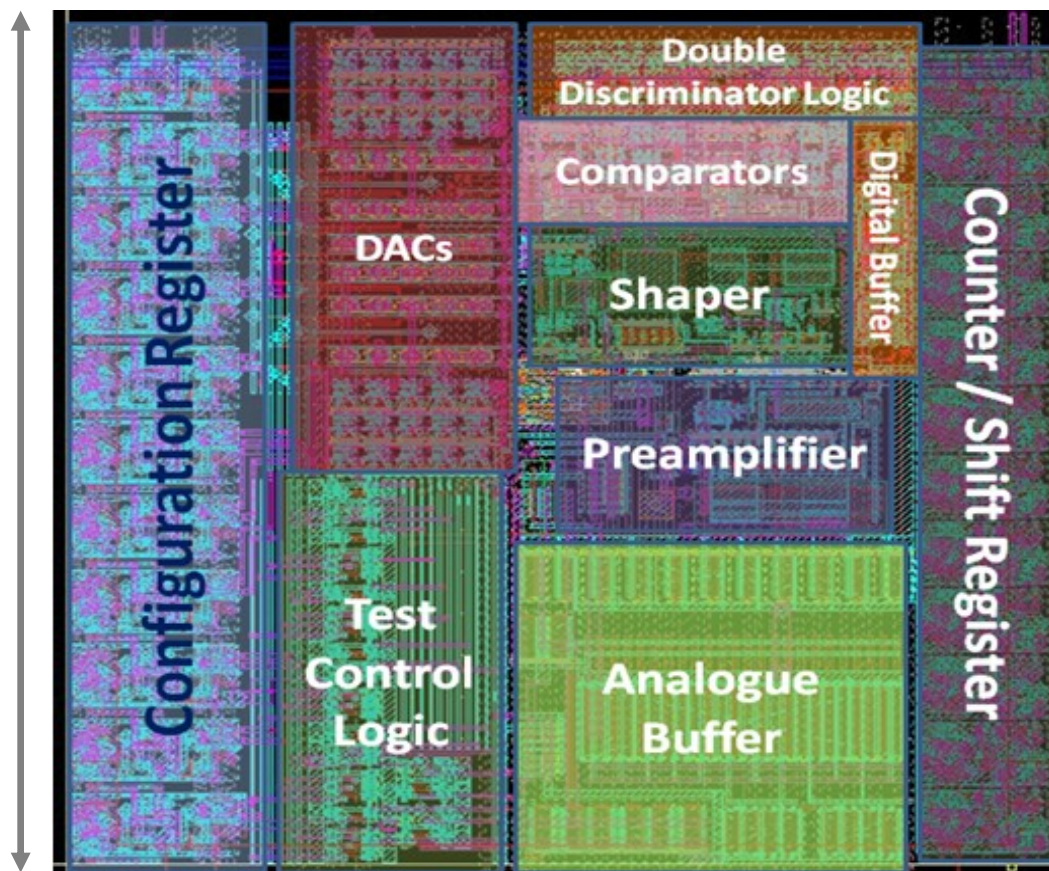
PMOS transistor



MAMBO III and IV, layout view



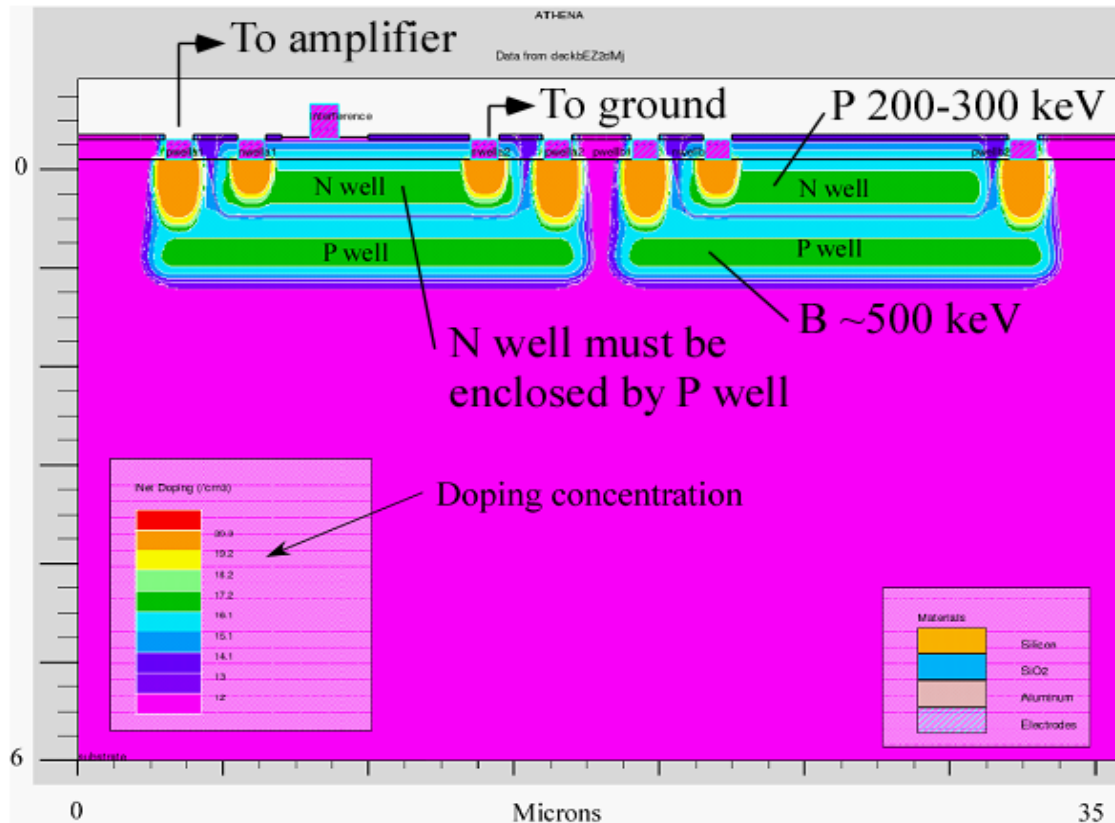
100 (105) μm



MAMBO 4



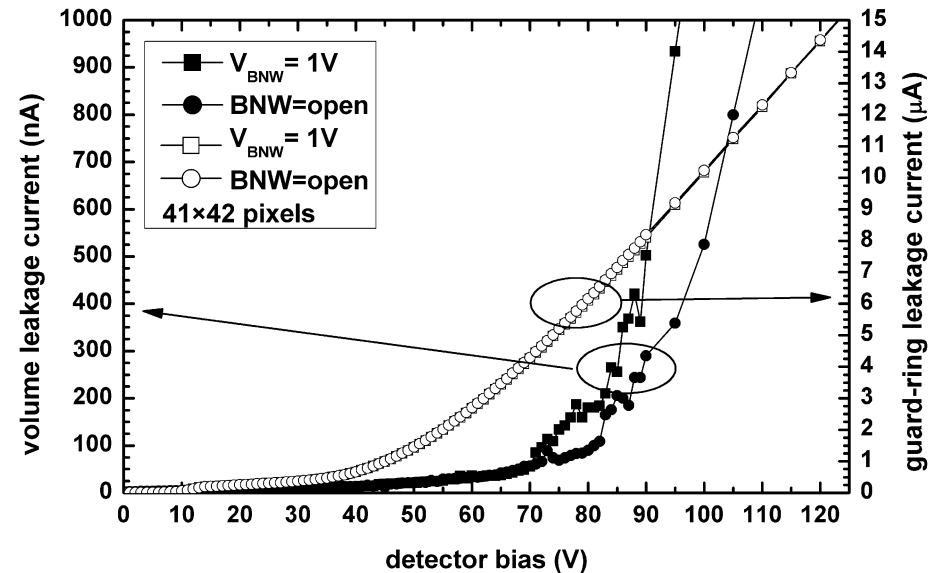
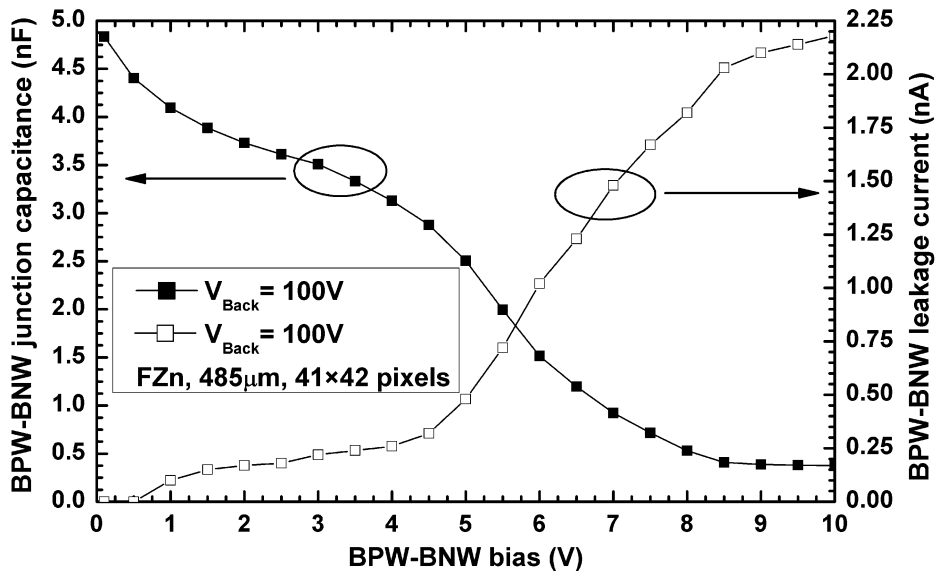
- explores nested well (BNW-BPW) on n-type substrate developed with OKI in August 2010
 - deep p-well to collect charge, shallow n-well at AC ground to shield,
- pixel $105 \times 105 \mu\text{m}^2$, ~ 950 transistors/pixel,
- 6 varieties of substrate material with and without nested BNW-BPW
- high resistivity FZn material – better quality



FZ Characterization



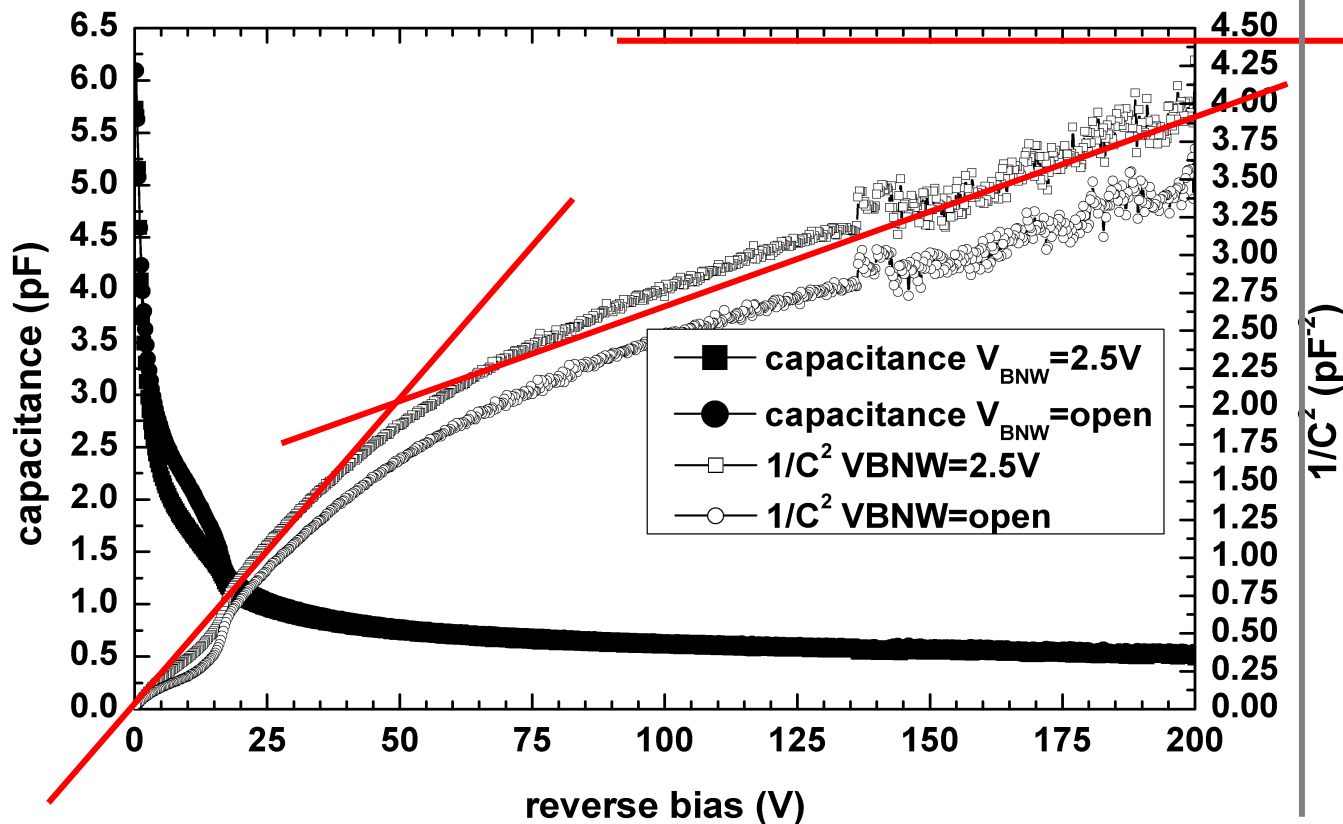
- Detector material FZn2, thickness=485 μ m
- Expected bias of BNW is ~ 1 or 2 V above BPW (not to affect V_T of FETs),
- Leakage current negligible ~ 100 pA/pixel,
- ΔX of BNW-BPW junction is $< 1\mu$ m thus $C_d = \sim 2$ pF/pixel (large !!! But it was predicted).
- pixel leakage current < 100 nA/cm²
- guardrings take most of leakage, probably edge of die current



MAMBO 4



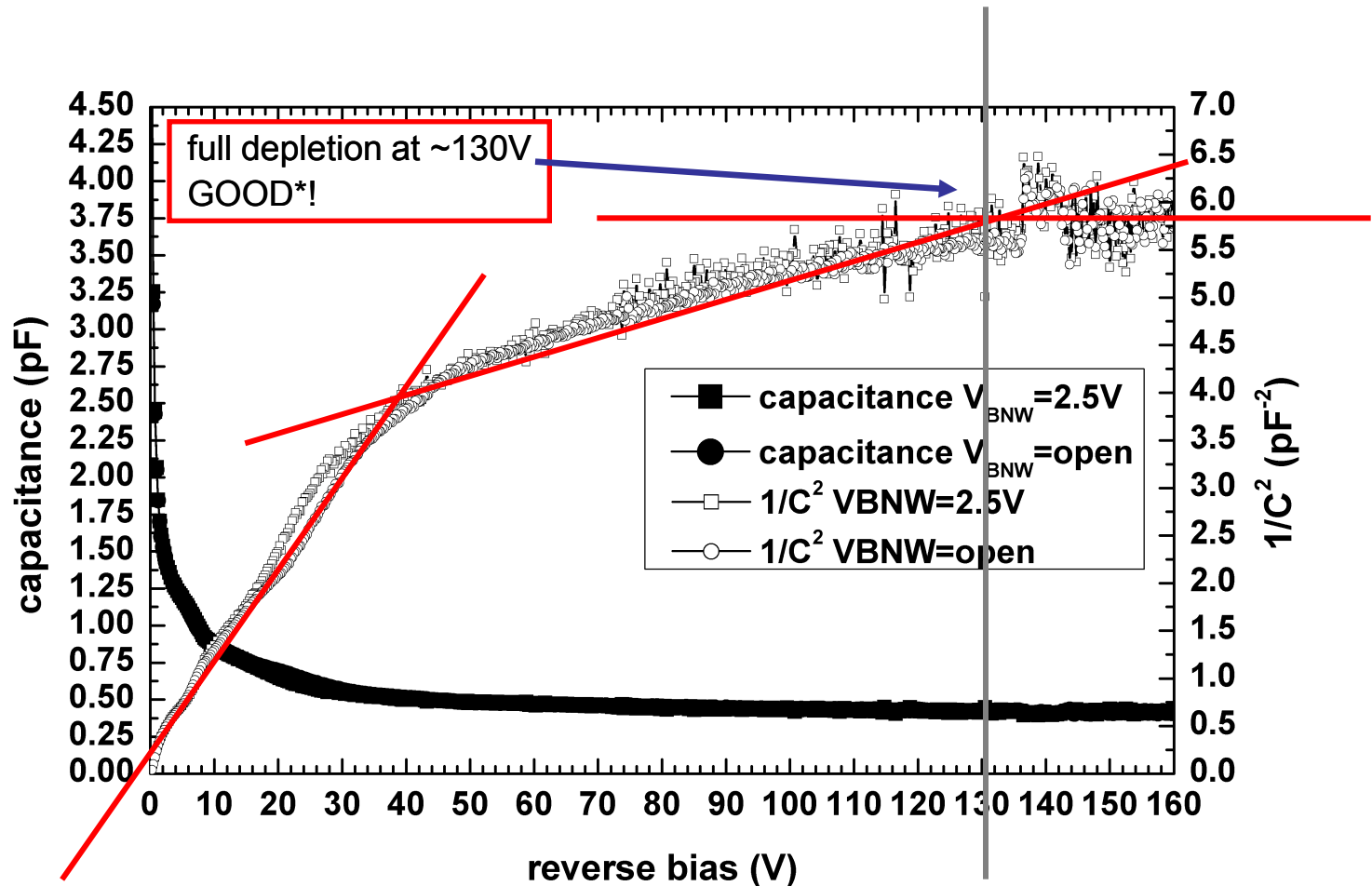
- HR1 substrate $< 1 \text{ kW/cm}$, $285 \mu\text{m}$ thick device (optical measurements)
- Test structure $900 \times 450 \text{ mm}^2$ BNW/BPW TEG - C/V $f=100 \text{ kHz}$



Float Zone Substrate



- FZn substrate $\sim 7.1 \text{ kW/cm}$, 485 mm thick device (optical measurements)
- test structure $900 \times 450 \mu\text{m}^2$ BNW/BPW TEG - C/V $f=100 \text{ kHz}$



OKI Development Plan

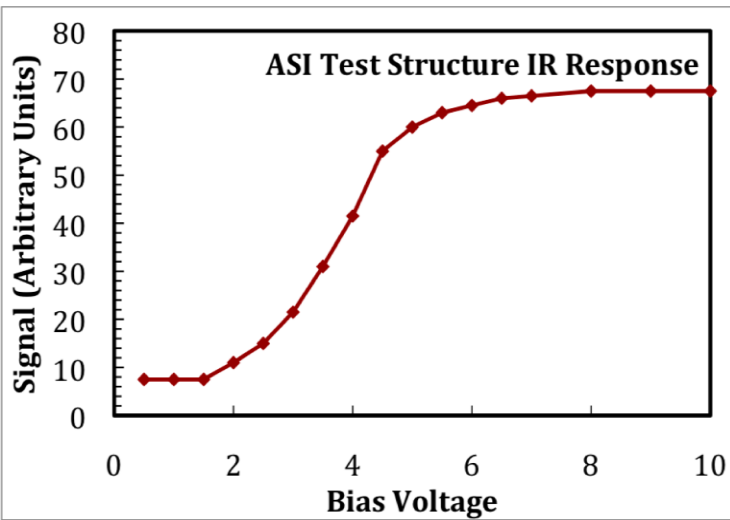
- We can now fully deplete a thick detector without tuning off the topside transistors
- The successful BPW/BNW run will be taken as a baseline for further development
 - Optimize BPW and BNW depths to minimize pixel capacitance
 - Can use higher energy implant to separate wells
- Next version will be a “large area” 1 x 1 cm chip
- Use laser anneal process to process backside
 - Thin to 50-100 microns
- Stitched arrays



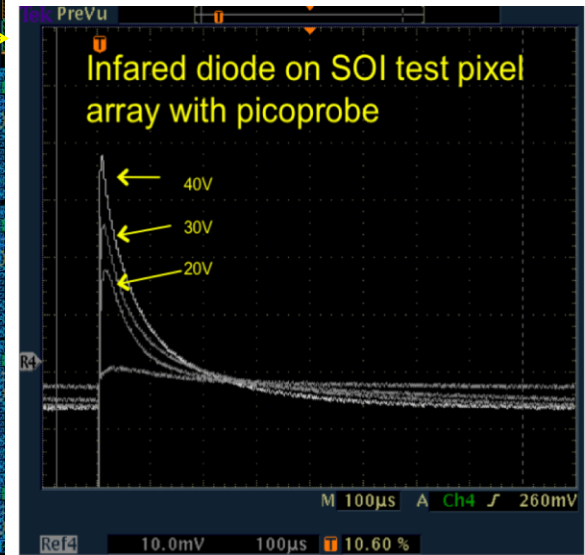
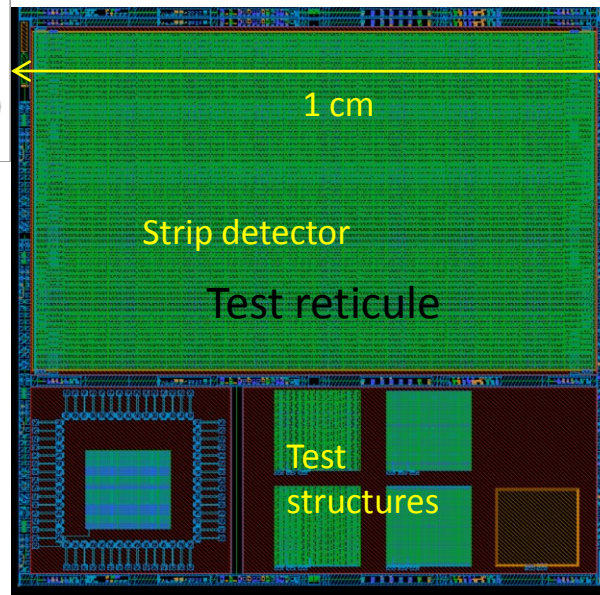
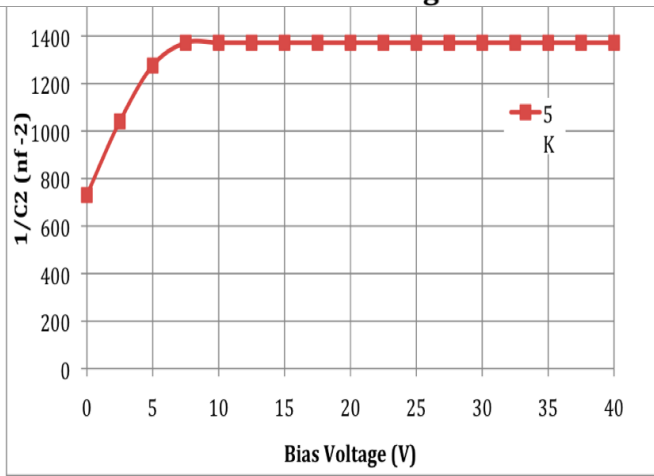
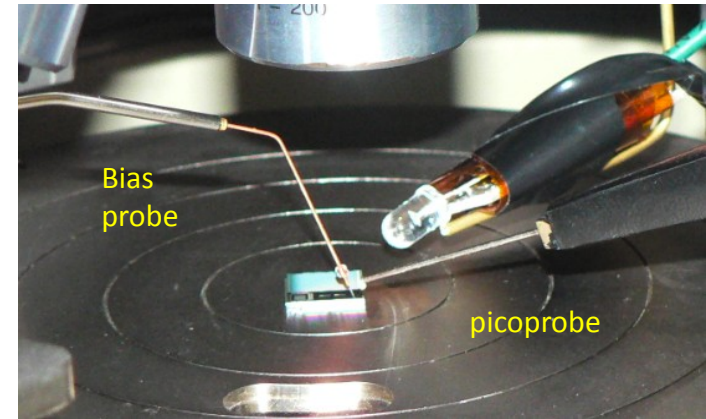
Backside Processing



- We have previously developed a process to take an SOI wafer,
- thin the sensor to 50 microns, and implant and laser anneal the backside.
- Demonstrated with American Semiconductor wafers



Signals measured directly using Pico probe and 1060nm diode



Conclusions



Substantial progress and some real breakthroughs

- 3D multiproject chips being tested
- 3D process commercialized
- SOI process developed which is robust against backgate effects and digital to analog coupling.
- First detector test with electronics integrated with float zone silicon

I believe that we would be ready to proceed to full-sized fully functional devices in either SOI or 3D. Both the circuit design and chip/sensor technology has become mature enough for full scale prototypes.

There is no funding and no pressing need to do this – we intend to proceed with technology development with x-ray, LHC and perhaps B factory applications. We intend to turn back to ILC/CLIC/muon collider applications when the time scales become clearer.

Much of this work is in close collaboration with KEK and OKI/Miyagi. Our best wishes go out to our colleagues affected by the earthquake and tsunami.