The Bean: BeamCal Instrumentation ASIC

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March 20th, 2011

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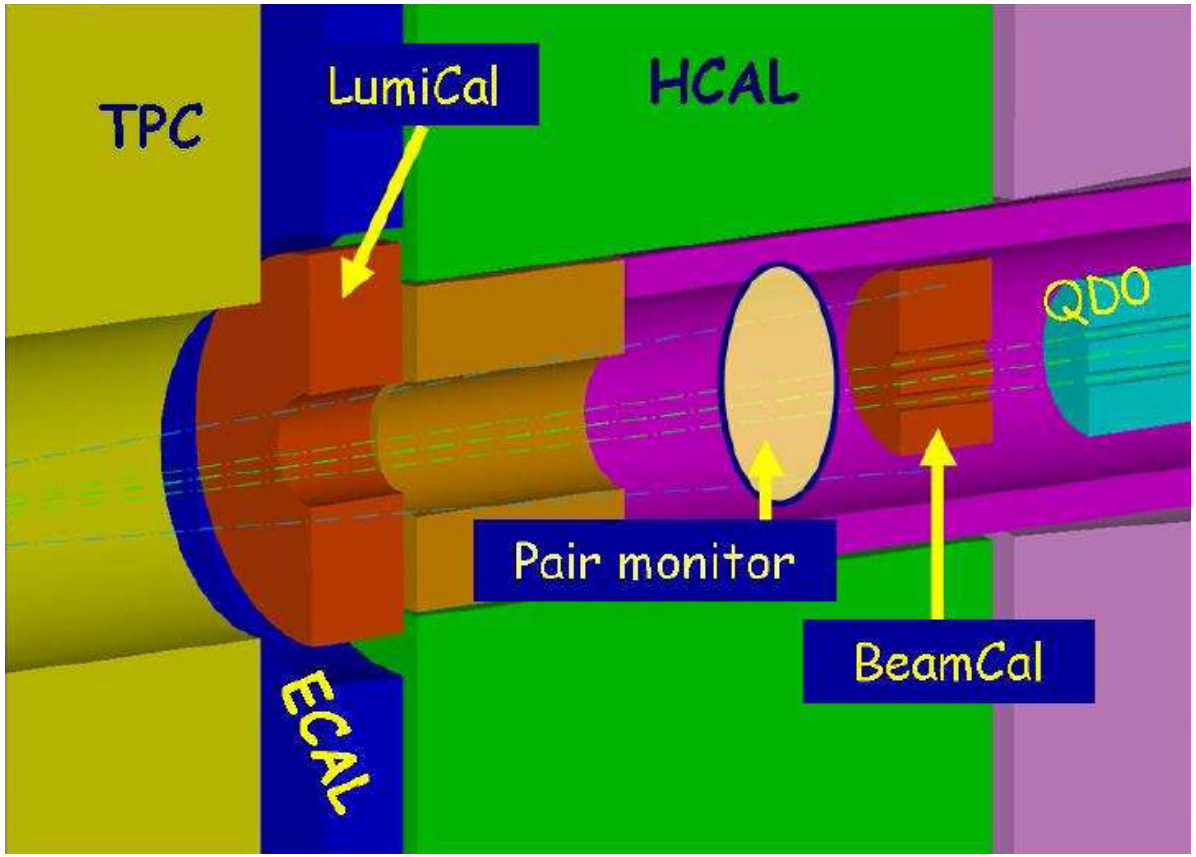
Outline

- Introduction
- The Bean Design
- Test Results
- Conclusion

Introduction

Context: Instrumentation for the Very Forward Region of the ILC

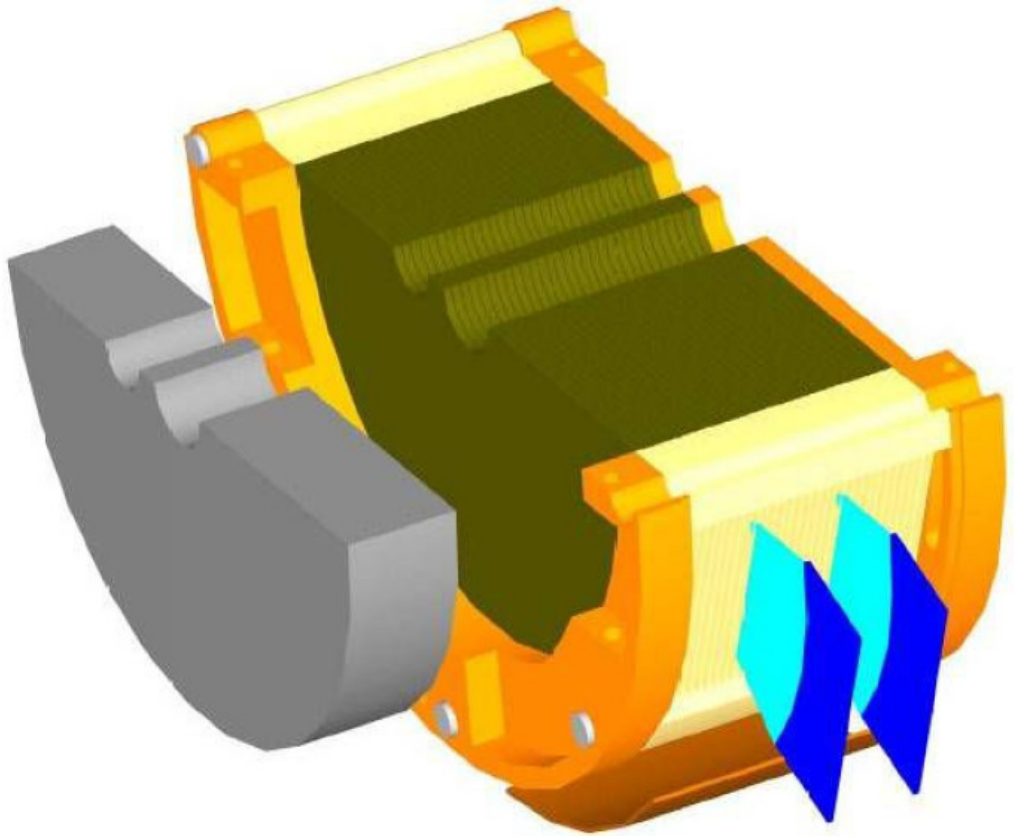
- Four sub-detectors:
  - LumiCal
  - GamCal
  - **BeamCal**
  - Pair-monitor



http://www-zeuthen.desy.de/ILC/fcal/

The BeamCal Calorimeter

- 30 layers, 45360 pixels per side
- BeamCal mission
  - Extend the calorimeter to small polar angles
  - Reduce backscattering from pairs into the detector center
  - Provide a low latency output for beam tuning



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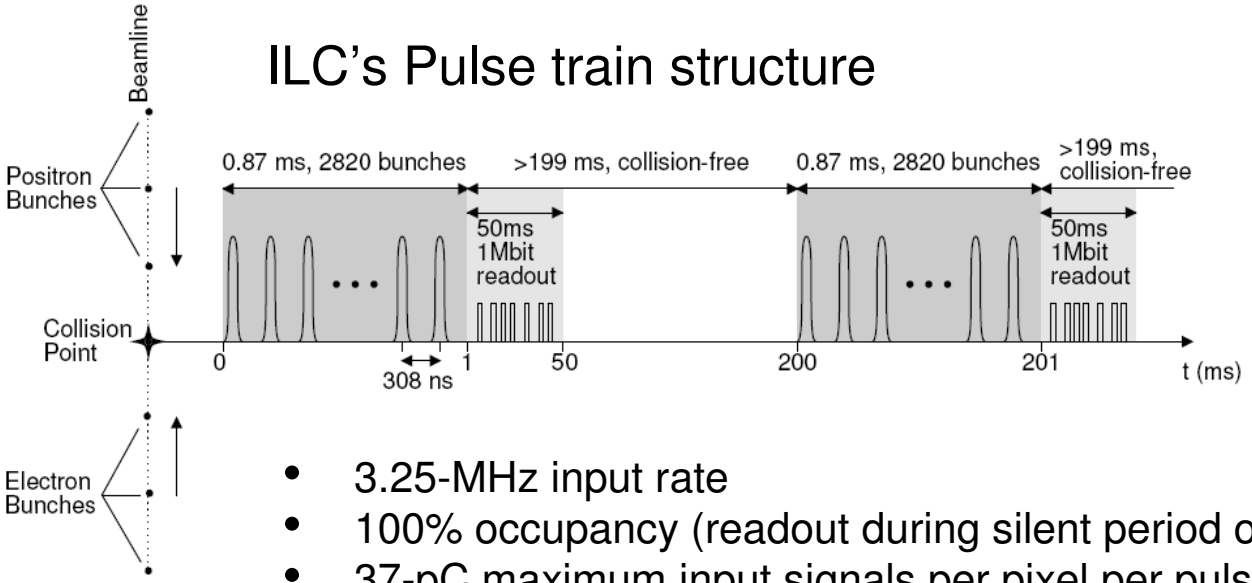
BeamCal Instrumentation ASIC Specs

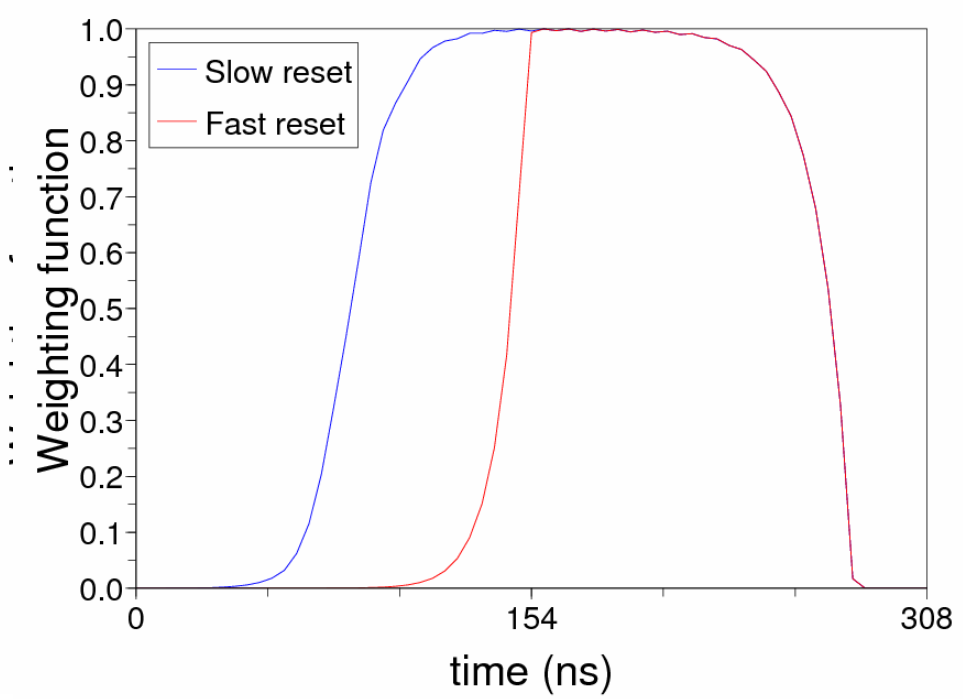


- 3.25-MHz input rate
- 100% occupancy (readout during silent period of pulse trains)
- 37-pC maximum input signals per pixel per pulse[1]
- 40-pF input capacitance[1]
- 10-bit resolution
- Dual gain (50x) for different modes of operation: standard data taking (SDT) and detector calibration (DCal)
  - SDT: large input signal; slew rate, bandwidth and adder challenges
  - DCal: smaller input signal; noise, baseline restoration and linearity challenges (tighter design space)
- 32 channels per chip
- Full-chip output (8-bit, 1-μs latency) for beam diagnostics
- Radiation tolerance to 1 Mrad total dose

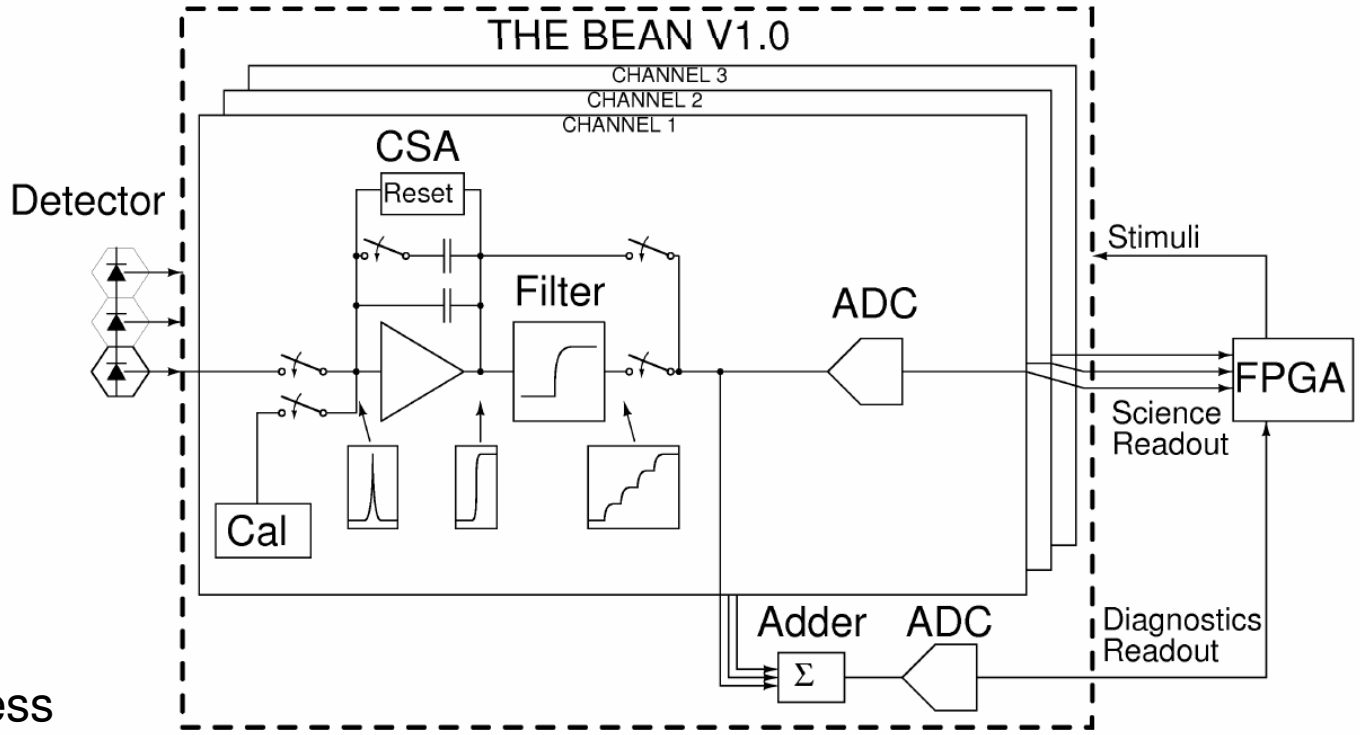
1: This specification depends on the final detector design

Low Noise Design Considerations

- 308 ns period → noise dominated by series component
  - Must limit weighting function slopes
- CSA bandwidth suffices for limiting negative slope
- Two choices to limit positive slope:
  - CDS
  - **Slow reset release**

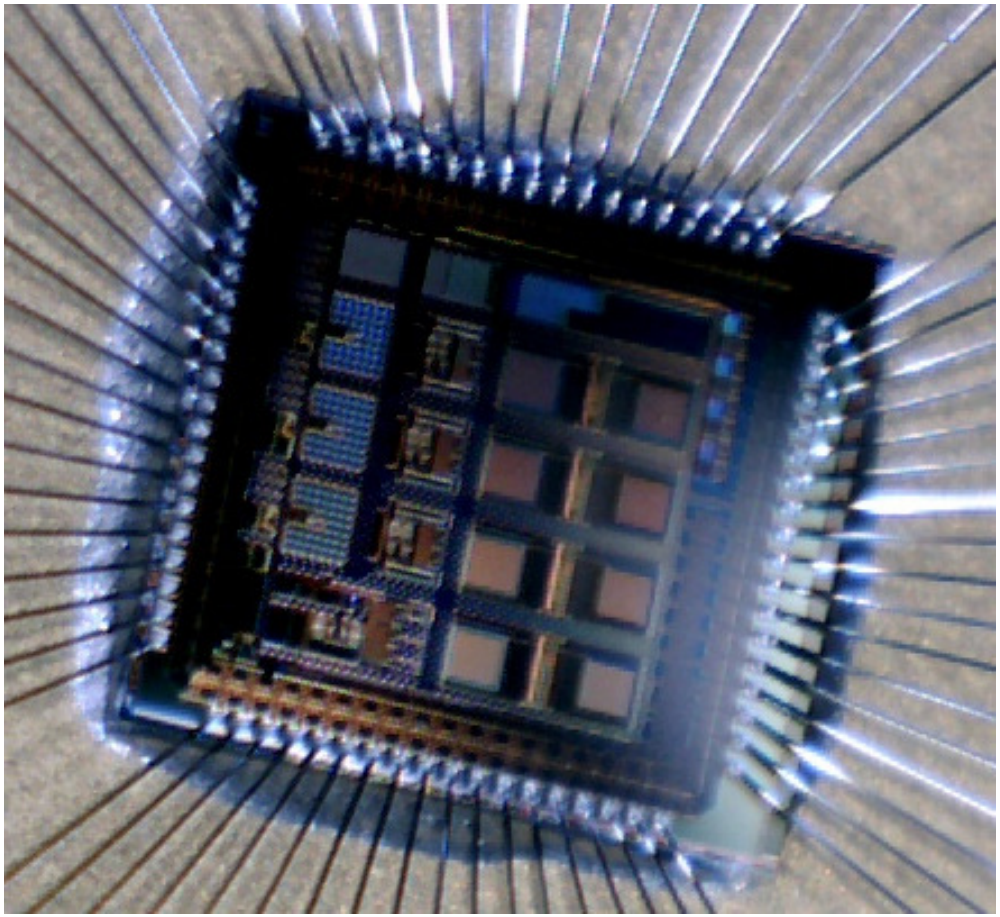


The Bean Prototype: System-Level Design

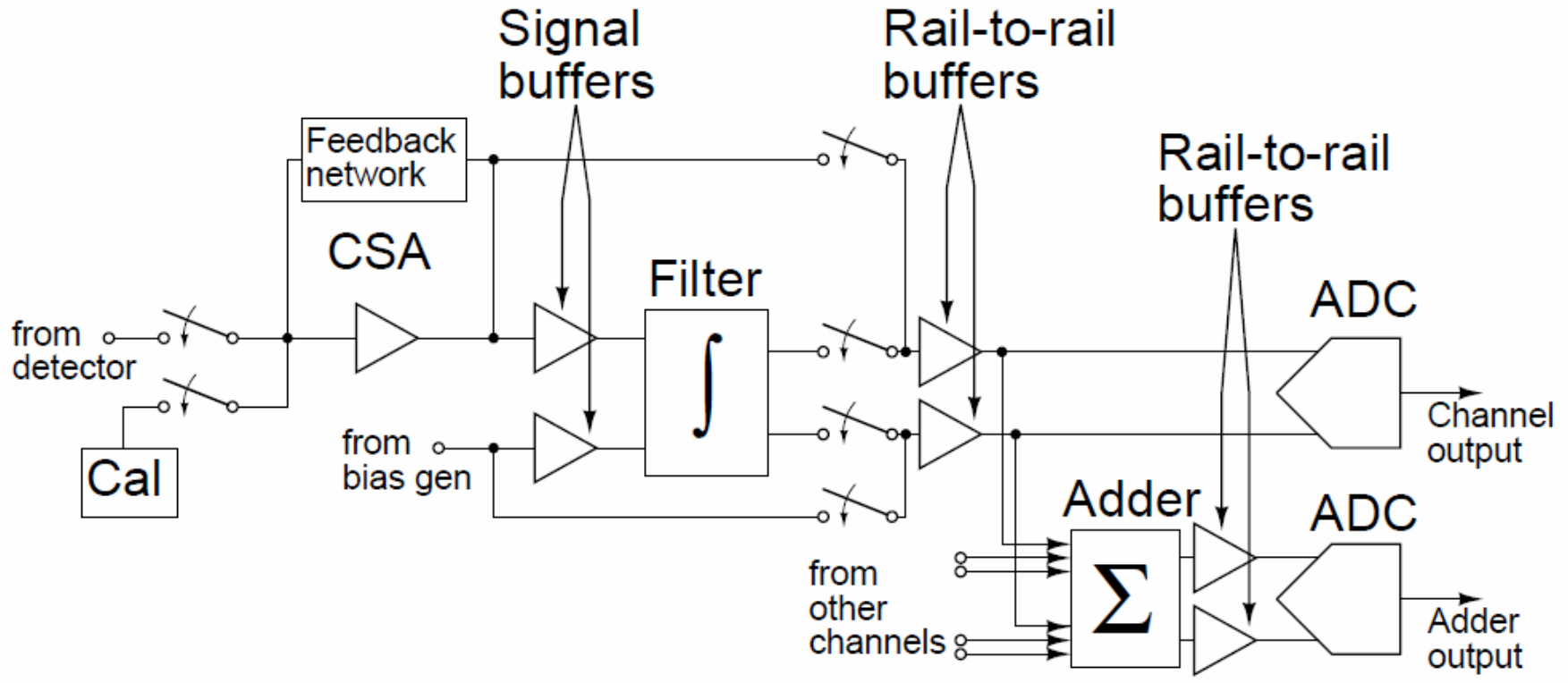


- 180-nm TSMC process
- Fully independent channels
- Digital memory to store 32 channels x 2820 x 10-bit results per ASIC
- Precharge circuit for the charge-sensitive amplifier (CSA) to maximize output swing
  - CSA precharger doubles as on-chip pulser for electronics calibration
- SC adder followed by a dedicated ADC
- Gated reset for quick baseline restoration
  - This has noise consequences in DCal mode

The Bean Design

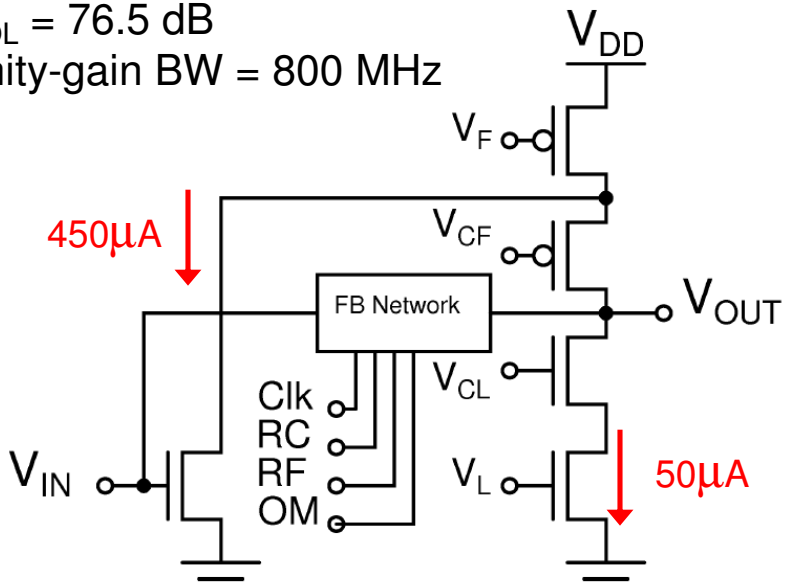


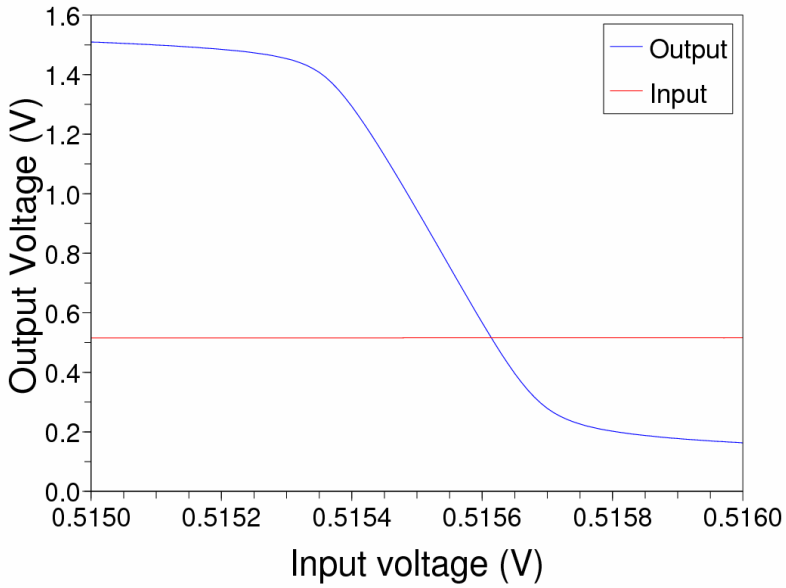
The Bean Detailed Block Diagram, Single Channel



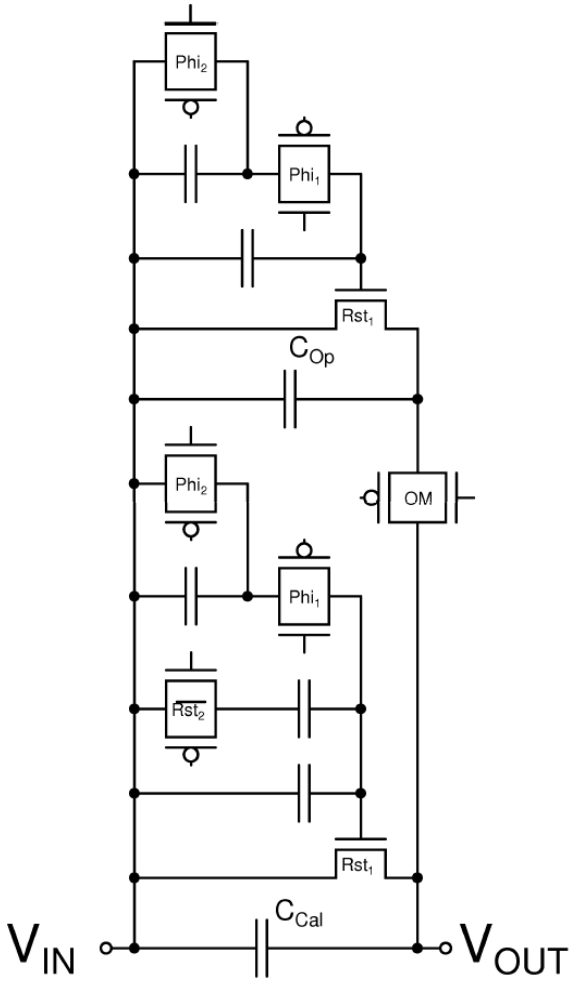
CSA & Feedback Network

A_{OL} = 76.5 dB
Unity-gain BW = 800 MHz

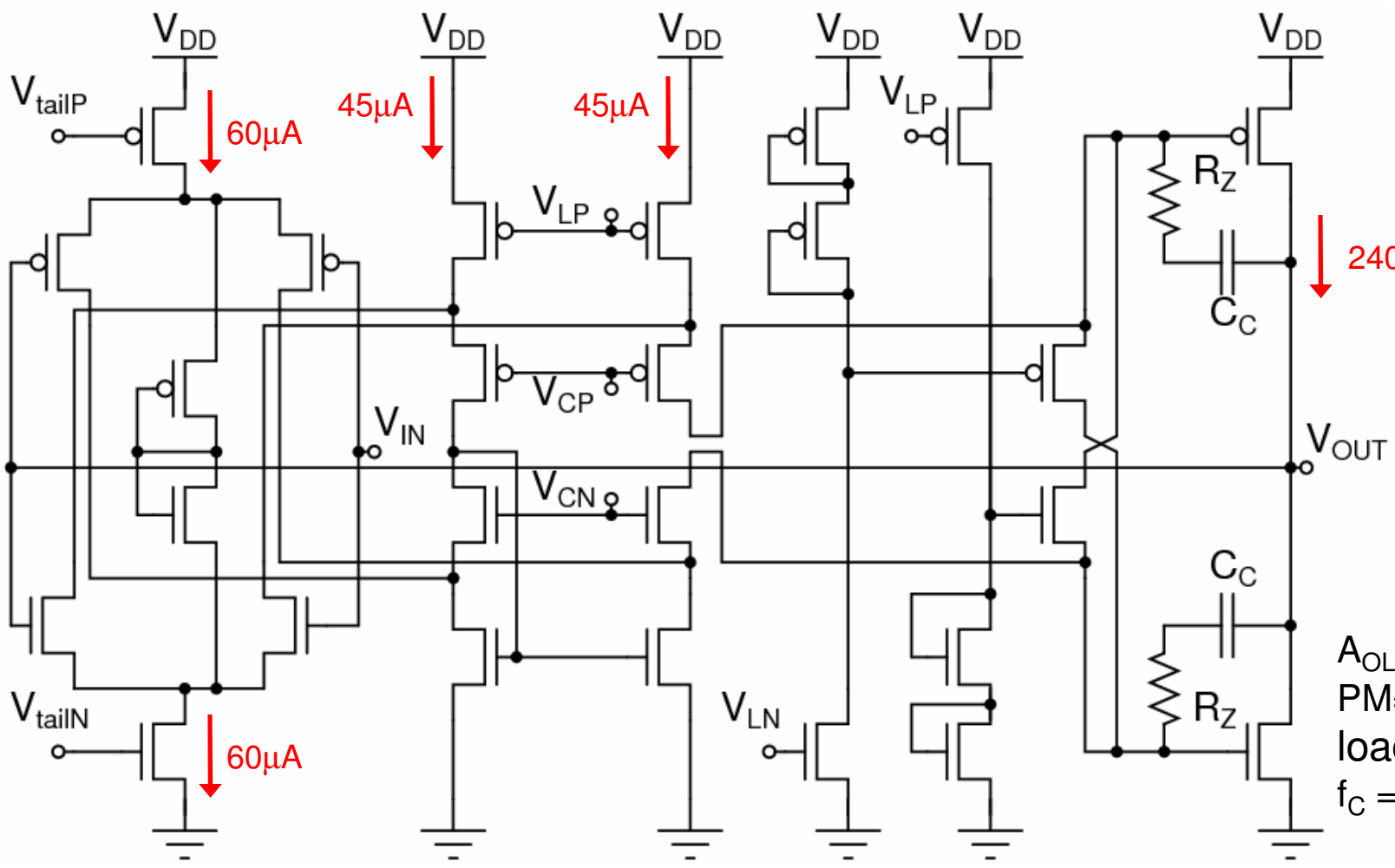




Feedback network



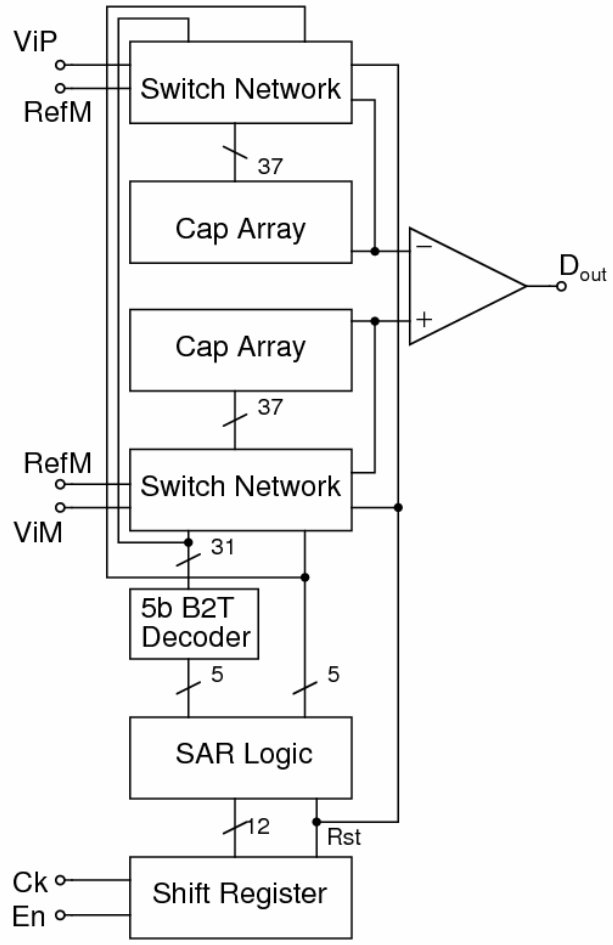
Rail-to-Rail Buffers



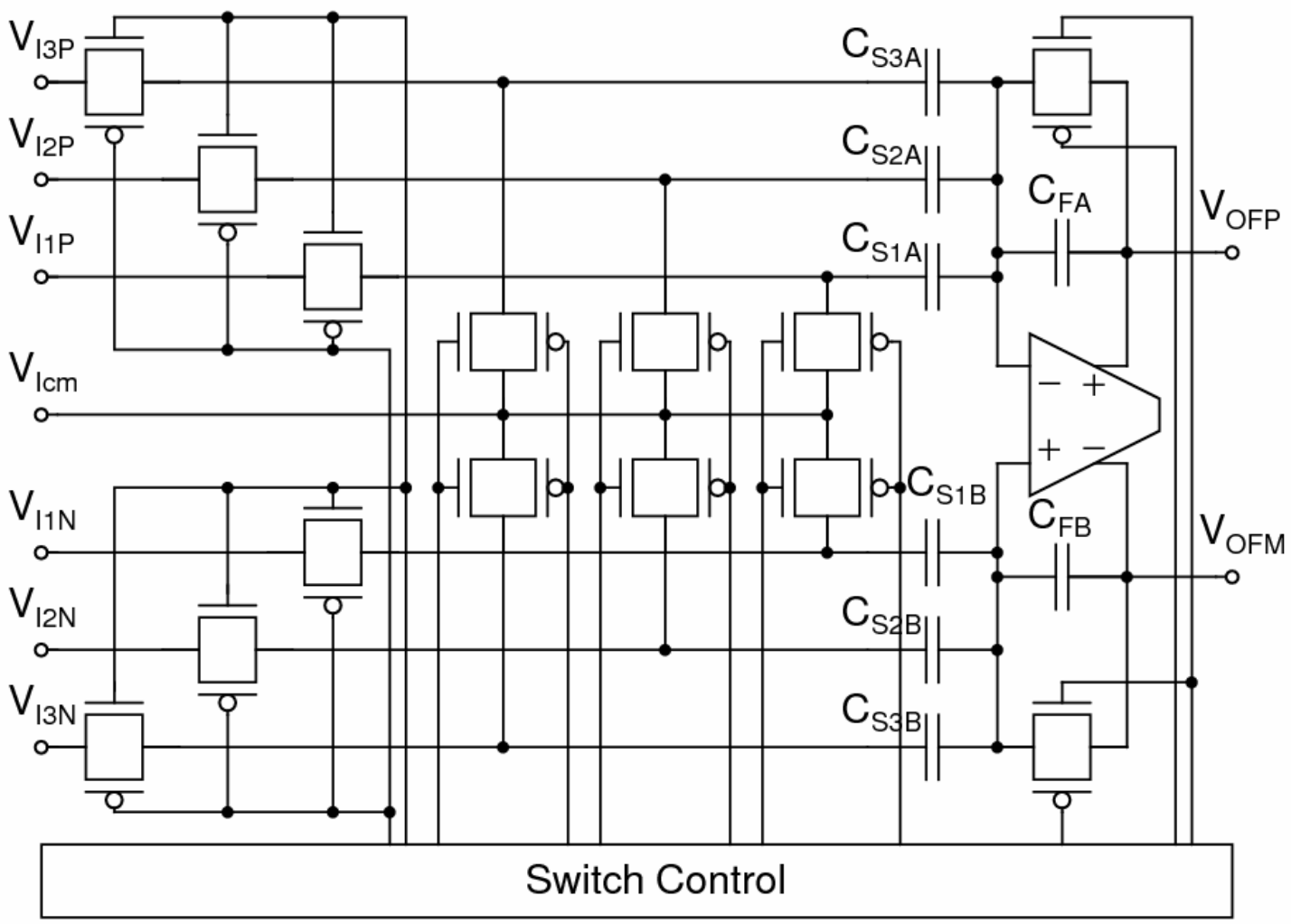
A_{OL} = 101.6 dB
PM=80.3° (8 pF load)
f_C = 49 MHz

10-bit SAR ADC

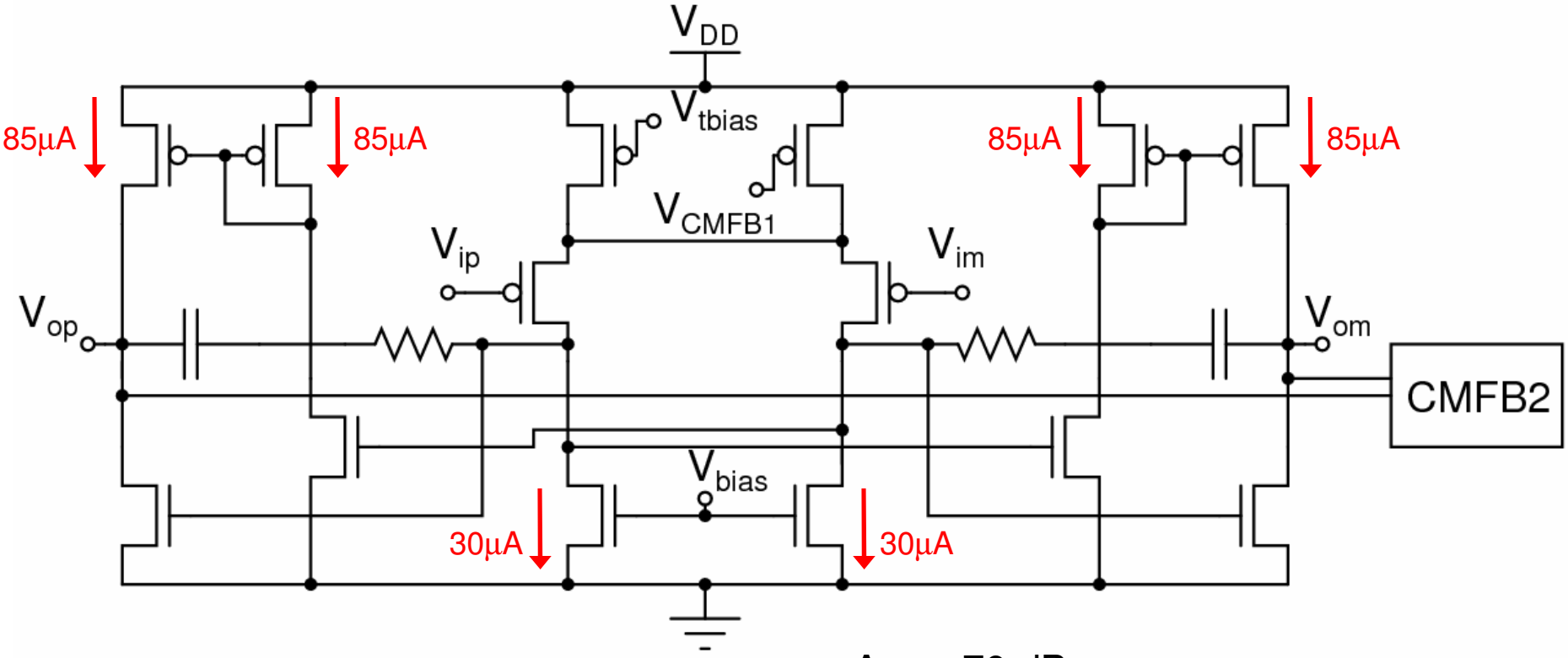
- Fully differential SAR architecture
- 16-fF MIM unit capacitances
  - 2-fF MOM unit cap ADCs were designed and successfully tested, too
- 5 bits thermometer-coded, 5 bits binary-coded
- P_{AVG} = 200 μW @ 3.25 MS/s



Switched-Capacitor Adder



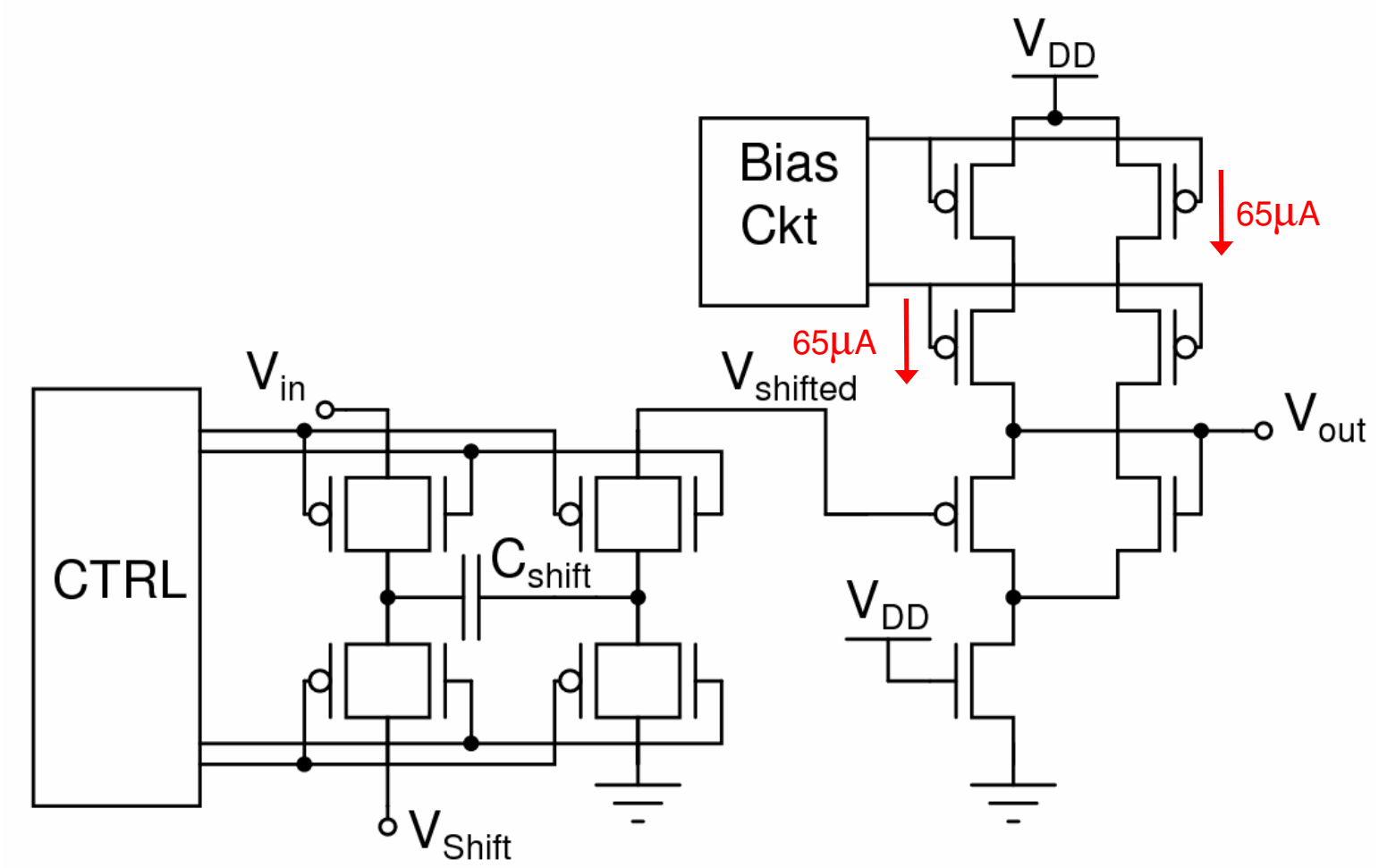
Amplifier for Switched-Capacitor Circuits*



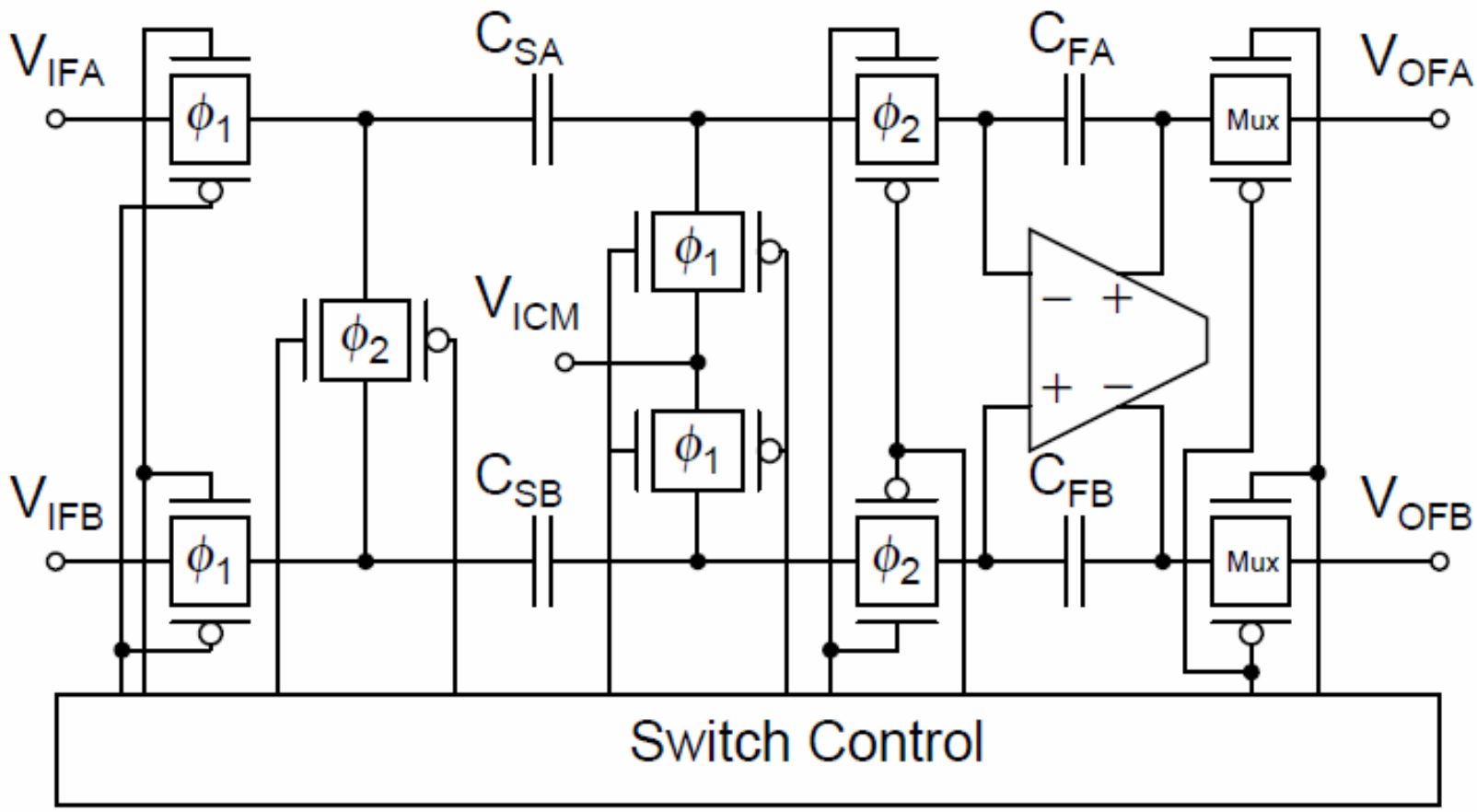
A_{OL} > 70 dB
PM = 83° (integrator configuration)
f_C = 144 MHz

* Rabii, S. et al, JSSC, Jun 1997

Signal Buffer and Level Shifter



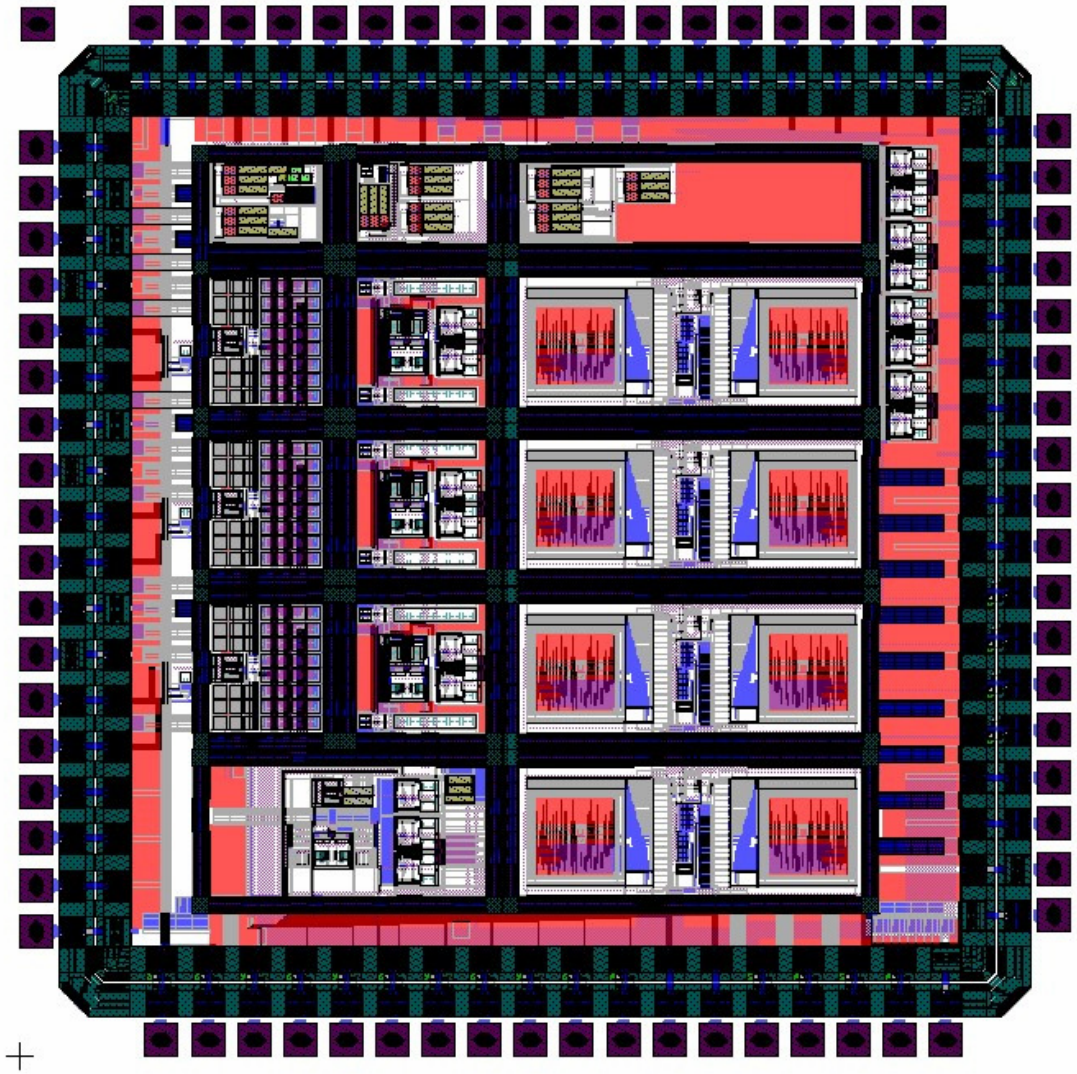
Switched-Capacitor Integrator



P_{avg} = 850μW

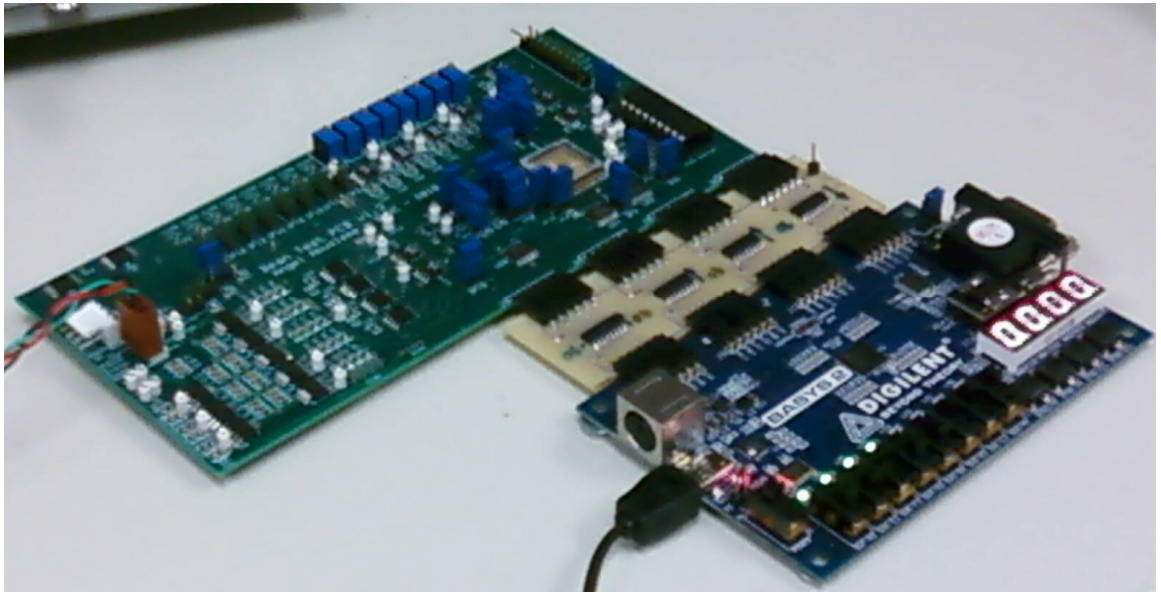
*Reset transistors not shown

The Bean Prototype: Layout



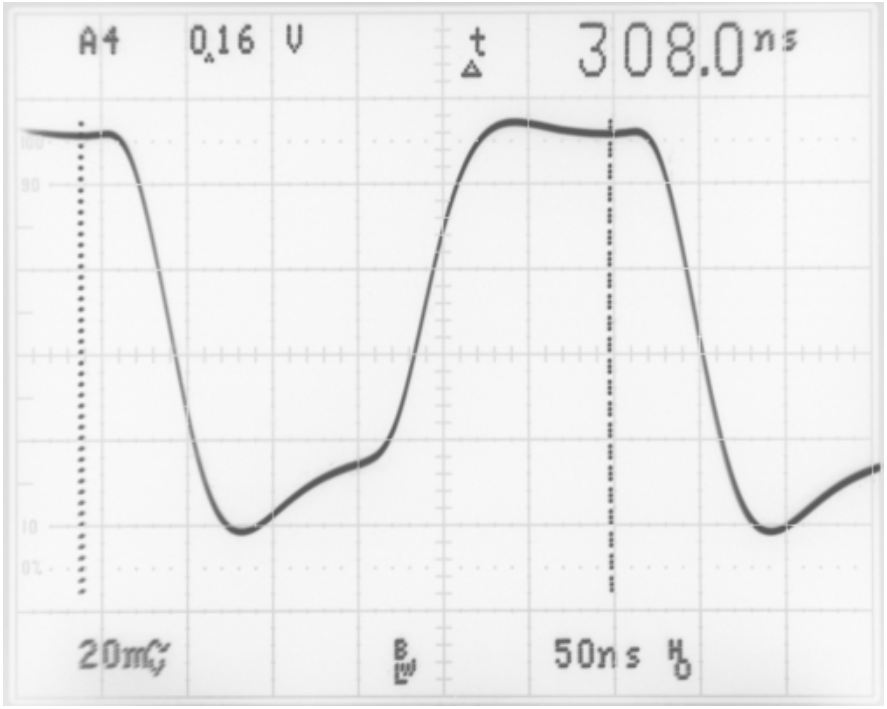
- 72 pads, 2.4mm x 2.4mm (including pads)
- 7306 nodes, 35789 circuit elements
- 360-µm channel pitch (including power bus)
- 3 charge amplifiers, 4 x 10-bit, fully diff. SAR ADCs, 1 SC adder, 3 SC filters, etc.

Test Results

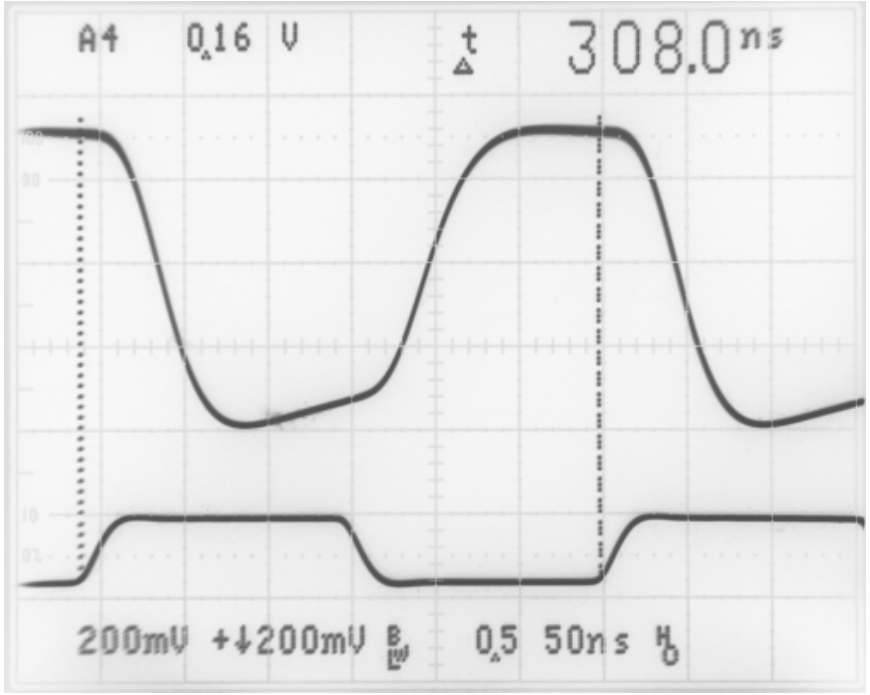


Functionality Test: Waveforms

CSA Output, standard data taking
Nominal speed

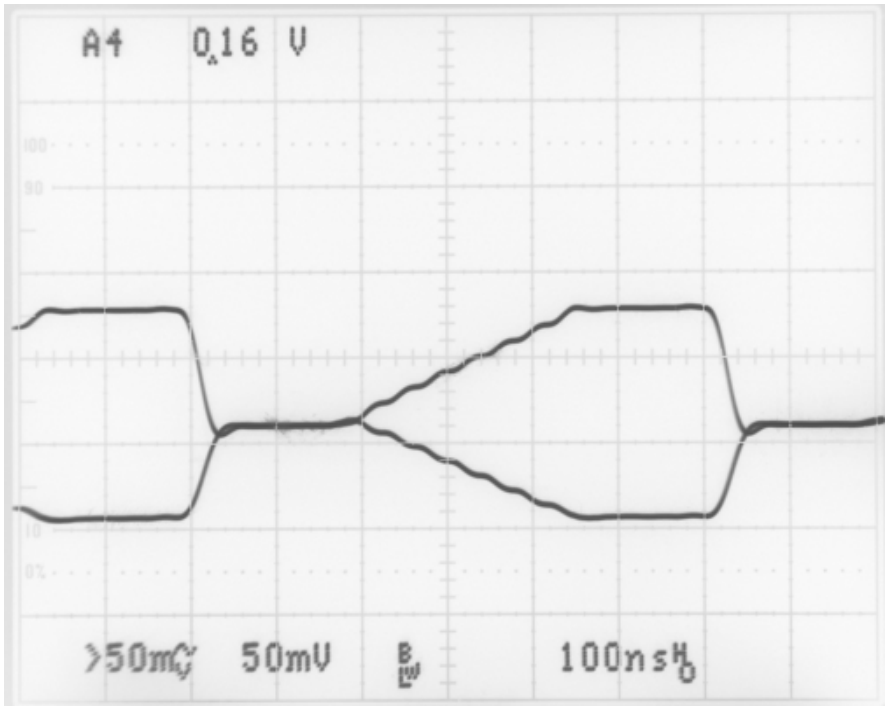


CSA Output and reset signal,
Calibration mode,
Nominal speed

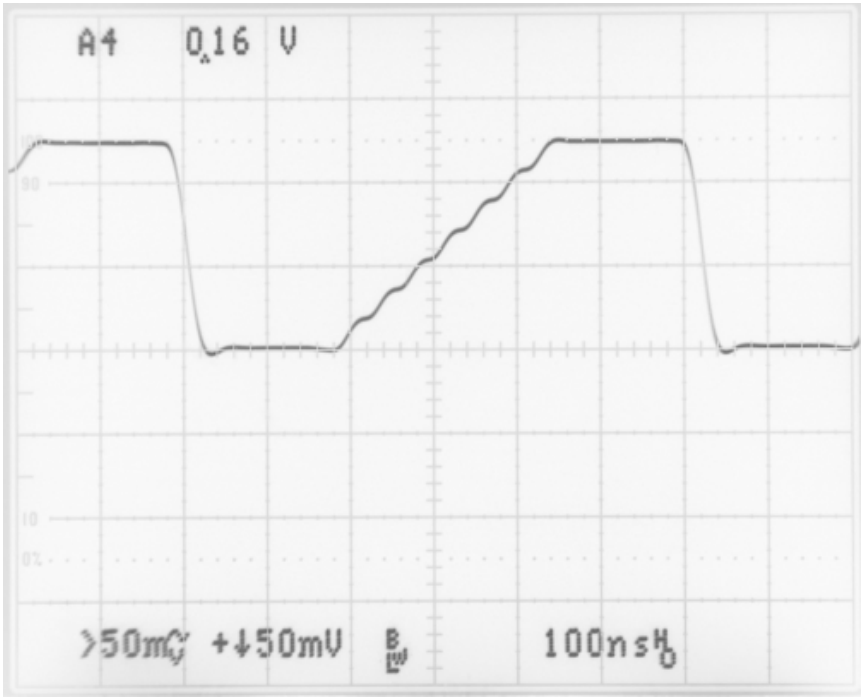


Functionality Test: Waveforms

Filter output, single ended
½ speed

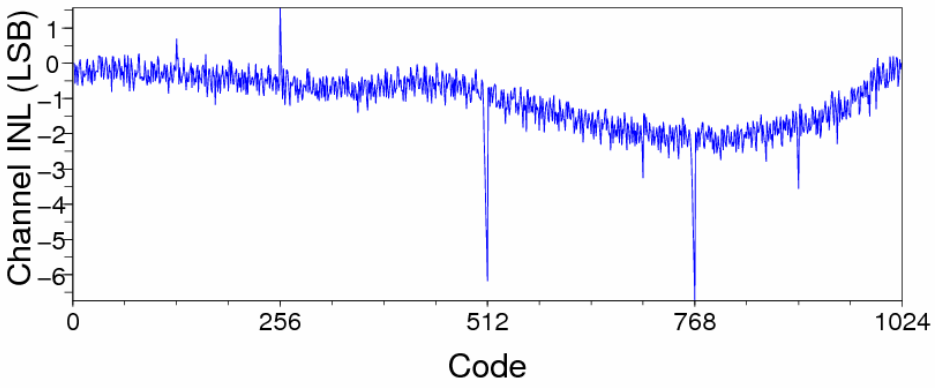


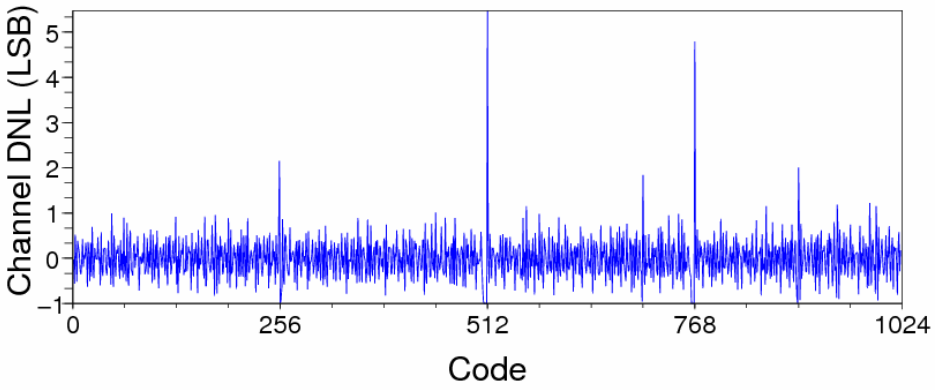
Filter output, fully differential
½ speed



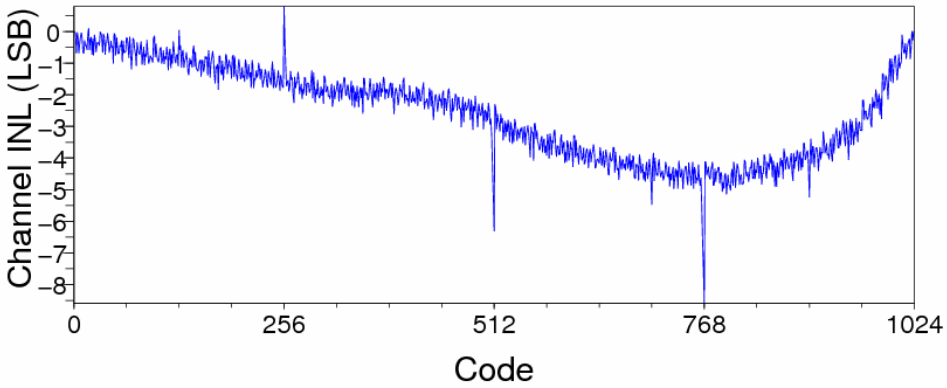
Linearity Test Results, SDT Mode

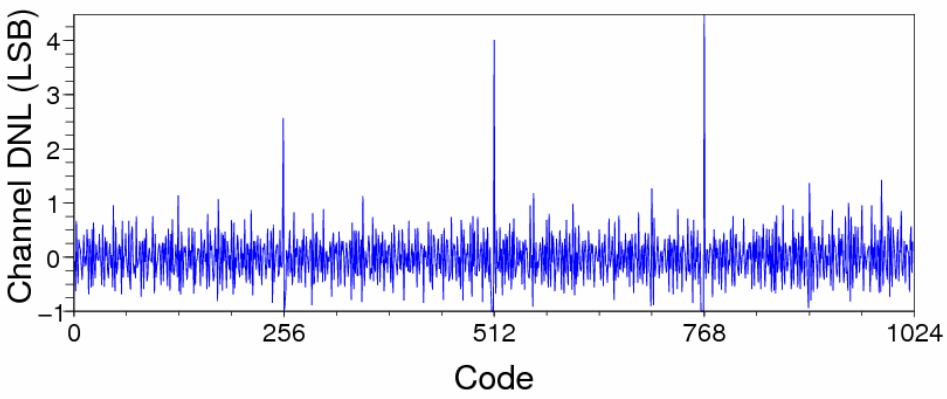
0 - 37pC input range





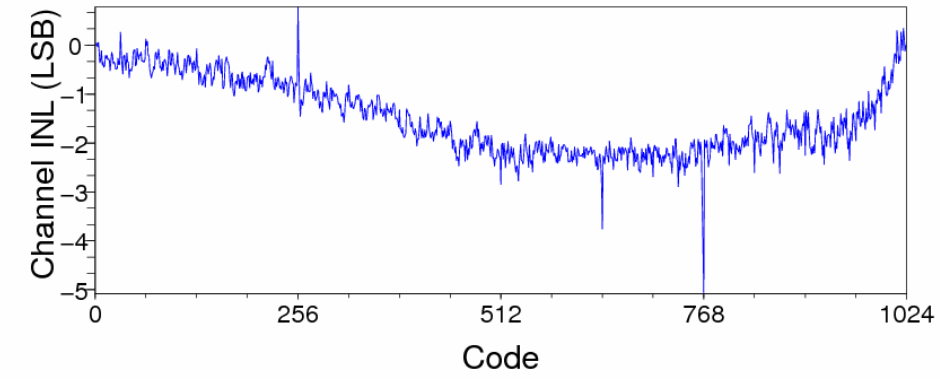
0 - 40pC input range

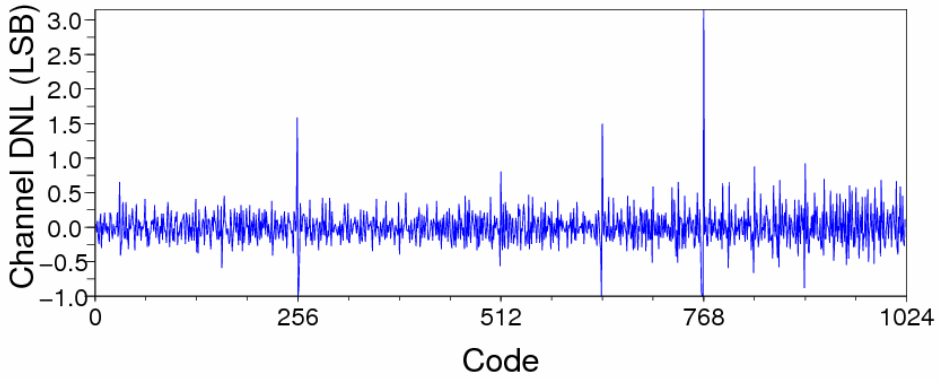




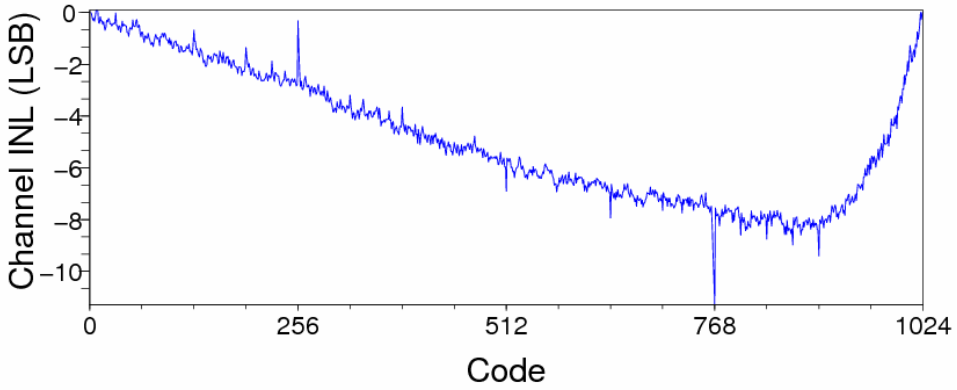
Linearity Test Results, DCAL mode w/Filter

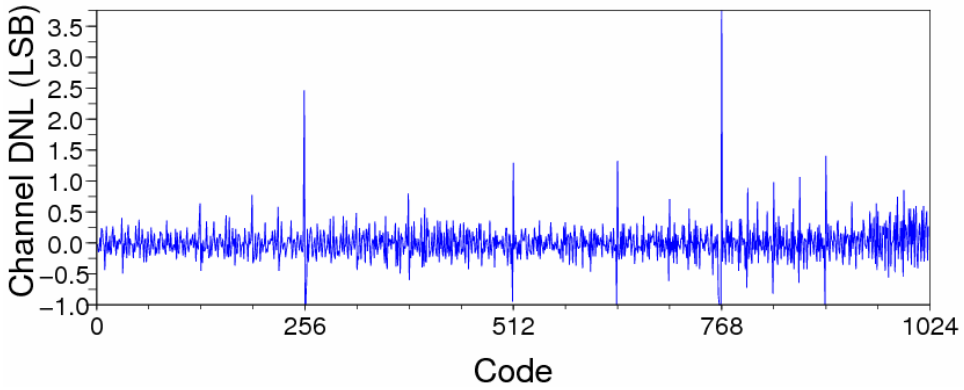
0 - 0.74pC input range





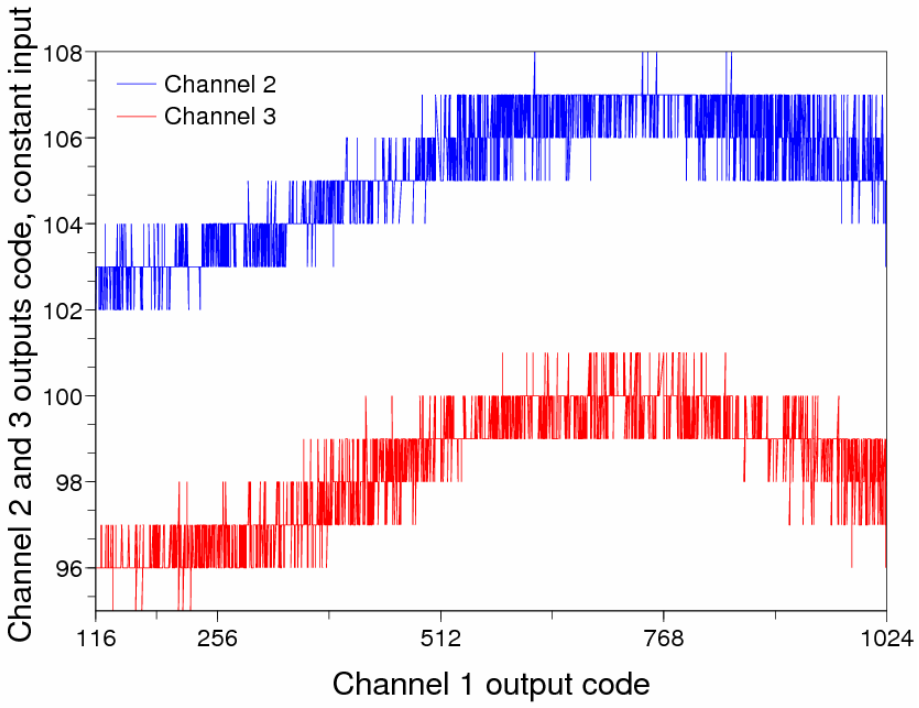
0 - 0.86pC input range



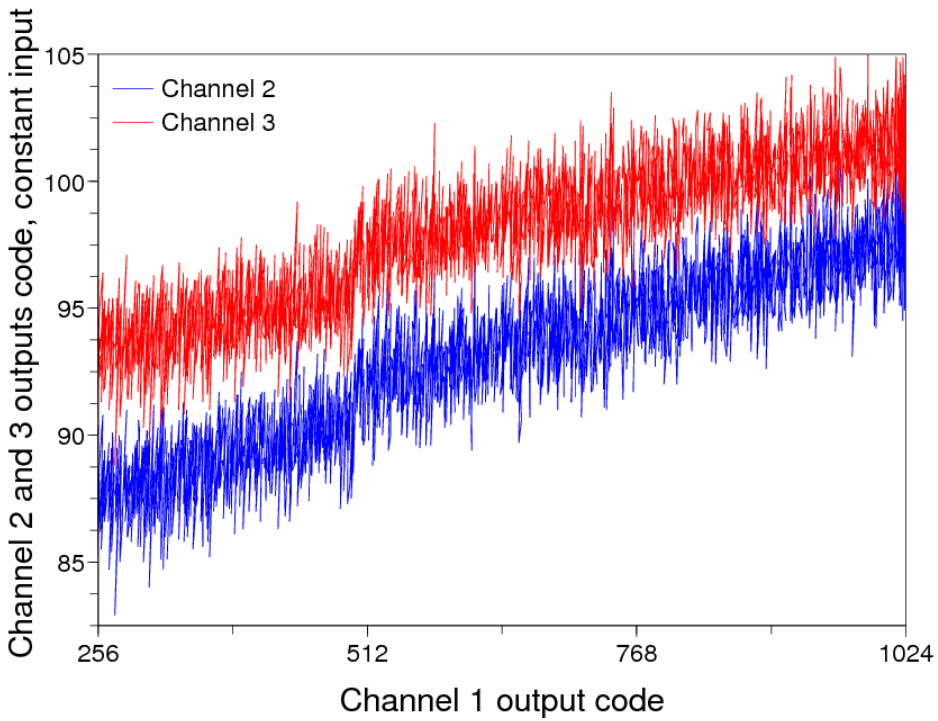


Crosstalk Tests

SDT Mode

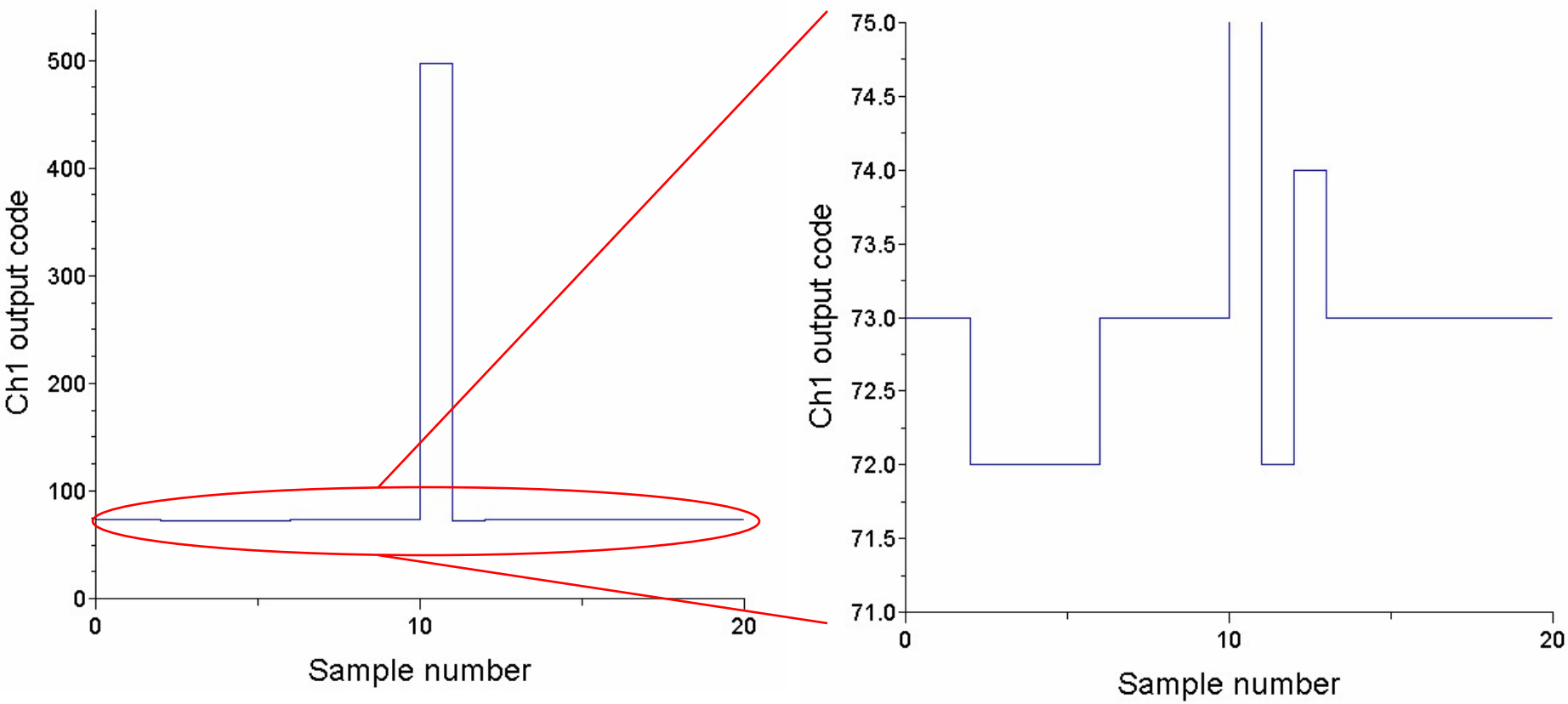


DCal Mode



Bandwidth Test, SDT Mode

- Input injected on 10th cycle only
- Digital output recorded, nominal speed



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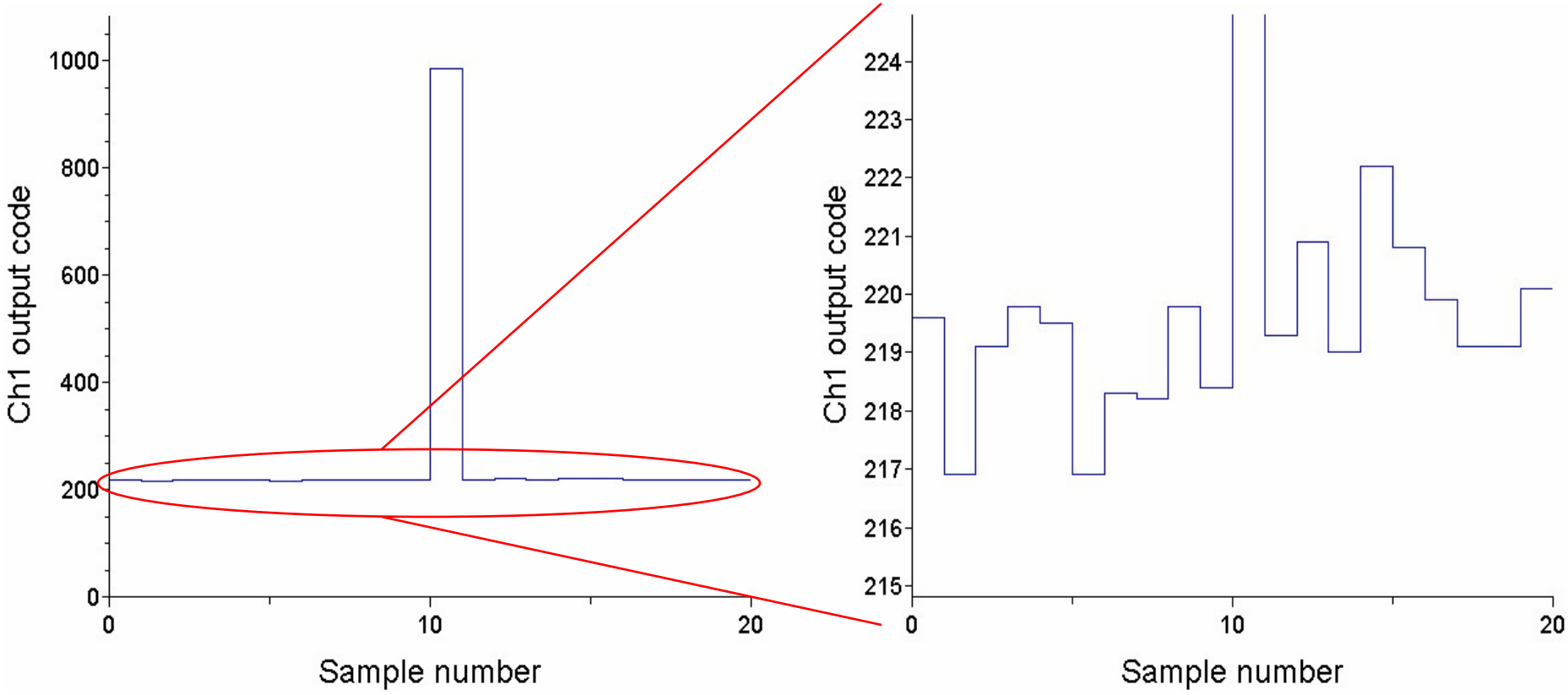
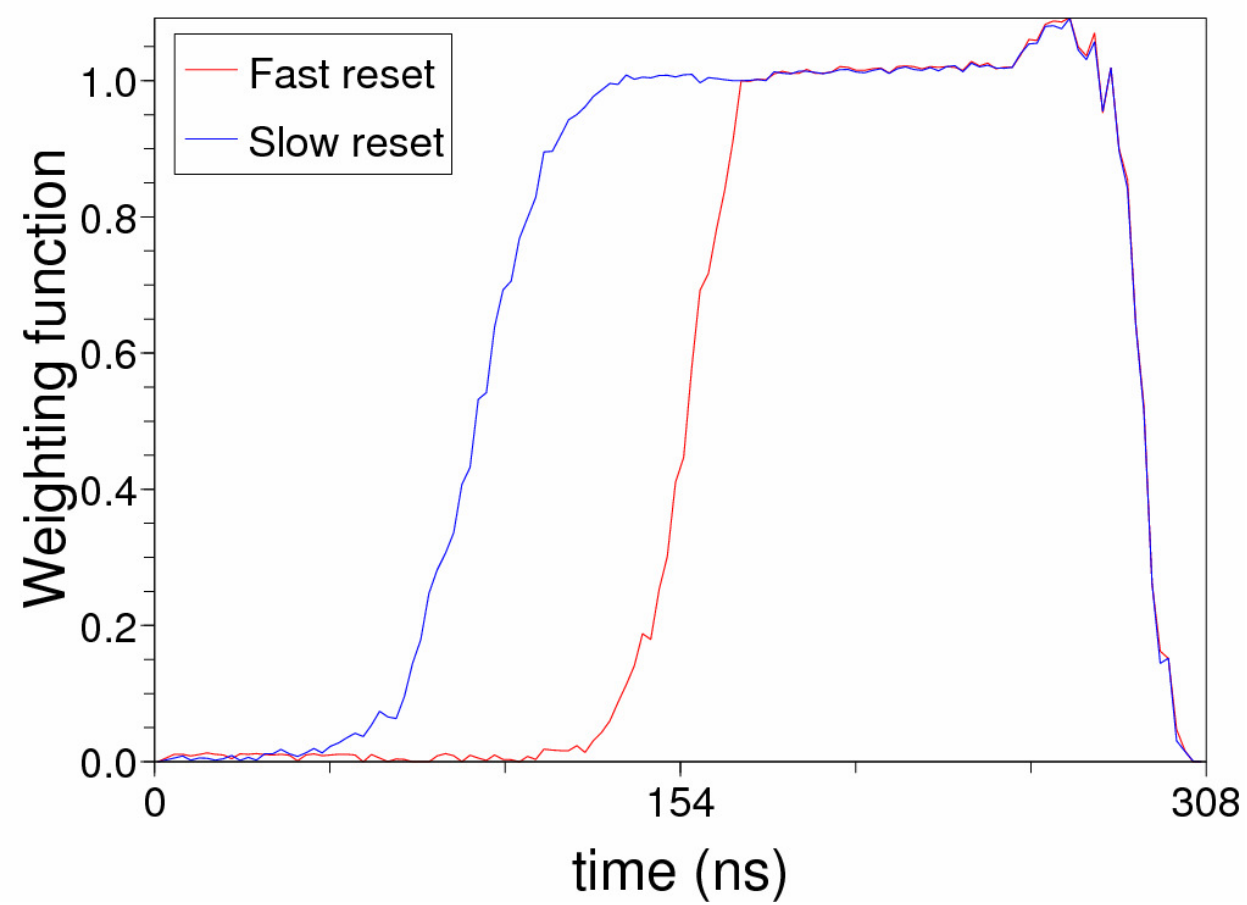


Weighting Function Measurement, SDT Mode

Time resolution: 4.8 ns



Weighting Function Measurements, DCal Mode

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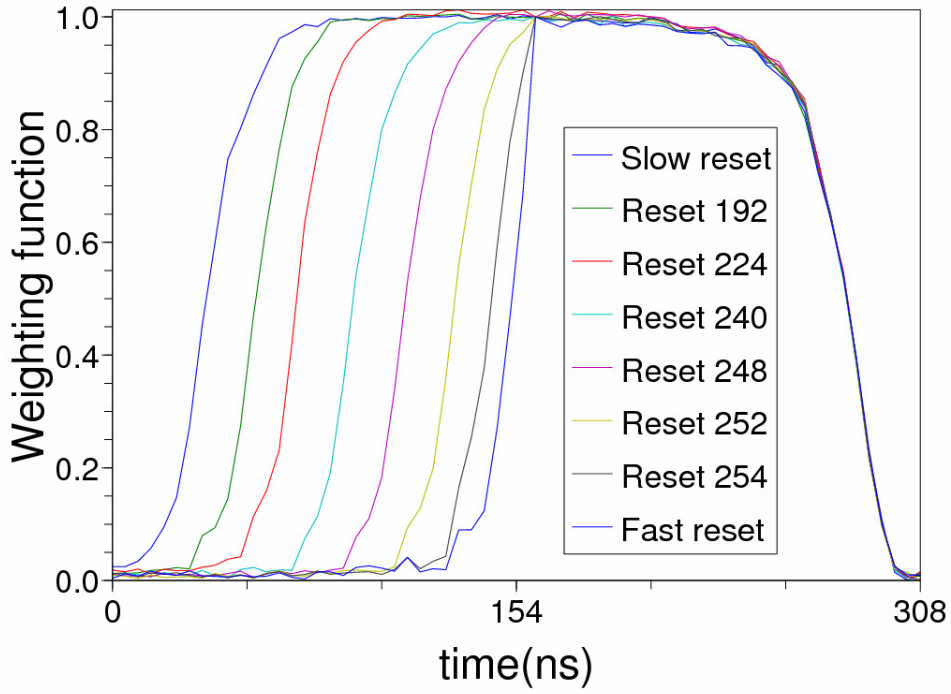
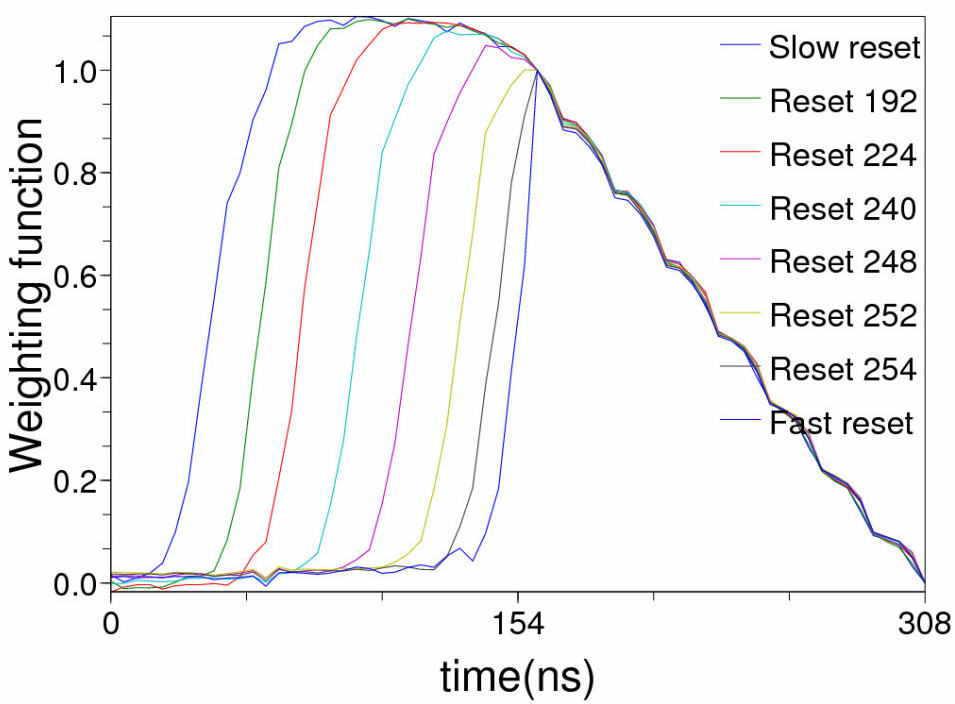


Series noise coefficient
ranges from $46.2\times10^6\ s^{-1}$
to $65.7\times10^6\ s^{-1}$

Time resolution: 4.8 ns

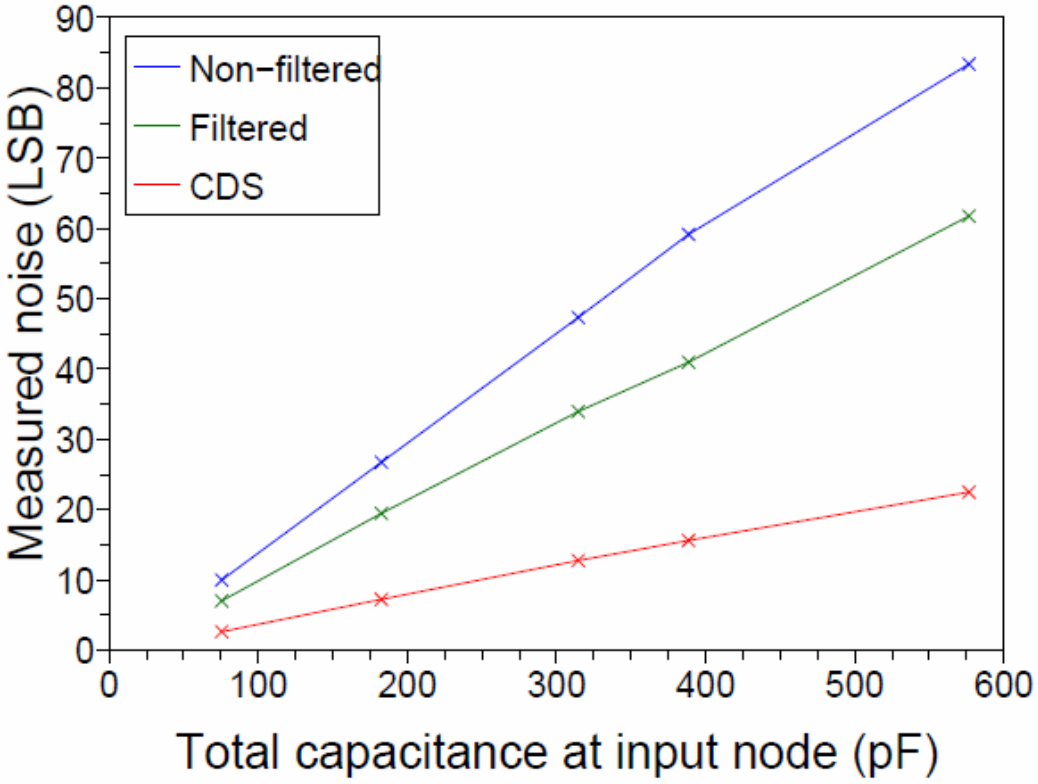


Series noise coefficient
ranges from $37.6\times10^6\ s^{-1}$
to $59.3\times10^6\ s^{-1}$

Noise Filtering, Increasing Input Capacitance

Test done at 1.63 MHz clock (32x slower than nominal speed)

- Filter reduces series noise by 26% (fixed reset scheme)
- Filter + digital CDS reduces series noise by 73%
- Measurements deviate 0.52% from weighting functions calculations

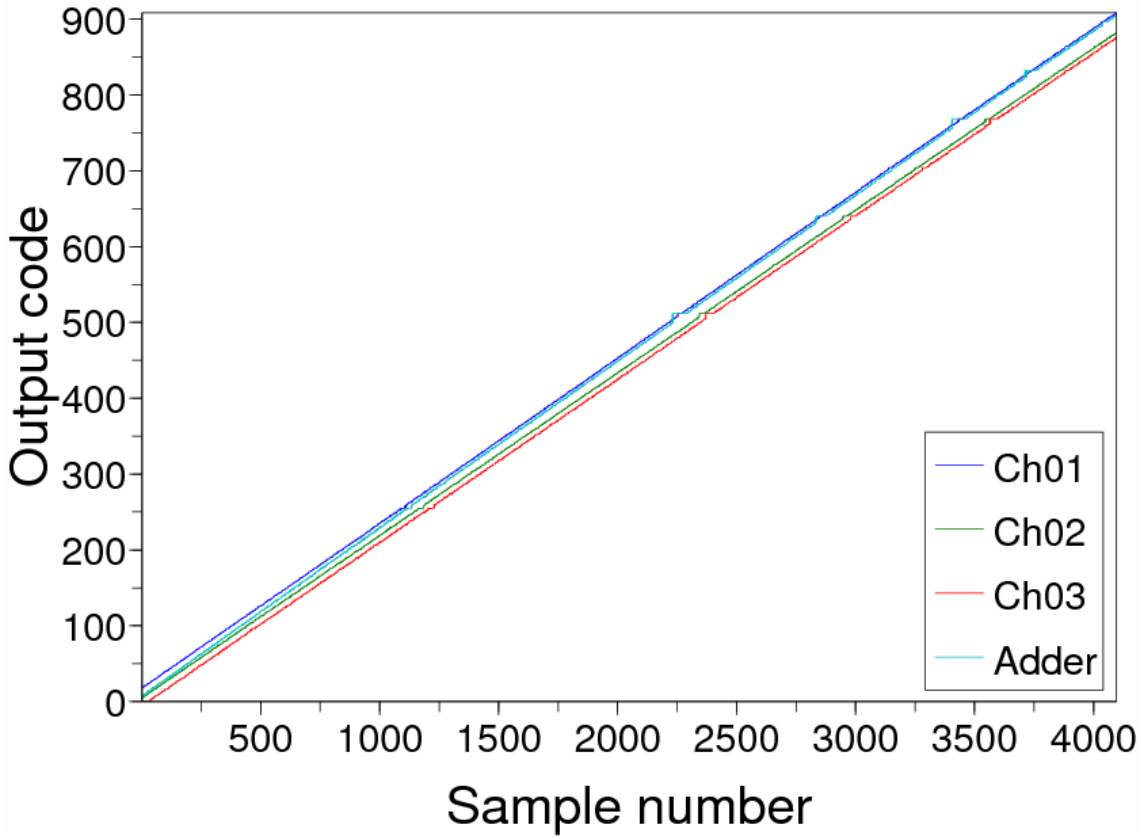


Noise Measurements

- SDT mode
  - Channel noise was computed for different input levels
  - An average of 0.6 LSB rms was measured
  - Noise for slow and fast reset are similar
  - But measured weighting function analysis predicts that slow reset cuts series noise power by 20%
  - Conclusion: CSA does not contribute significantly to the channel noise in standard data taking mode
- DCal mode
  - Channel noise was computed for zero input
  - Input capacitance was estimated as 75.5 pF (88.8% higher than nominal), so noise measurement needs to be scaled accordingly
  - Noise was estimated at
    - 0.62 LSB no filter, and
    - 1.41 LSB with filter
  - Filter removes about 2/3 of the series noise when operating at nominal speed, but adds about 1.35 LSB of noise due to its amplifier noise

Fast Feedback Adder Test

- Adder proved full functionality at nominal speed of operation
- Gains from individual channels to Adder range from 0.329 to 0.345



Conclusion

- A PP instrumentation ASIC for 100% occupancy has been successfully designed and tested
- CSA precharge circuit allows to increase output swing, improving SNR
- Slow reset-release technique effectively halves measured noise in DCal mode
- SC filtering has been proven as a solution for pulse processing in PP experiments
- The low latency adder output meets the required specifications for beam diagnostics purposes

Future work

- Add power cycling feature
- Include small capacitors ADC
- Buffer references internally
- Study radiation hardness

Acknowledgments

- Professor Bruce Wooley (Stanford U.)
- Professor Martin Breidenbach (SLAC)
- Professor Boris Murmann (Stanford U.)
- Dr. Dietrich Freytag (SLAC)

Thank you!