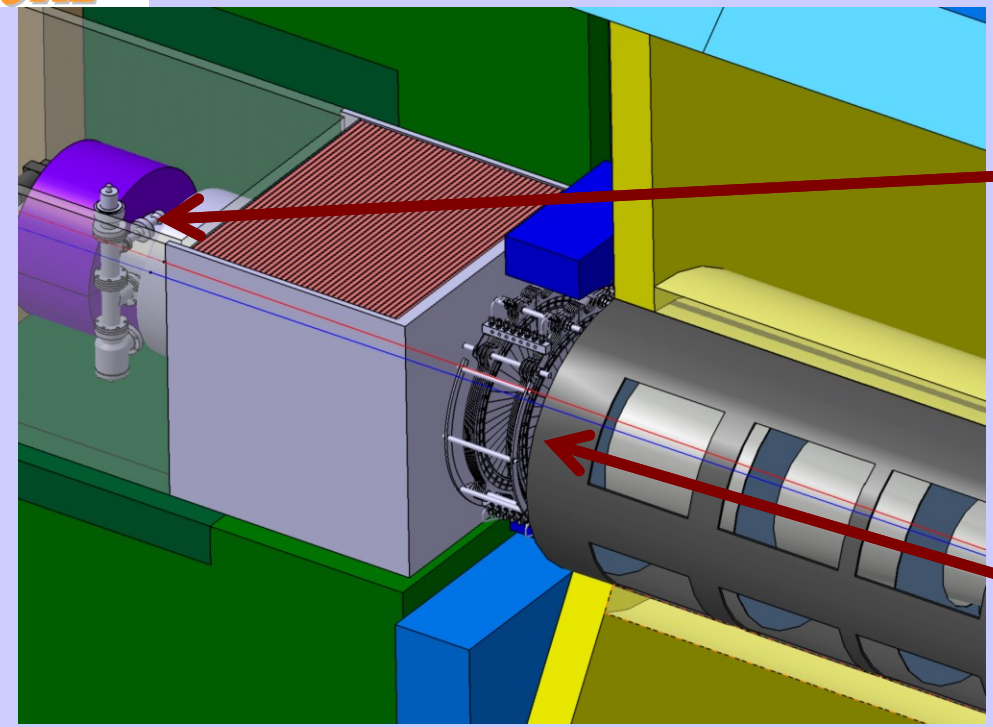
Wolfgang Lohmann,

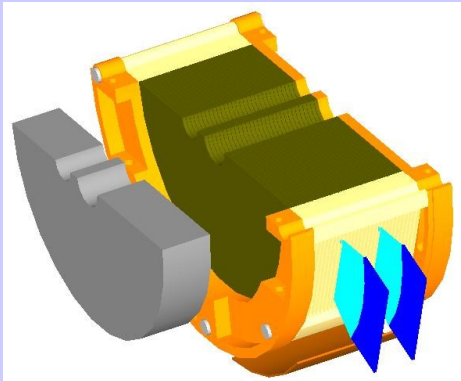
BTU and DESY

Labs involved: Argonne, Vinca Inst, Belgrade, Bukharest IFIN, CERN, Univ. of Colorado, Cracow UST, Cracow INP, JINR Dubna, Royal Holloway, NCPHEP Minsk, Santa Cruz, Stanford University, SLAC Tuhoku Univ., Tel Aviv Univ., DESY (Z.)

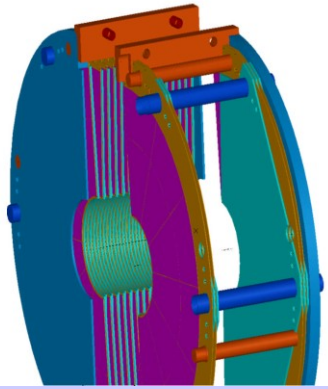
Very Forward Instrumentation- Example ILD



BeamCal + Pair Monitor



LumiCal



- precise luminosity measurement,
- hermeticity (electron detection at low polar angles),
- assisting beam tuning (fast feedback of BeamCal data to machine)

Challenges:

radiation hardness (BeamCal), high precision (LumiCal) and fast readout (both)

Detector Design Studies, 500 GeV

Design studies, background, systematic effects for 500 GeV advanced

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Forward Instrumentation for ILC Detectors

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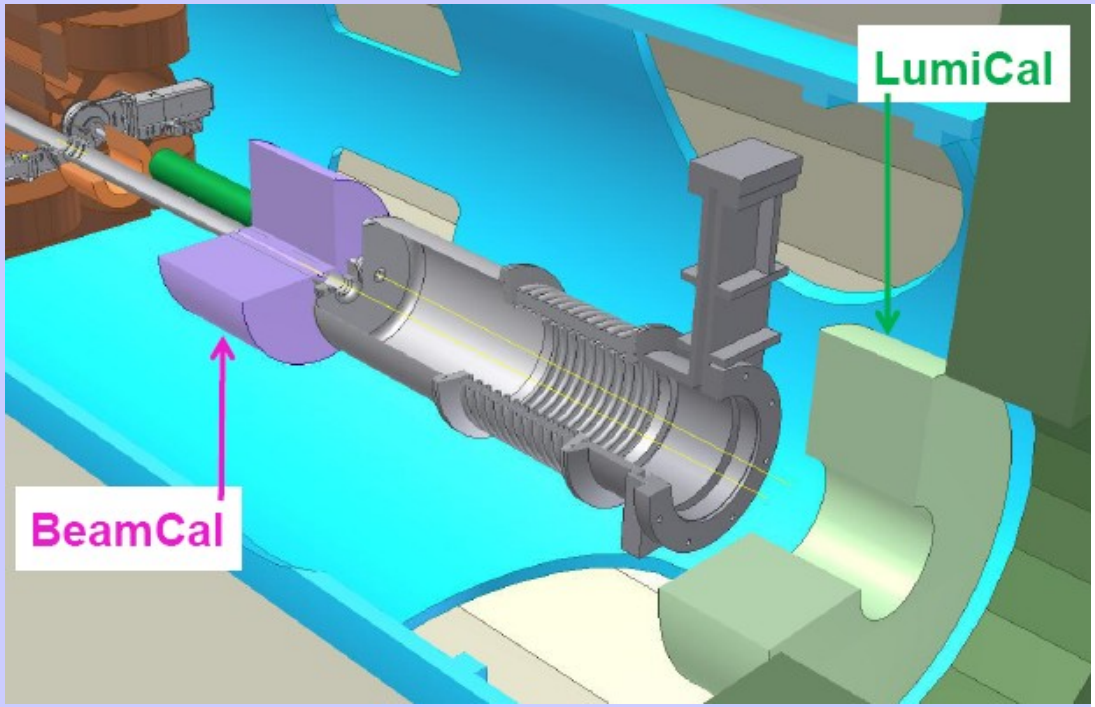
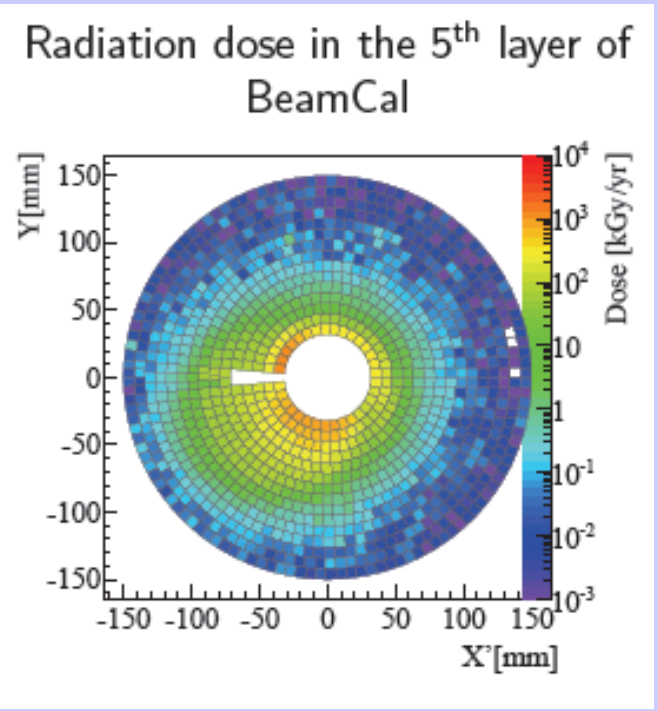
ABSTRACT: Two special calorimeters are foreseen for the instrumentation of the very forward region of the ILC detector, a luminometer designed to measure the rate of low angle Bhabha scattering events with a precision better and a low polar angle calorimeter, adjacent to the beam-pipe. The latter will be hit by a large amount of beamstrahlung remnants. The amount and shape of these depositions will allow a fast luminosity estimate and the determination of beam parameters. The sensors of this calorimeter must be Both devices will improve the in the search for new particles . Due to the high occupancy fast front-end electronics is needed. The design of the calorimeters developed and optimised with Monte Carlo simulations is presented Results on the performance of these major components are summarised.

Detector Design Studies, 3 TeV

Focus is now on the design of the forward region of a CLIC detector





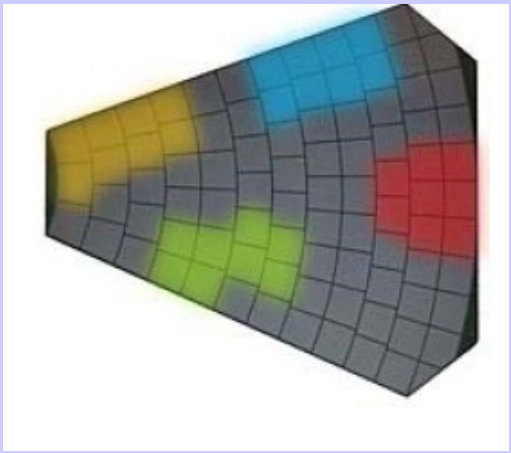
LumiCal is designed to measure the Luminosity with a precision of 10^{-2} at 3 TeV

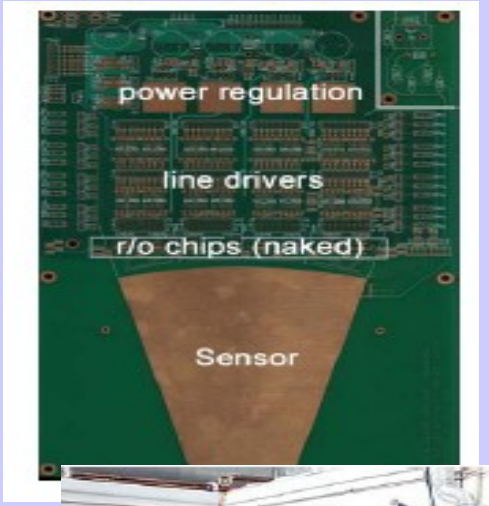
BeamCal feasible, details need more studies

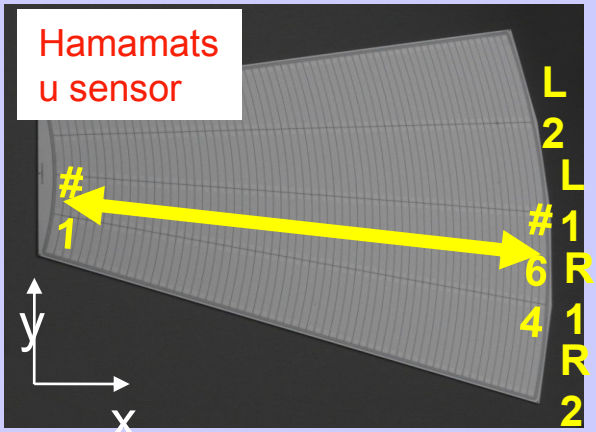
Results presented by Konrad Elsener

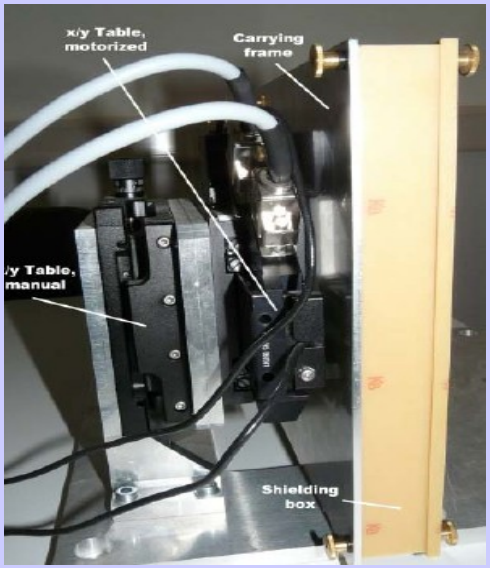
Succesfull test-beam venture in August

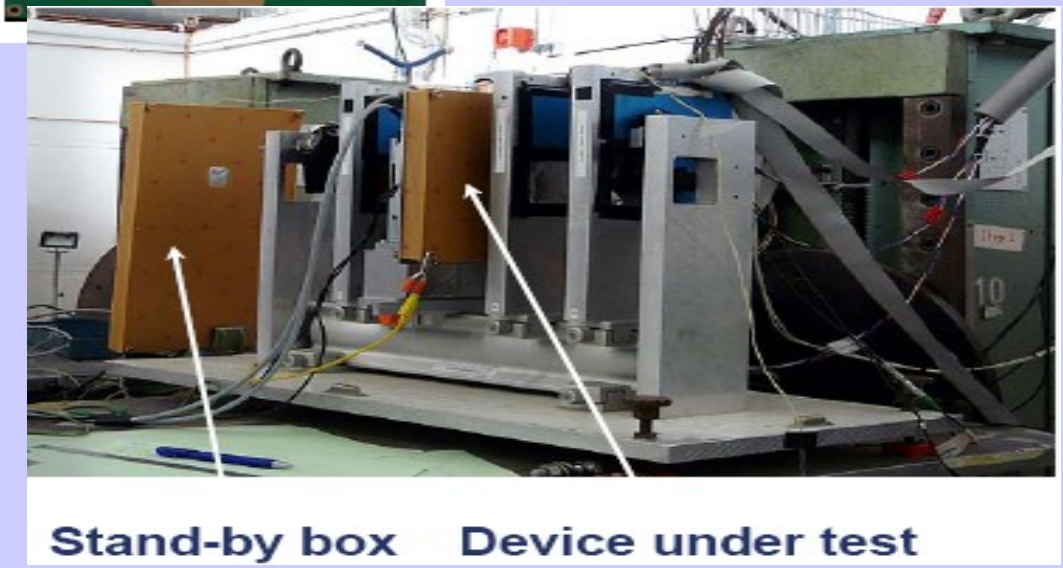
Beam 22 at DESY, 4 GeV electrons, sensors equipped with FE ASICs from UST Cracow









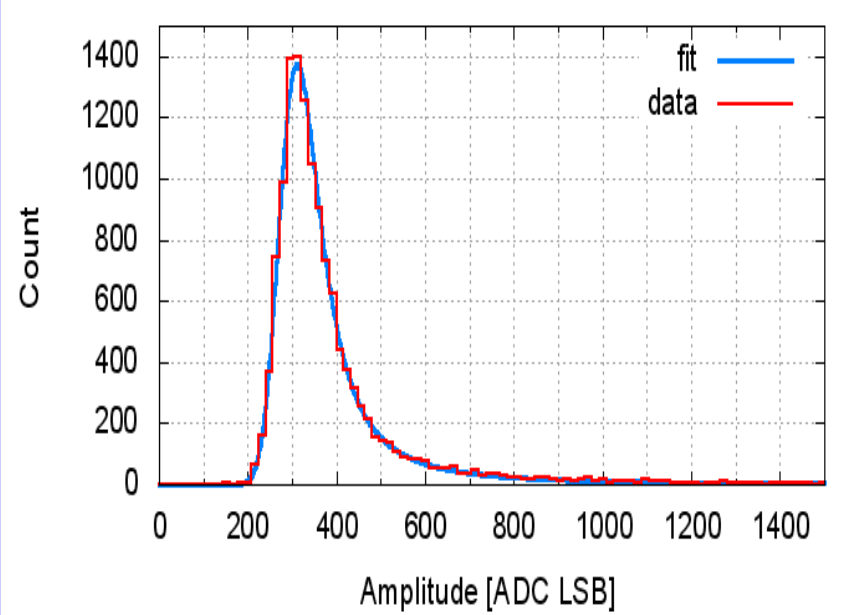


Results presented by Olga Novgorodova

Successfull test-beam venture in August

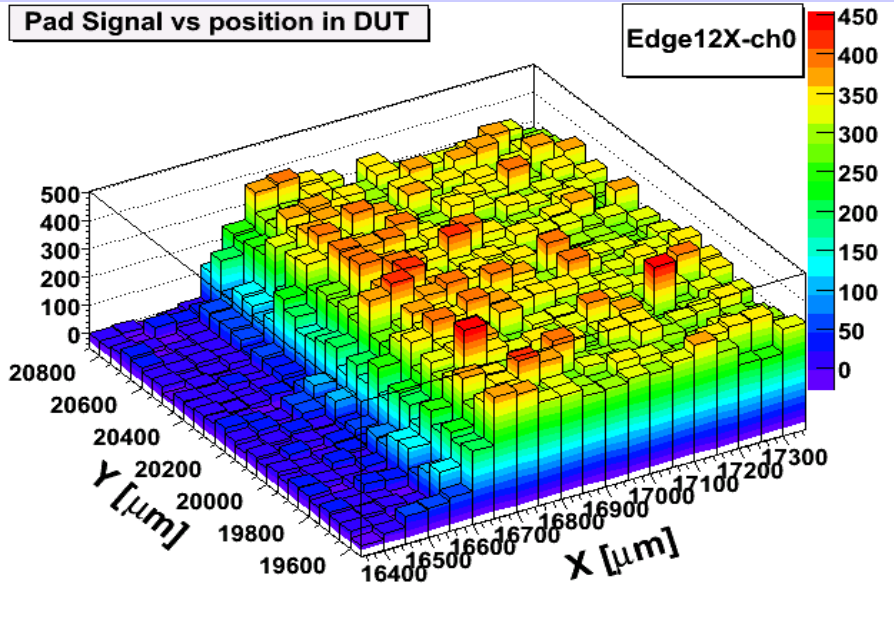
LumiCal

Signal spectrum



Homogeneity of the response

BeamCal



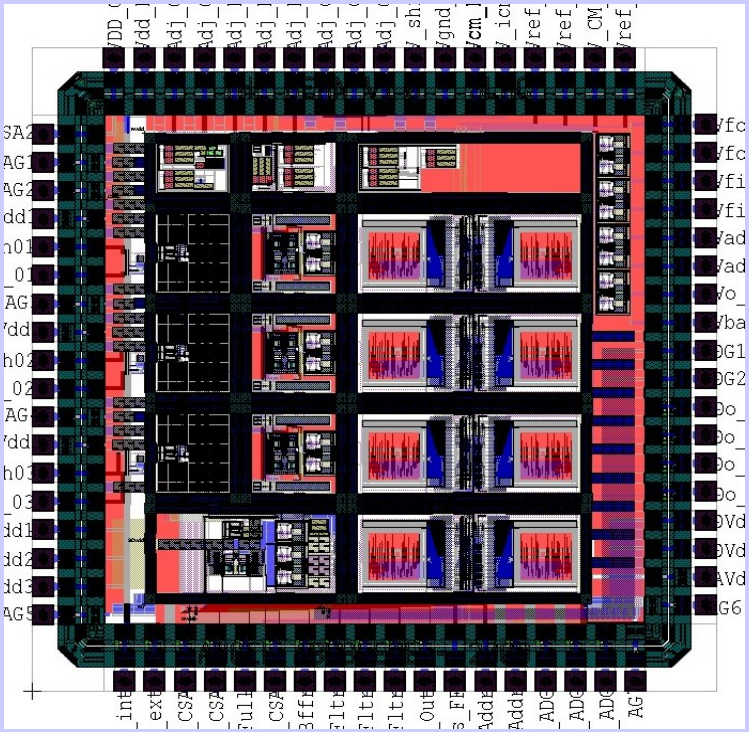
S/N ~ 20

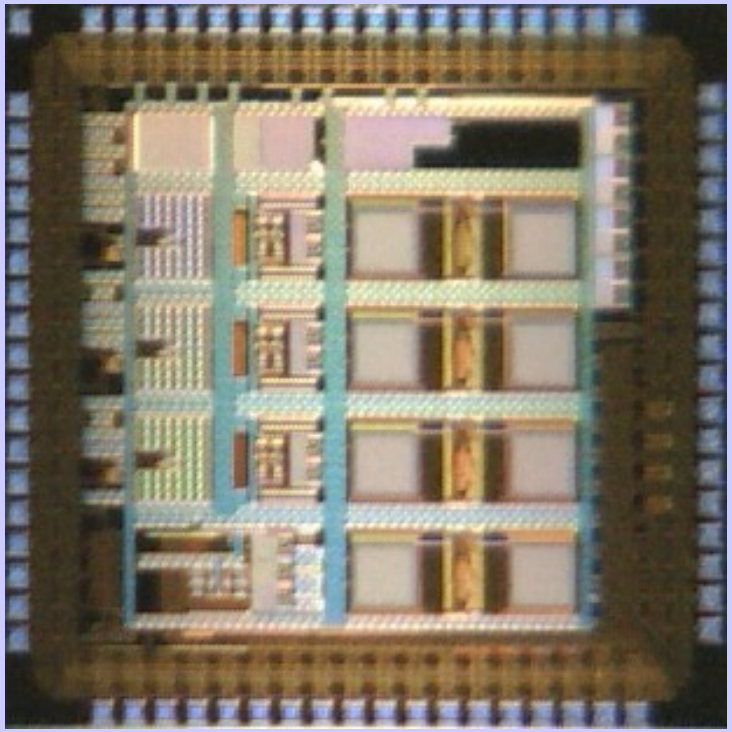
Cross talk: ~ %

In addition: study of stability, edge effects

FE ASICs (KPiX)

Designed especially for BeamCal (fast feedback function)



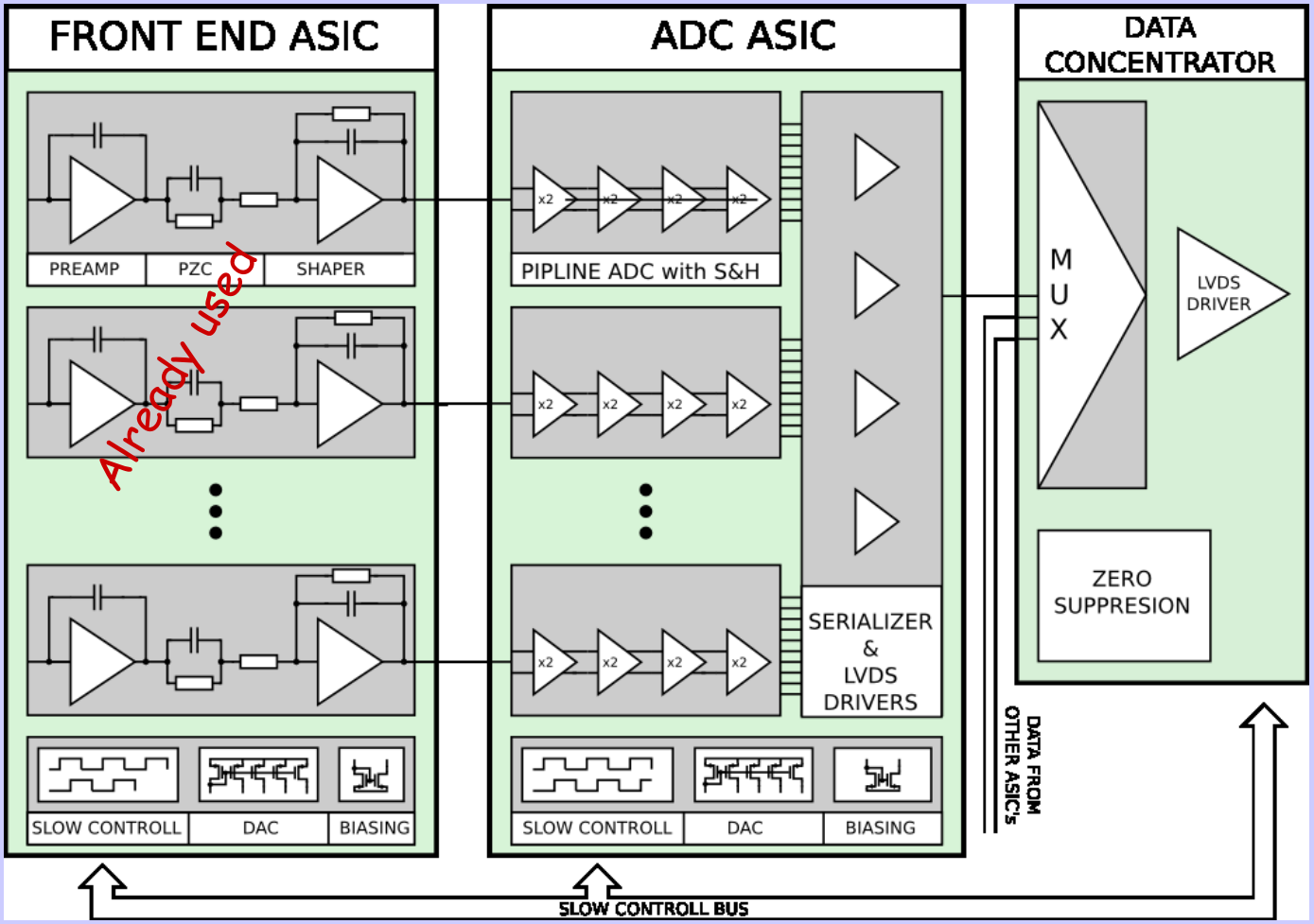


- TSMC 0.18um, 1.8V
- 72 pads, 2.4mm x 2.4mm (incl. pads)
- 3 charge amplifiers, 4 x 10-bit, fully diff. SAR ADCs, 1 SC adder, 3 SC filters

Status presented by Angel Abusleme

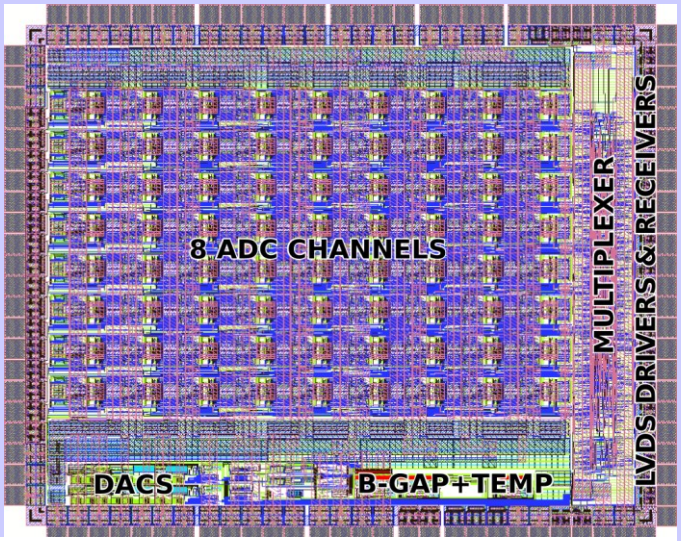
Electronics readout chain

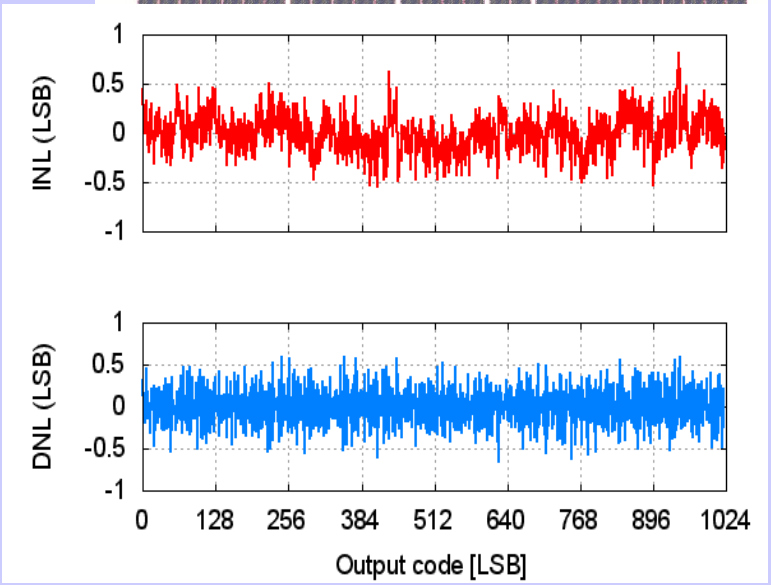
LumiCal version



ADC ASIC prototype

8 Channel ASIC ADC chips tested connected to the FE ASICs





- 8 channel pipeline ADC:
- Scalable power(~1mW/MHz) and sampling frequency(up to ~25MHz)
- Digital multiplexer/serializer:
  - Serial mode (<300MHz): one data link per all channels (max fsmp ~ 3 MSps)
  - Parallel mode (~250MHz): one data link per channel (max fsmp ~ 25MSps)
  - Test mode (single channel readout)
- High speed LVDS I/O (~1GHz)
- Low power DACs references/bias
- Precise BandGap reference source and Temperature sensor

Few results:

ENOB ~9.7

INL < 0.8 LSB

DNL < 0.6 LSB

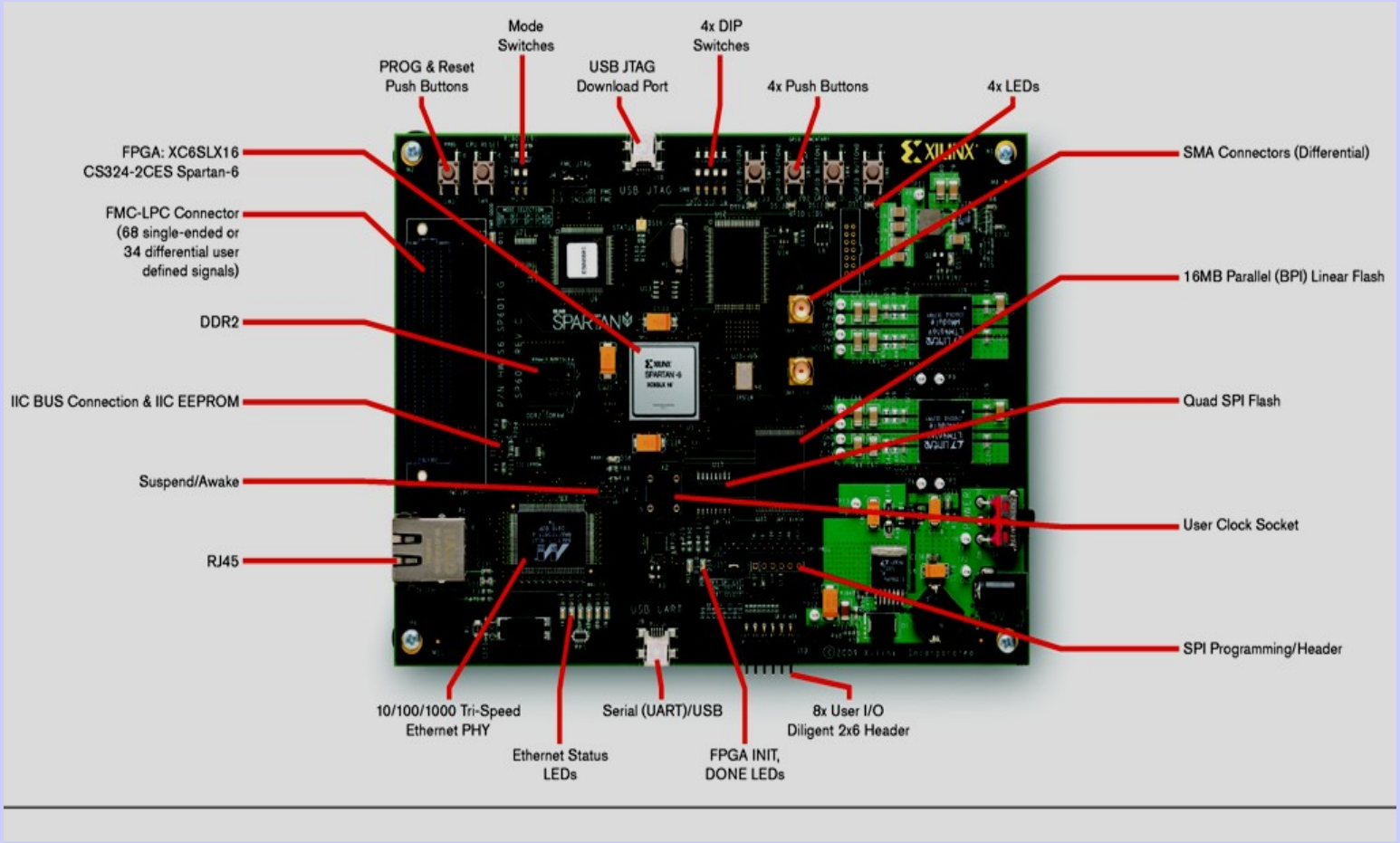
New Developments

Developments just started:

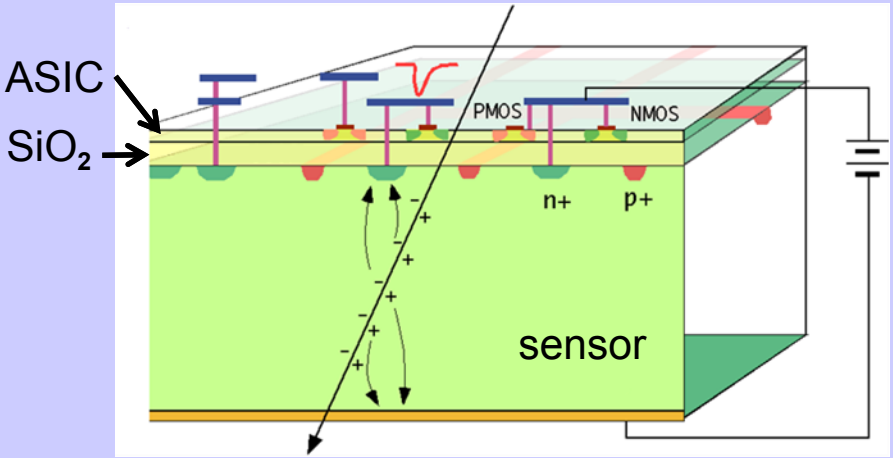
- Development of data concentrator (FPGA or ASIC)
- Development of 64 channels front-end and ADC ASICs (130nm technology) (AGH-UST Cracow)

DIF-link to detector DAQ

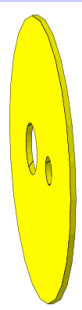
- Design of FCAL DIF under work (LumiCal version)
- For next test beam the DIF functionality is implemented by a commercial FPGA – SPARTAN6 (XILINX SP601) board



Pair Monitor



- Pixel size: 400 x 400 μm²
- Radius: 10 cm
- Total number of pixels: ~200,000

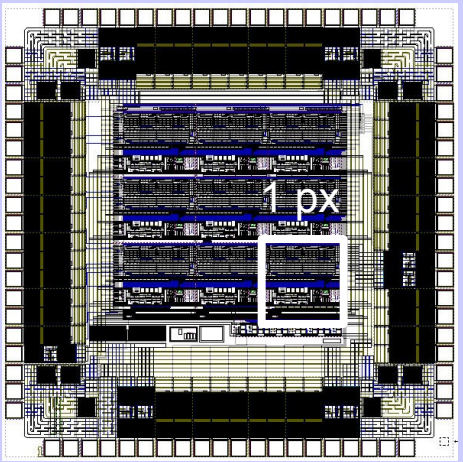


→Monolithic construction allows the elimination of the bump-bonding process.

- First step: design of a readout prototype ASIC for 3x3 pixels: digital readout (preamp, discriminator, counter)

- manufactured chip (CMOS 0.2 μm, SOI technology)
- performance measurements done

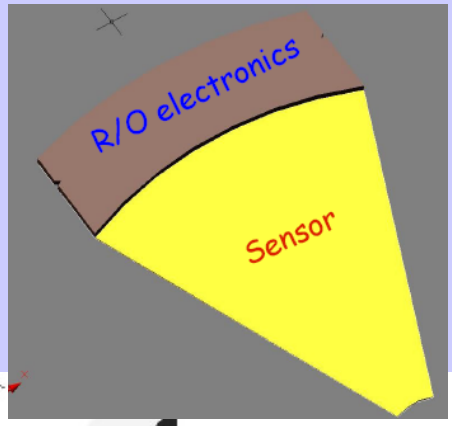
Publication accepted !

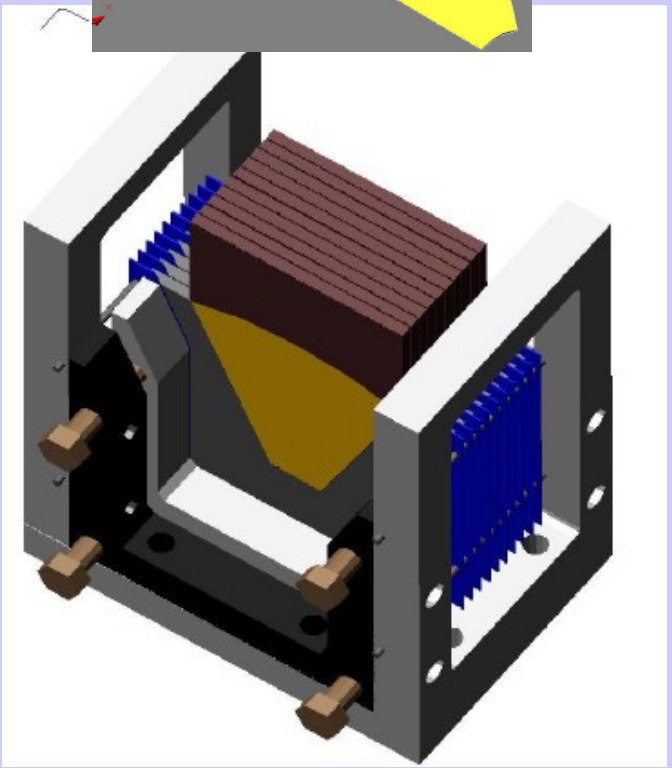


AIDA (EU supported)

Preparation of a prototype Calorimeter:

- Flexible, high precision tungsten structure,
- Fast FE Readout
- Innovative connectivity scheme
- Position control devices
- Fully assembled sensor planes, covering ≥ 30^0
- Power pulsing





Infrastructure common with others:

- Data acquisition
- Tracking in front of the calorimeter

Participating Institutes: AGH-UST (Cracow), CERN, DESY (Zeuthen), IFJPAN (Cracow), TAU (Tel Aviv)

AIDA Schedule

- Flexible tungsten structure: design 2012, manufacturing 2013, ready 2014
- Multichannel readout ASICs: design start 2011, 1st prototype production, 2012, 2nd 2013
- Complete prototype of sensor plane 2012
- DAQ: 1st DIF prototype 2011, prototype of complete DAQ 2012, ready 2013
- Design fixed beginning 2013
- Production 2014

Dates Ahead

- ILC detector DBD 2012
  - refining design considerations (MC studies)
  - completing the measurements with fully assembled sensor plane prototypes

- CLIC CDR (2011)
  - completing design studies

Summary

- Design studies are focused now on a CLIC detector
- FCAL started test-beam measurements to test assembled prototype sensor planes, Results so far satisfactory
- The readout will be completed in a few steps, beam-tests planned
- Long term goal is a calorimeter prototype, ready in 2014, including
  - power pulsing
  - DIF to standard DAQ
  - position monitoring