Performance of FONT at ATF2

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Feedback On Nanosecond Timescales

Beam-based FB R&D for future Linear Colliders

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Valencia, CERN, DESY, KEK, SLAC

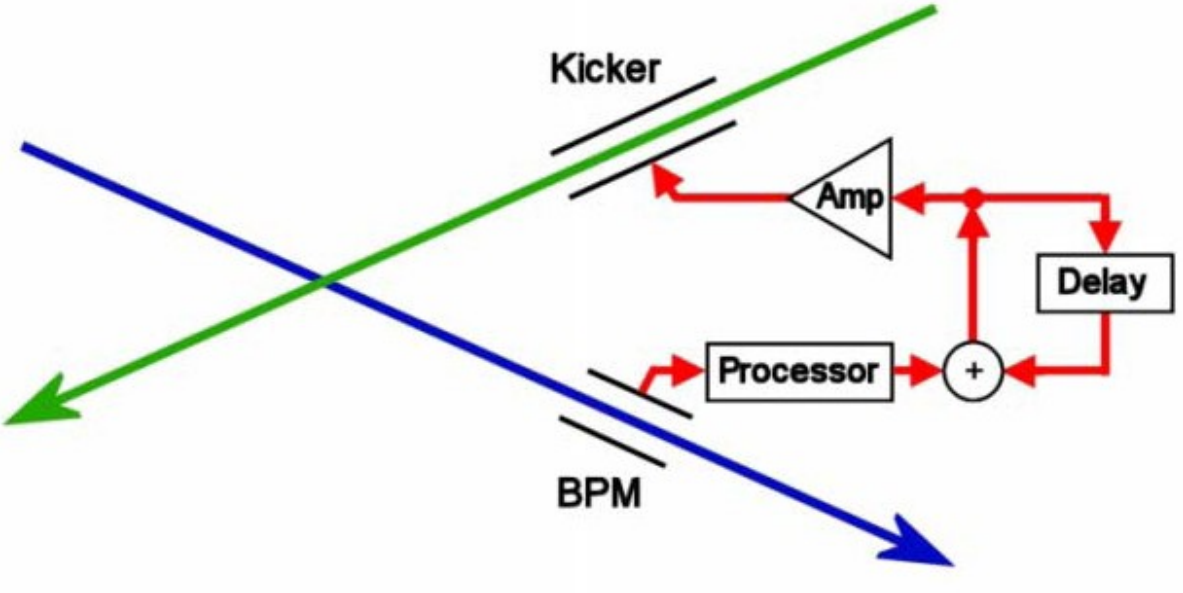
Outline

- Brief reminder of intra-train feedback system
- Implementation in ILC + CLIC IRs
- Prototype hardware development

  (FONT systems)
- Summary + outlook

IP intra-train feedback system - concept

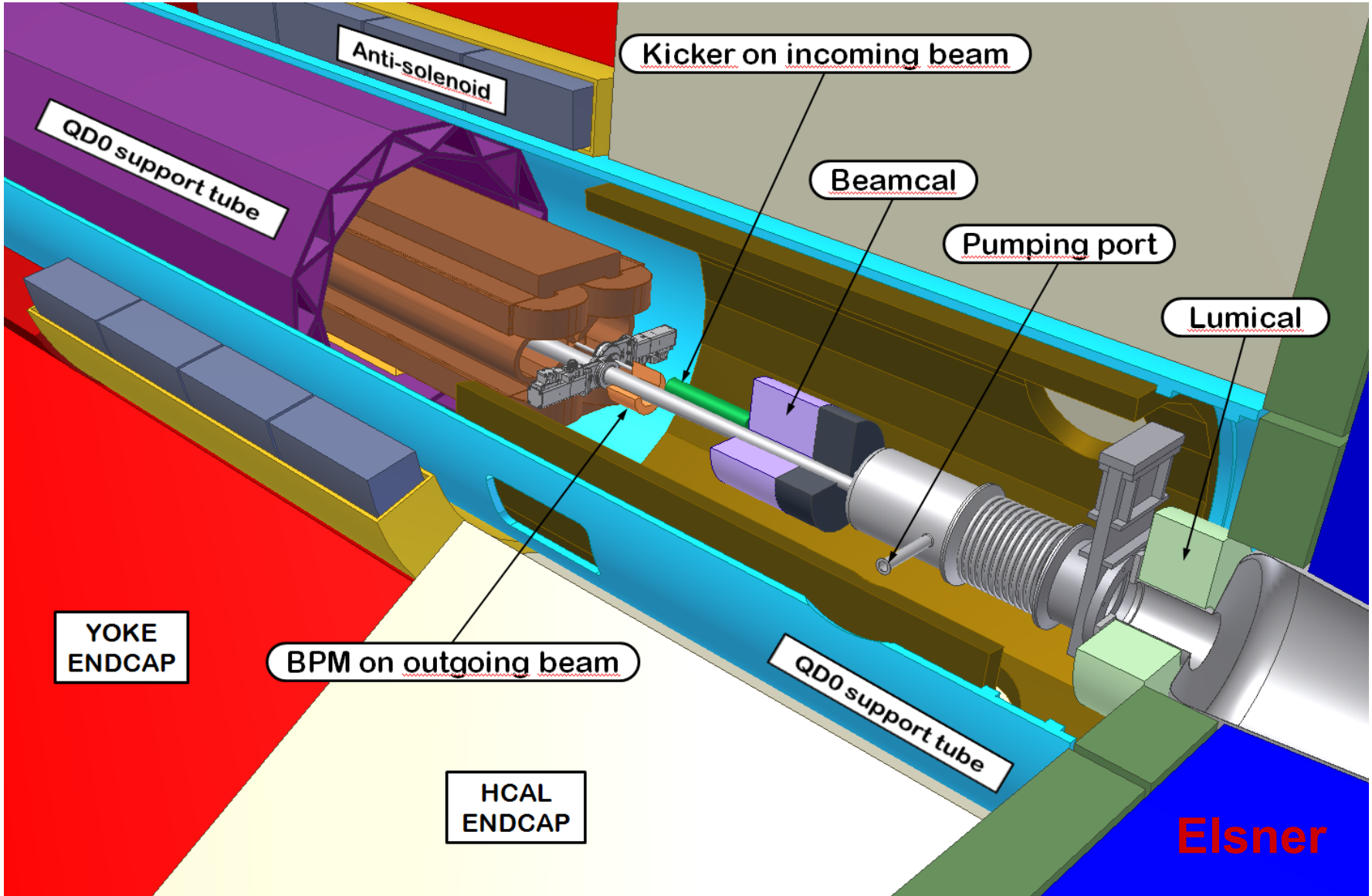
- Last line of defence against relative beam misalignment
- Measure vertical position of outgoing beam and hence beam-beam kick angle
- Use fast amplifier and kicker to correct vertical position of beam incoming to IR



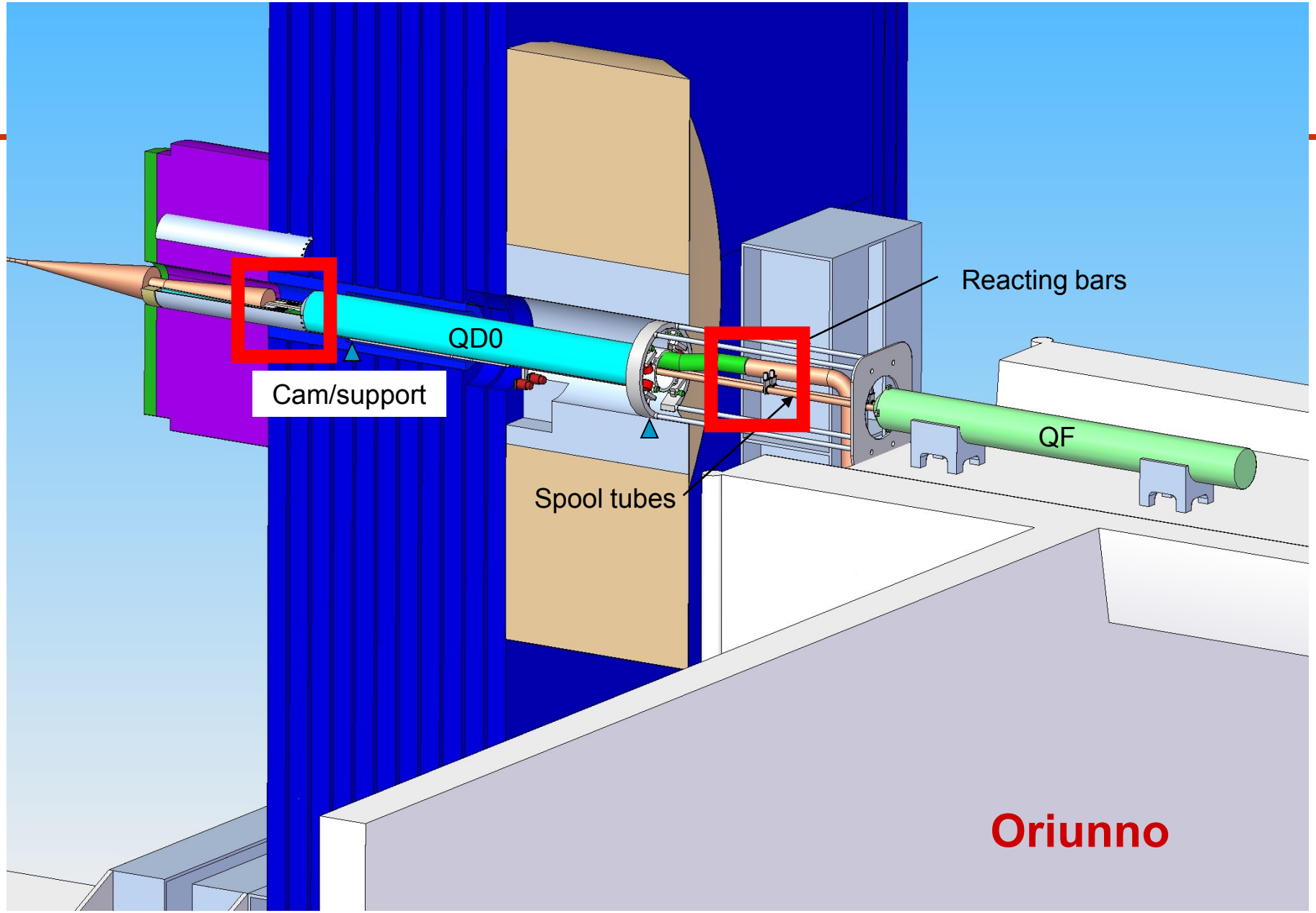
FONT – Feedback On Nanosecond Timescales

(Oxford, Valencia, CERN, DESY, KEK, SLAC)

CLIC FD region



ILC Final Doublet Region (SiD for illustration)



Remaining issues

- **Engineering of real hardware optimised for tight spatial environment: BPM, kicker, cables …**
- **Further studies of radiation environment for FB:**

  was studied for ILC, less so for CLIC;

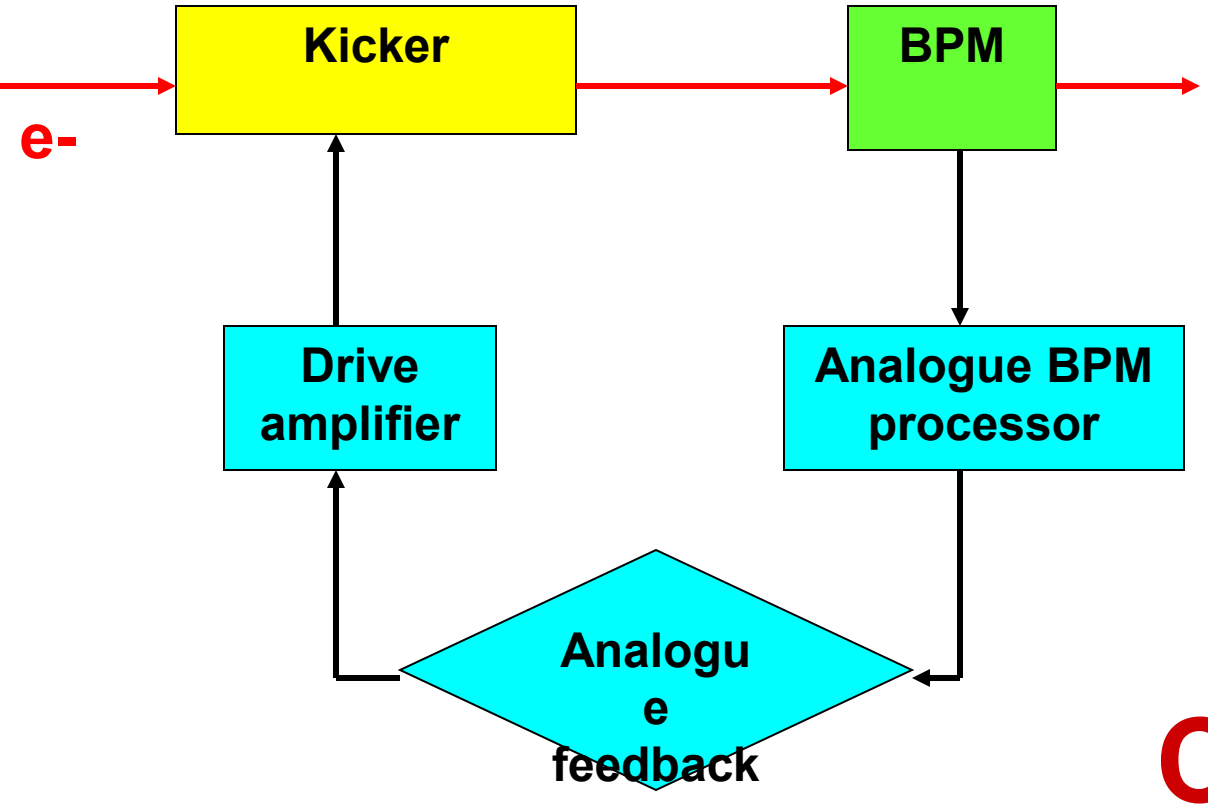
  where to put electronics?

  need to be rad hard? shielded? off to side?
- **EM interference: beam ←→ FB hardware**

  kicker ←→ detector

Prototyping status

FONT system prototype (schematic)

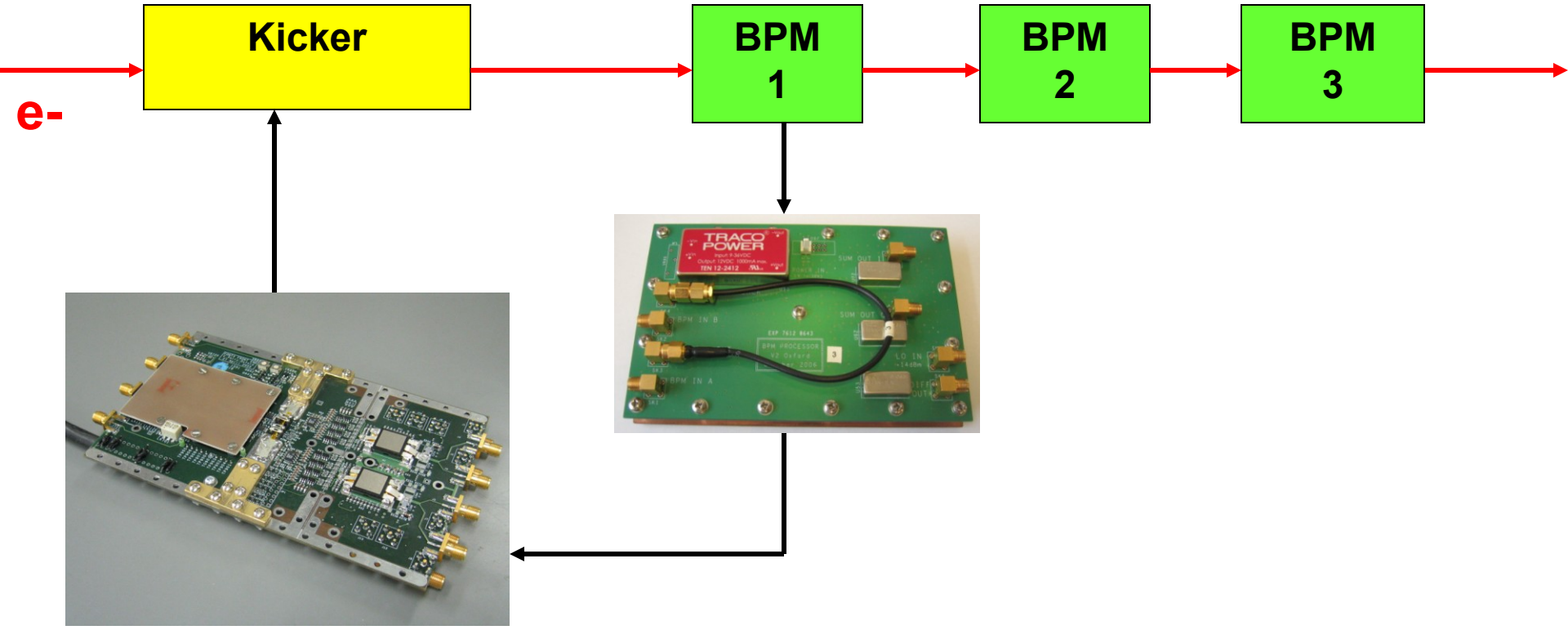


CLIC

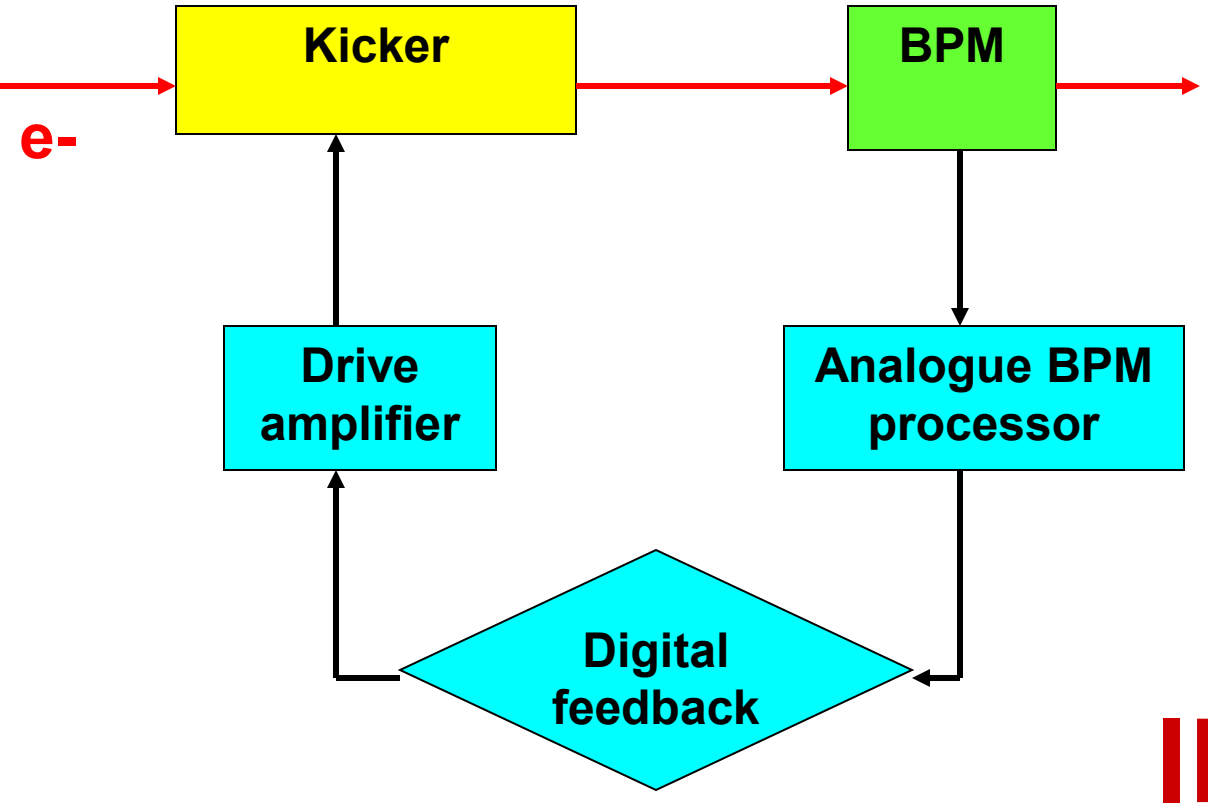
FONT3 CLIC prototype at KEK/ATF

(2004-5)

56ns train of bunches separated by 2.8ns



FONT system loop (schematic)

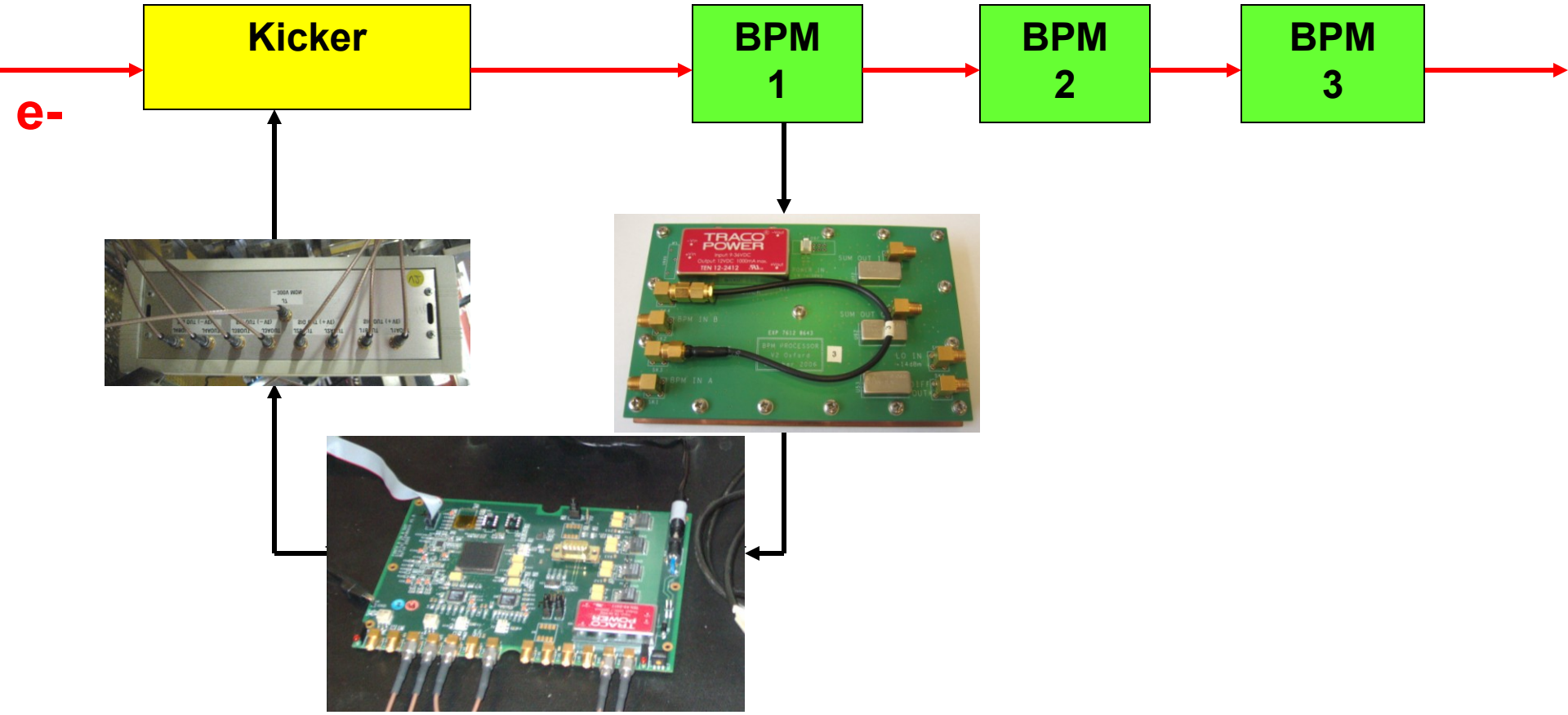


ILC

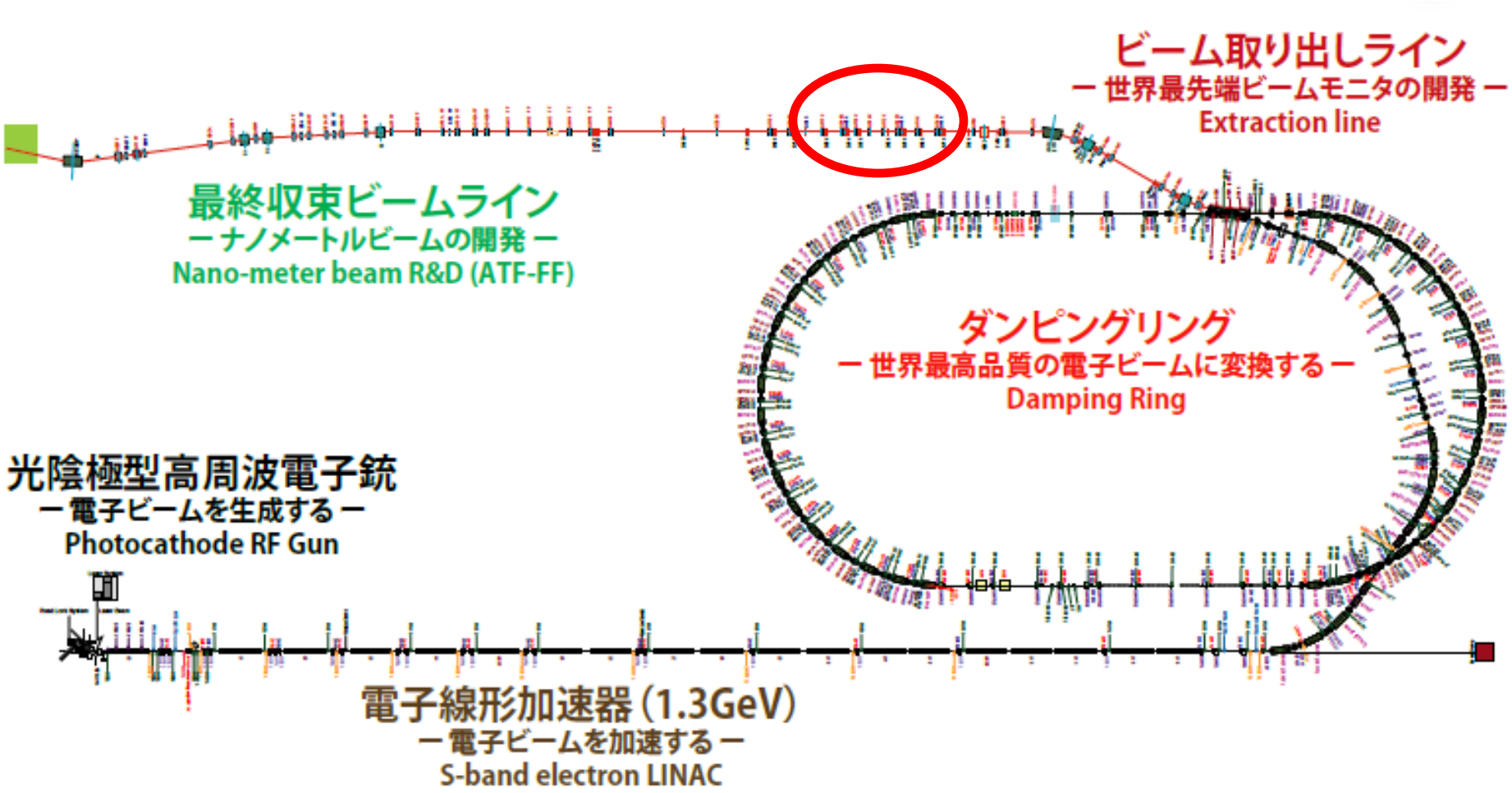
FONT4 ILC prototype at KEK/ATF

(2006-9)

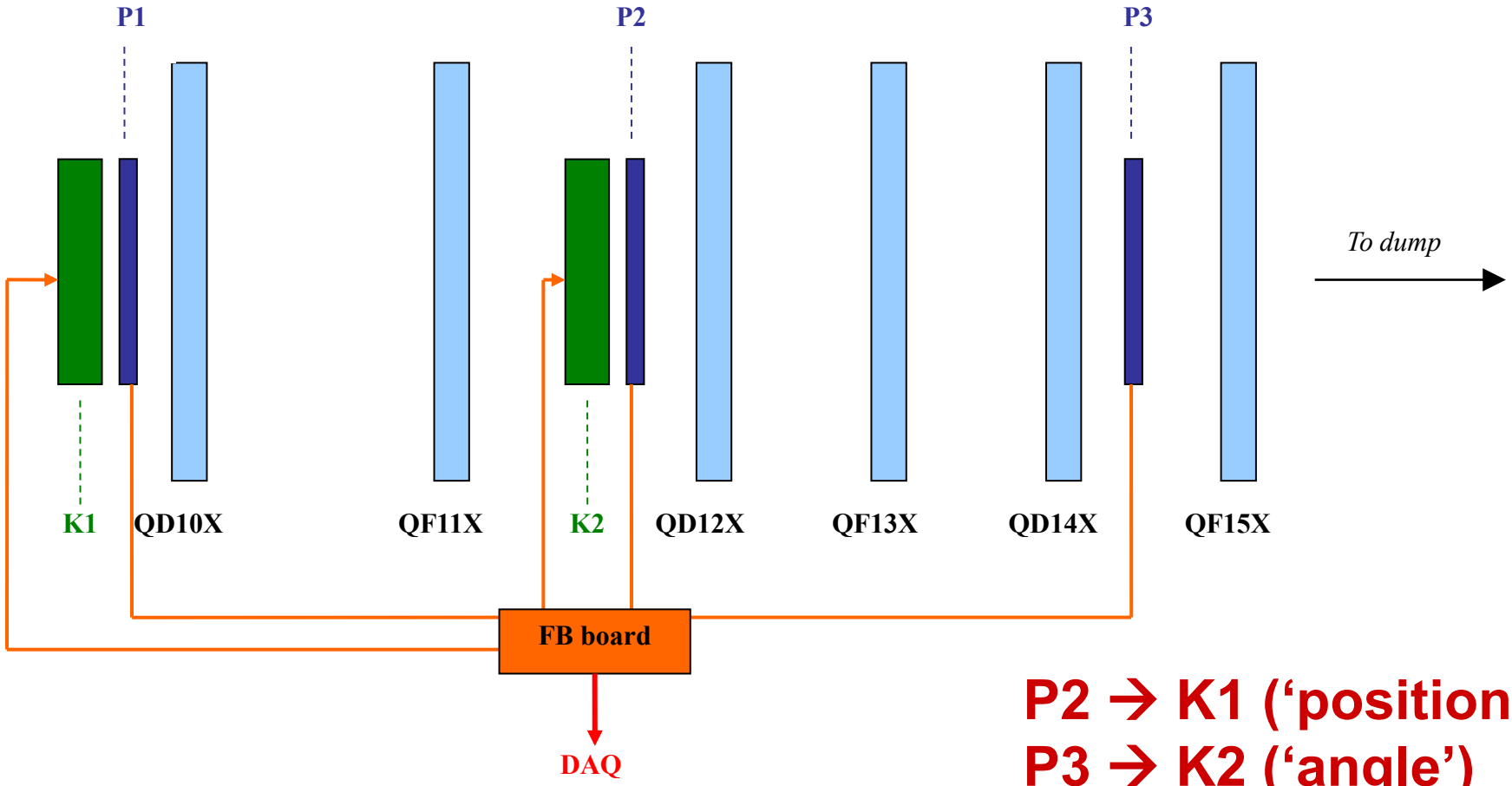
300ns train of bunches separated by 150ns



FONT5 location



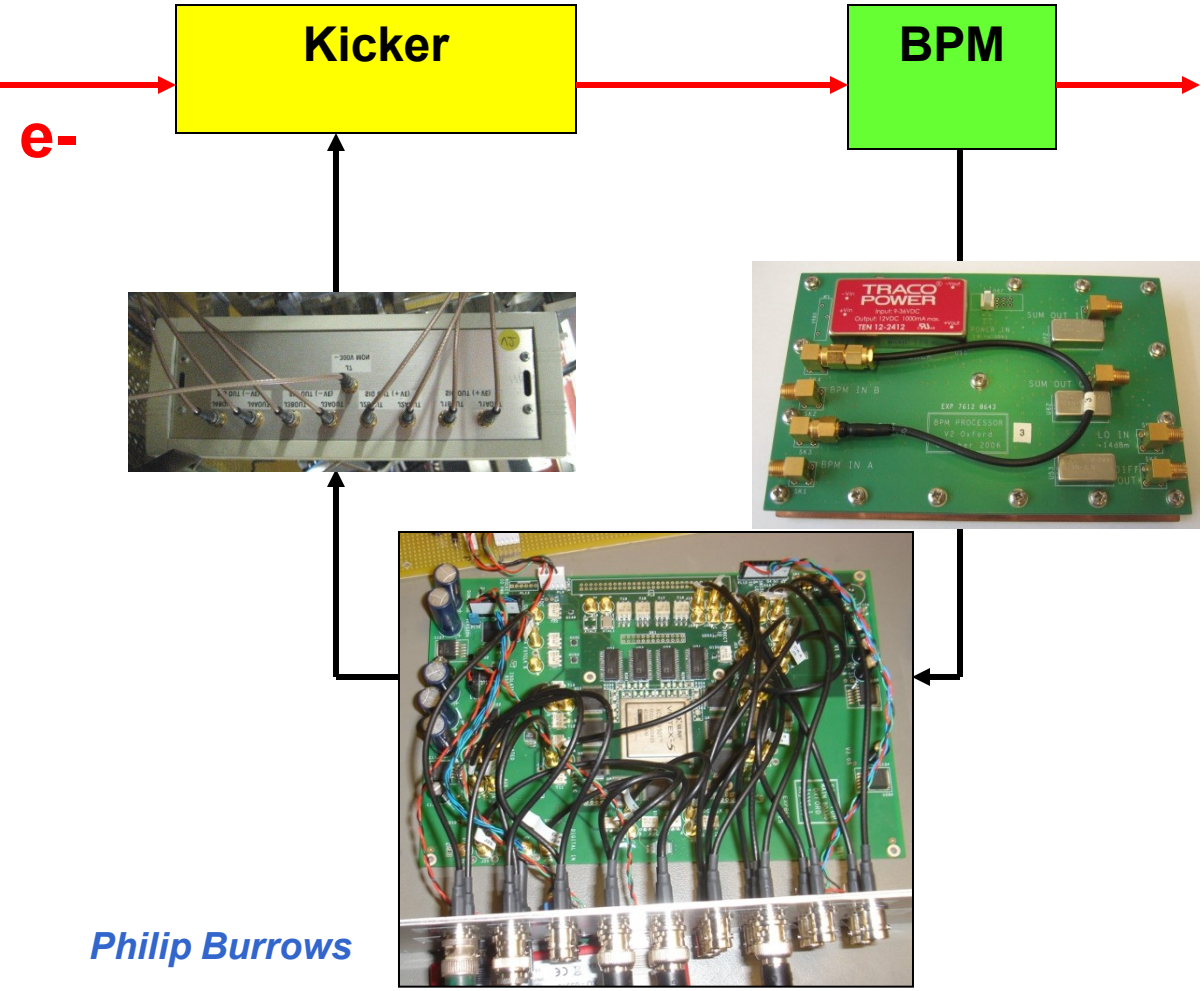
FONT5 schematic



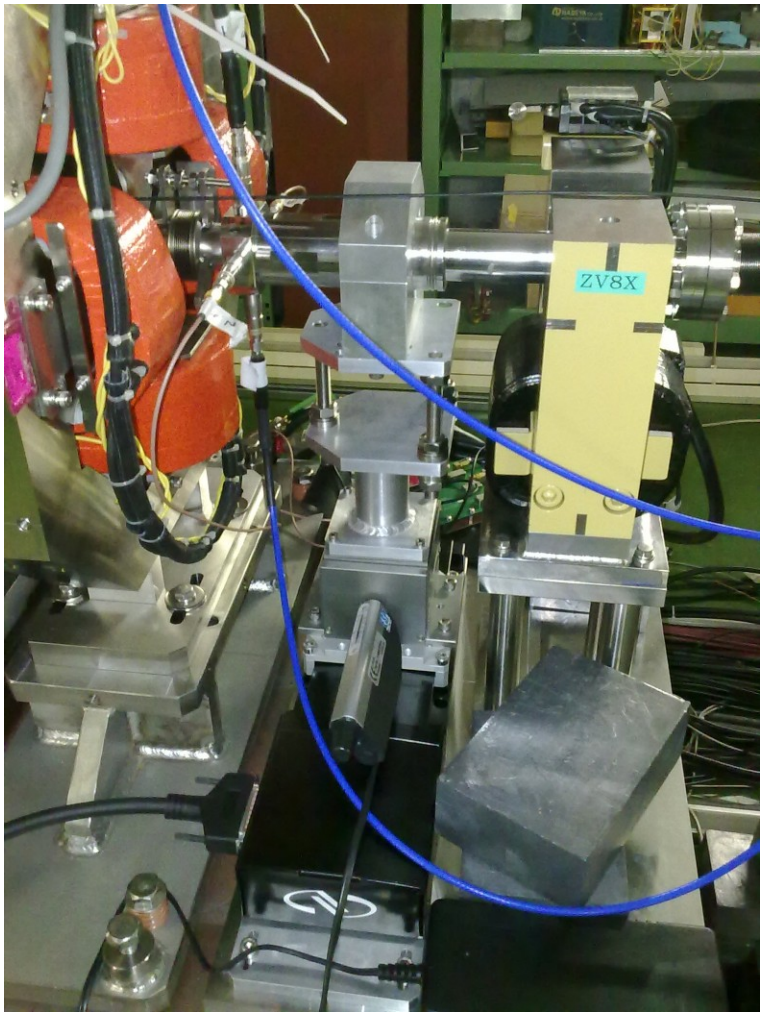
P2 → K1 ('position')
P3 → K2 ('angle')
P3 → K1

Each FONT5 system loop

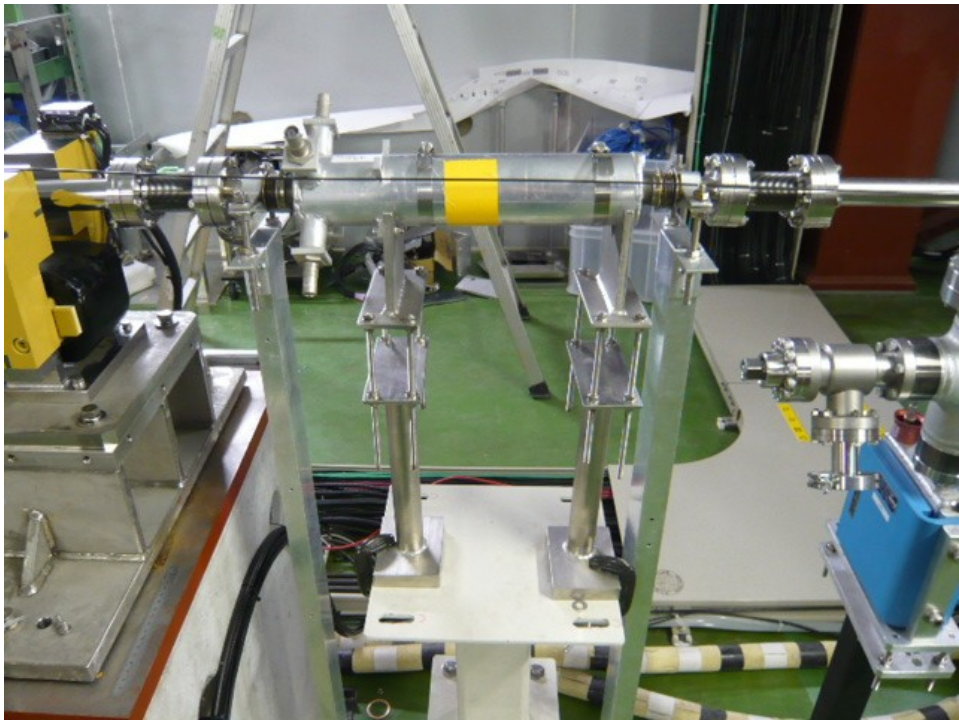
300ns train of bunches separated by 150ns



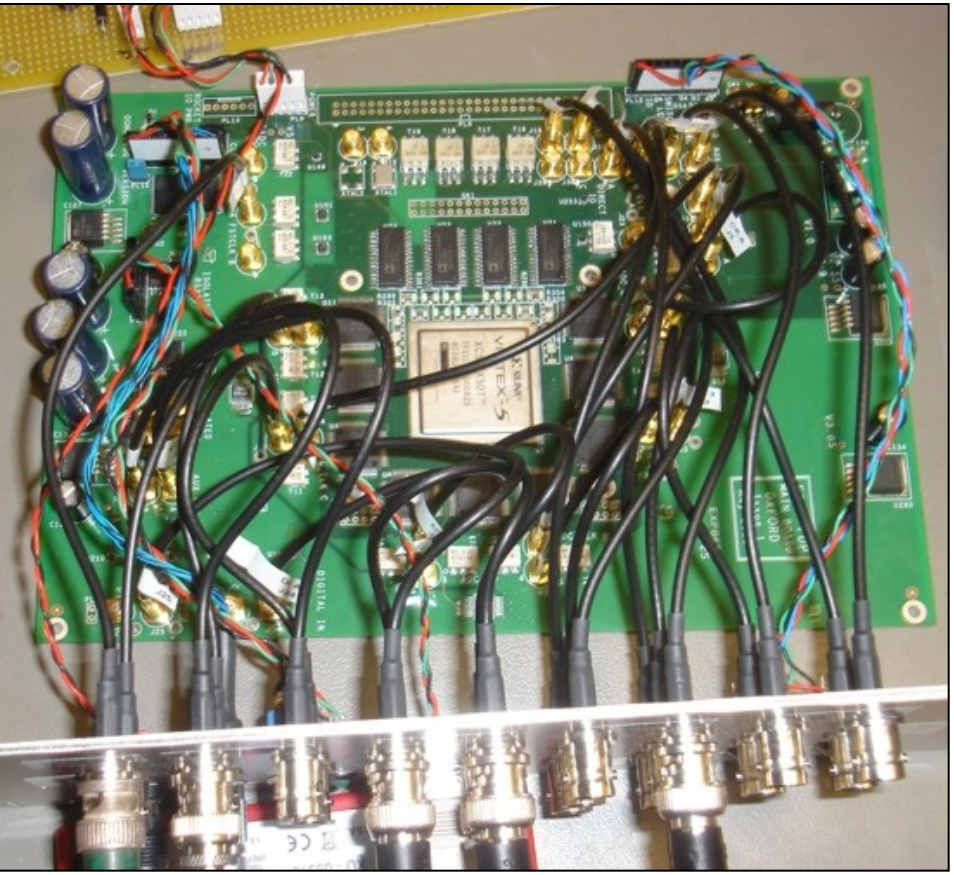
FONT5 beamline hardware



3 new BPMs and 2 new kickers installed in new ATF2 extraction line February 2009; BPM movers installed 2010



New FONT5 digital FB board



Xilinx Virtex5 FPGA

9 ADC input channels (TI ADS5474)

4 DAC output channels (AD9744)

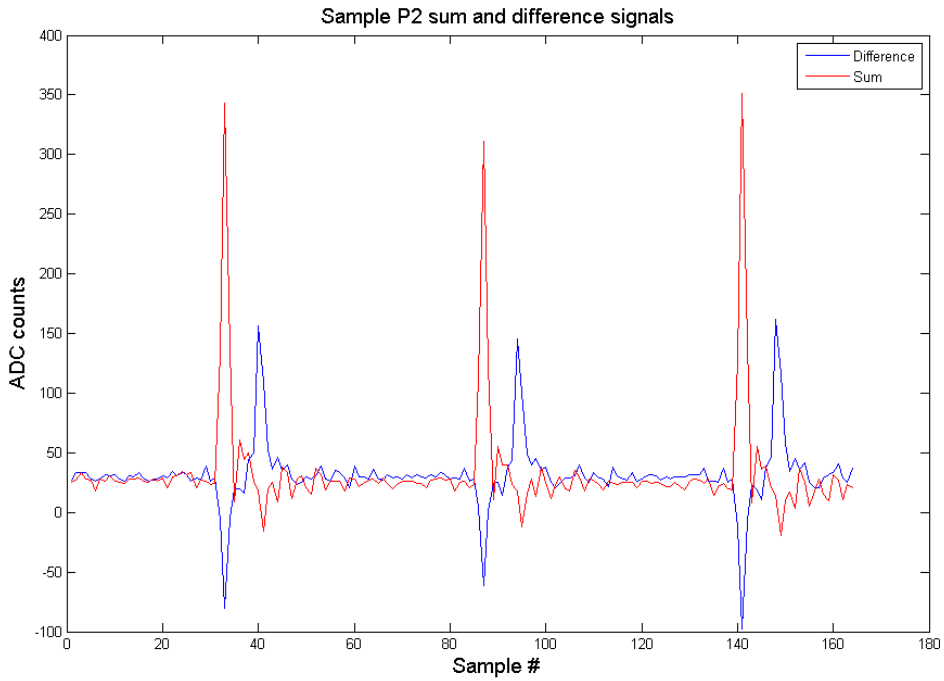
Clocked at 357 MHz phase-locked to beam

4x faster than FONT4

FONT5 DAQ

One damping ring cycle (463ns) data returned each pulse:

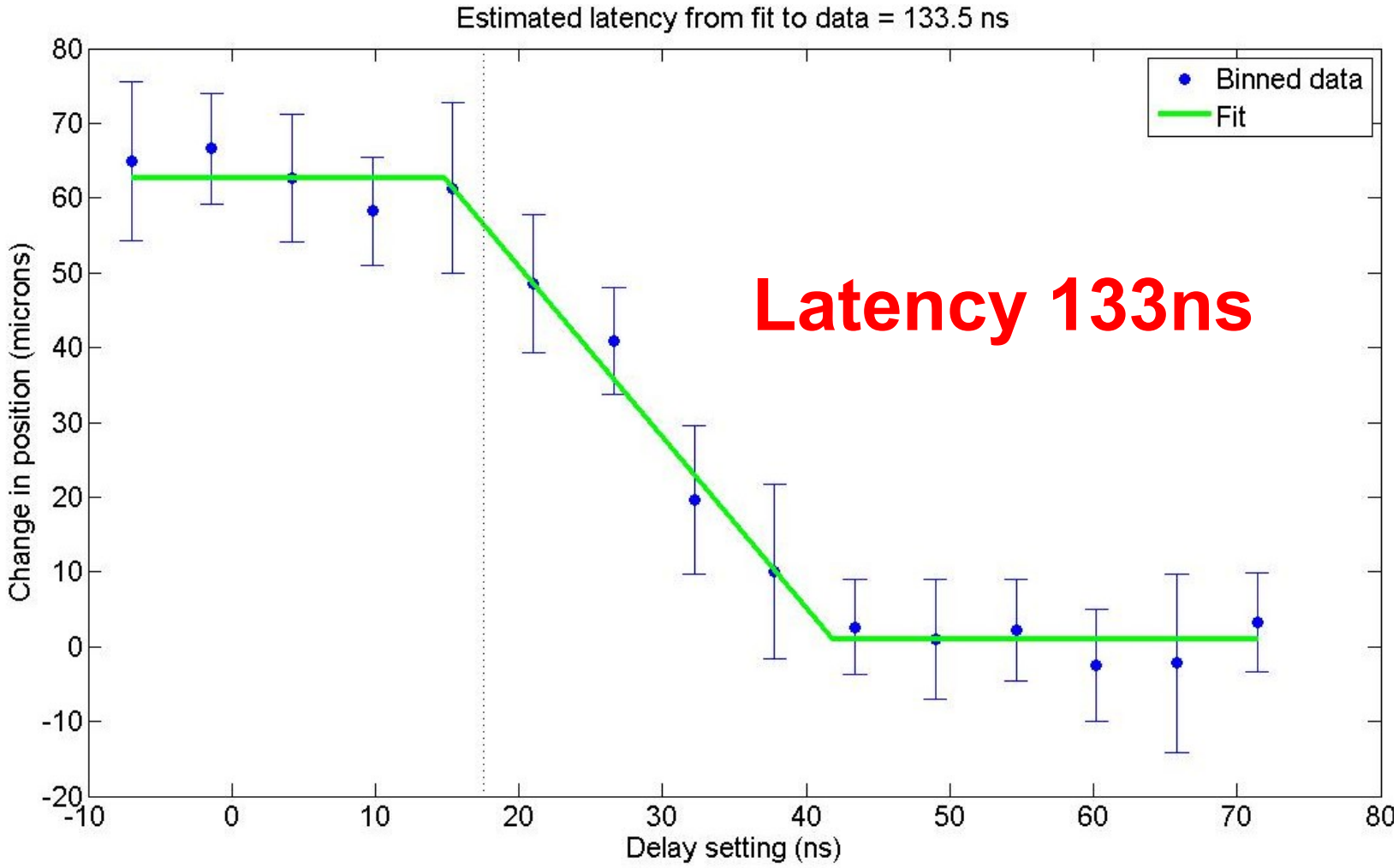
- **RS232 over ethernet**
- **All BPM sum (charge) and difference signals**
- **Absolute sample time adjustable in 70ps taps: accurate peak sampling**
- **Ratio of difference to sum peaks gives y-position**
- **Pedestal subtraction w. on-board trim DACs (no latency gain)**



Outline of FB results

- Latency
- Basic loop performance
- Banana correction
- Coupled-loop FB results
- Next steps

FONT5 latency: P2 → K1 loop



Latency estimate

- Time of flight kicker – BPM: 12ns
- Signal return time BPM – kicker: 32ns

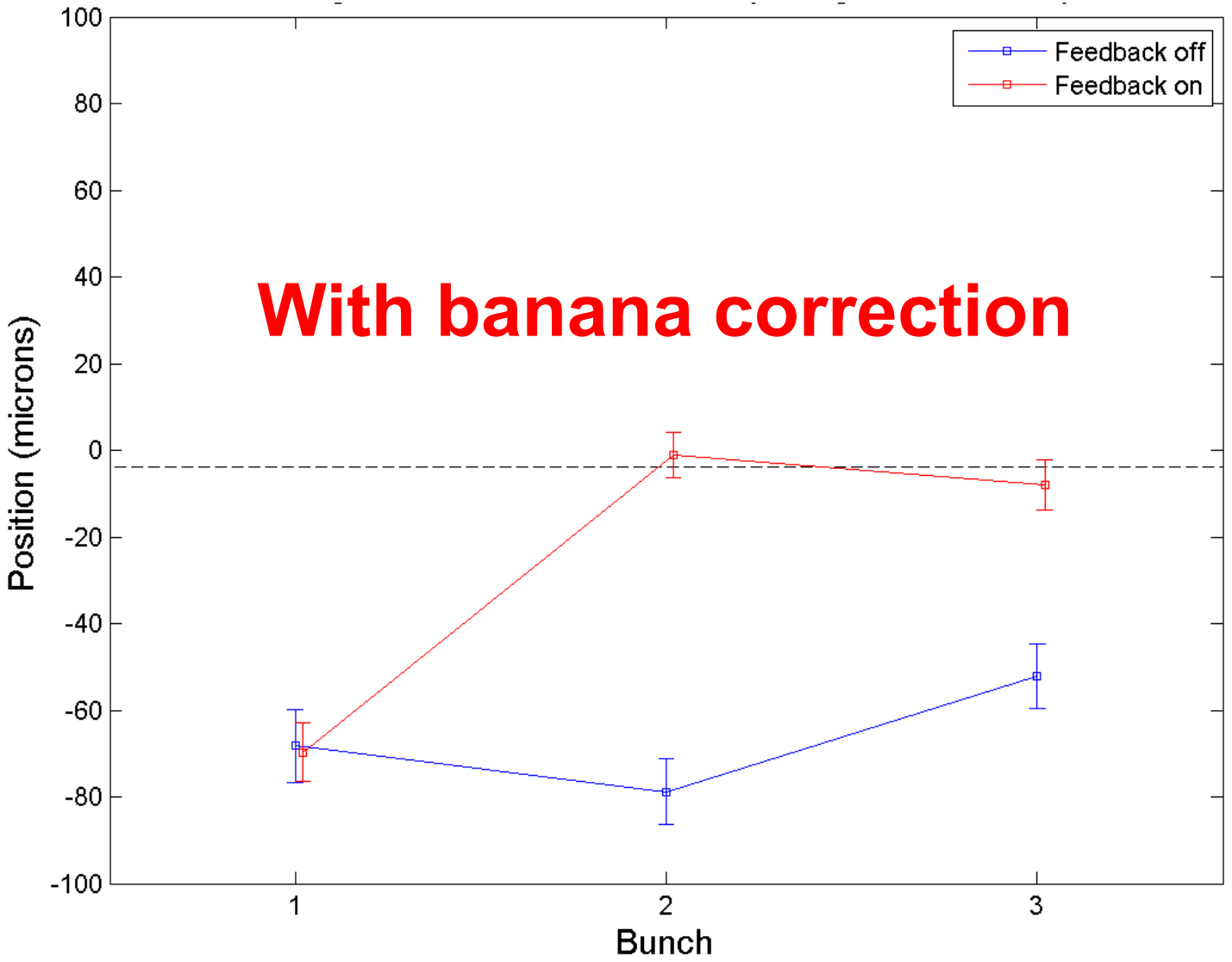
  Irreducible latency: 44ns

- BPM processor: 10ns
- ADC/DAC (4.5 357 MHz cycles) 14ns
- Signal processing (8 357 MHz cycles) 22ns
- FPGA i/o 3ns
- Amplifier 35ns
- Kicker fill time 3ns

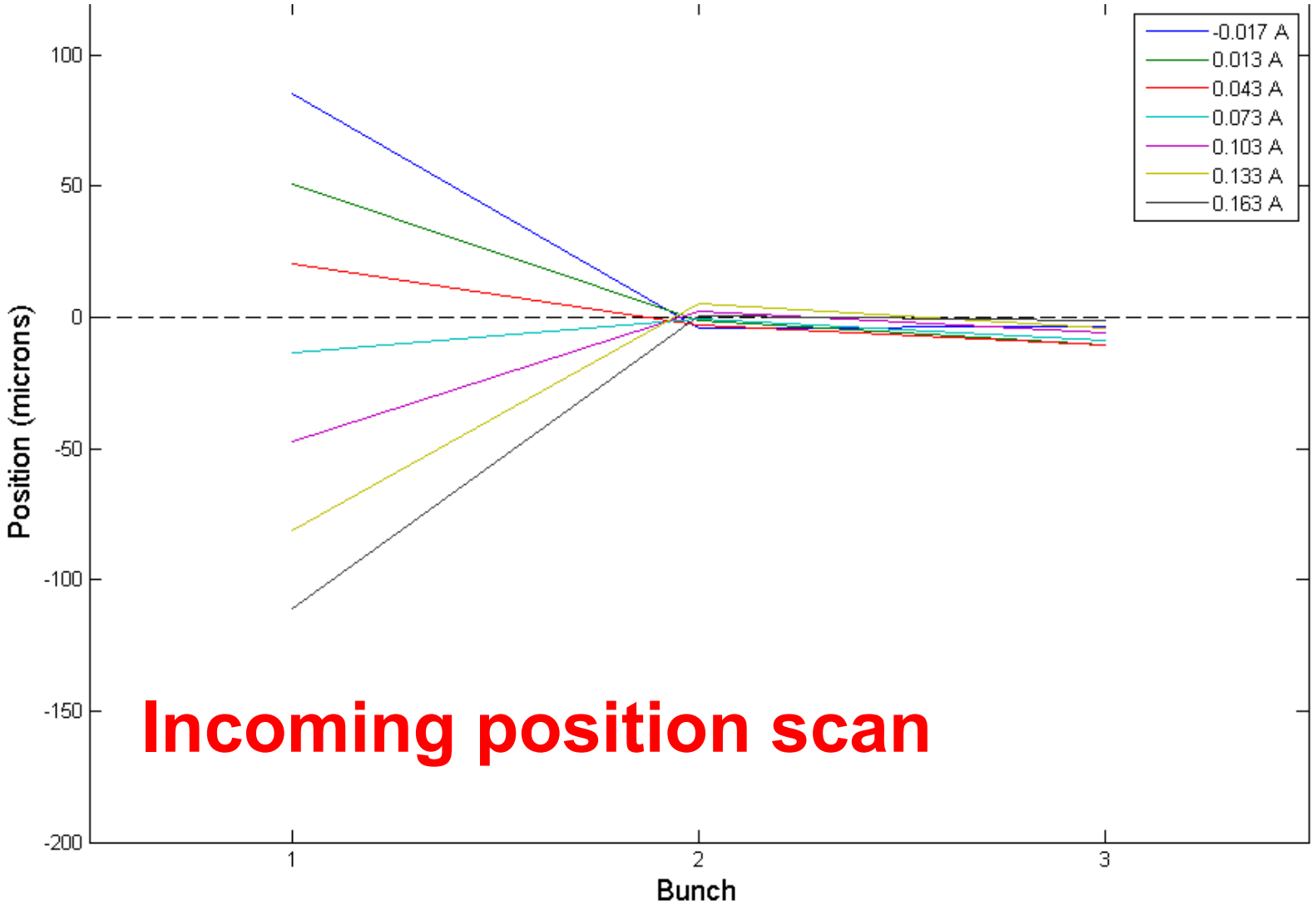
  Electronics latency: 87ns

- Total latency budget: 131ns

P2 → K1 loop performance

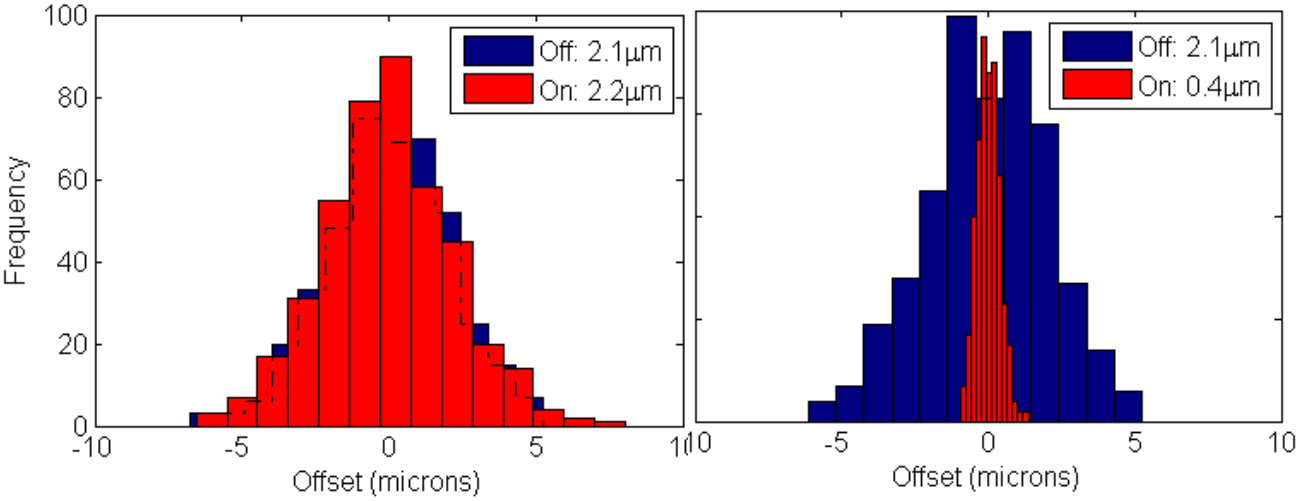


P2 → K1 loop performance



P2 → K1 loop jitter reduction

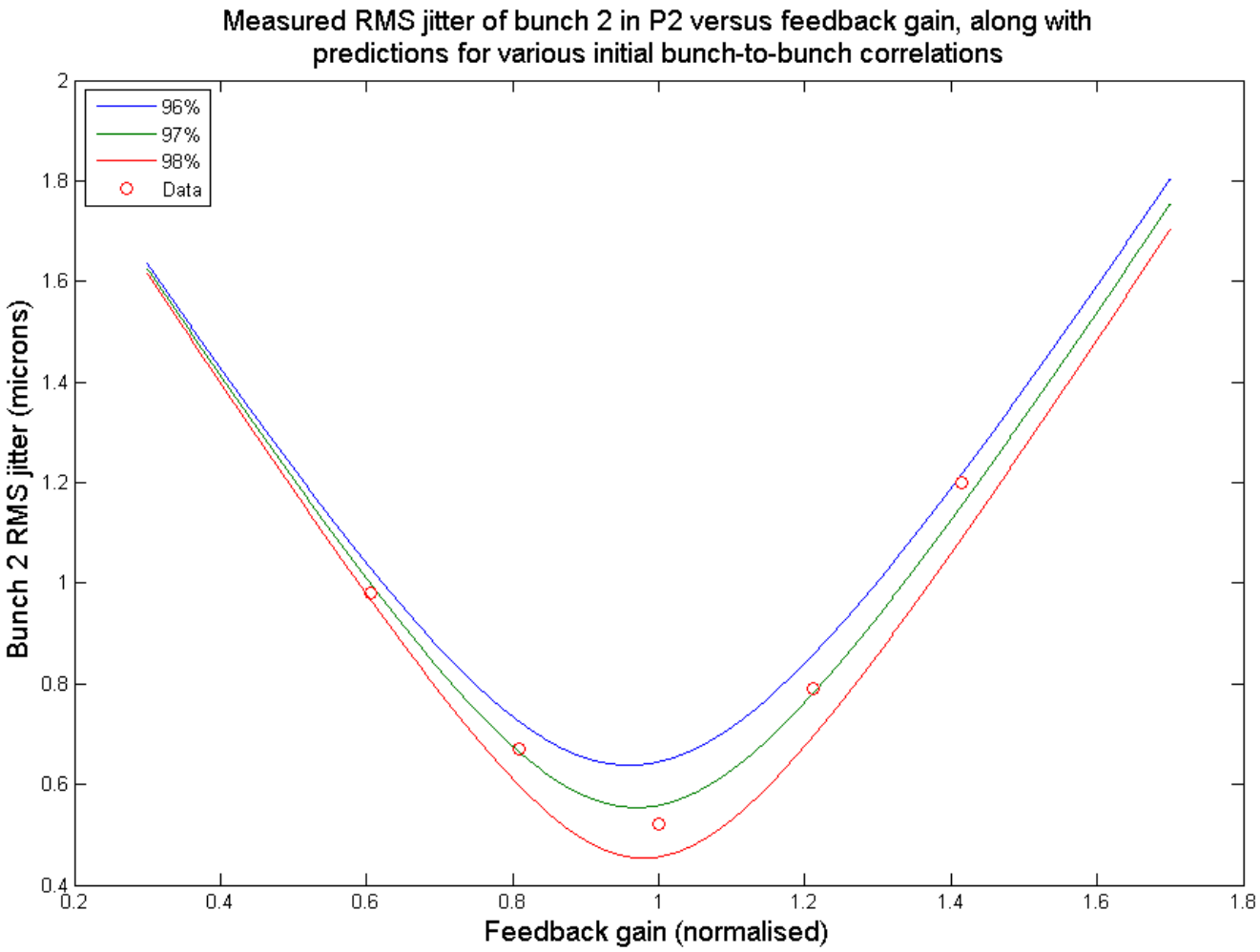
Bunch 1 **Bunch 2**



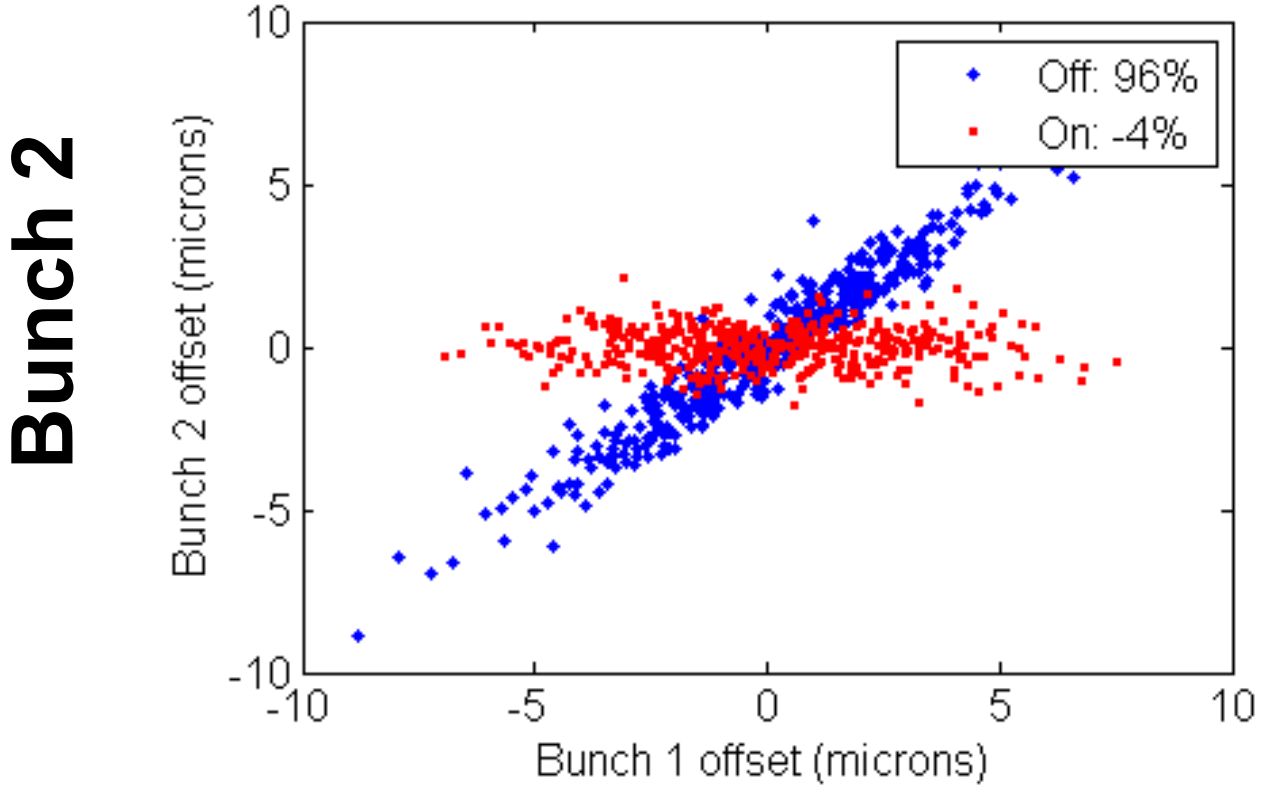
2.1 um → 0.4 um

Factor of 5 jitter reduction

Bunch 2 jitter vs. gain

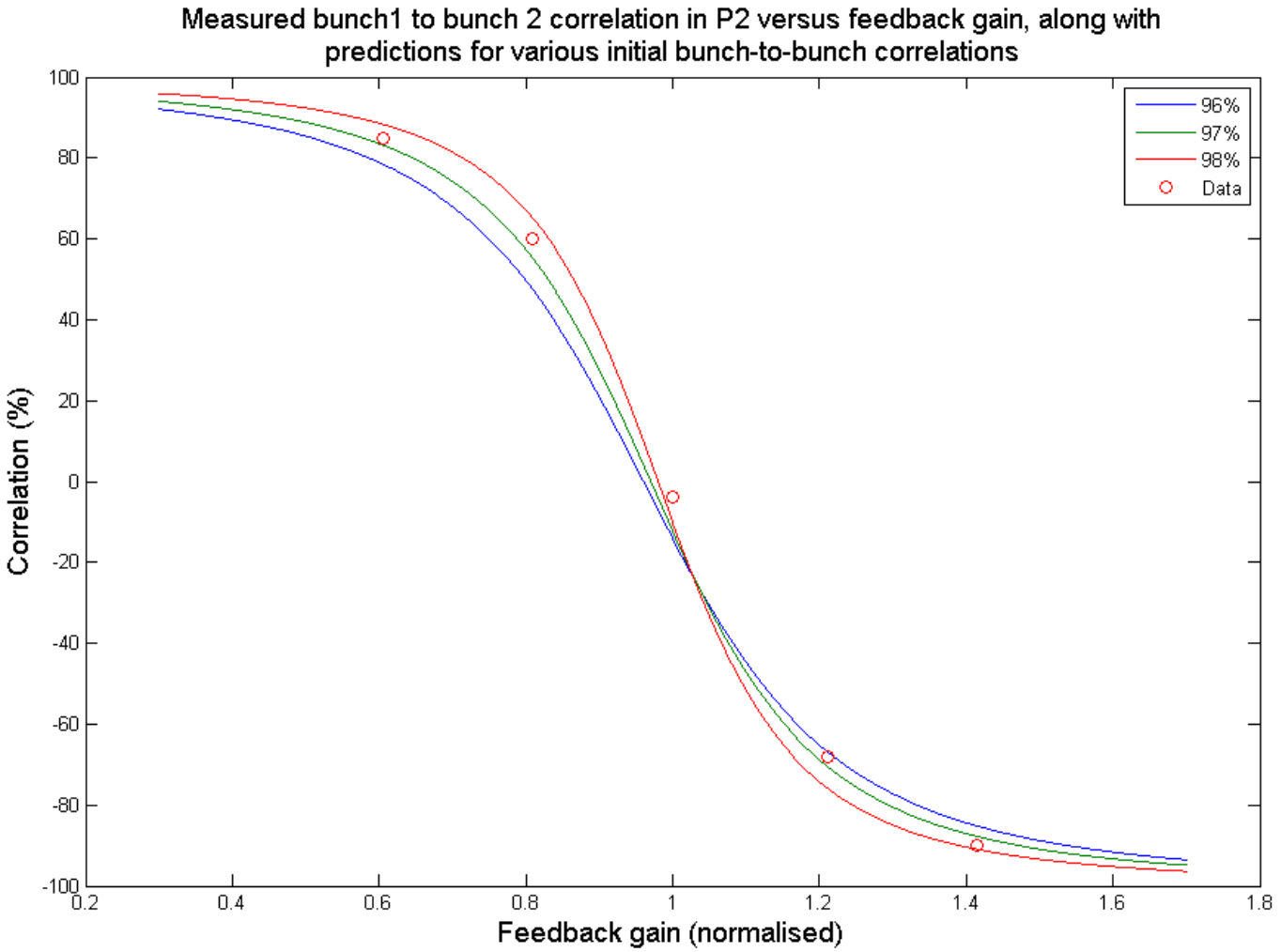


Bunch 1-2 correlations

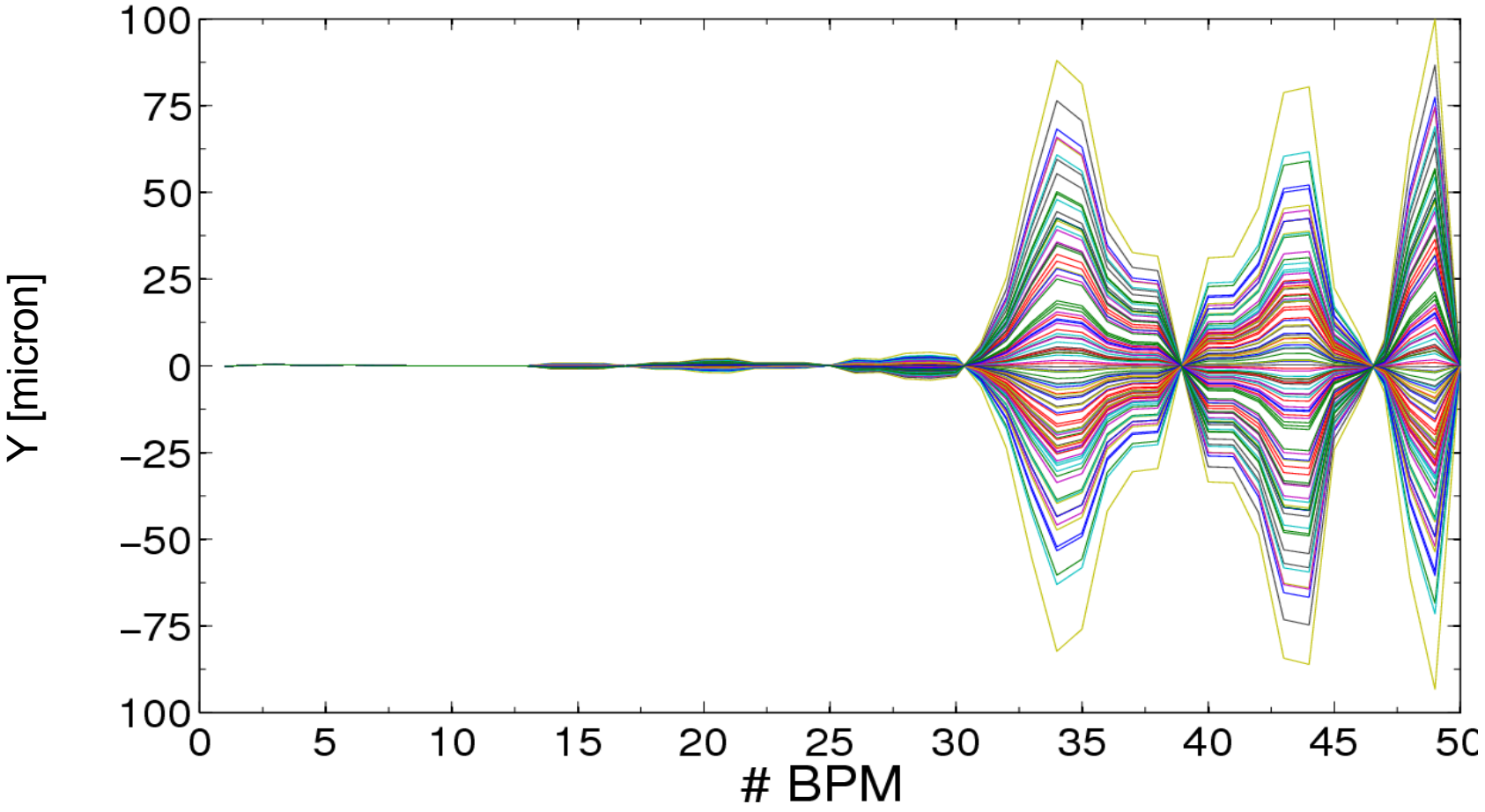


Feedback removes bunch correlations

Bunch 1-2 correlations vs. gain

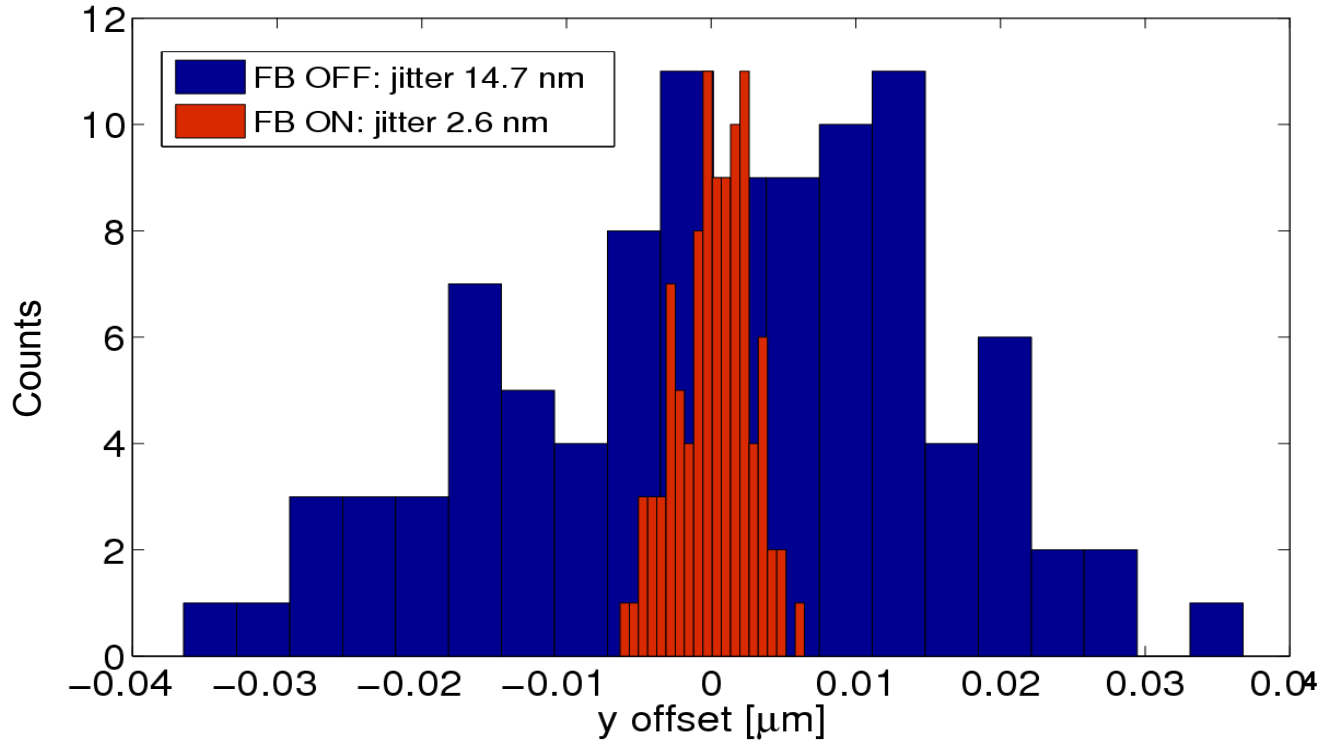


0.4 micron jitter propagation



Jitter propagation to ATF2 IP

Assuming perfect lattice, no additional jitter sources (!)



Summary so far

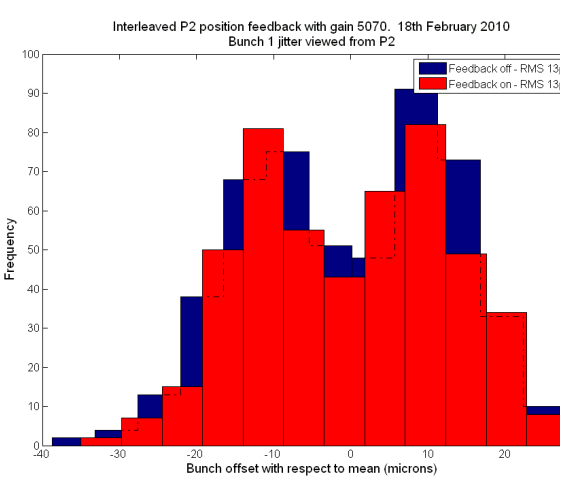
- **These spectacular results were obtained with beam of exceptional quality:**

Incoming train jitter:	**2um**
Bunch 1-2 correlations:	**96%**
Bunch 2-3 correlations:	**80%**

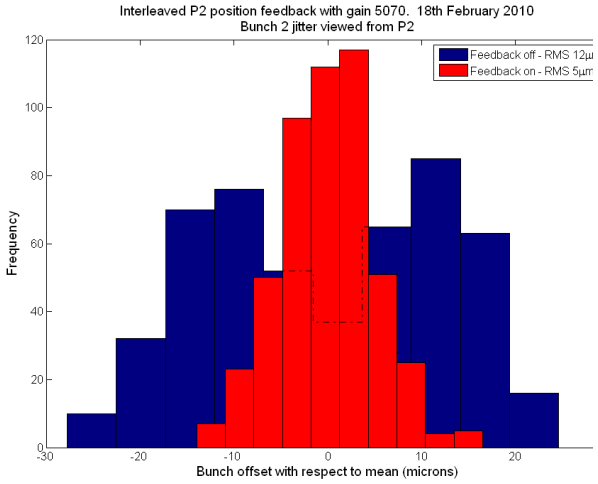
This is NOT typical!

P2 → K1 loop jitter reduction

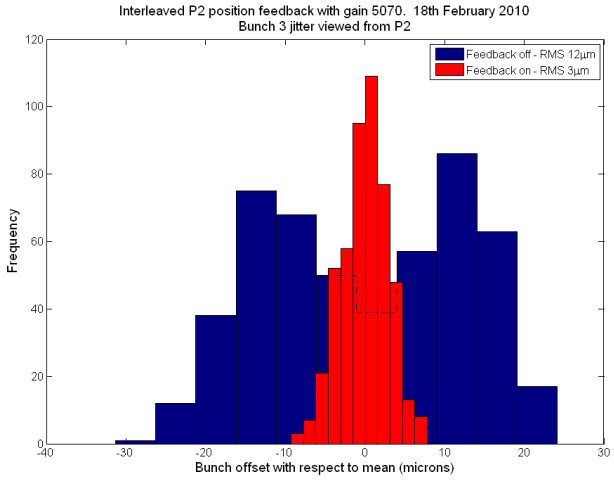
Bunch 1



Bunch 2



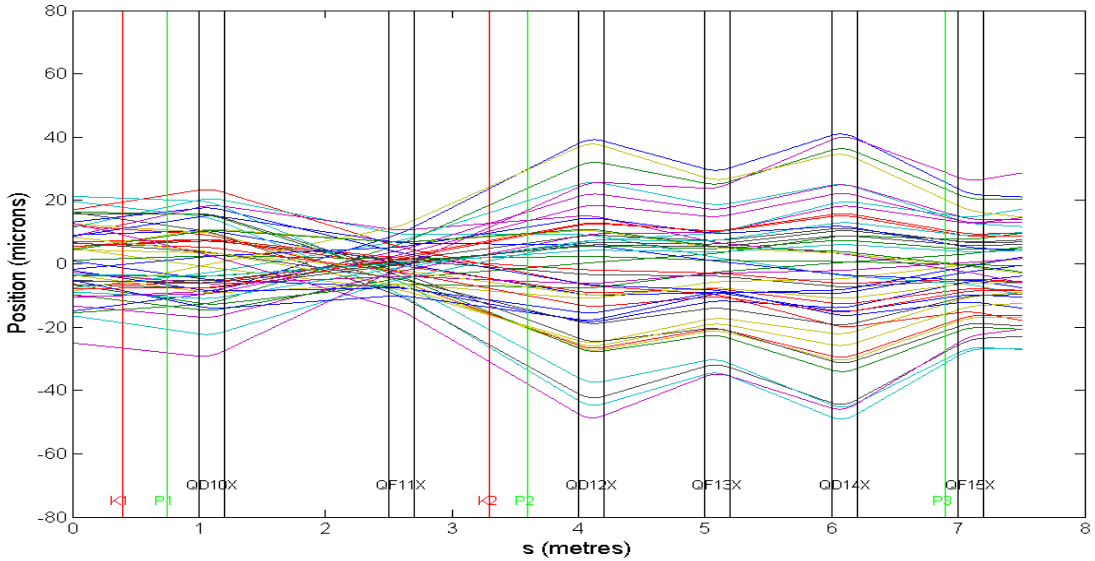
Bunch 3



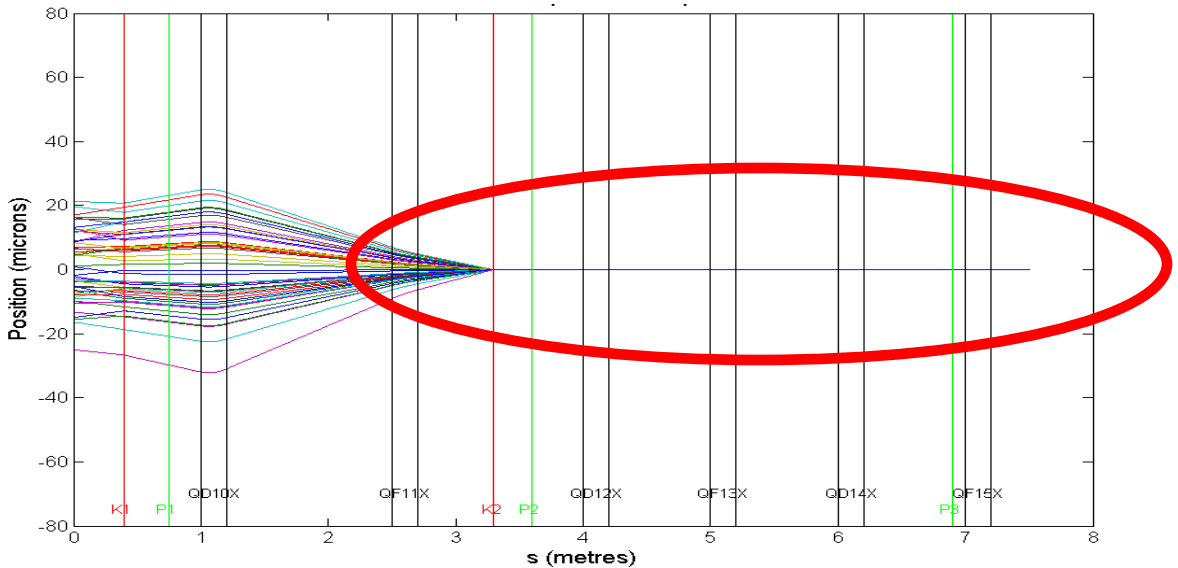
13 um → 5 um → 3 um

FB simulation: P2-K1+P3-K2 coupled

Bunch 1



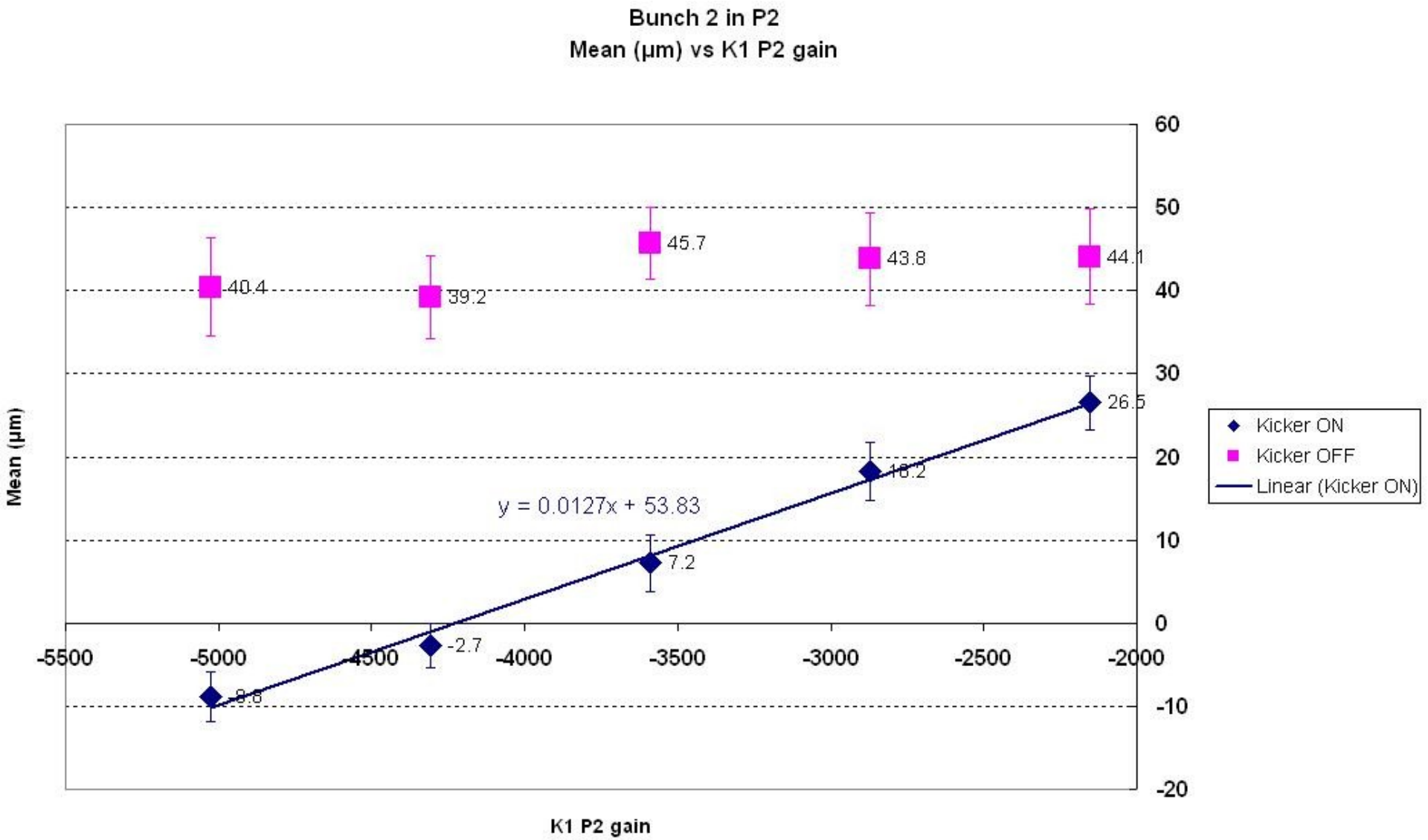
Bunch 2



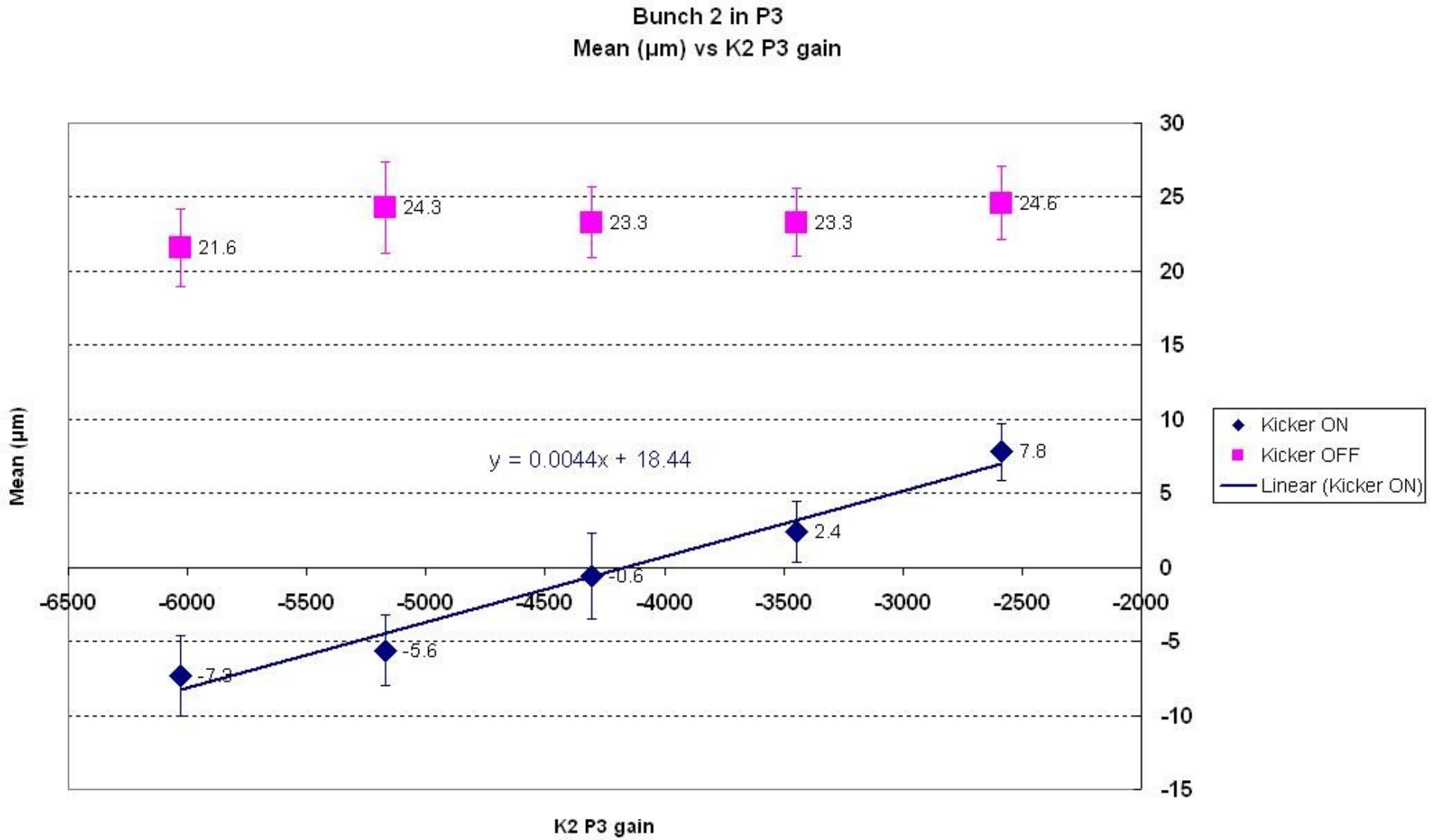
Further Feedback Tests

- K1 – P2 loop
- K2 – P3 loop
- K1 – P2 + K2 – P3 uncoupled
- K1 – P2 + K2 – P3 coupled

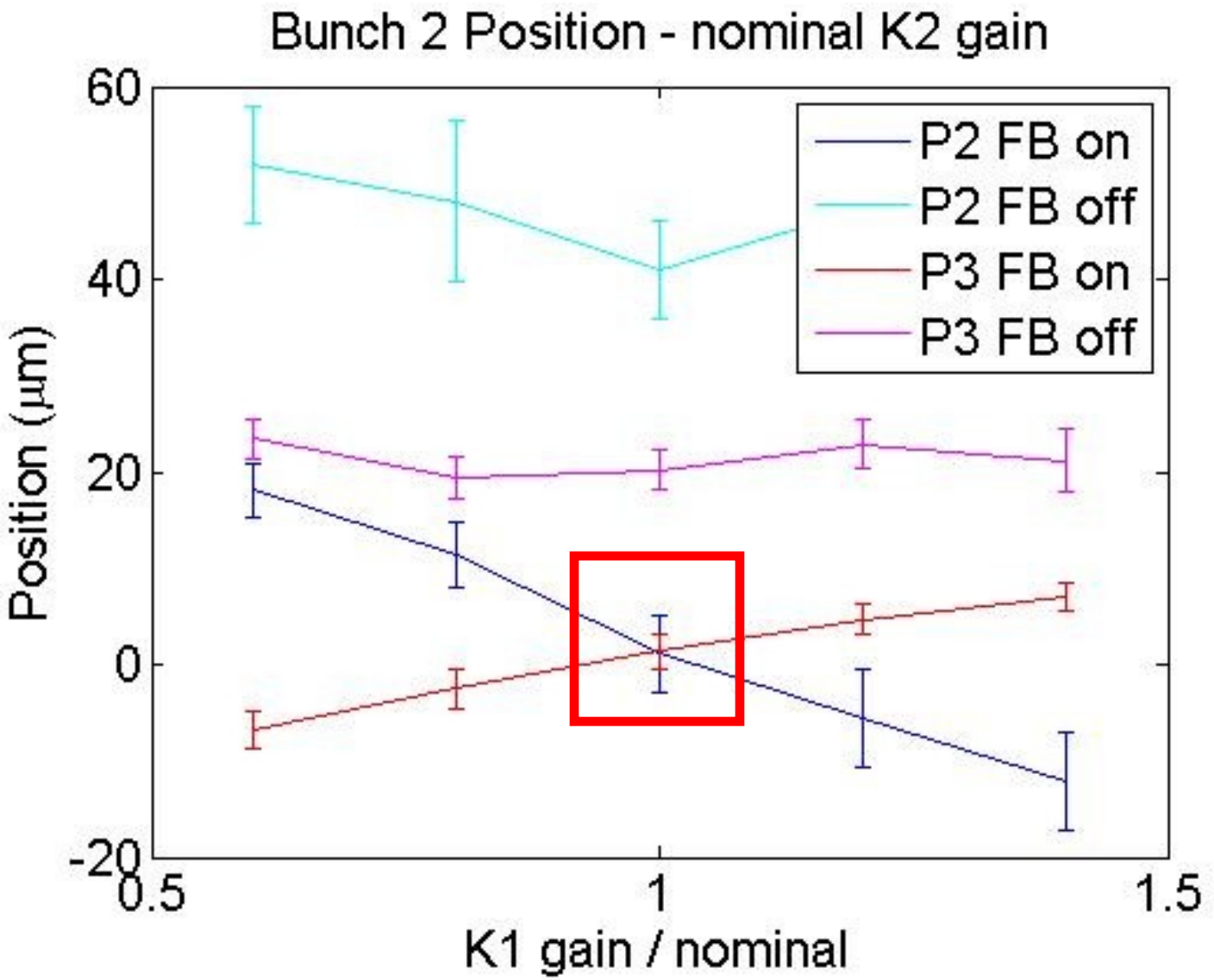
K1 – P2 loop gain scan



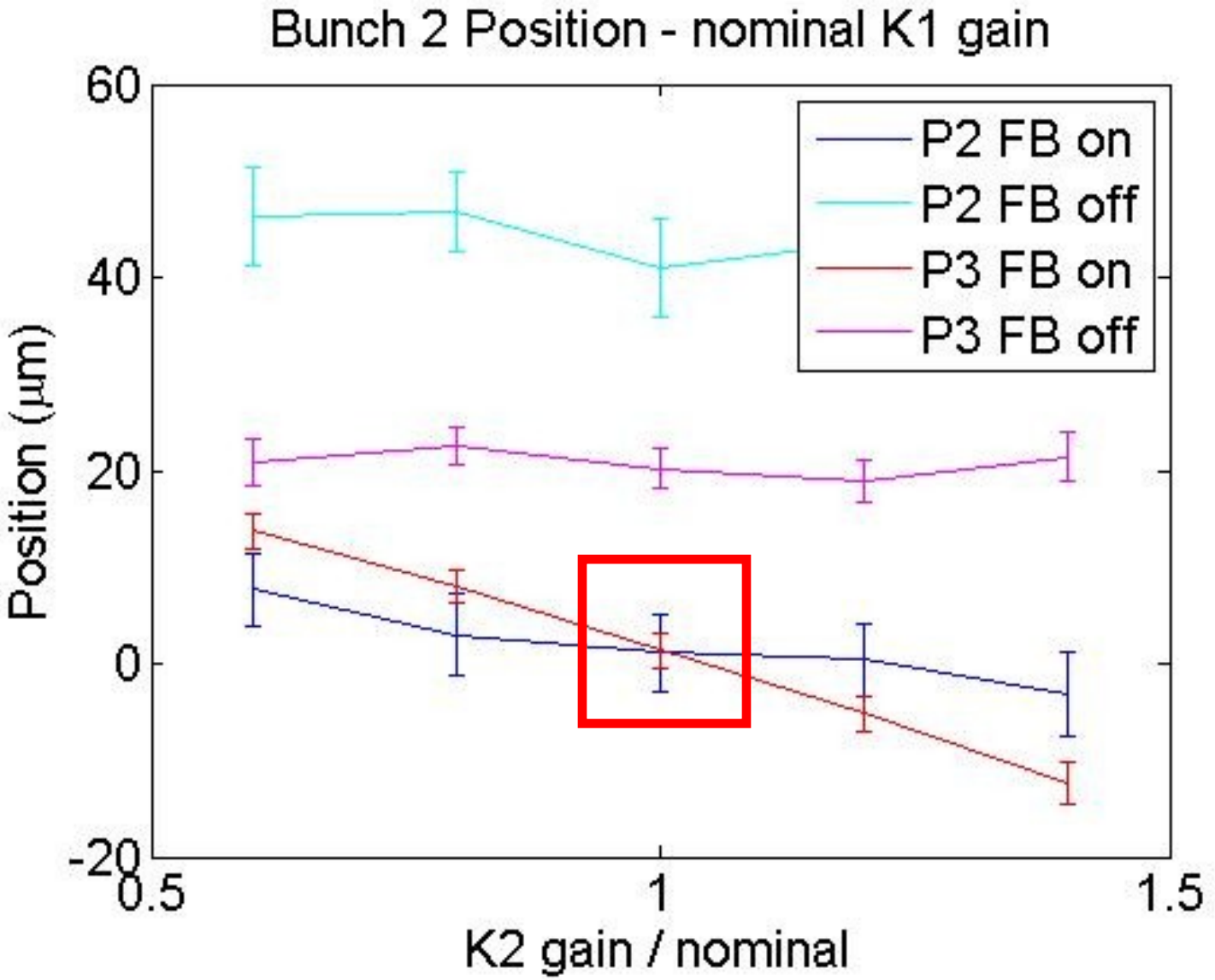
K2 – P3 loop gain scan



K1 – P2 + K2 – P3 coupled: K1 gain scan

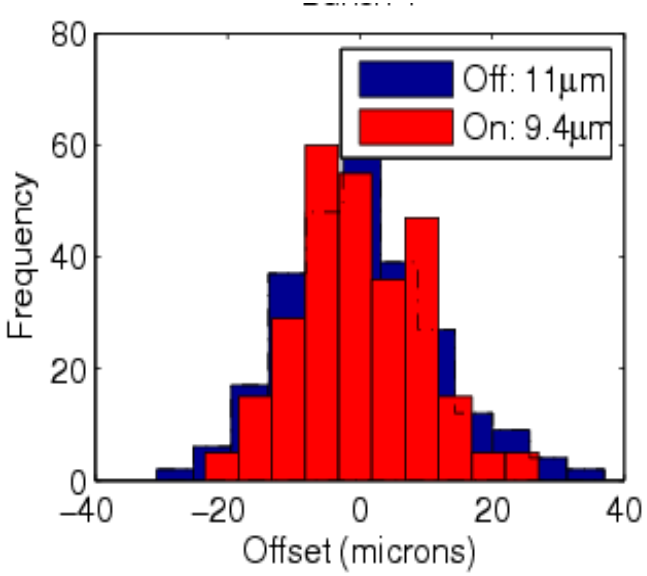


K1 – P2 + K2 – P3 coupled: K2 gain scan

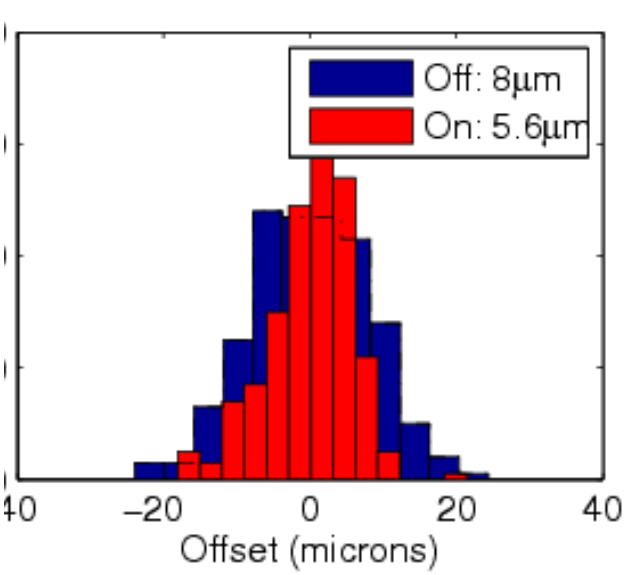


Coupled loop jitter reduction

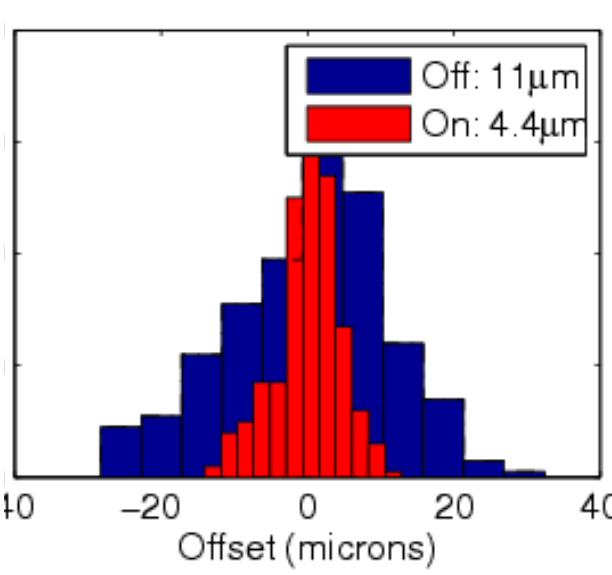
Bunch 1



Bunch 2



Bunch 3

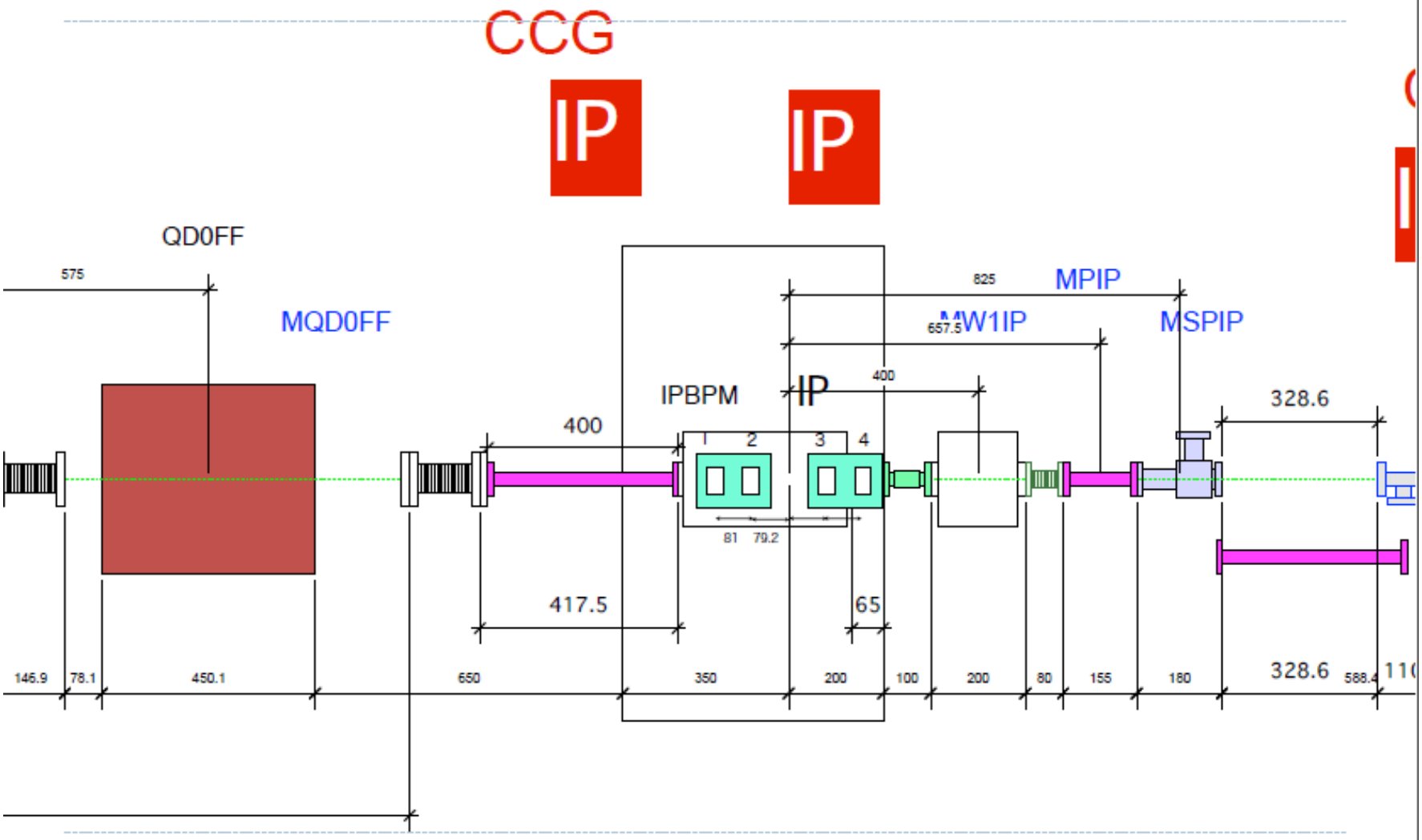


9.4 um → 5.6 um → 4.4 um

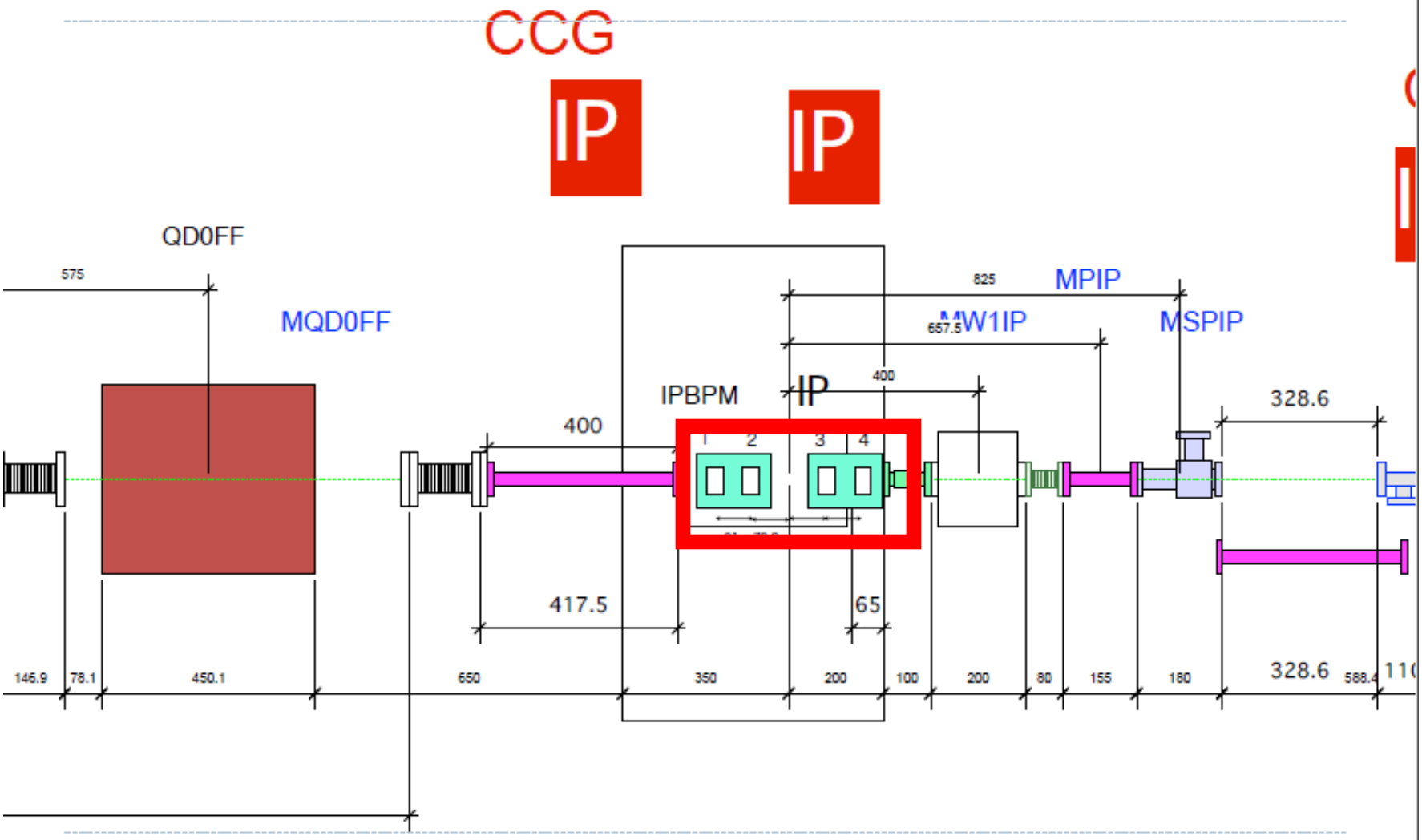
Summary: FONT5

- IP feedback concept well advanced
- Prototype meets ILC technical requirements in terms of BPM resolution, kicker drive and latency
- Future effort focussed on achieving ATF2 goals

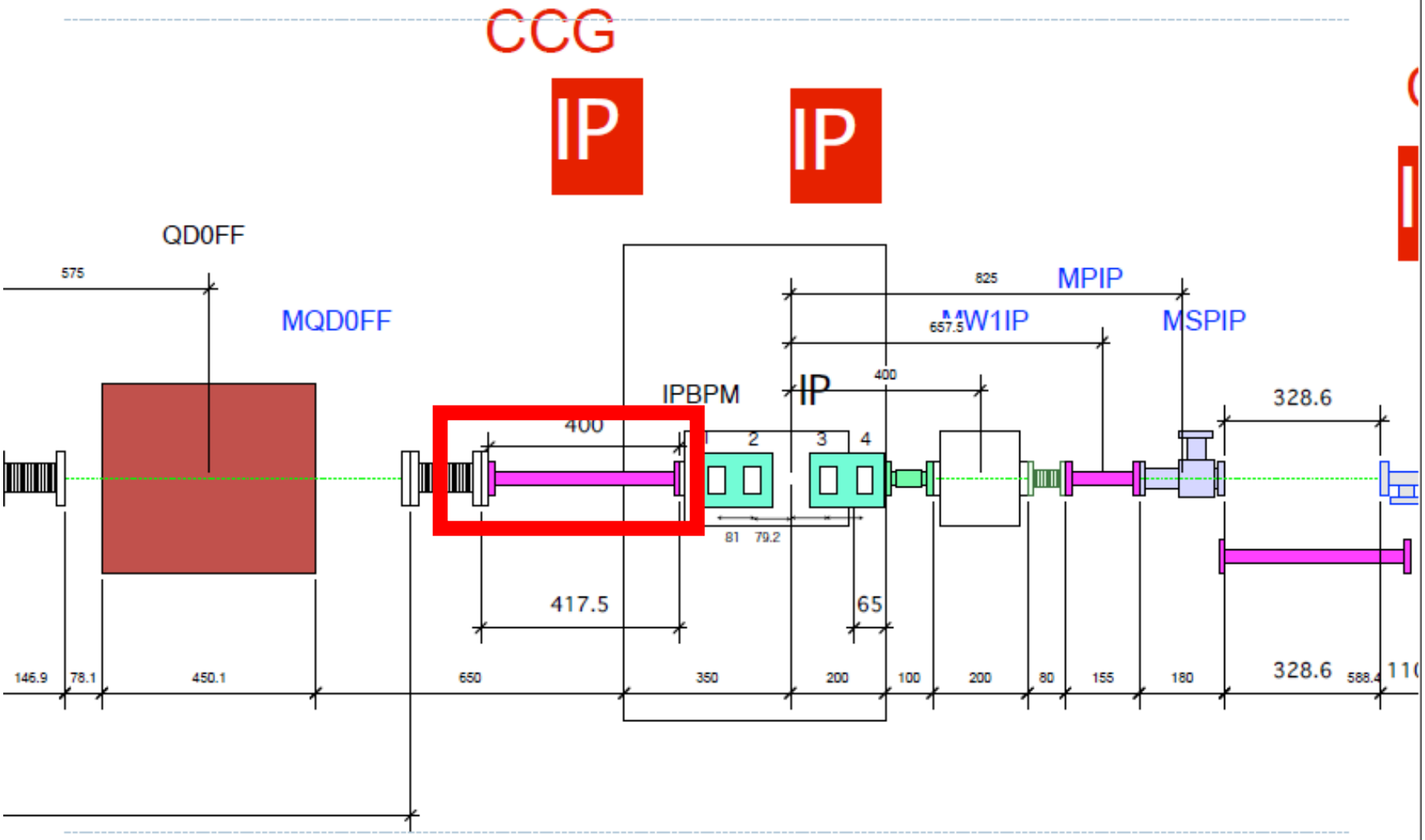
IPBPM configuration



IPBPM configuration



Kicker location



Some working assumptions (1)

- Kicker centre ~ 0.5m upstream of IPBPM
- Kicker aperture 40mm (?)
- Kicker length ~ 15 cm (?)
- Matched 50 Ohm terminations

→ Half of current FONT5 sensitivity:

0.5 urad / Amp

(can easily scale from above assumptions)

Some working assumptions (2)

Dynamic correction range:

- **Beam size 37 nm**
- **Beam y jitter ~ beam size (?)**
- **2 sigma correction**

  → 70 nm @ IP = 140 nrad kick

  → drive current = 0.15/0.5 ~ 0.3 A (per strip)

Some working assumptions (3)

Amplifier:

- **Peak power = 0.3 **2 x 50 = 5 W per strip**

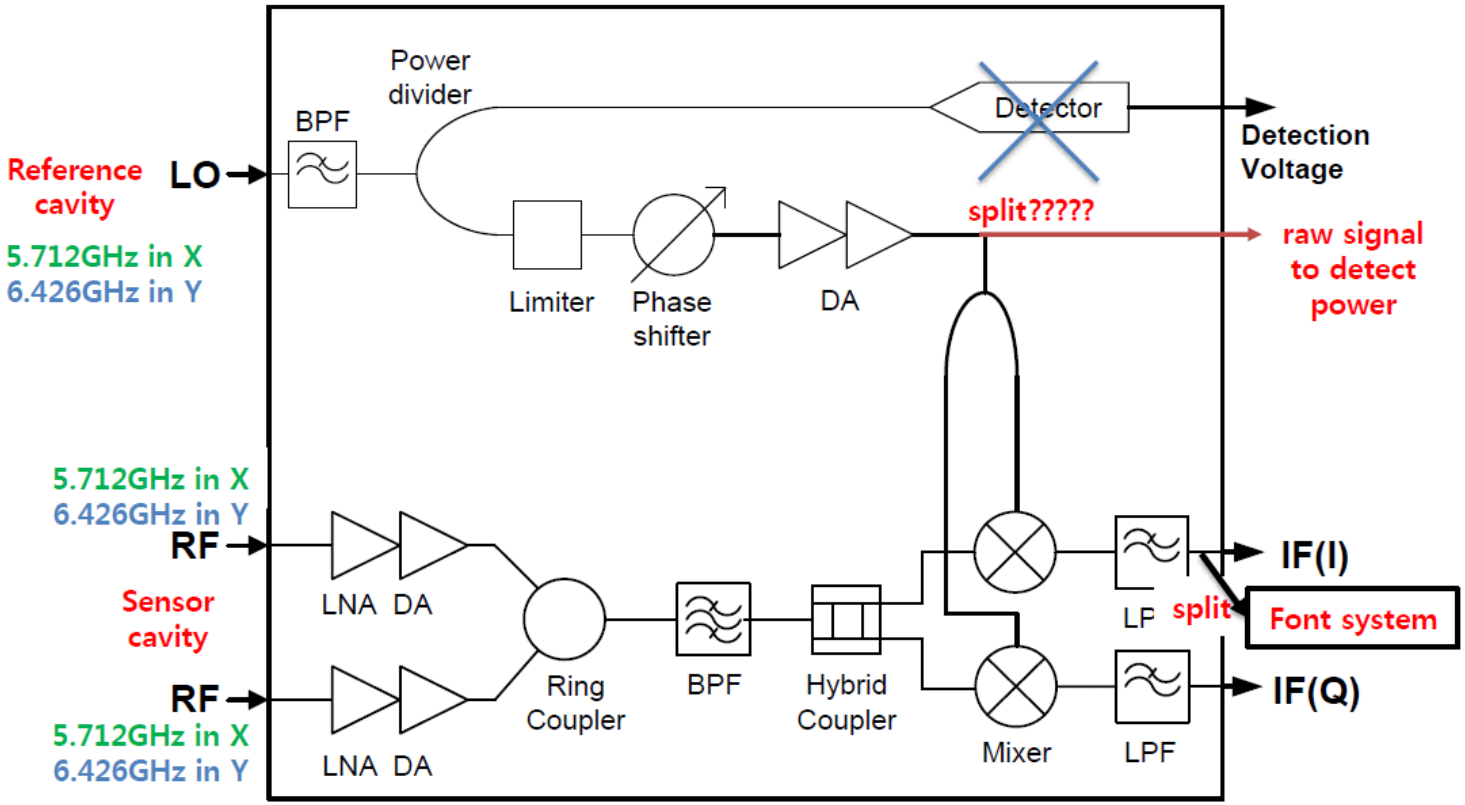
  → eg. Minicircuits: 10W, 5 → 500 MHz

- **Low latency (5 ns)**
- **Output can be pulsed for long bunch train**
- **No margin for kick**

IPBPM electronics

(Aeyoung Heo)

1. Improved conversion gain
2. Low Noise Figure
3. Narrow Bandwidth
4. Latency: less than 20ns

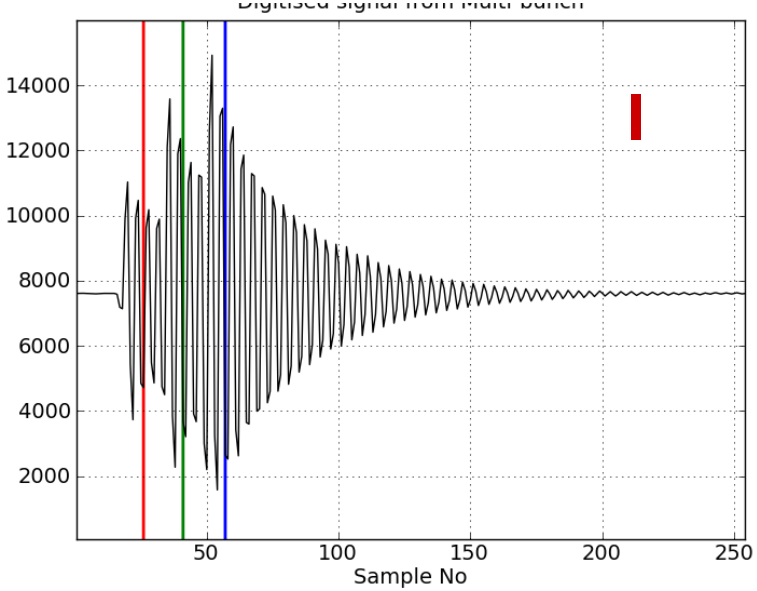


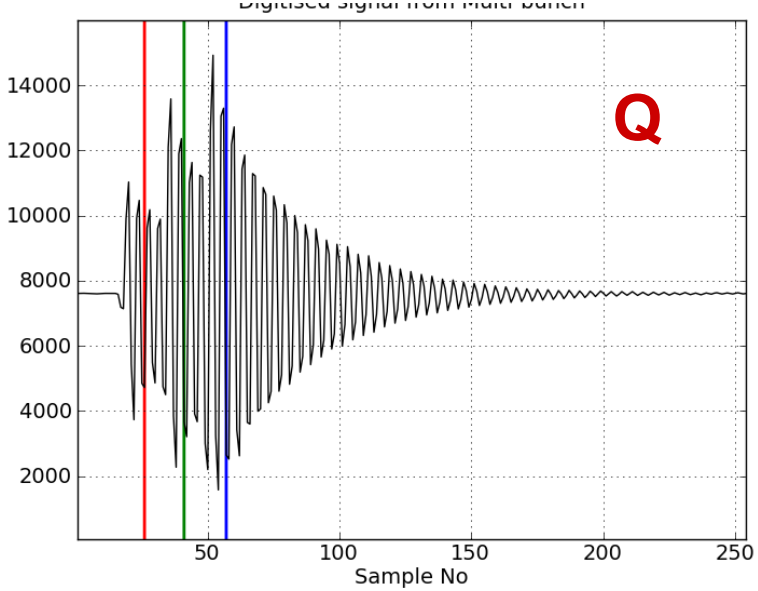
Digitisation of IPBM signal

- Digitise I and Q signals
- Derive amplitude and phase

  → charge-independent position signal
- FONT5 ADCs (TI ADS5474) clocked at 357 MHz
- Very high bandwidth sample point
- Sample time adjustment sensitivity c. 100ps

FONT Digitisation





$$I(n) = \frac{A_{BPM}}{A_{REF}} \cos(\phi_{BPM} - \phi_{REF})$$

$$Q(n) = \frac{A_{BPM}}{A_{REF}} \sin(\phi_{BPM} - \phi_{REF})$$

Joshi

Digitisation of IPBM signal

- Digitise I and Q signals
- Derive amplitude and phase

  → charge-independent position signal
- FONT5 ADCs (TI ADS5474) clocked at 357 MHz
- Very high bandwidth sample point
- Sample time adjustment sensitivity c. 100ps
- Up- and downstream IPBPM signals needed

Latency estimate

• Amplifier (as described)	5ns
• Kicker fill (15cm)	0.5ns
• Beam flight time amplifier → IPBPM	2ns
• Cables (3 x 1.5m?)	23ns
• IPBPM electronics	40ns?
• Digital processing	60ns
Total	**131ns**

Summary of ATF2 IP FB

- Conceptual design for IP FB system
- System parameters look feasible
- Critical parameters:

  dynamic correction range, bunch spacing
- Digitisation of IPBPM I and Q signals is easiest approach
- Technical details need to be finalised:

  locations of BPM + kicker, kicker aperture,

  cable runs …

Extra material

- Conceptual design for IP FB system
- System parameters look feasible
- Critical parameters:

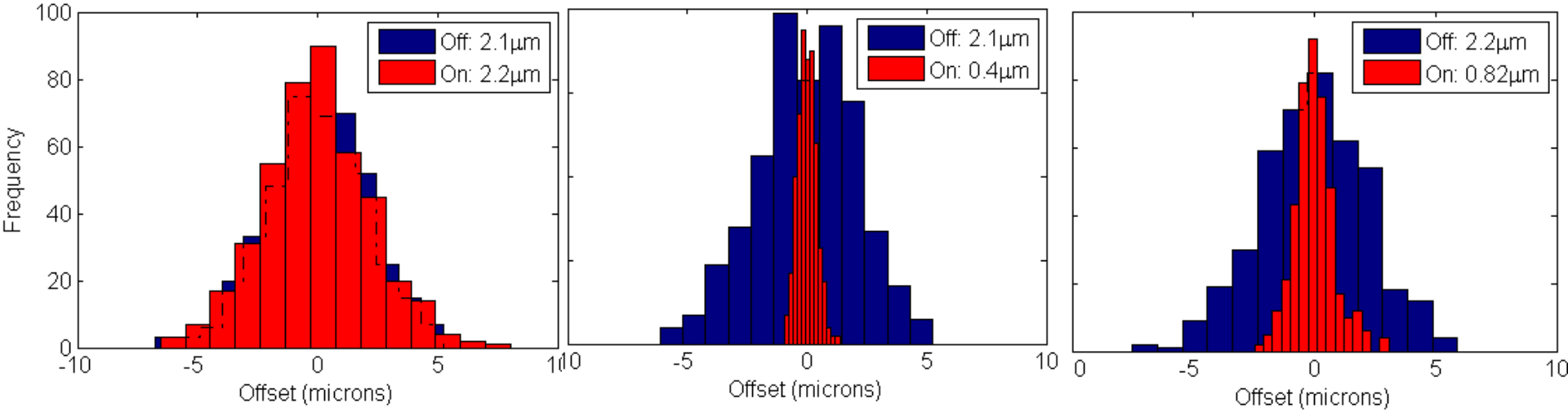
  dynamic correction range, bunch spacing
- Digitisation of IPBPM I and Q signals is easiest approach
- Technical details need to be finalised:

  locations of BPM + kicker, kicker aperture,

  cable runs …

P2 → K1 loop jitter reduction

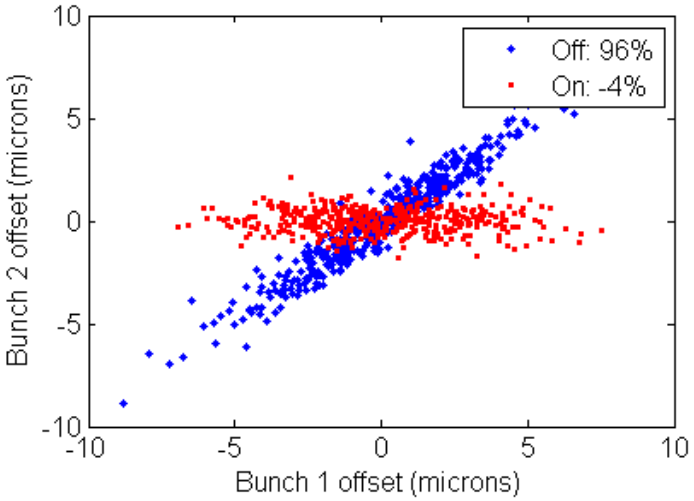
Bunch 1 **Bunch 2** **Bunch 3**



2.1 um → 0.4 um → 0.8 um

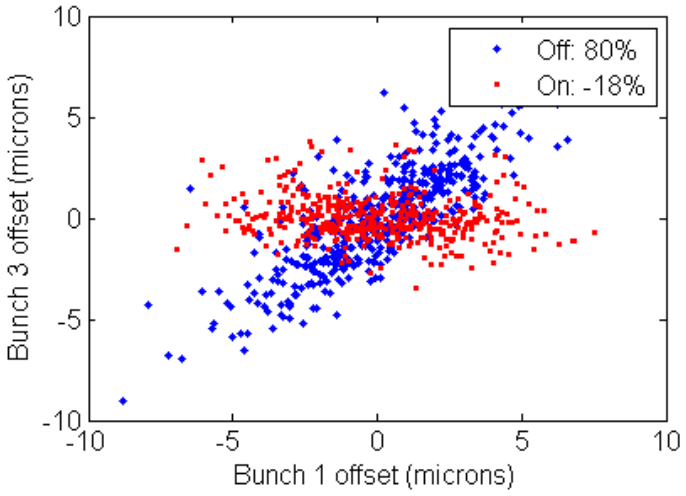
Bunch correlations

Bunch 2



Bunch 1

Bunch 3



Bunch 2