Concept and status of the CALICE AHCAL engineering prototype

Mark Terwort

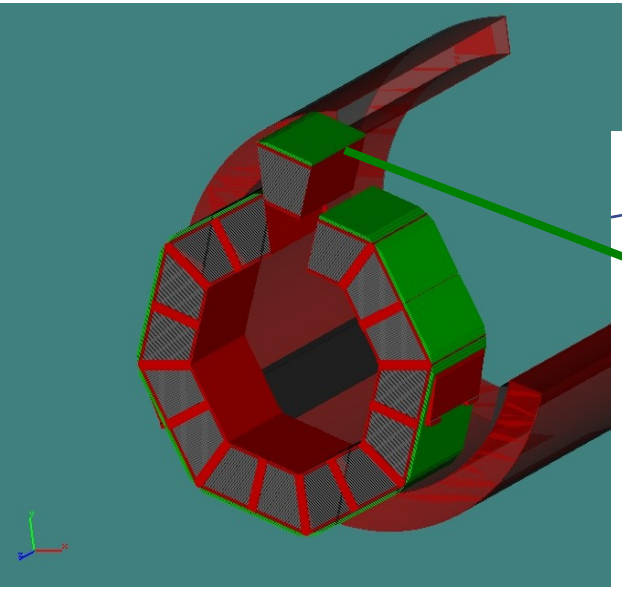
ALCPG Workshop

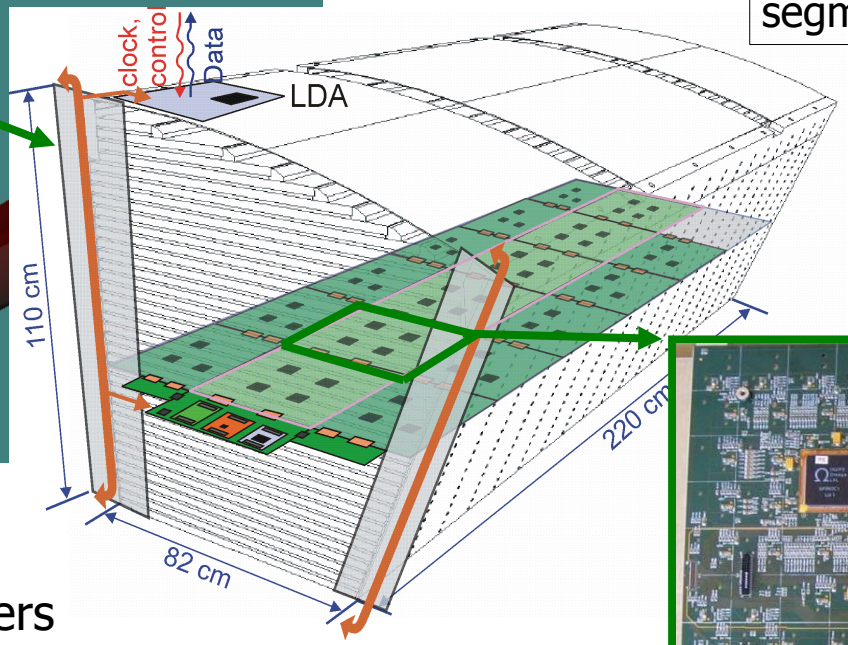
March 22nd, 2011

- Status of components/DESY activities
  - Tiles and LED calibration system
  - SPIROC auto-gain tests
  - DAQ integration
- Summary and outlook

The engineering AHCAL prototype

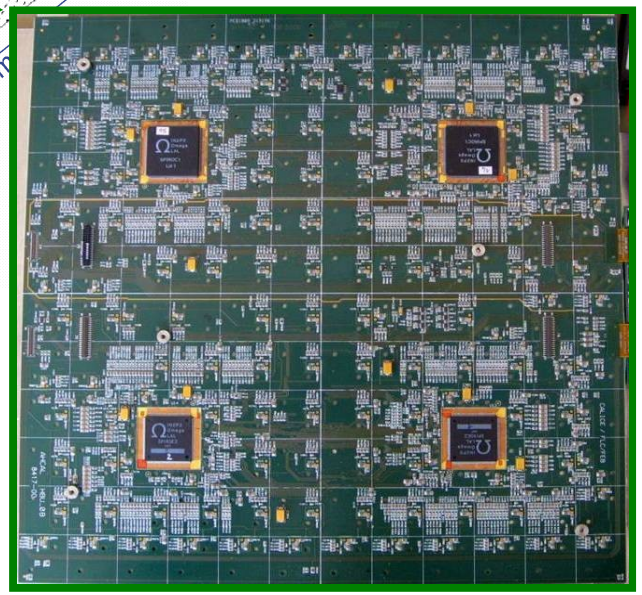
Development of scalable LC detector based on successful experience with physics prototype





Octagonal shape, 16 equivalent wedges, segmented in two along z

PCB with 4 SPIROCs, 144 scintillator tiles, SiPM readout



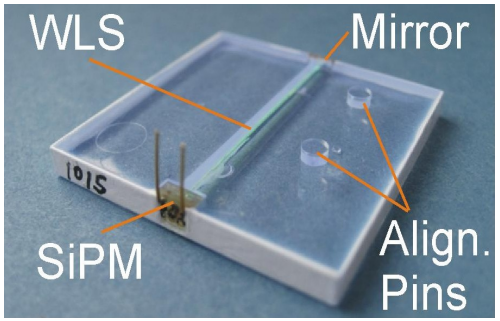
Challenges:

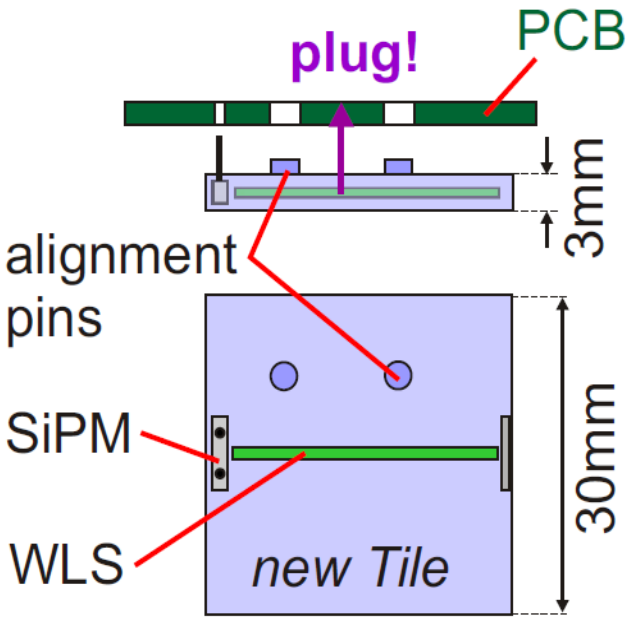
- No spacer between layers
- Minimize dead material between wedges
- Minimize gap between barrel and endcap

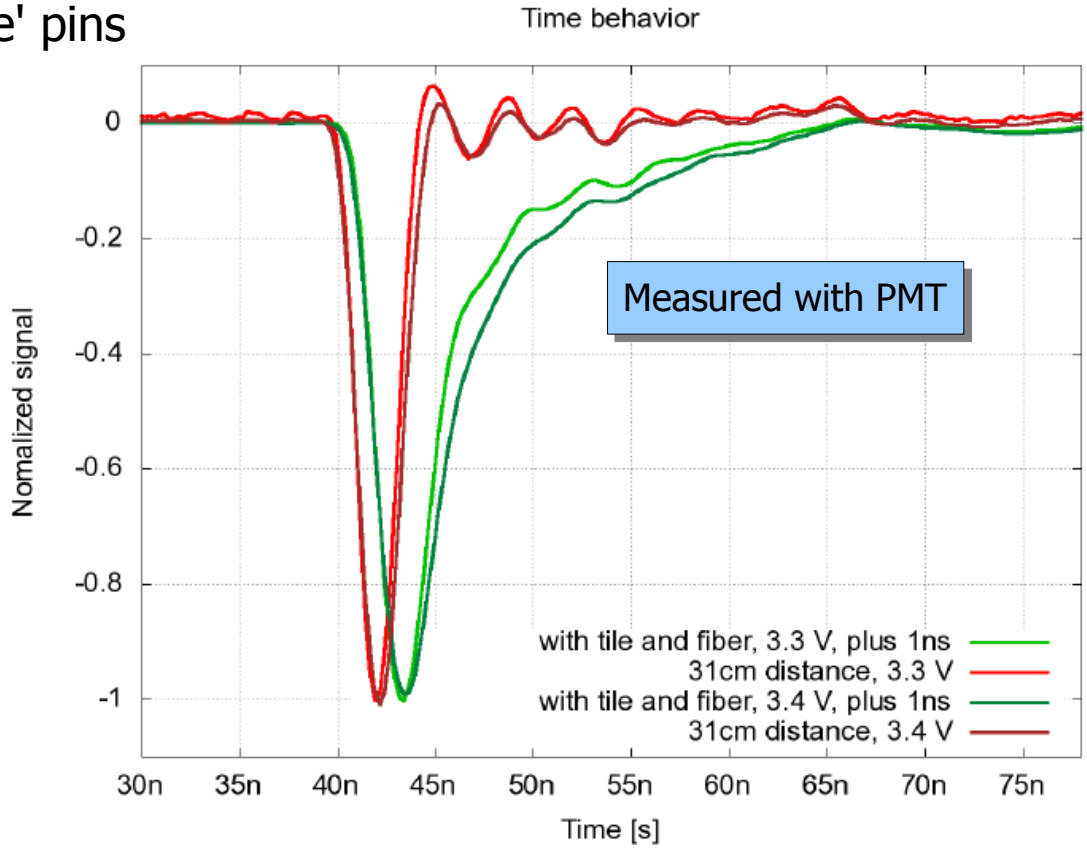
→ Integrated readout electronics

Scintillating tiles

- Signal sampled by scintillating tiles
  → 3x3x0.3cm^3, 2592 tiles per layer
- Wavelength shifting fiber, since SiPMs most efficient for green light
- Plugged into PCB with 'lego-like' pins
  → Nominal tile distance 100µm

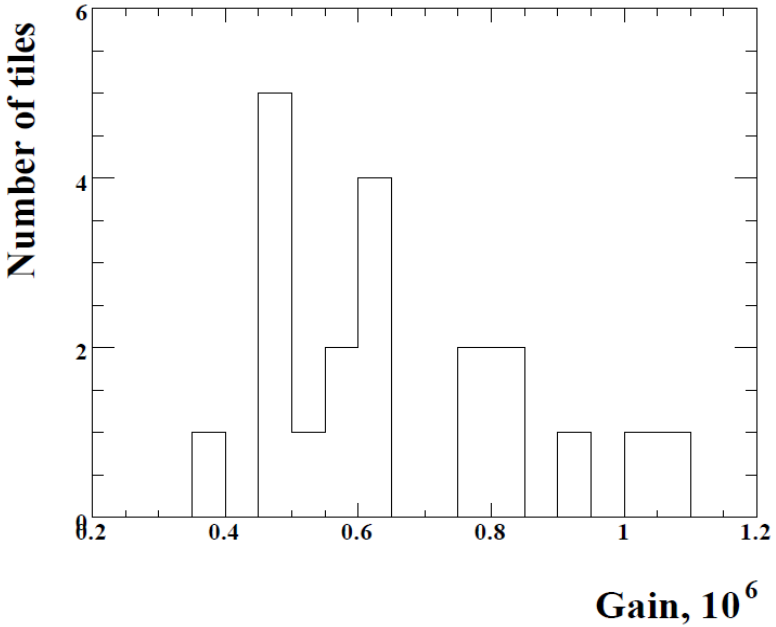


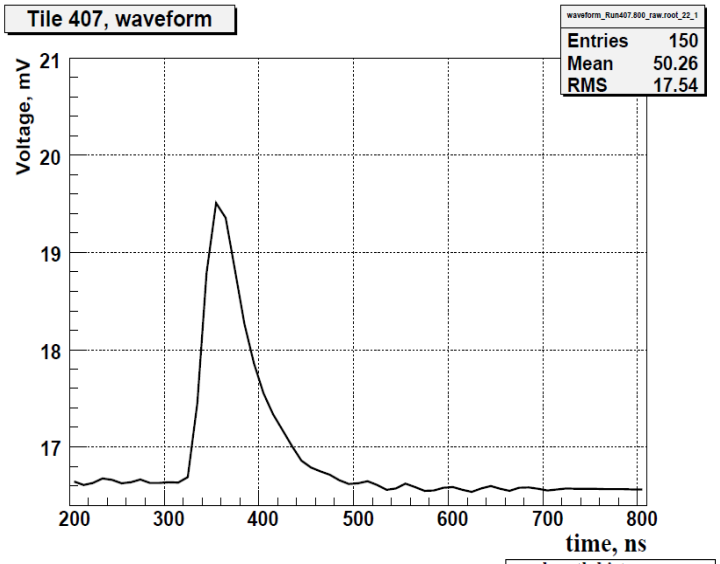


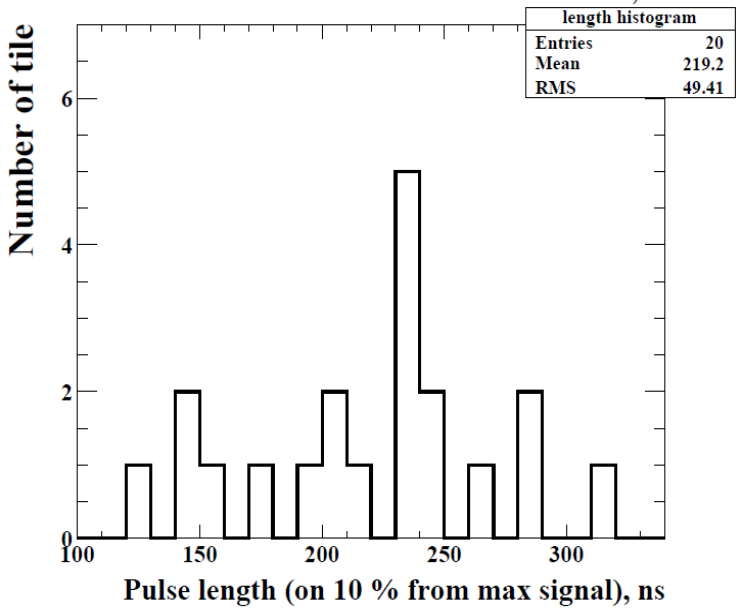


Scintillating tiles

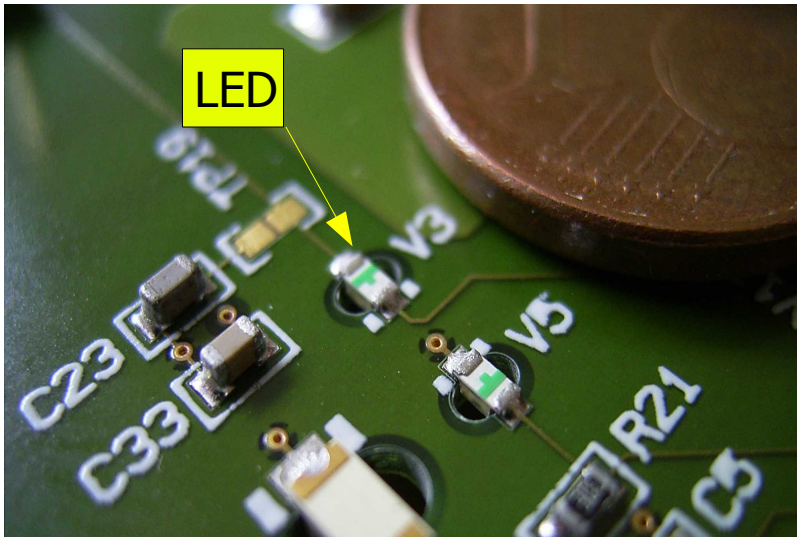
- First batch of new tiles with SiPMs with 796 pixels have been tested on simple testbench and with full readout chain
- Pulse length 120ns – 320ns
- Gain 0.4 – 0.8 * 10^6
- Calibration system needed for SiPMs







LED calibration system

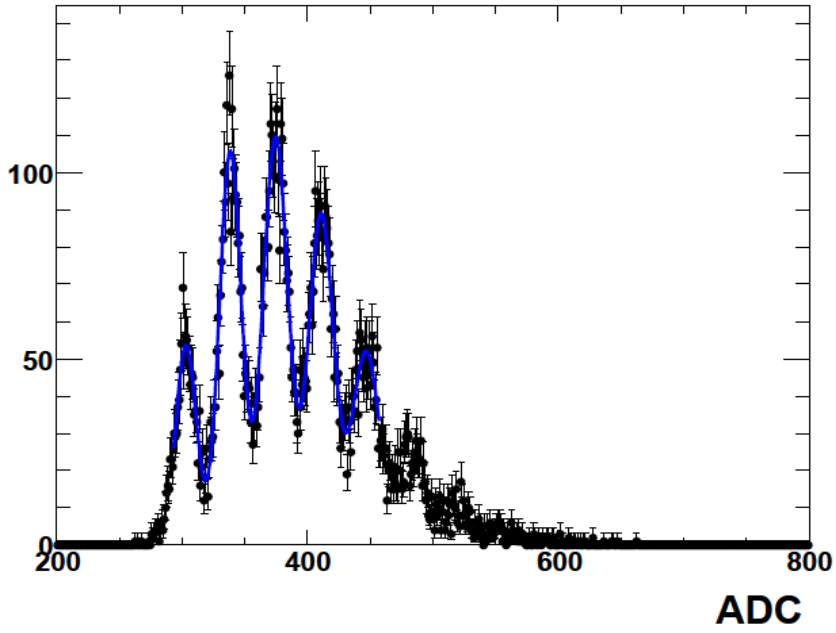


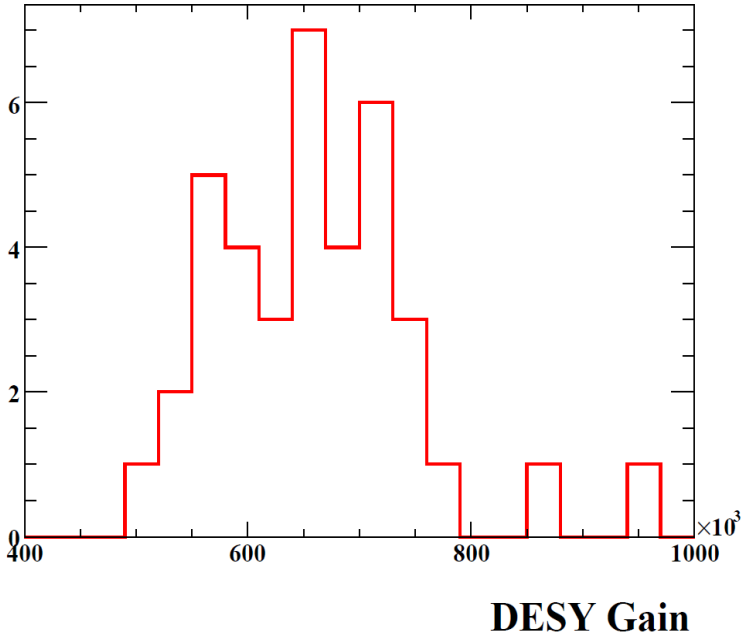
System task:

- SiPM gain calibration via single pixel spectra
- SiPM saturation curves

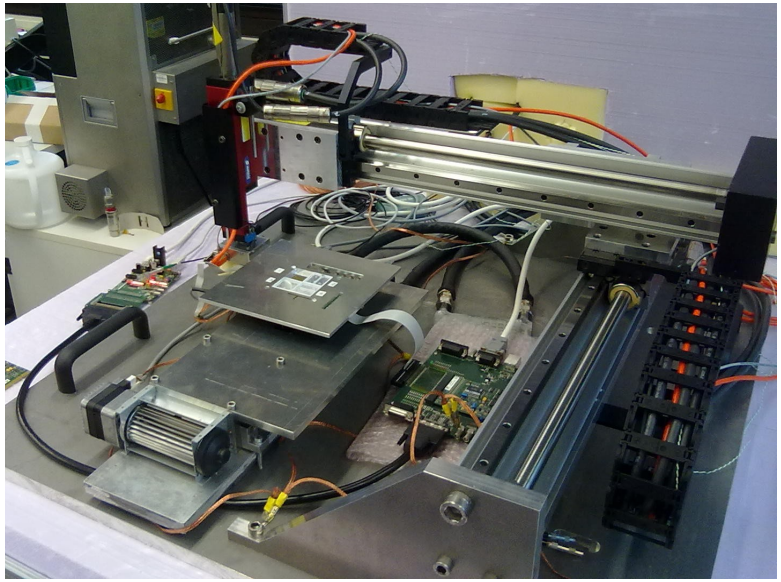
Wuppertal solution:

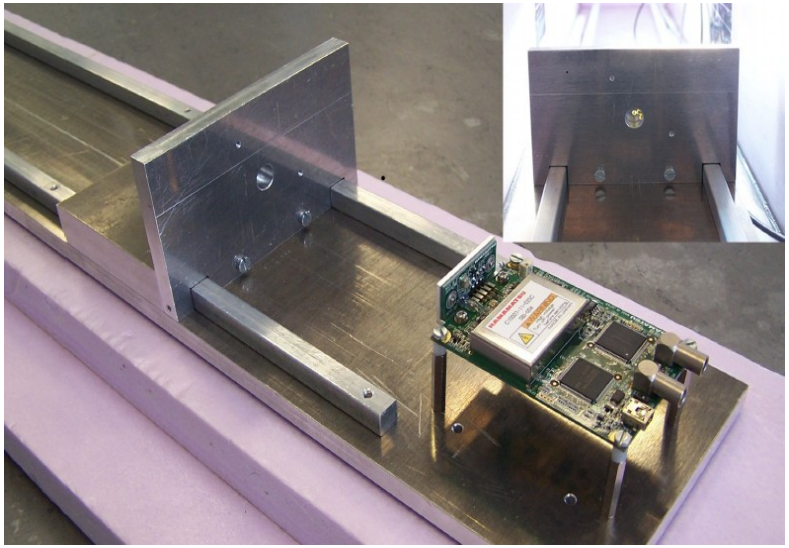
- Light directly coupled into the tile by 1 integrated LED per channel





LED calibration system





Blue vs UV LEDs

- High internal capacitance for blue LEDs (market requires high light output...)
- Blue pulses too long for current ITEP tiles

  → Chose UV LEDs, blue option for future

Test results:

- System tested with PMT and full tile/SiPM readout
- LED pulse stays short (~10ns) in amplitude scan
- Compensation capacitors defined to improve uniformity of LED output

→ Design of LED driver circuit finished, tested and implemented in new HBU design

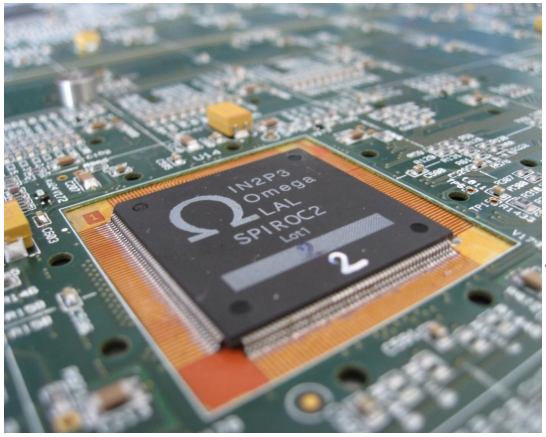
SPIROC2

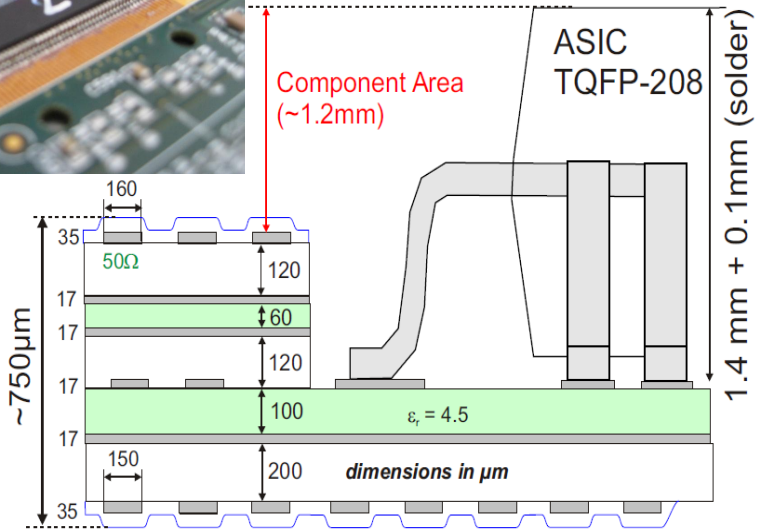
Specific chip for SiPM readout:

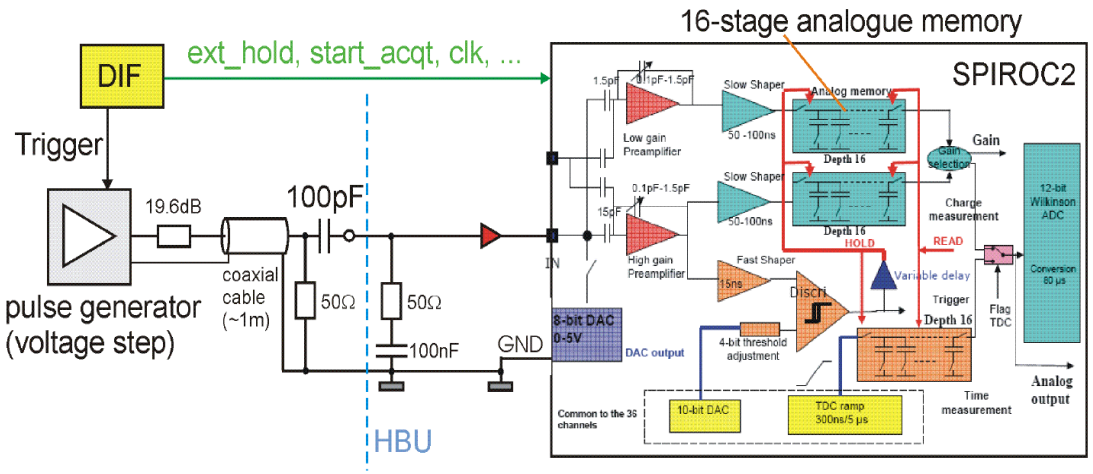
- Input DAC for channel-wise bias adjustment (36 channels)

Designed for ILC operation:

- Power pulsing → 25µW/ch
- Dynamic Range 1-2000pe with dual-gain setup per channel
- Internal ADC
- Autotrigger mode
- Time stamp (~100ps)







Charge injection setup

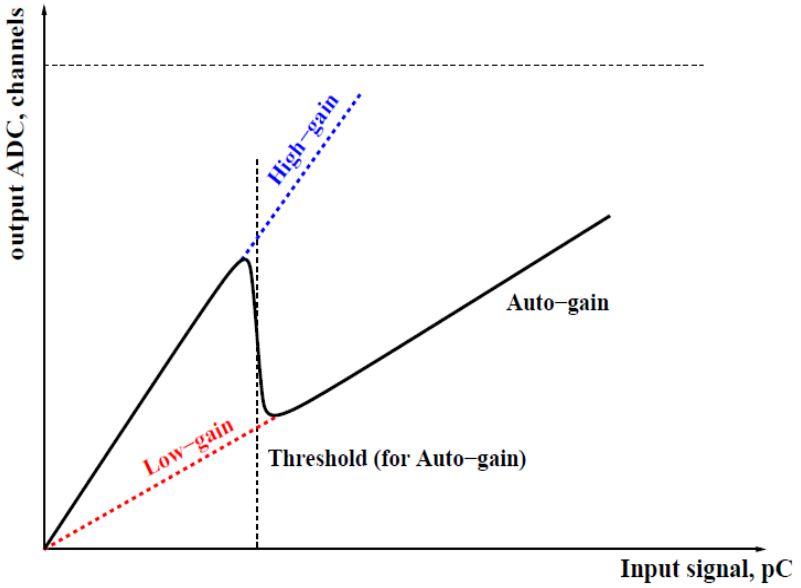
Placement of components in PCB cutouts

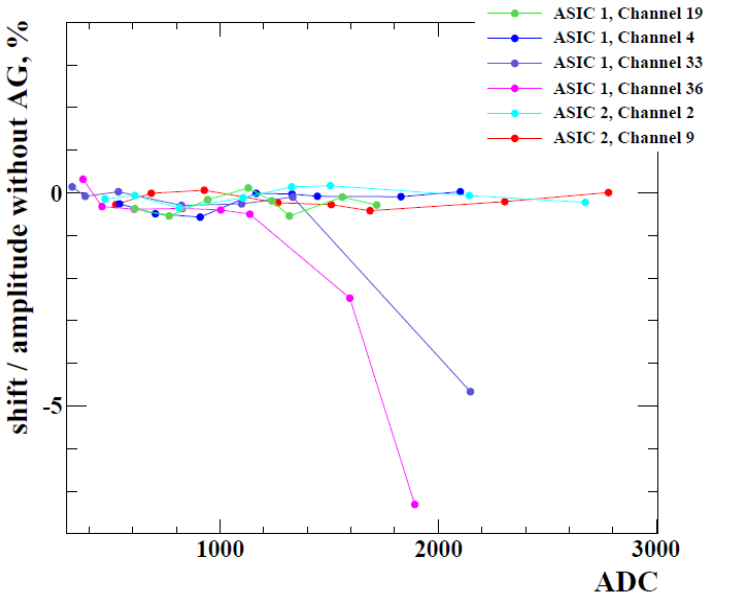
→ 300µm/layer

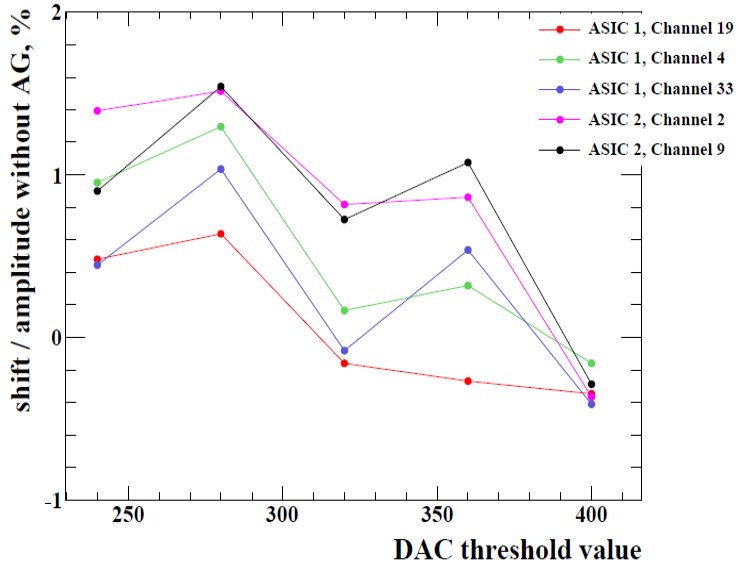
→ 30mm in total!

Autogain performance - Linearity

- Autogain: automatically switch between high gain and low gain mode
- Compare signal with predefined (10 bit) DAC threshold
- Good linearity, but still slightly depends on:
  - Amplitude
  - Distance to threshold

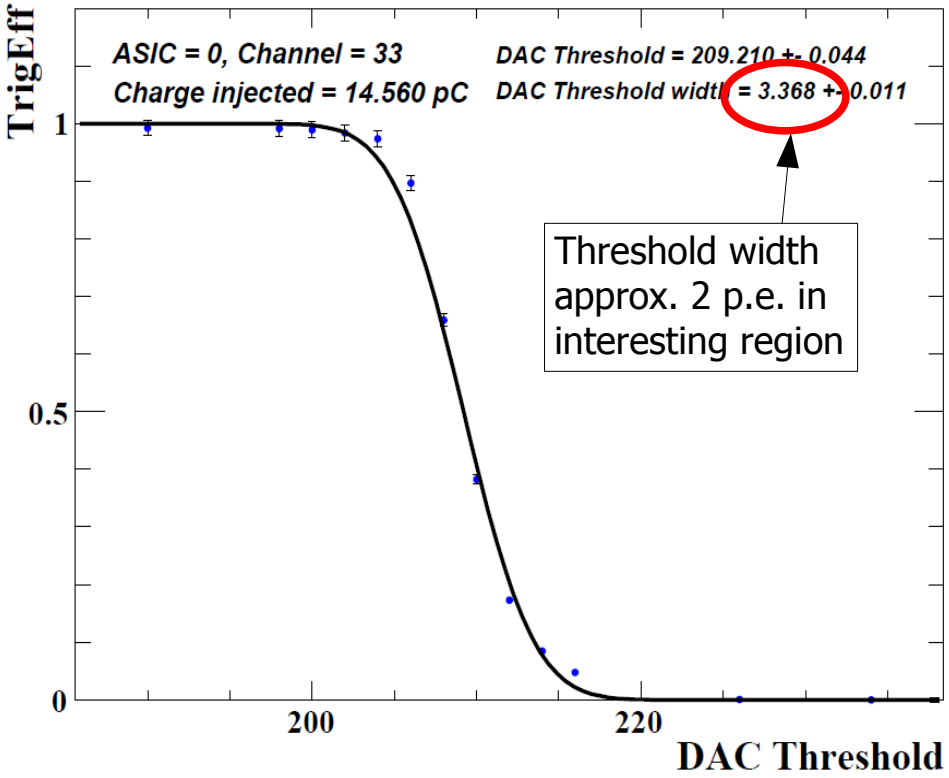


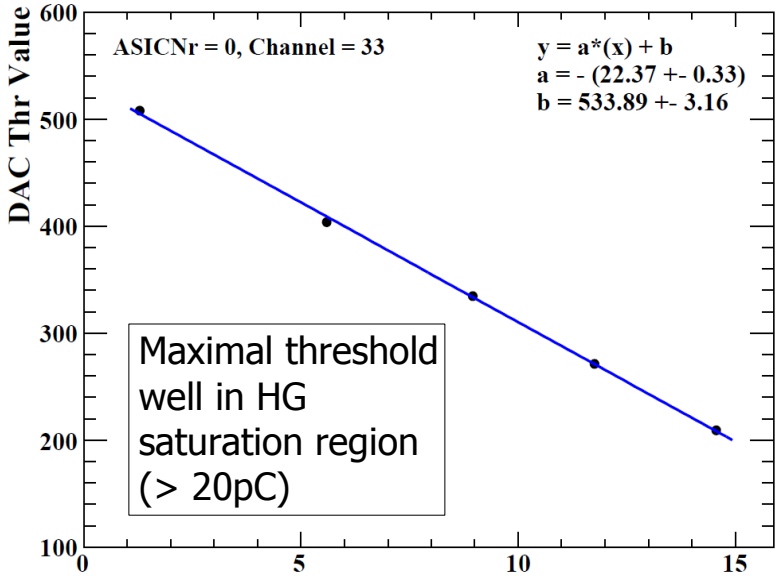


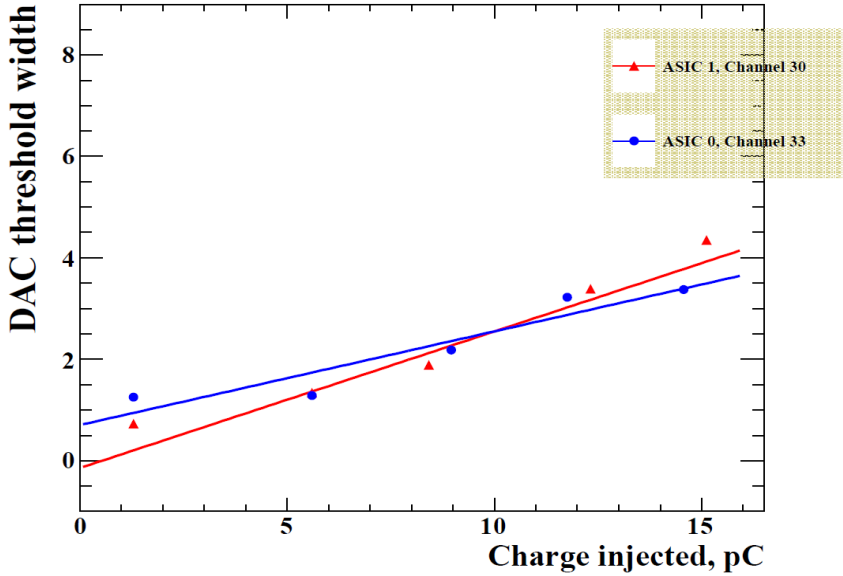


Autogain performance - Thresholds

- Autogain: automatically switch between high gain and low gain mode
- Compare signal with predefined (10 bit) DAC threshold
- Similar performance as for autotrigger

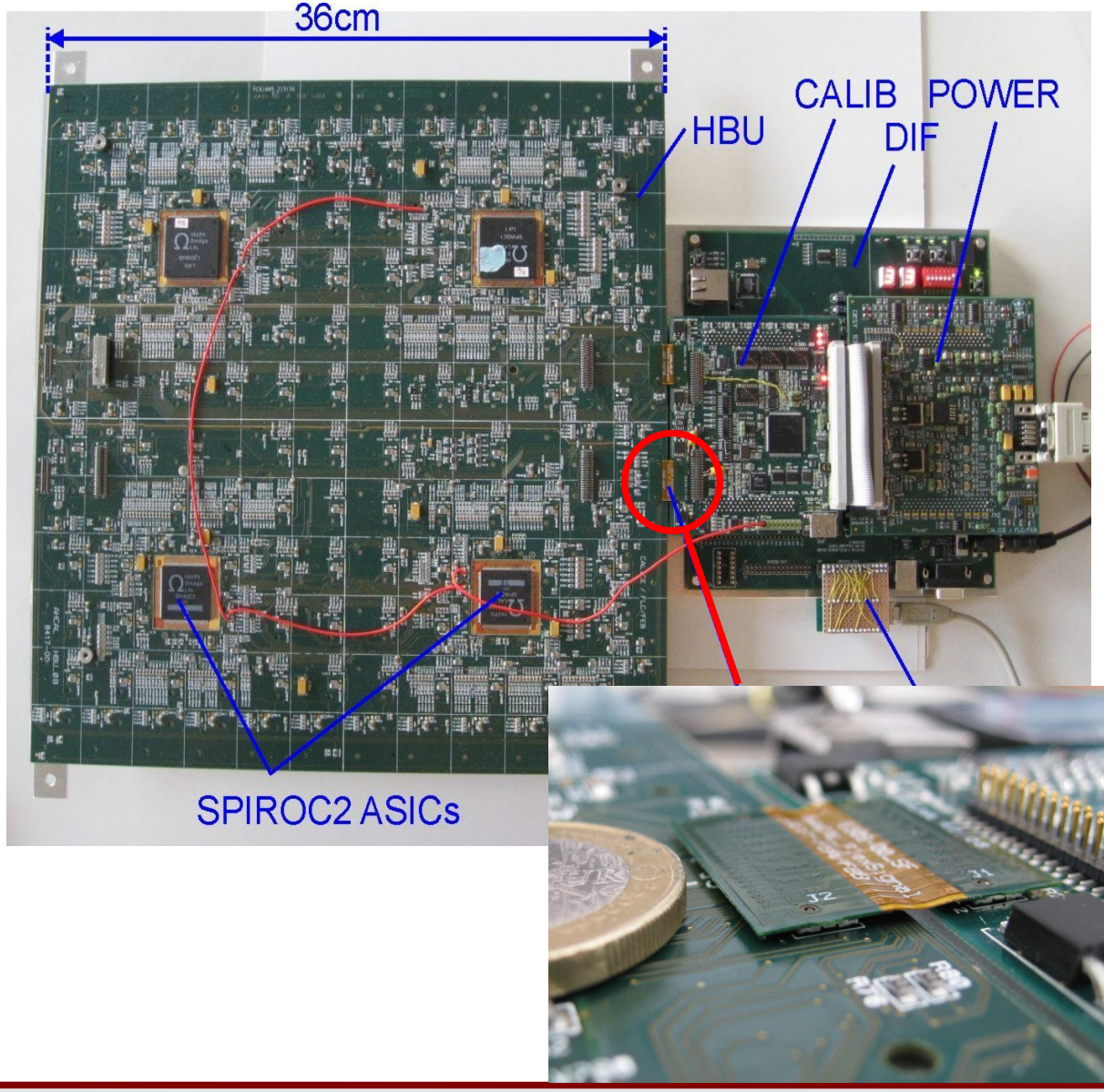




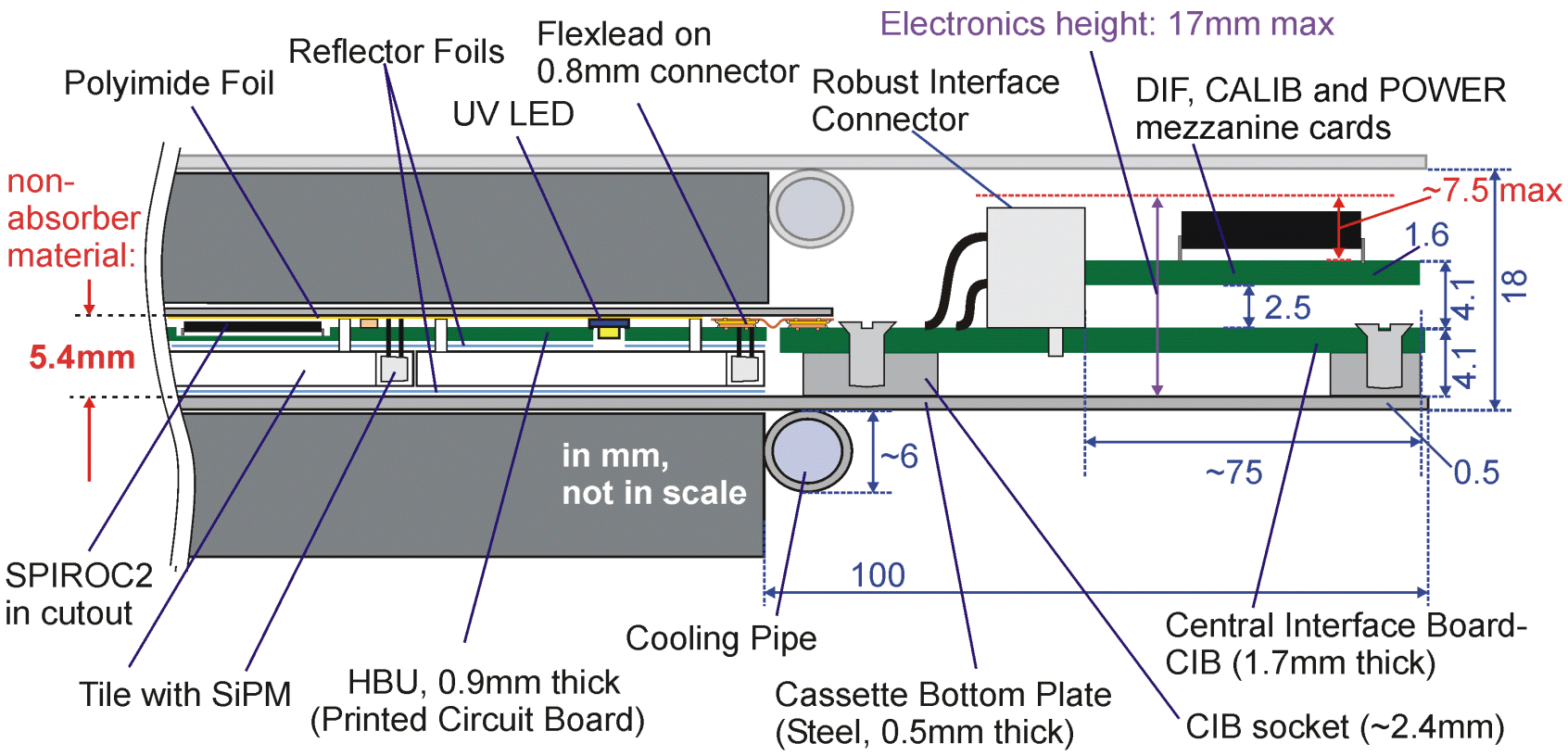


HCAL Base Unit (HBU)

- At DESY 2 setups (HBUs) available
- 1 for charge injection and LED calibration tests
- 1 for testbeam operation with 2GeV electron beam
- Multiple ASIC tests performed and issues discussed with Omega
  - SPIROC2b now used at DESY
  - SPIROC3 design ongoing
- Redesign of HBU finished, production ongoing

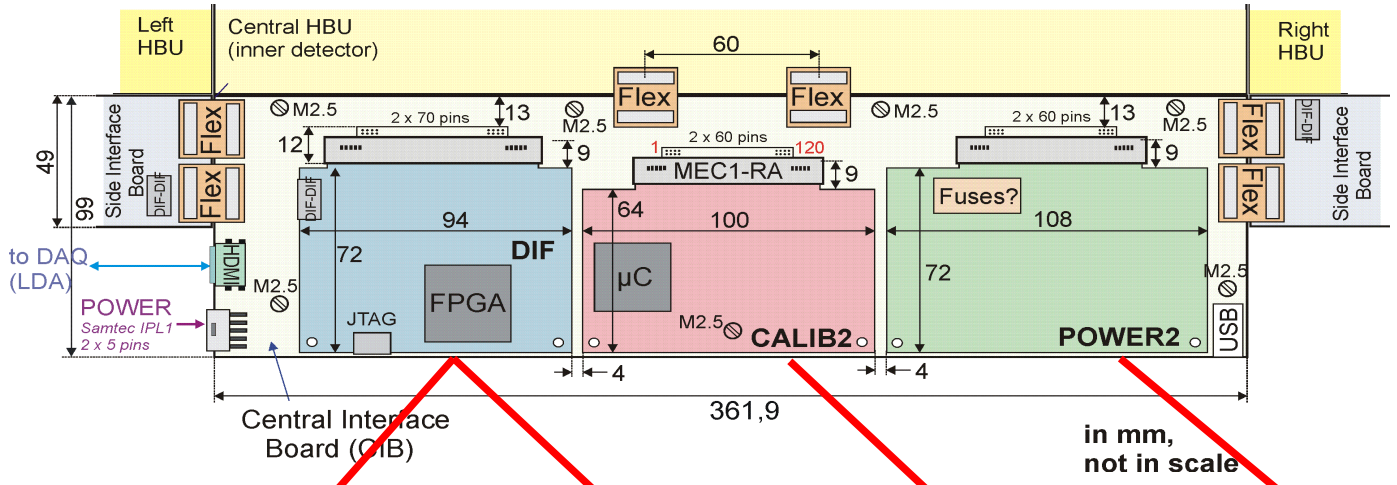


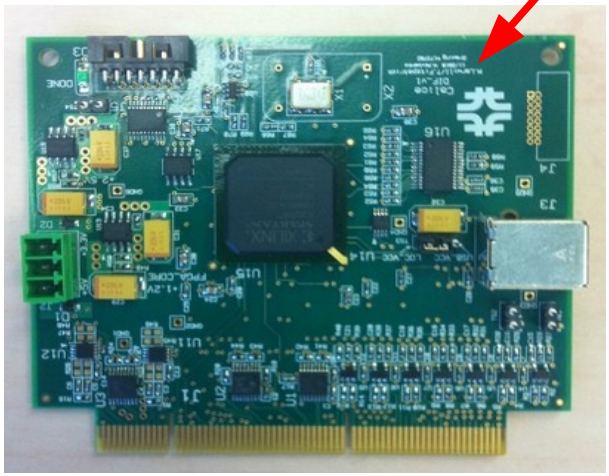
AHCAL layer – cross section

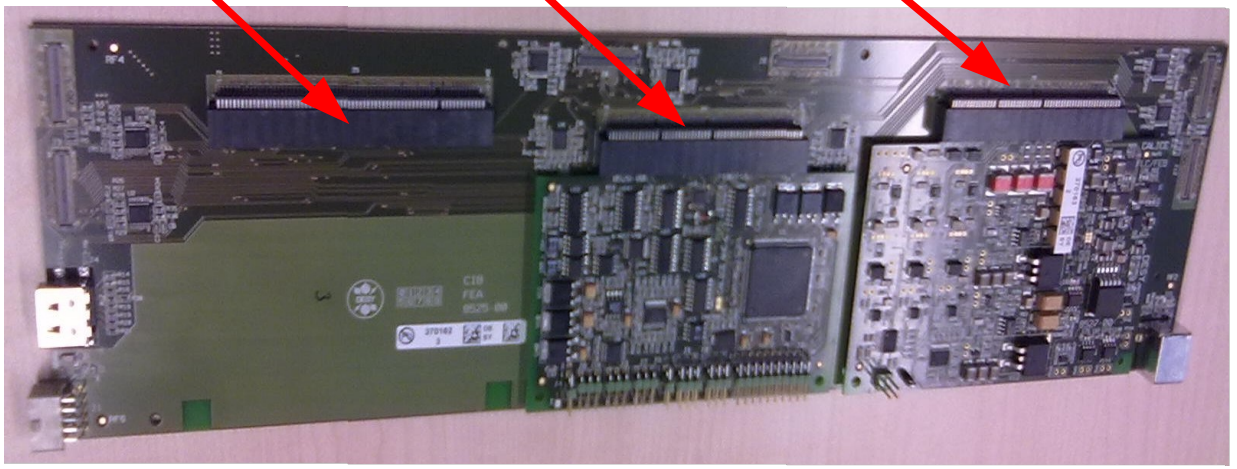


- Redesign and production of subcomponents ongoing or finished (DIF, CALIB2, POWER2, HBU2 (in production), CIB (last bugfix), Flexleads (SIB not needed yet))
- Electronics height compliant with steel and tungsten options

CIB, POWER, DIF and CALIB



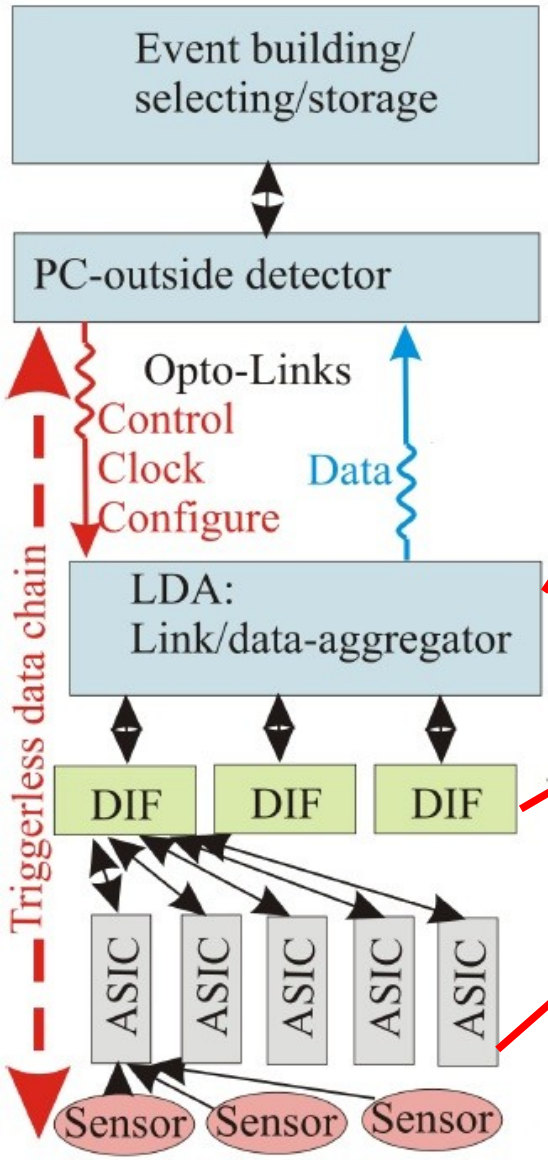


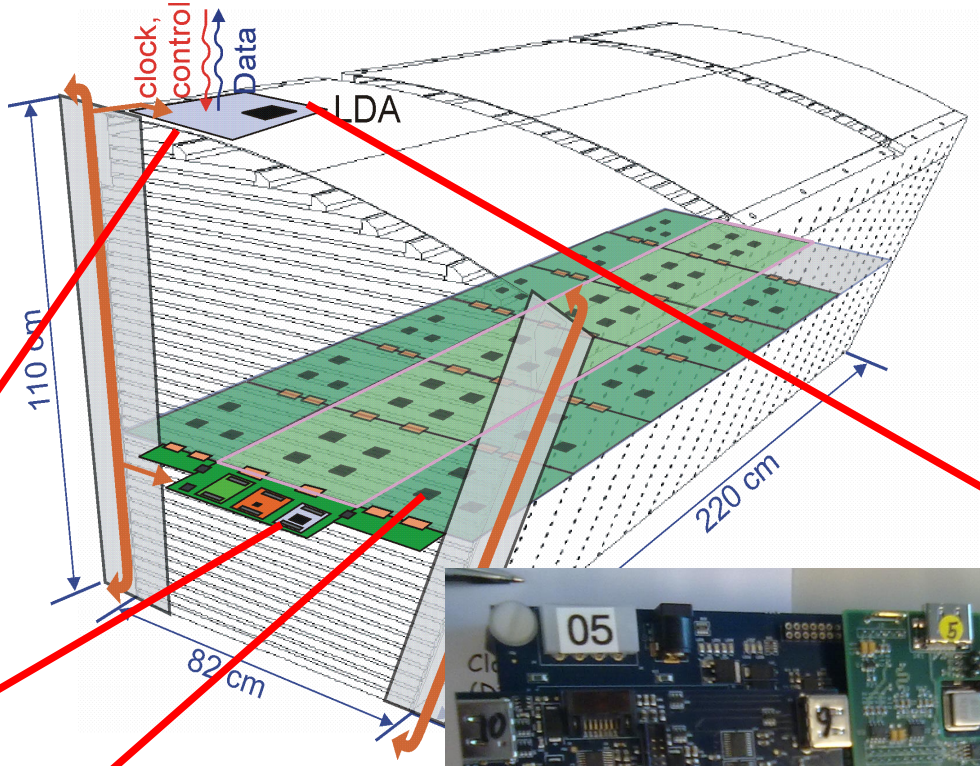


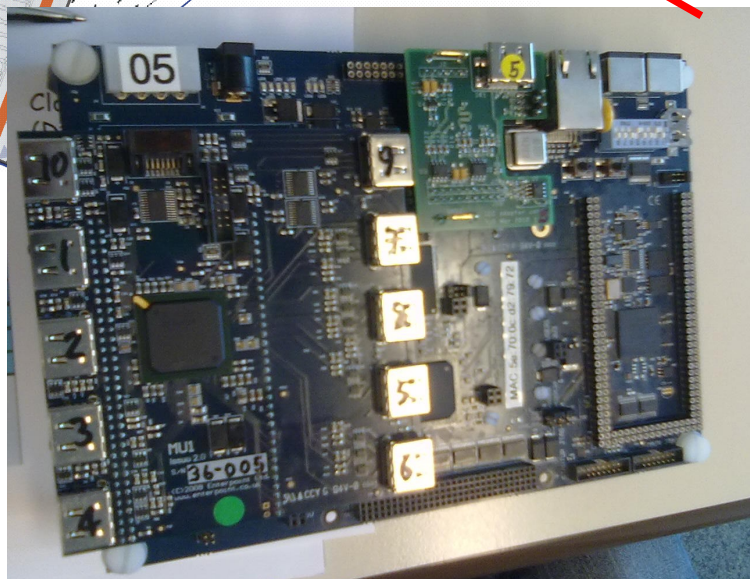
- DIF currently under test at NIU, will be sent to DESY soon

  → Plug everything together for testing the full readout chain

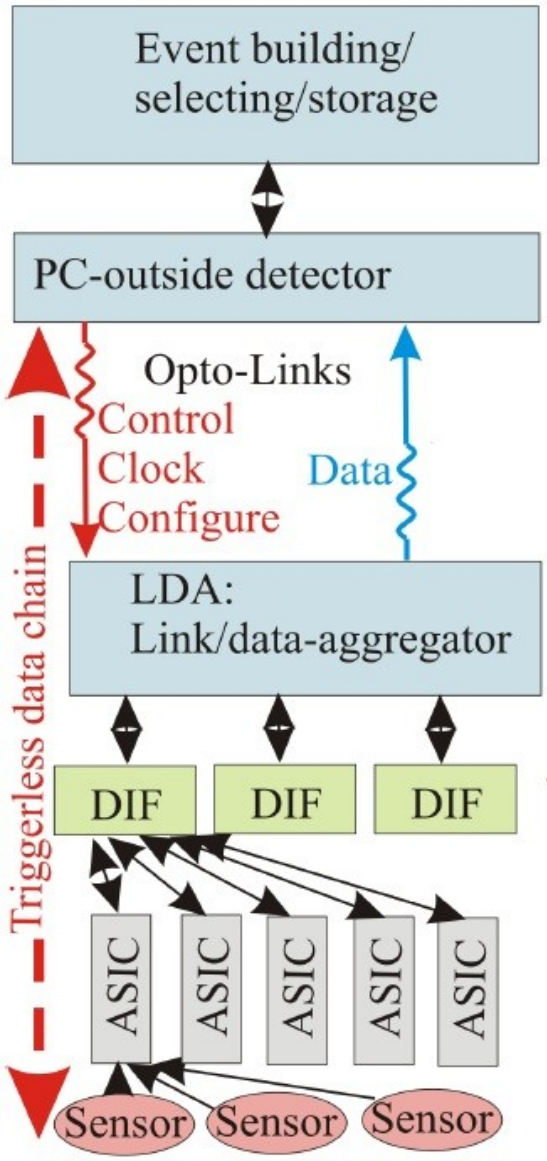
Data acquisition interface

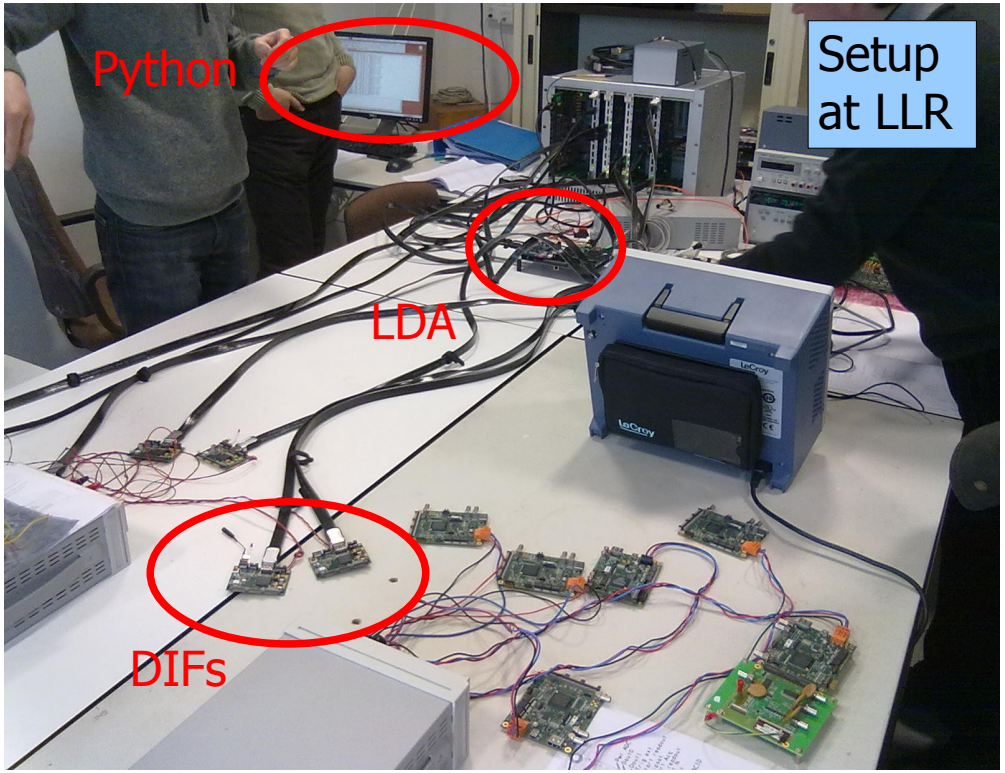






Data acquisition interface





- Whole chain established at LLR
- DAQ modules available at DESY (8 LDAs, 2 CCCs, 1 ODR, cables, fibres …)
- Started to integrate all modules at DESY

Summary and outlook

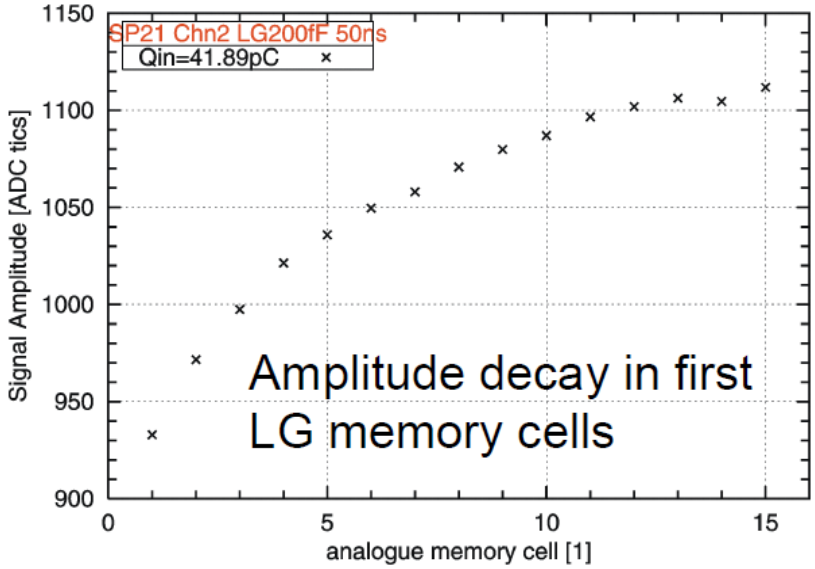
- New technological AHCAL prototype under development
- 2 setups running in Hamburg
  - Successful testbeam operation and MIP calibration
  - Tests of SPIROC2 with charge injection (e.g. AT and AG)
- New tiles tested, communication with ITEP ongoing
- LED calibration system development for new HBU finished

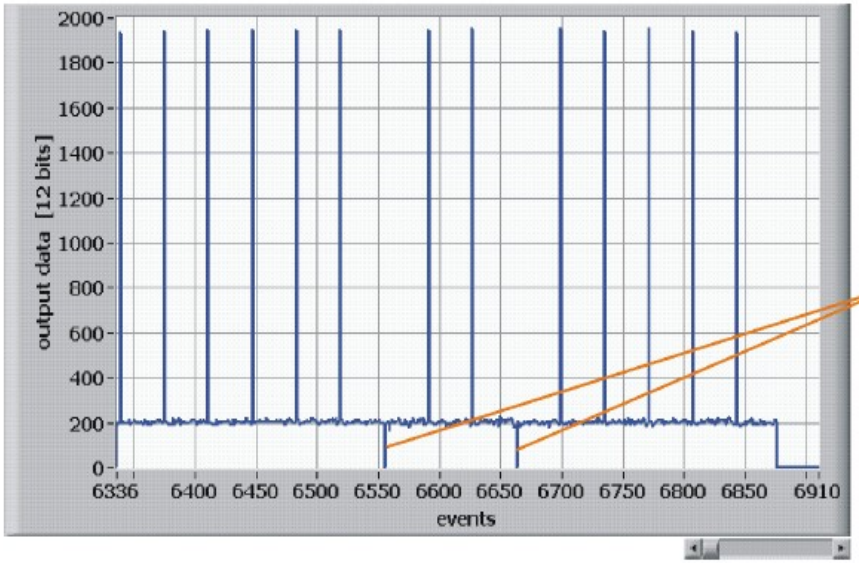
  → Redesign of HBU finished, in production
- DAQ modules available now

To do

- Further tests of power pulsing (with SPIROC2b)
- SPIROC2b tests (e.g. channel-wise gain adjustment)
- DAQ integration
- This year: Integration to full slab (2.2m calorimeter layer)

Open SPIROC2 Issues





Cell dependent gain:

- Depends on pulse shape and injection pattern (time between 2 bursts of 16 events)

  → Too small bias current for dynamic feedback resistor

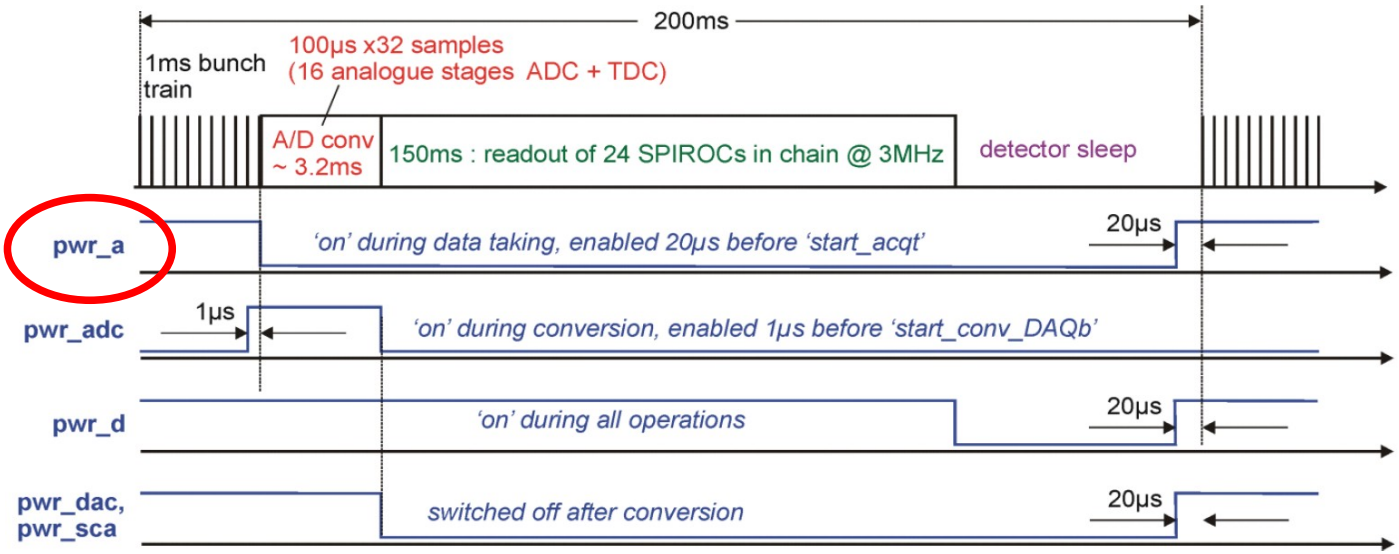
  → Role of compensation capacitors?

Zero-events:

- All channels show randomly events with 'zero' as output
- Not understood so far

Power pulsing

- Needed to restrict power consumption and needs for cooling
- Bug in SPIROC2:
  - Open-collector outputs (e.g. data output) switched off, if power_on_analog is switched off
  - BUT: power_on_analog most important power pulsing signal, immediately switched off after data taking
  - Bug fixed in SPIROC2b



Autotrigger performance

- Autotrigger: mode of ILC operation
- Compare fast shaped signal with predefined (10 bit) DAC threshold
- Set threshold to minimize noise hits and maximize MIP efficiency