JRA3 Front End Electronics and summary

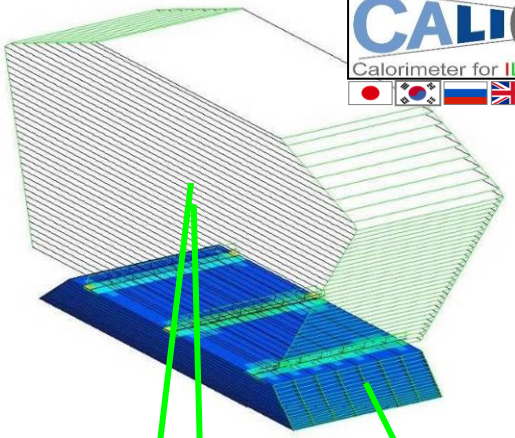
C. de LA TAILLE
OMEGA-LAL Orsay

Orsay MicroElectronic Group Associated

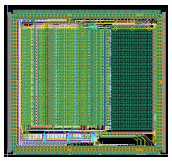
Second generation ASICs for EUDET

- Add auto-trigger, analog storage, digitization and token-ring readout !!!
- Include power pulsing : <1 % duty cycle
- Optimize commonalities within EUDET (readout, DAQ…)
- Dedicated run produced in march 2010
  - 25 wafers received in june (<1€/ch)
  - Plastic packaging in the US

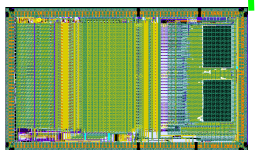
FLC_PHY3 (2003)



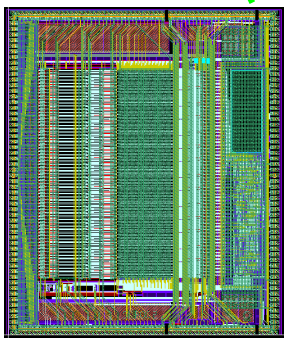
HARDROC2
SDHCAL RPC
64 ch 16 mm²



SPIROC2
AHCAL SiPM
36 ch 30 mm²

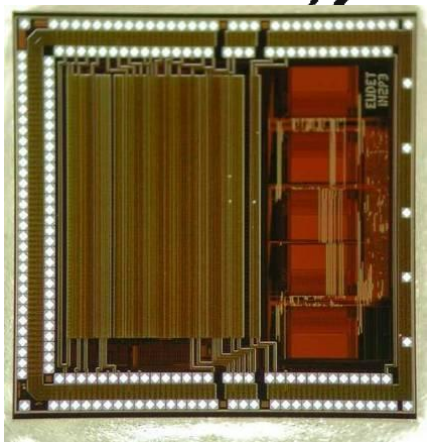


SKIROC2
ECAL Si
64 ch. 70 mm²

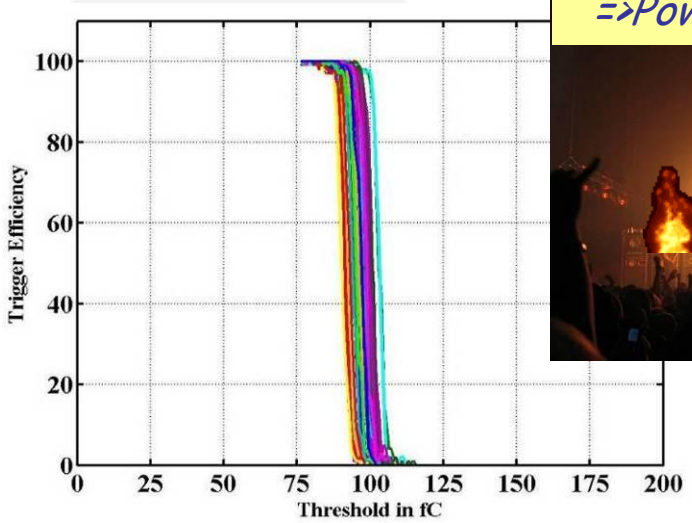


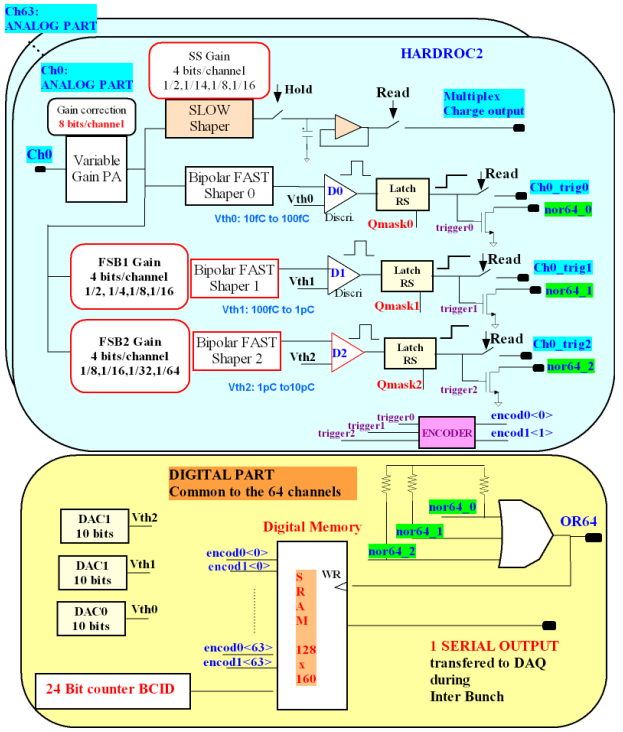
HaRDROC : ILC DHCAL readout

- Hadronic Rpc Detector Read Out Chip
  - 64 inputs, preamp + shaper+ 3 discris
  - Full power pulsing => 7 µW/ch
  - Chip embedded in detector
  - in beam in 2008-2009
  - 10 000 chips produced
  - collab. LLR, IPNL, LAPP, LAL/OMEGA

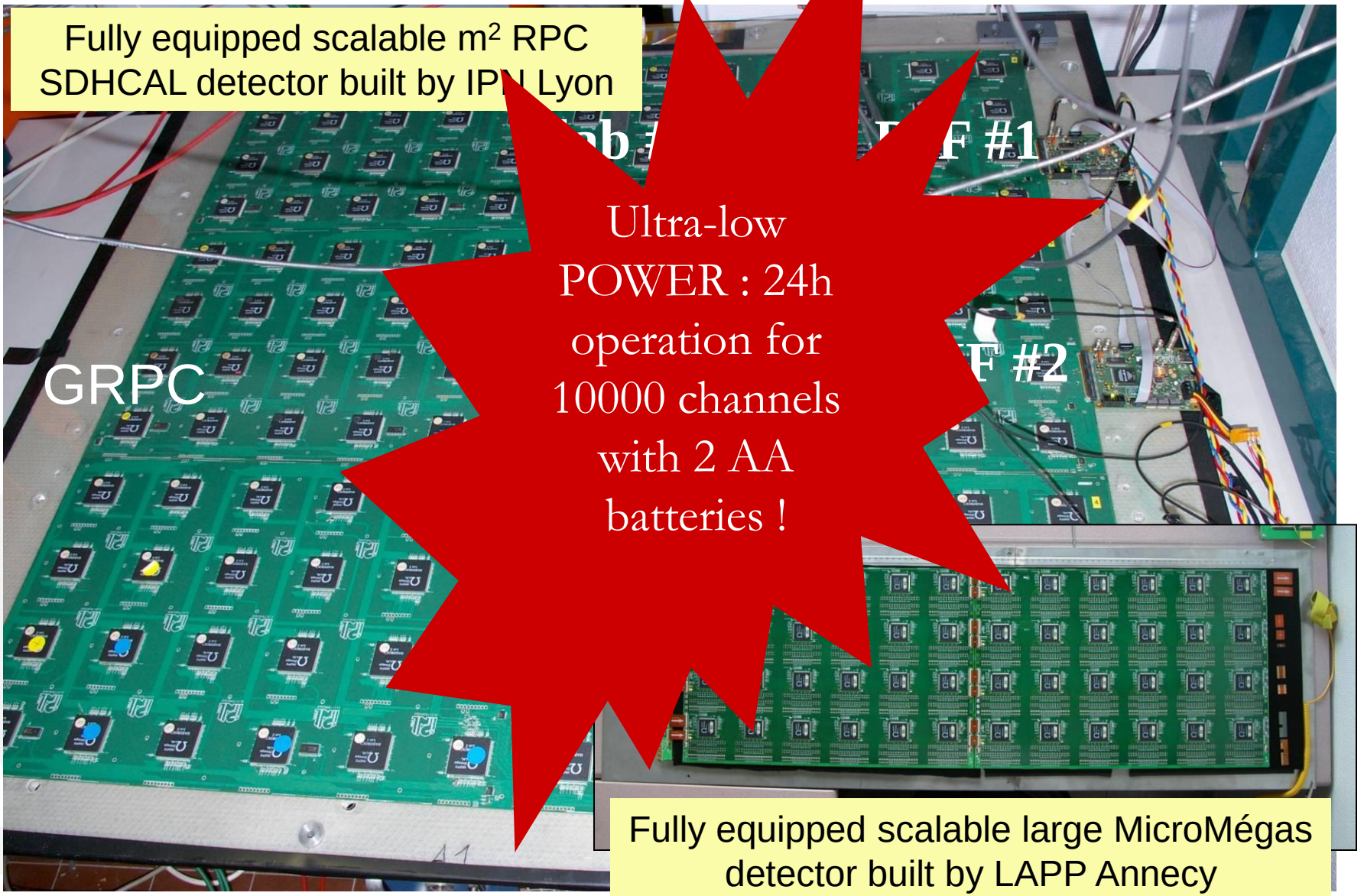


- **Readout and DAQ2 validated with µMegas and RPC m² detectors**





Towards an ILC technological prototype

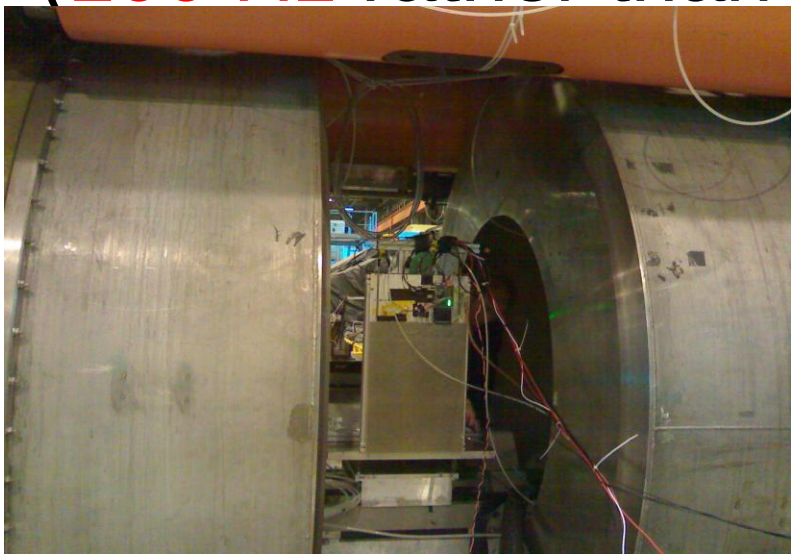


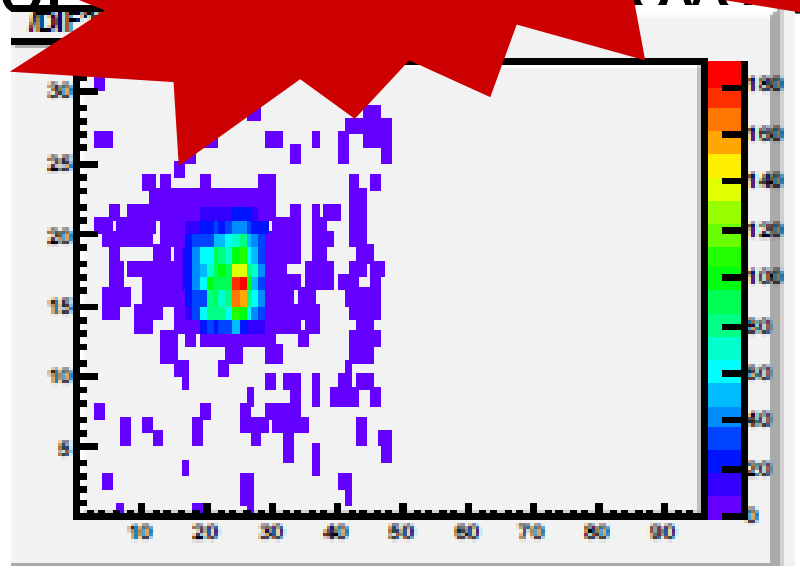
POWER PULSING is ON and working in 3-Tesla field

First power-pulsed detector

Cycle of 2 ms power puls

(100 Hz rather than co

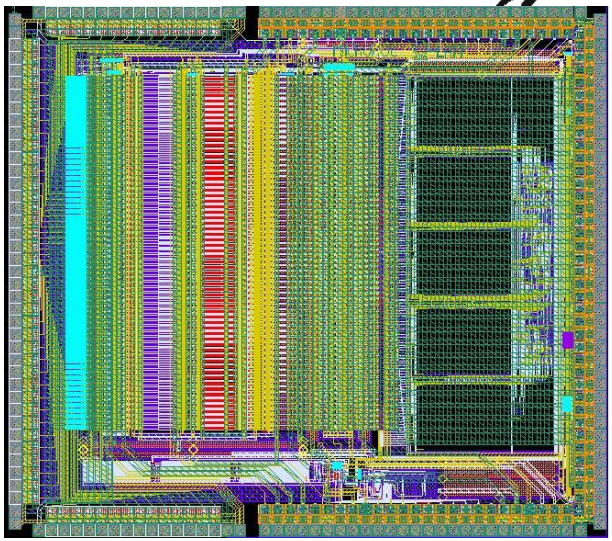




Efficiency is almost the same (2% less) but this probably due to the acquisition starting time which is to be fine-tuned.

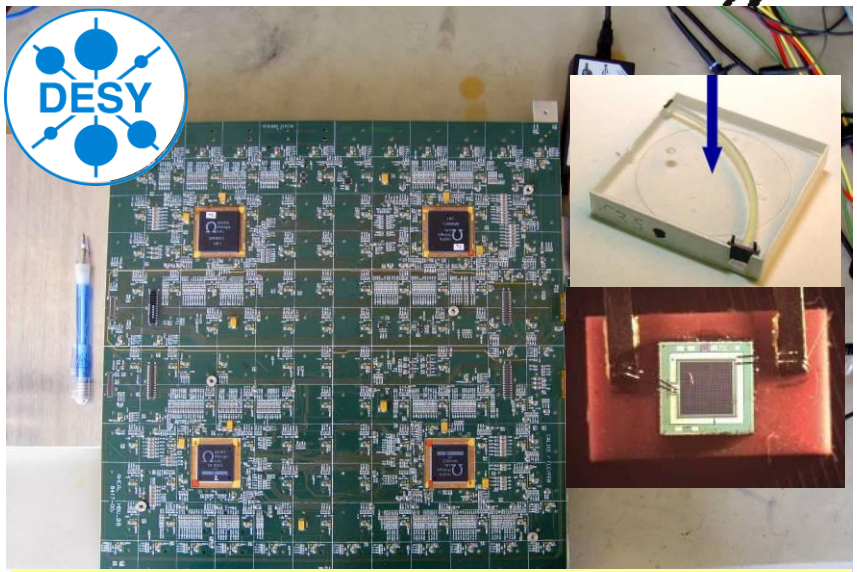
MICROROC status

- MICROROC : MICROMEGAS Read Out Chip
  - Same as HARDROC but with charge preamp input stage + HV protection [R. Gaglione] and slower shaping + 4bit DAC/channel [N. Seguin]
  - Preamp optimized for Cd=80 pF, noise = 0.2 fC. Cf=0.4pF Rf=5M
  - Maximum input charge : 500 fC
  - Bi-gain shaper (G1-G4), peaking tunable 50-200 ns (2 bits)
  - 3 thresholds. Lowest threshold ~2 fC
  - Pin to pin compatible with HR2
  - Chip sent in MPW june 10, exp sept

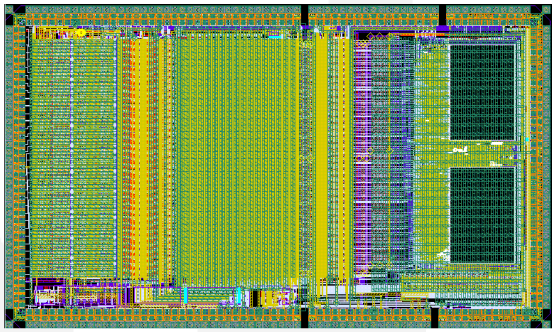


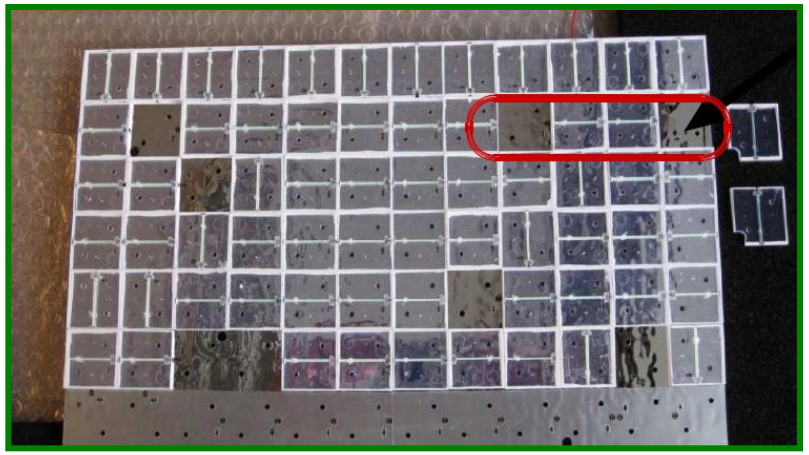
SPIROC : ILC AHCAL & ECAL readout

- SPIROC : Silicon Photomultiplier Integrated Readout Chip
  - 36 channels
  - Internal 12 bit ADC/TDC
  - Charge measurement (0-300 pC)
  - Time measurement (< 1 ns)
  - Autotrigger on MIP or spe (150 fC)
  - Sparsified readout compatible with EUDET 2nd generation DAQ
  - Pulsed power -> 25 µW/ch
  - Also External users (PET, hodoscopes, µ-imaging… (@ Aachen, Napoli, Pisa, Roma…)

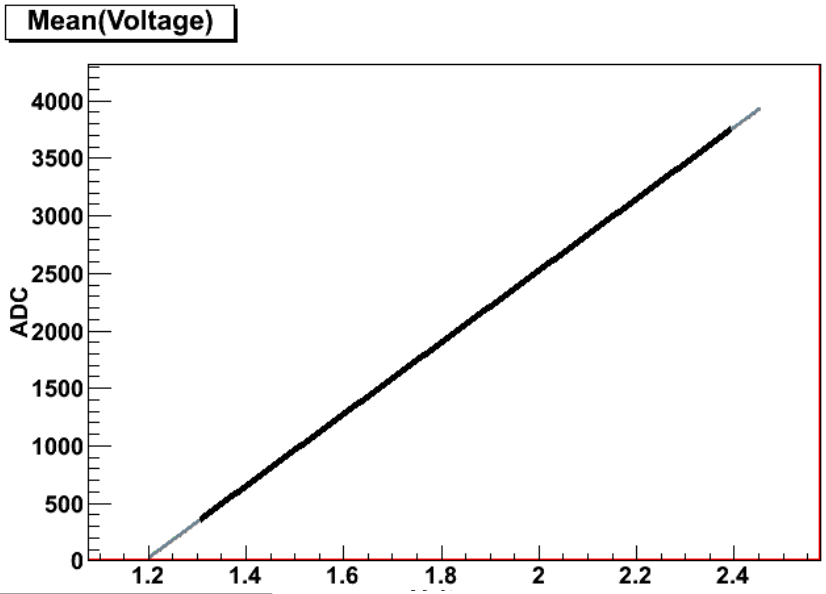


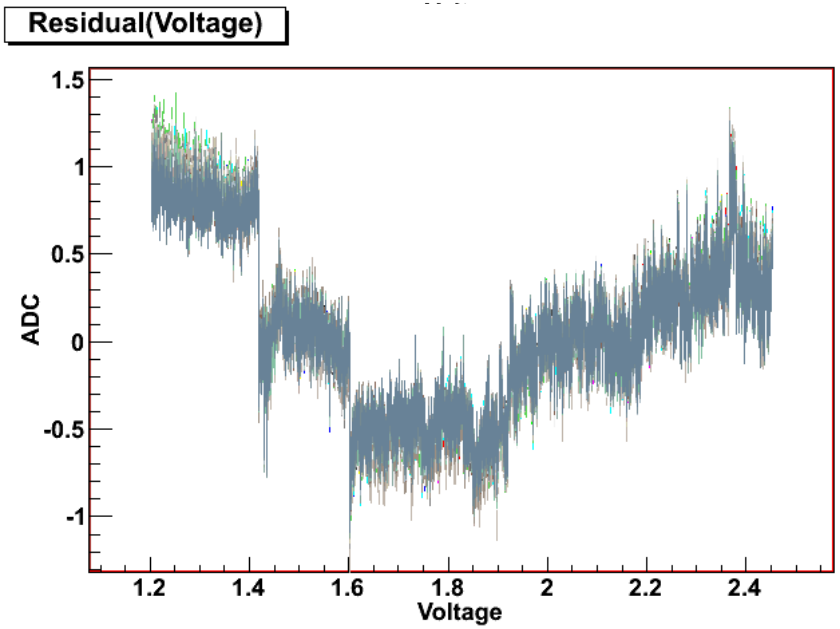
(0.36m)² Tiles + SiPM + SPIROC (144ch)

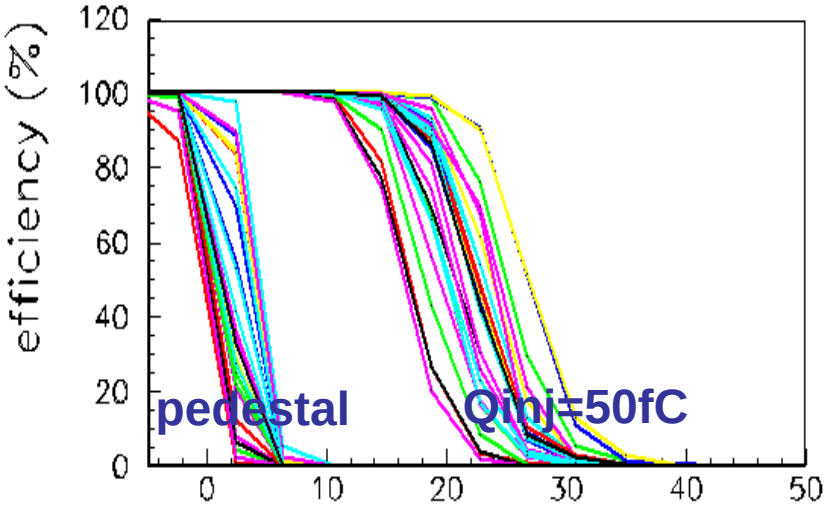


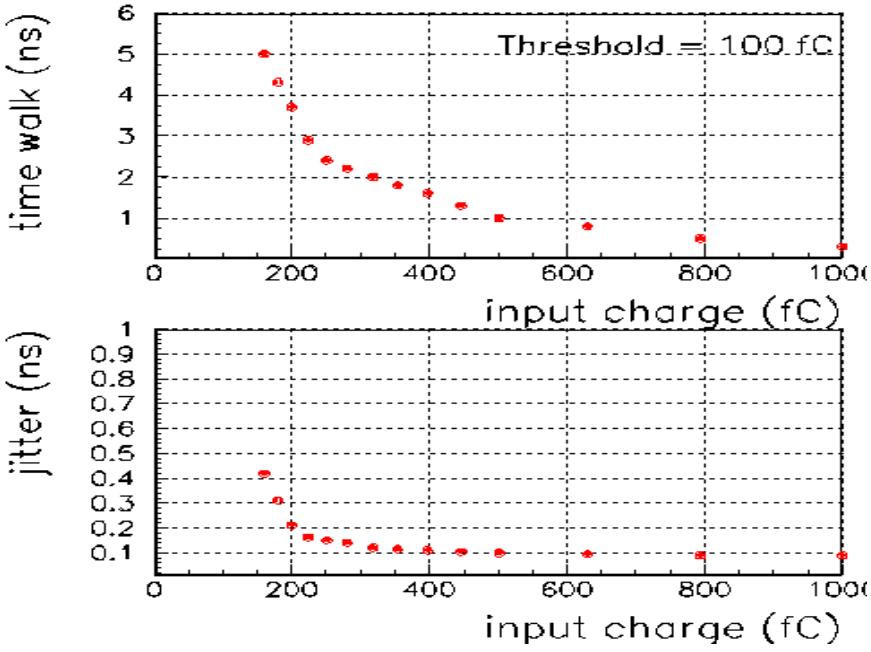


Performance

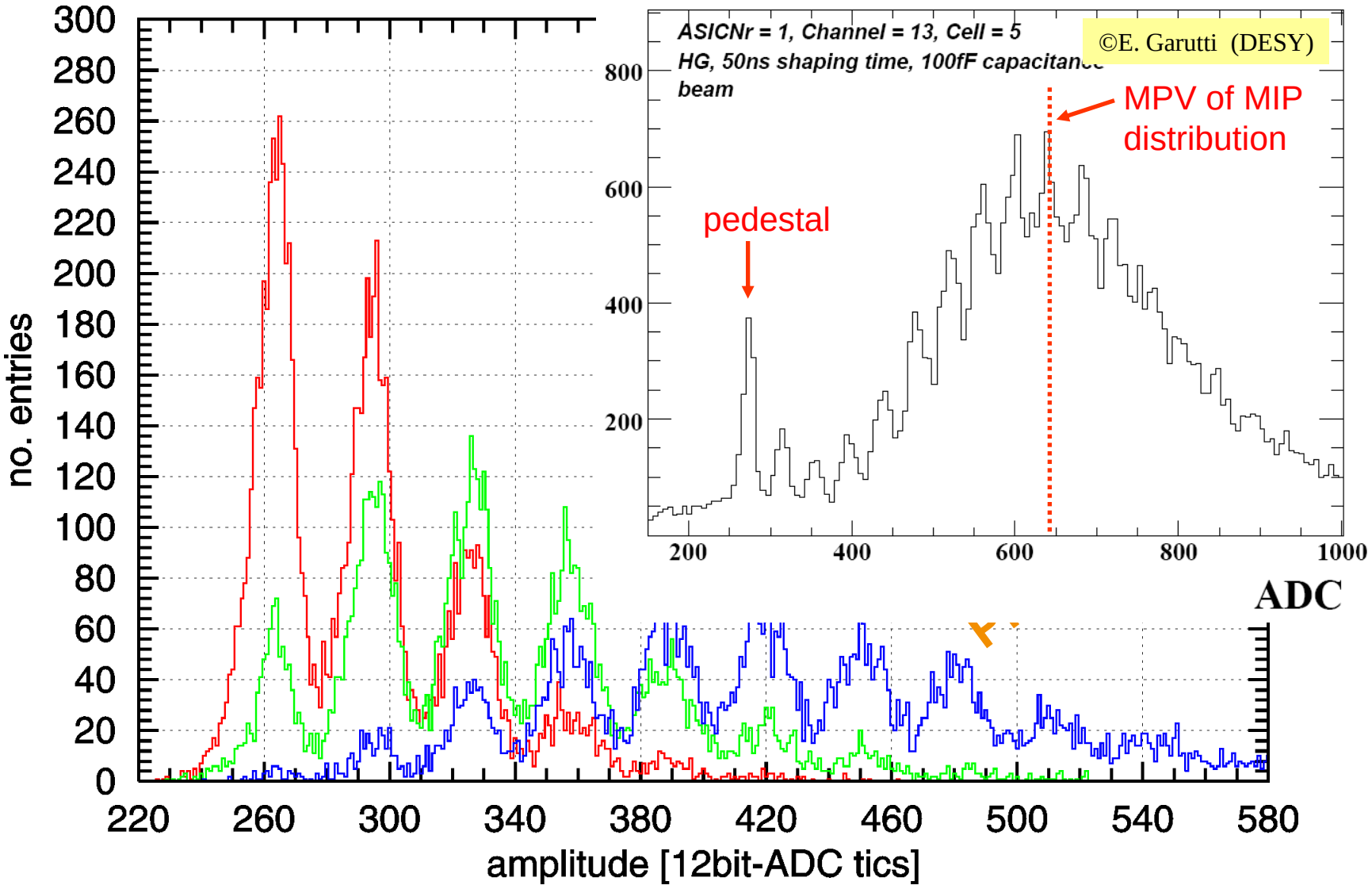








Single-Photon Peaks I



SPIROC status

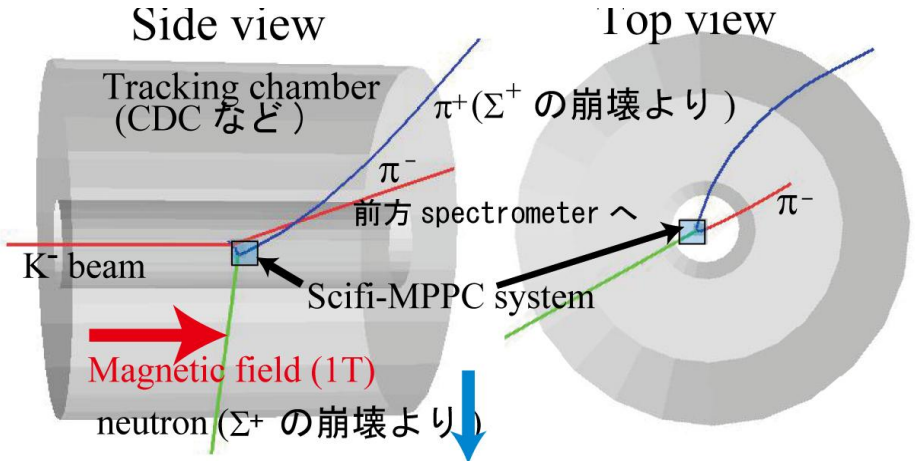
- 50 chips SPIROC2 produced in june 2008 to equip AHCAL and ECAL EUDET modules
  - **EUDET milestone**
  - Package TQFP208
  - Difficult slow control loading
- Measurements slowly coming in : complex chip
  - Collab LAL, DESY, Heidelberg
- Full production run : march 2010
- 3750 chips SPIROC0 (analog) bare die
- 1000 chips SPIROC2A in TQFP208
  - Identical to SPIROC2 with slow control fixed
- 250 chips SPIROC2B in TQFP208
  - Pin to pin compatible with SP2
  - Individual gain adjustment
  - Better input DAC
- New alternative FE design in collaboration with Heidelberg
- Many external applications !

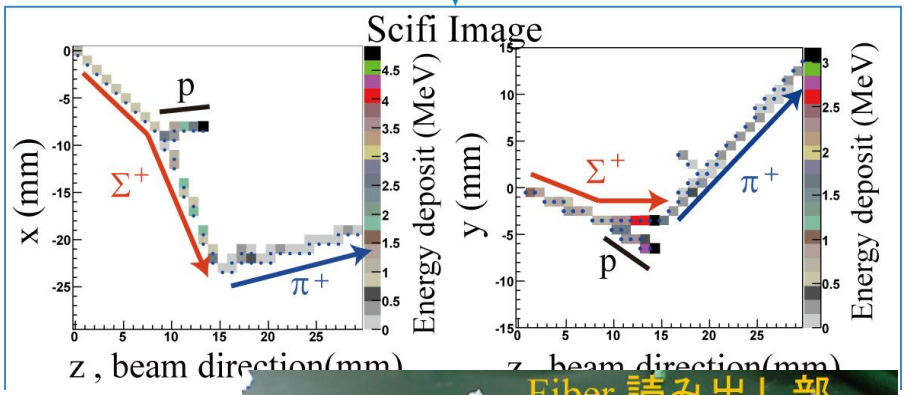
Active target with MPPC readout

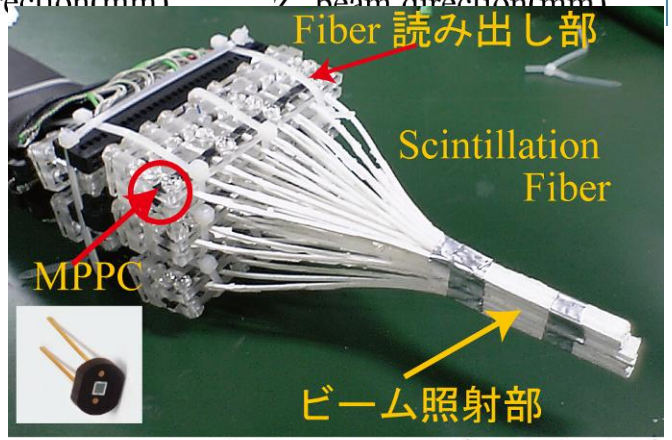
Tohoku Univ + KEK

- Characteristics
  - Fast time response
    - Work in a high beam intensity
  - Large gain (10^5~10^6)
    - Possible to detect 1 photon
  - Operation in the magnetic field
    - Combination of Imaging and Spectrometer
  - Trigger possibility

Test with small prototype





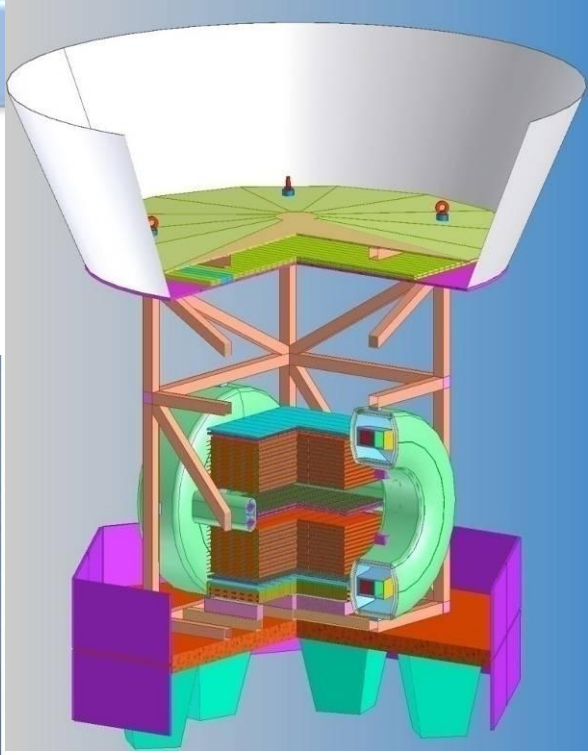


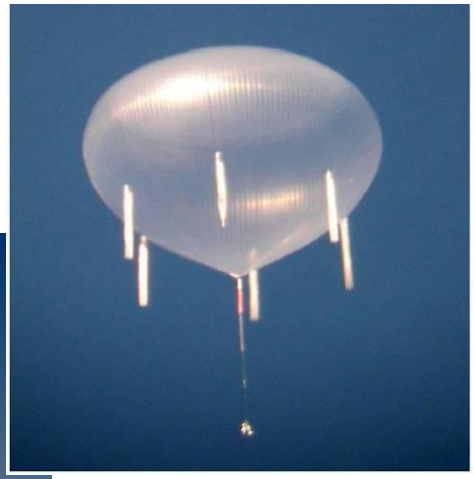
MPPC 50ch を用いた小型プロトタイプ

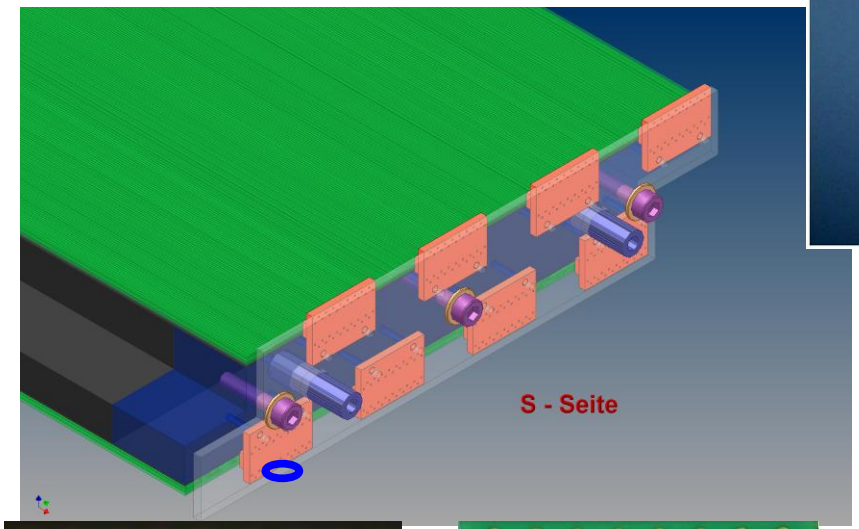
PEBS

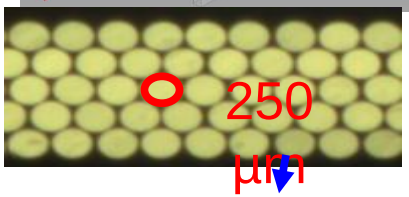
RTWH Aachen

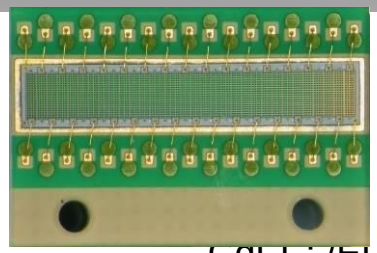
- **PEBS is a project in Research & Development phase**
  The purpose of the experiment is a precision measurement of the electron & positron cosmic ray flux in the energy range from 1 to 2000 GeV.

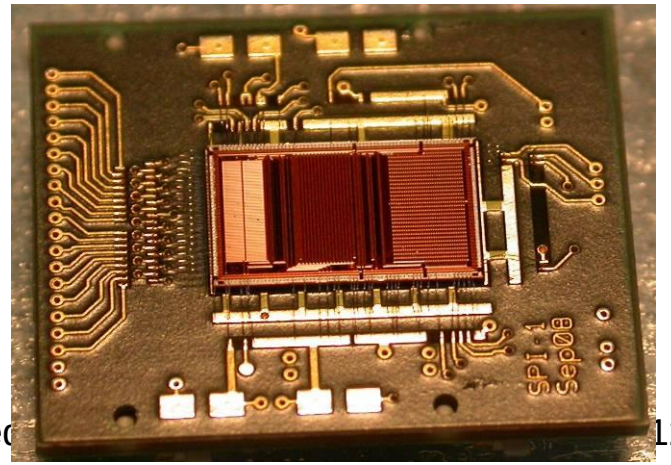




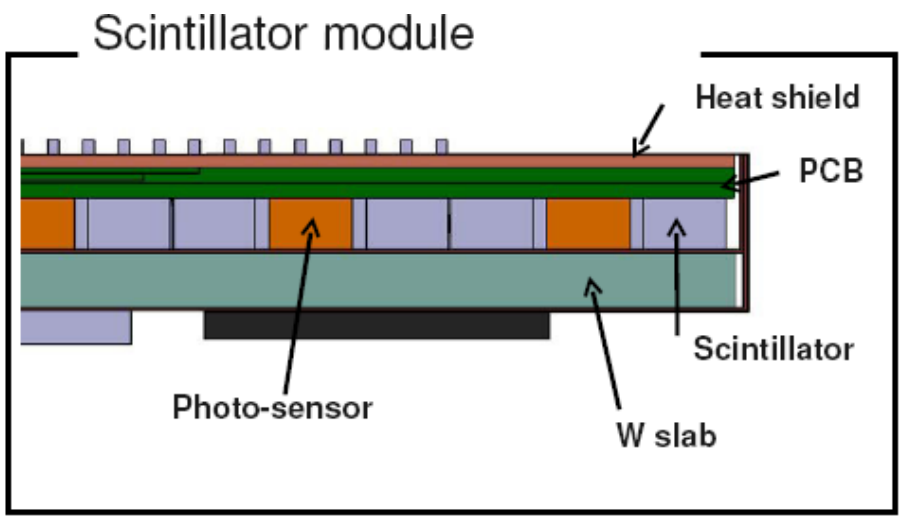


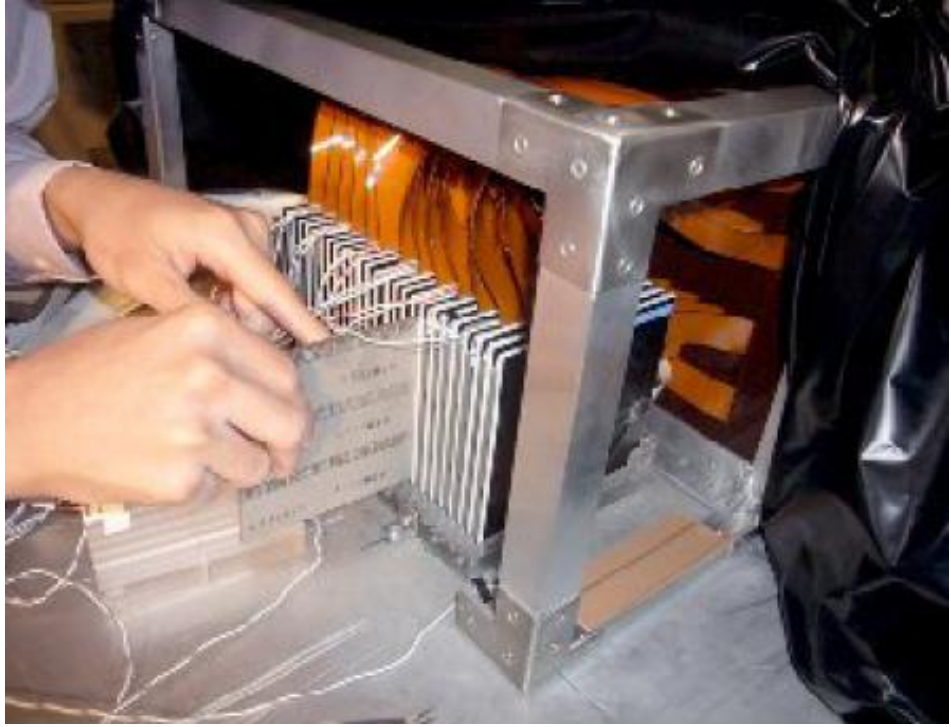






Shinshu Univ





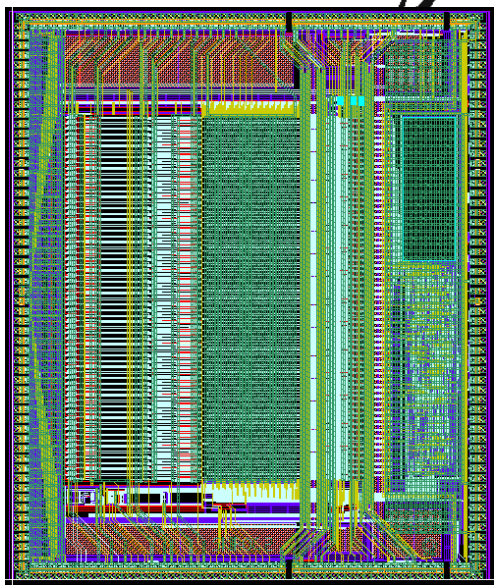
Single-sided slabs to fit into EUDET structure

~45x5 mm2 strips, MPPC readout

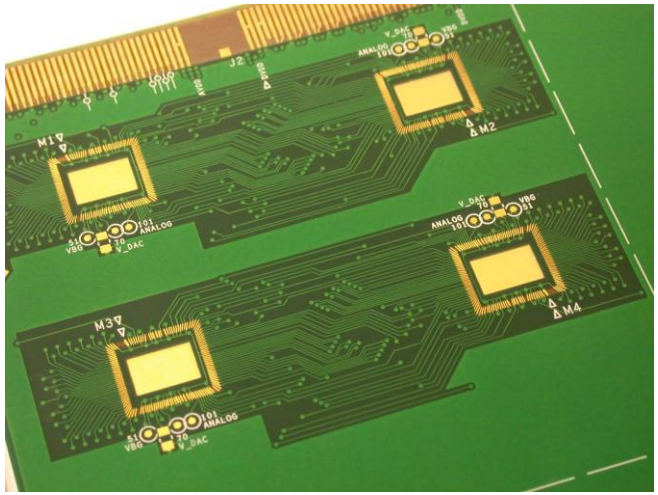
PCB: Similar requirements to AHCAL → work with DESY
- MPPC mounting/readout
- Gain monitoring system

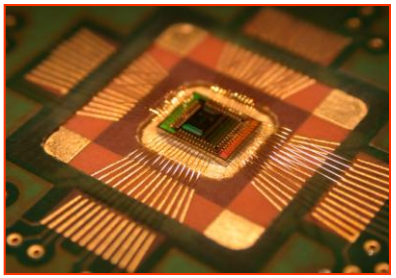
SKIROC : ECAL readout

- SKIROC2 : Silicon Kalorimeter Integrated Read-Out Chip
  - 64 channels, 70 mm^2
  - Very large dynamic range: HG for 0.5-500 MIP, LG for 500-3000 Mip
  - Collab. with LLR
  - Testability at wafer level



- Front End boards crucial element
  - Collab with Korea





JRA3 summary and perspective

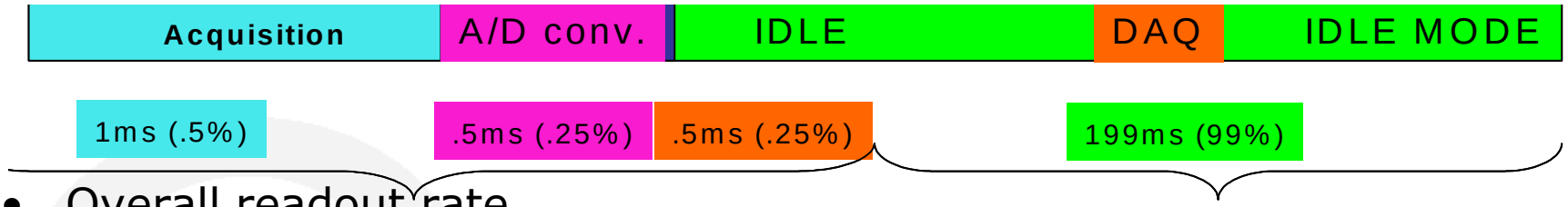
- Nice infrastructure essential to prove ILC calo feasibility
  - ECAL, HCAL : Mechanical infrastructure + new sensors
  - Light calibration system
  - Embedded electronics with 2nd generation DAQ
  - First power pulsing operation at system level
  - FCAL : new sensors and readout electronics

- All milestones completed, good starting point for AIDA
  - Large scale mechanical structure
  - Thousands of readout chips
  - 2nd generation DAQ infrastructure
  - Lots of important tests ahead : Power pulsing, coherent noise, power dissipation, timing, system aspects, DAQ…
  - Small Testbeam program starting

Backup slides

Test beam with technological prototype

- Data rate (Spiroc/Skiroc) : naive estimate
  - Volume : 36ch*16sca*50bits=30 kbit/chip
  - Conversion time : 16*100 µs = 1.6 ms
  - Readout speed 5 MHz (could be increased to 10-20 MHz)
  - 8 chips/DIF line (one FEV only)
  - Total : 1.5ms + 30000*200ns*8 = 50 ms/16 events = 3 ms/evt => 300 Hz during spill



- Overall readout rate
  - « Add » 1-10% power pulsing : 3-30 Hz effective rate
  - Pessimistic as assuming all chips full
  - **interesting tests to be done**

- Note : readout electronics designed for ILC low-occupancy, low rate detector **≠Testbeam** !!

Read out: token ring

- Readout architecture common to all calorimeters
- Minimize data lines & power