HCAL task status report

Erika Garutti

EUDET steering committee

DESY, 31 Aug. 2010

Deliverables

- HCAL mechanical structure
  - no latest update, structure(s) exist, ready to be equipped
- HCAL readout integrated electronics
  - new SPIROC integration tests and results
- HCAL calibration system
  - transnational access (DESY TB21) Prague+DESY

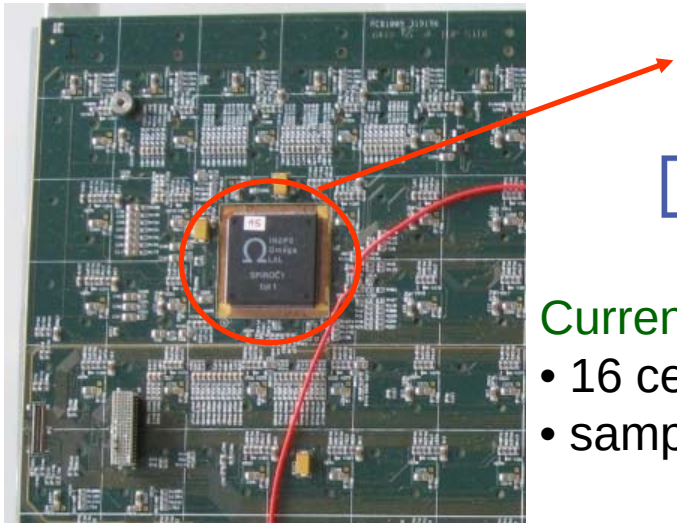
The SPIROC chip

Specific chip for SiPM:

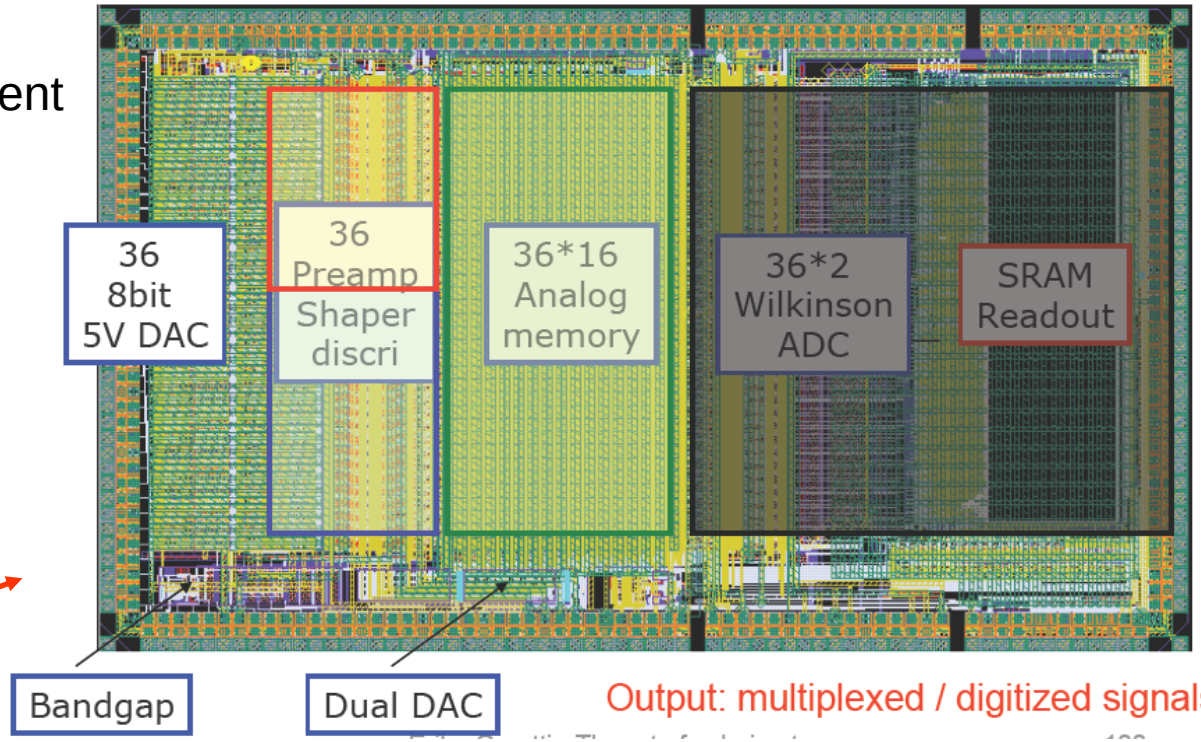
- input DAC for bias adjustment

Designed to work at ILC:

- power pulsing mode
- 25 μW /ch
- internal ADC
- auto-trigger mode
- time stamp (~1ns)



SPIROC layout (CALICE chip for Analog HCAL readout)



Output: multiplexed / digitized signals

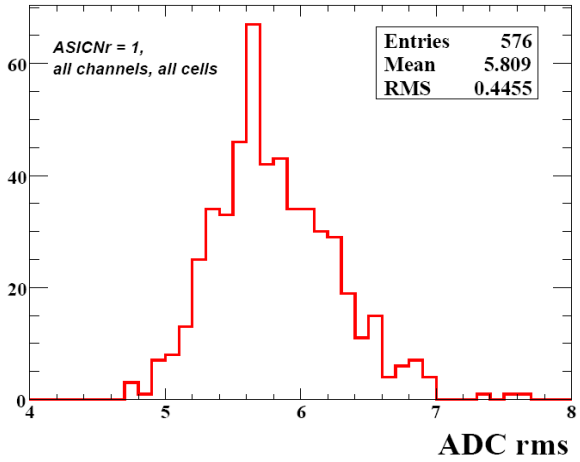
designed by Omega group LAL (Orsay)

Current challenges in chip understanding:

- 16 cell analog buffer memory ➔ characterize properties
- sample and hold method ➔ determine spread

SPIROC characterization

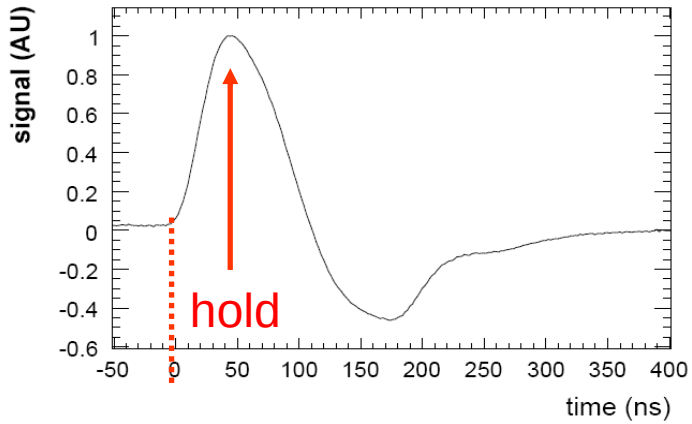
Electronic noise in the 16 buffer memory cells of the 36 channels of one chip



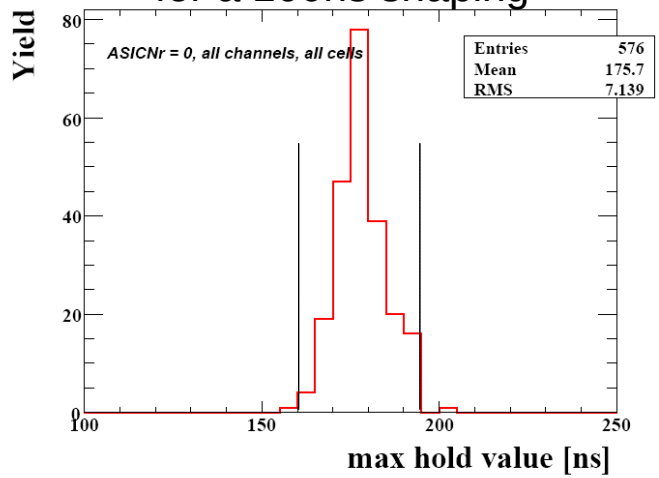
σ_{el} ~ 6 ADC ch. (on a 12-bit ADC)

- common hold to all channels in a chip
- spread of hold values in a chip ~ 7ns RMS
  (~ 40 ns min-to-max)
- <1% effect on signal meas. (max. -3.5 %)
- compensated by calibration

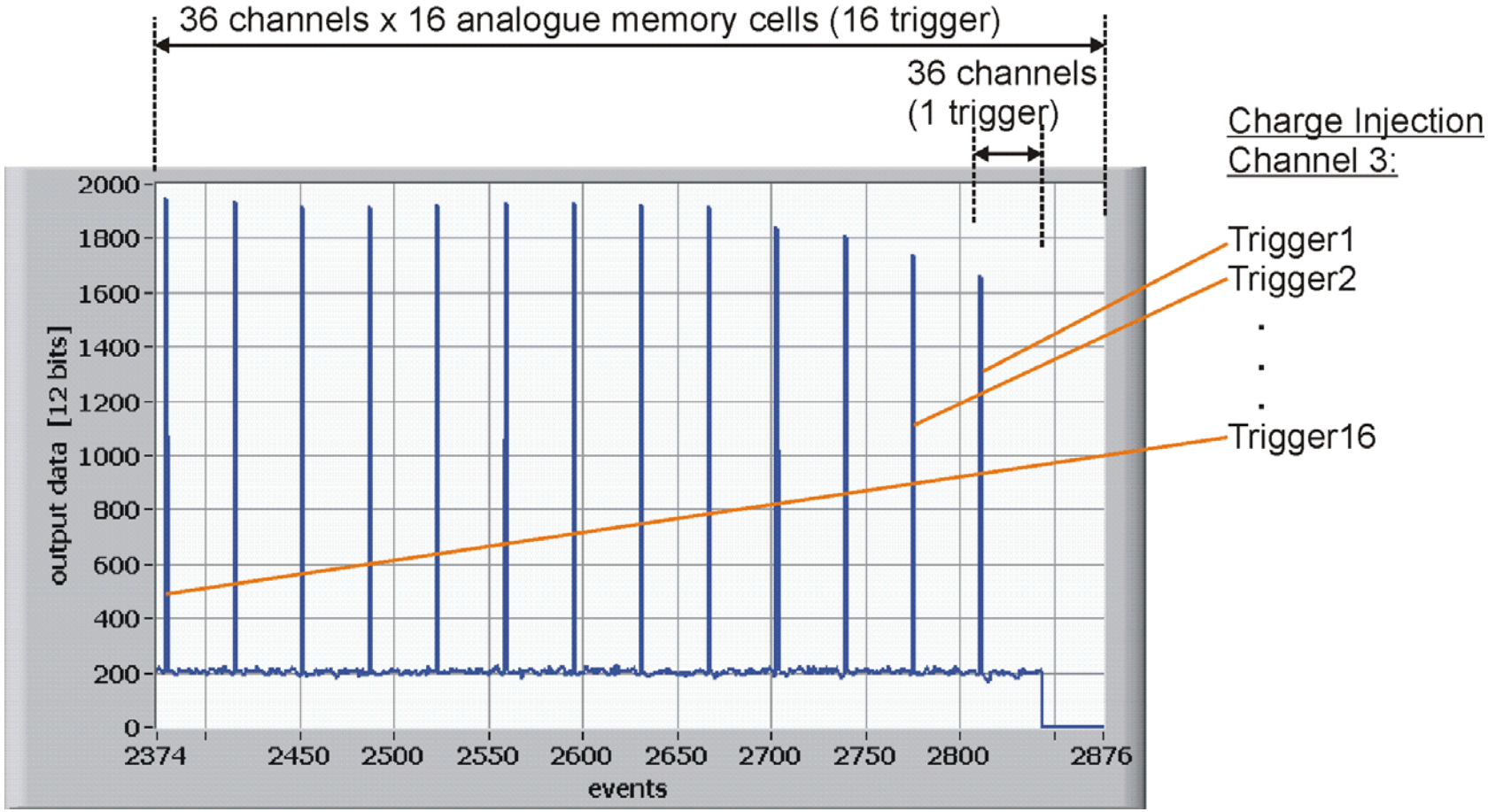
SiPM signal after preamp. & shaper



for a 100ns shaping

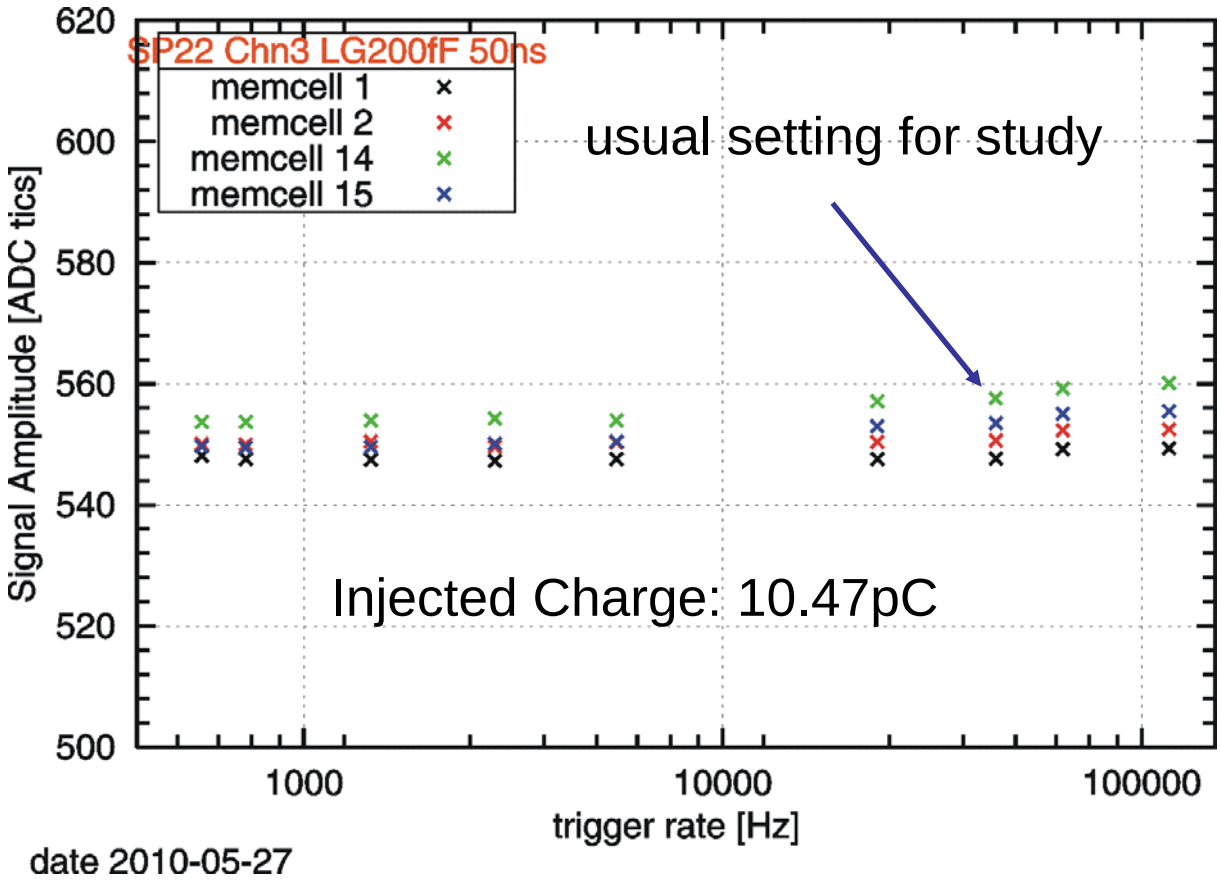


Investigation of the buffer memory cells



For a given input signal on one SPIROC channel observed a decrease of measured charge in the first buffer memory cells (early triggers)

Check dependency on trigger rate



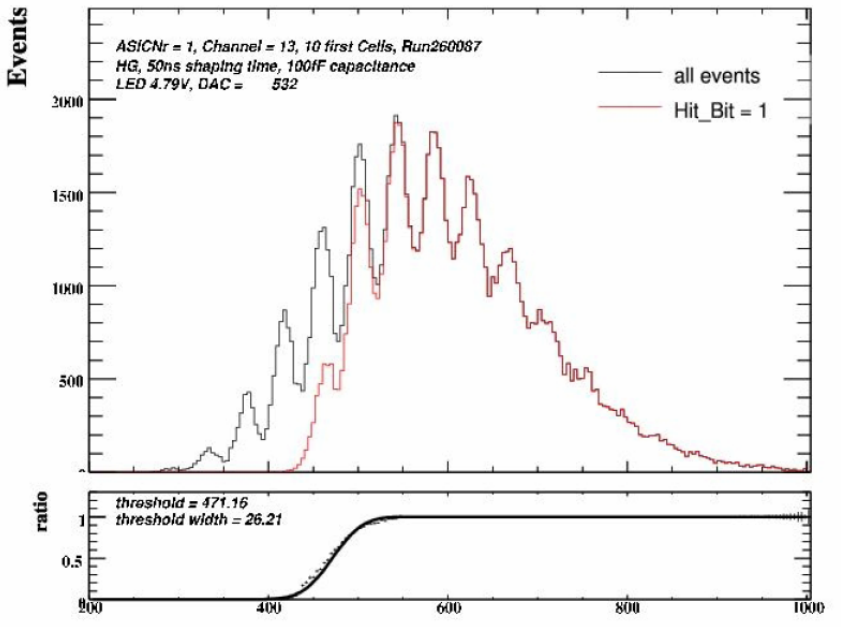
SP22,
LowGain,
small input charge

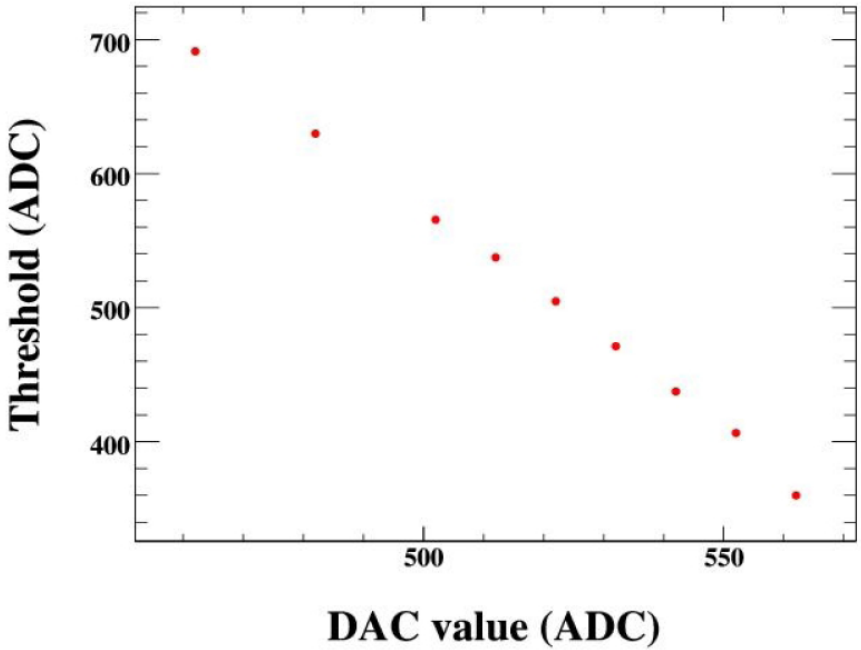
signal on memcell1 is stored the longest time.

No signal loss during storage in analogue memory can be observed!

Auto-trigger: Threshold Adjustment

Aim: understand how to set the auto-trigger threshold (DAC) for an input MIP signal, and study the auto-trigger behavior

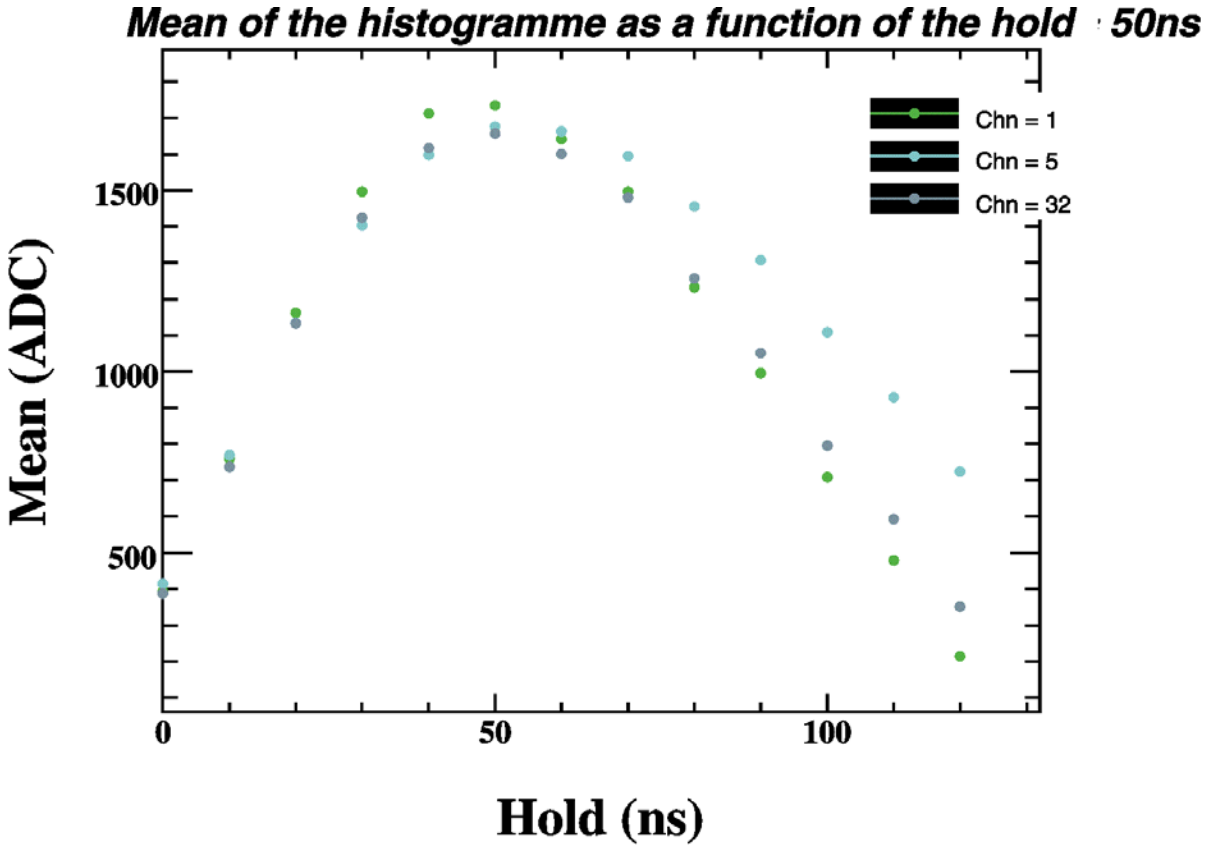




Results by
Jeremy Rouene

Auto-trigger: signal hold

Spread of hold signal in auto-trigger mode similar to external trig. mode



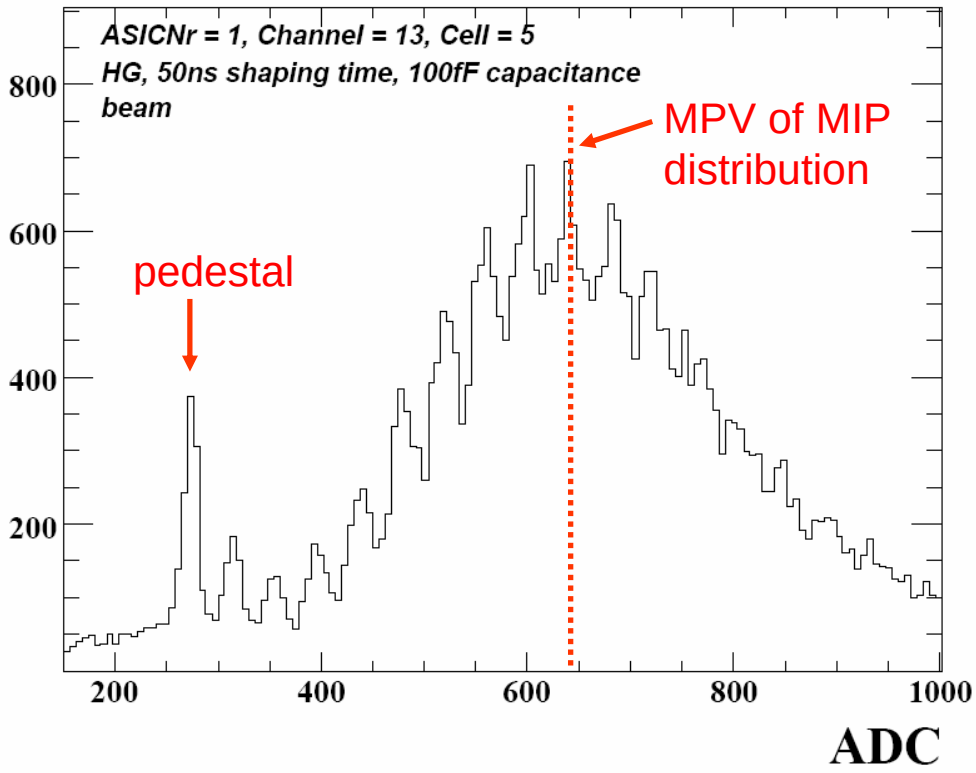
Results by
Jeremy Rouene

First look at test beam results

First cassette of AHCAL engineering prototype exposed to 3 GeV e^- beam at DESY

(no absorber plates)

- At MIP level S/N ~ 45
- Single p.e. spectrum visible in MIP energy distribution
- SiPM gain: $G_{LED} = G_{MIP}$ (~42 ADC ch.)
- σ_{ped} ~ 7.5 ADC ch.
- At single pixel level: S/N ~ 5.5



First look at test beam results

First cassette of AHCAL engineering prototype exposed to 3 GeV e^- beam at DESY

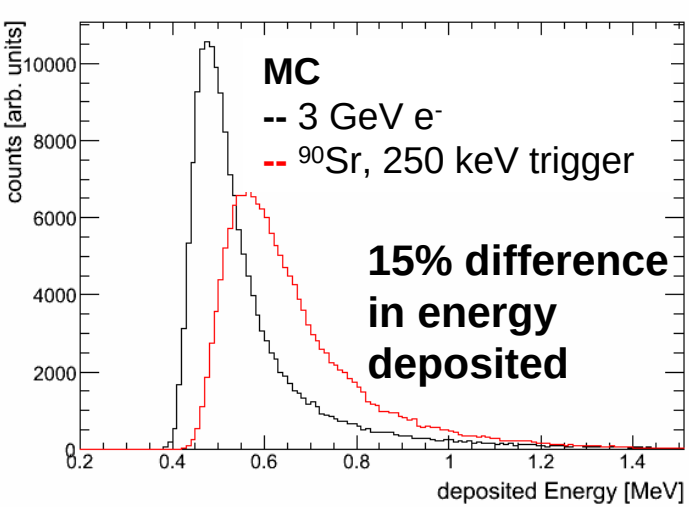
(no absorber plates)

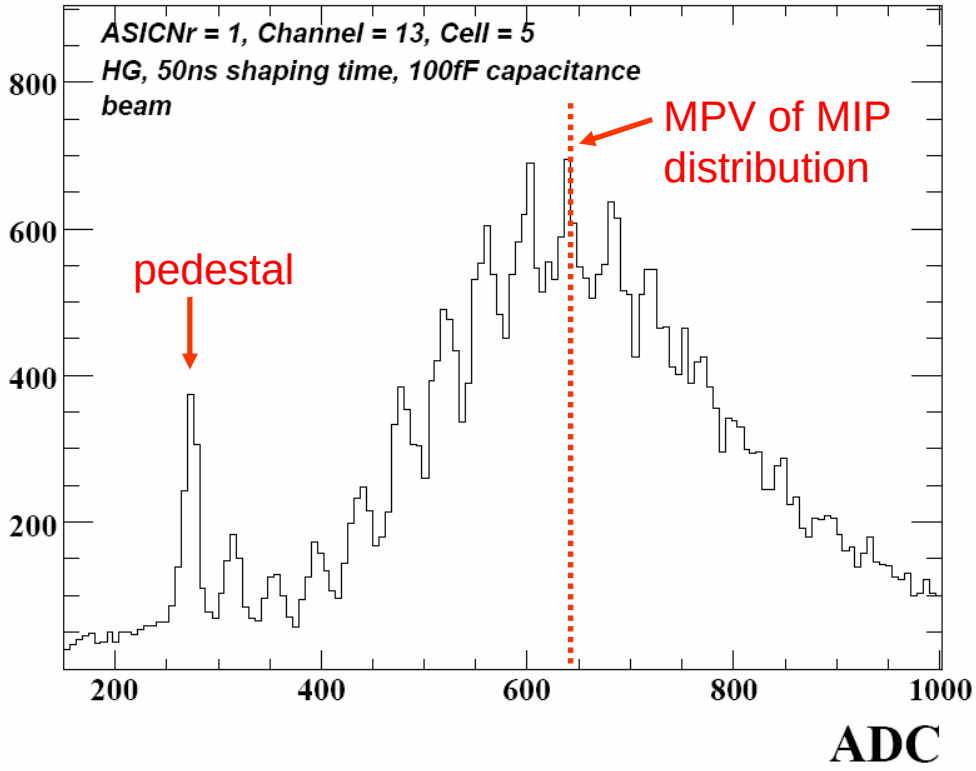
- At MIP level S/N ~ 45
- Single p.e. spectrum visible in MIP energy distribution
- SiPM gain: $G_{LED} = G_{MIP}$ (~42 ADC ch.)

- LY = 9 pix / MIP (3 Gev e^-)

Characterization from producer

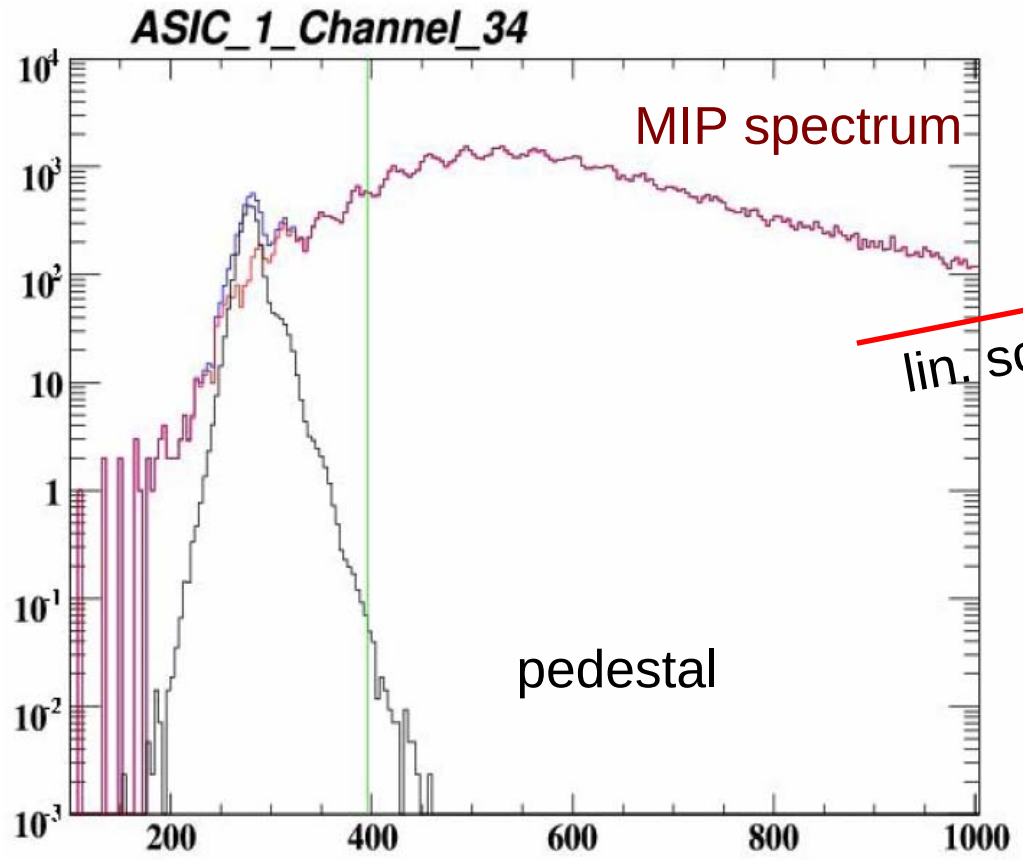
LY = 10.3 pix / MIP (1-3 MeV e^-, ^{90}Sr)



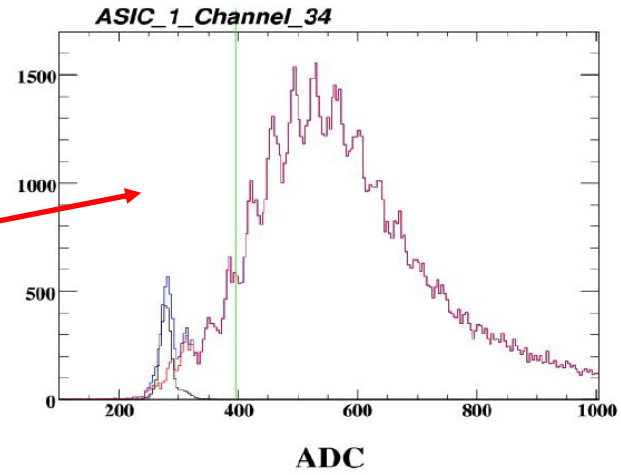


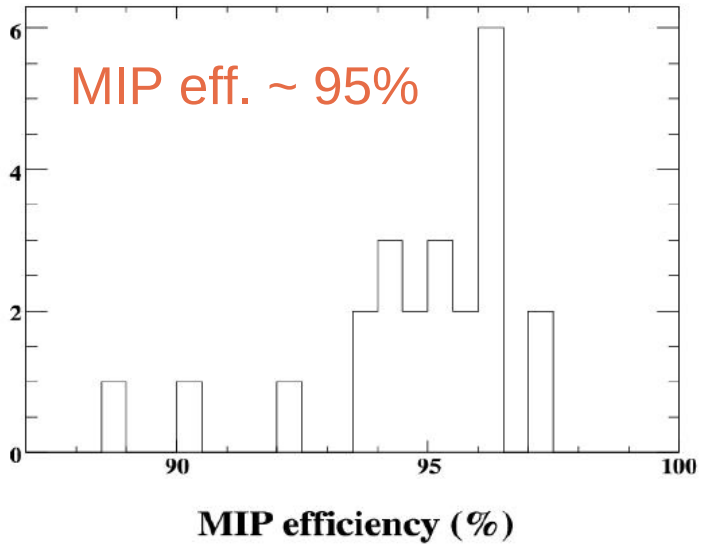
➔ LY in agreement considering different energy deposited by reference e-

Noise above threshold



lin. scale





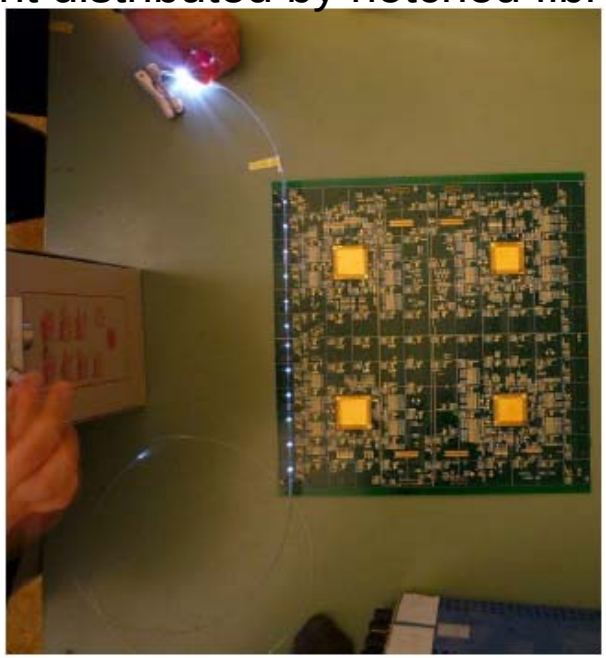
- fix threshold to have 10^{-4} hits / events above threshold
- adjust individual DAC threshold (not possible in current chip)

LED monitoring system(s)

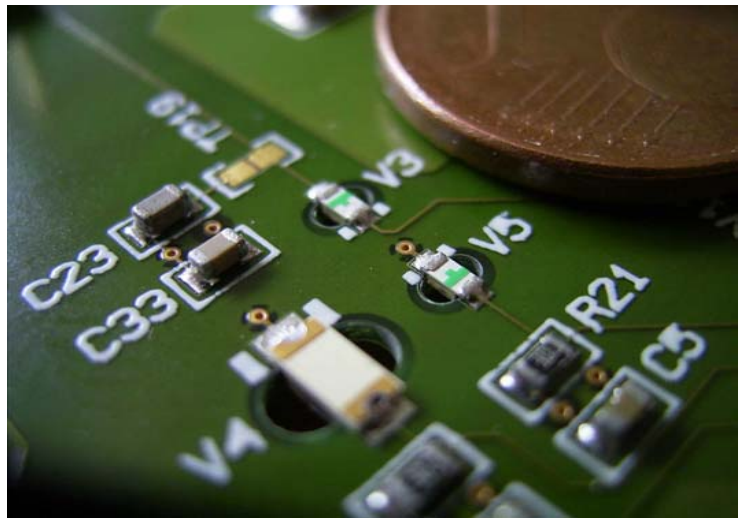
System task: SiPM gain calibration via single photoelectron peak spectra (~1-2 p.e.)
long term stability via response @ medium light (~20-100 p.e.)
measure SiPM saturation level (~2000 p.e.)

Two technological solutions:

Light distributed by notched fibres



Light directly on tile by SMD-LED - distributed LED

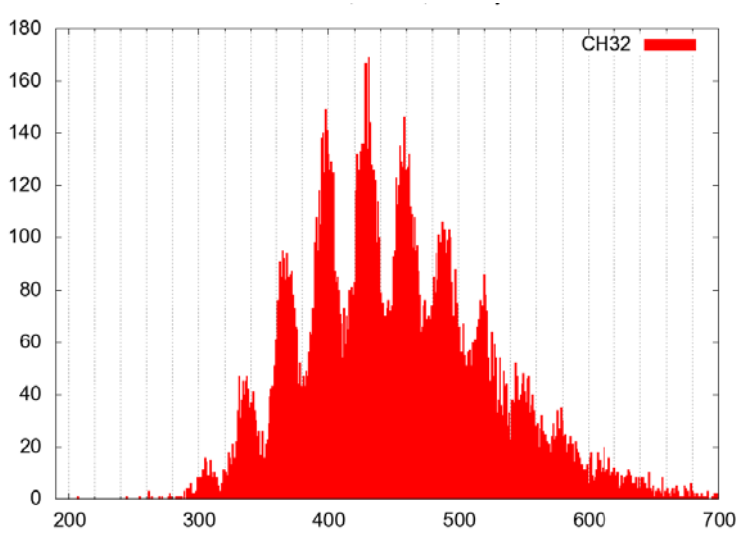


LED monitoring system(s)

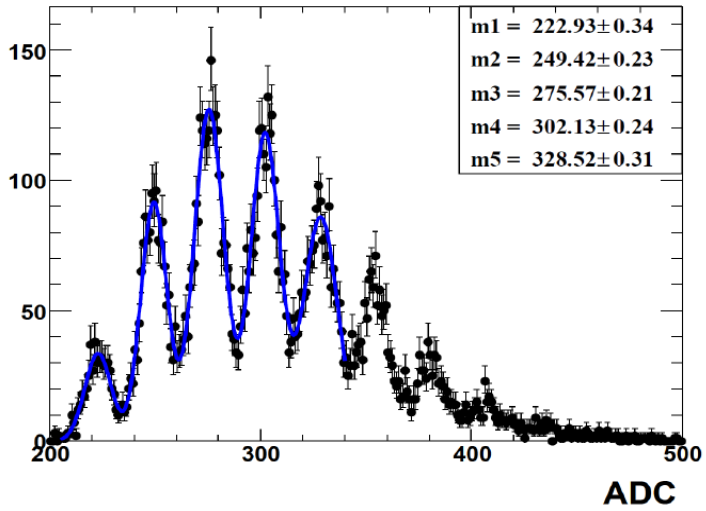
System task: SiPM gain calibration via single photoelectron peak spectra (~1-2 p.e.)
long term stability via response @ medium light (~20-100 p.e.)
measure SiPM saturation level (~2000 p.e.)

Two technological solutions:

Light distributed by notched fibres

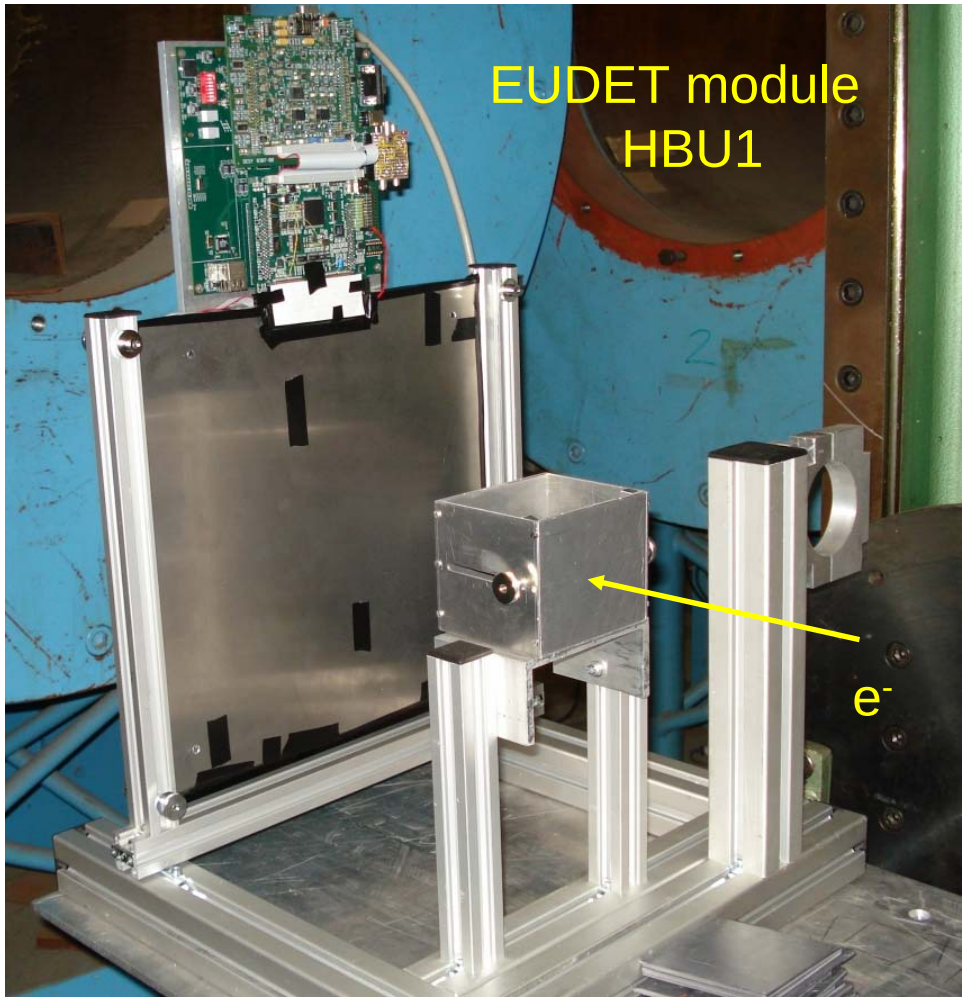


Light directly on tile by SMD-LED
- distributed LED



Both systems commissioned ➔ SiPM gain calibration achievable
Next step ➔ reduce spread in light intensity between channels

First transnational access in DESY TB21



EUDET module equipped with ITEP tiles + SiPM,

Prague LED distribution system and DESY LED on tile compared on the same device

Test beam setup

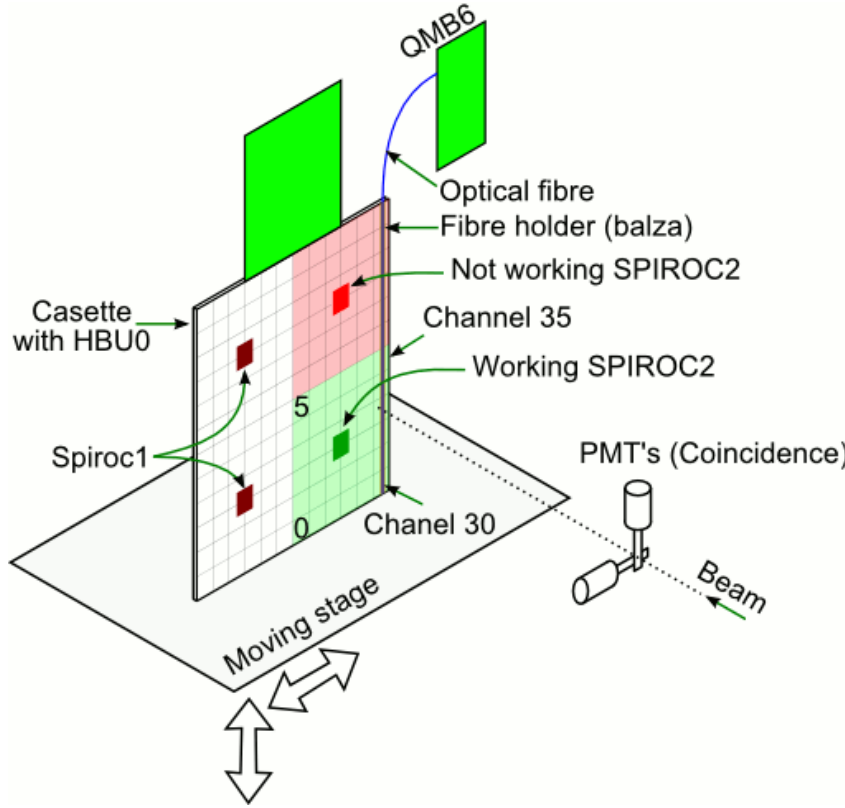
ASIC0 (green) fully working
Programming problems with ASIC1 (red)

Beam trigger: concidence of PMTs
Six channels iluminated by the notched fibre

Control: Labview DIF + QMB6 labview control

Modes of operation:
- Trigger from beam trigger
- Internal DIF trigger
- Autotrigger not tested at that time

Measured data:
- MIP signal in High gain and Low gain
- Gain between MIP in HG and LG using MIP signal
- Scan over various V1 setting of the QMB6
- Scan of the hold value
- Scan over the period of the internal trigger



slides from Jiri Kvasnicka

Preliminary Results

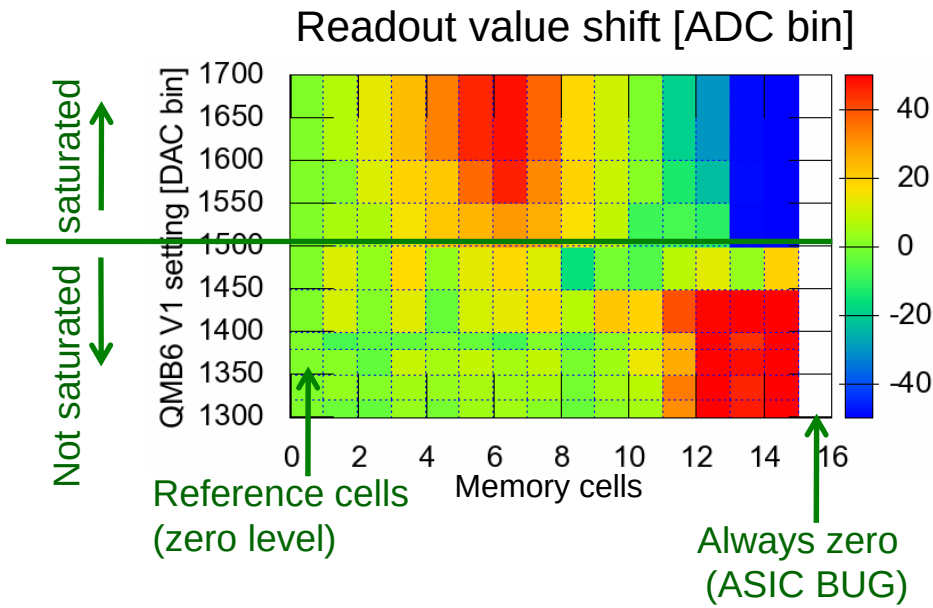
Inconsistence among the analog memory cells – hard to predict the shift

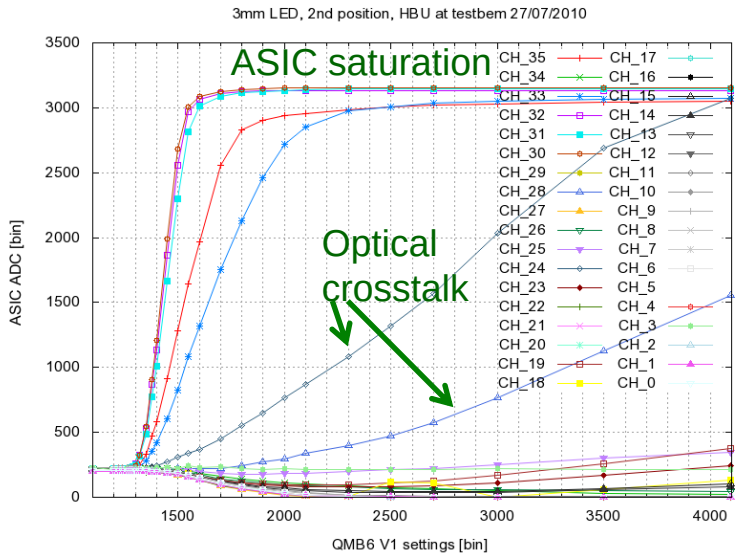
1 dead channel discovered in ASIC1 (Ch. 3)

1 bad tile/channel (Ch. 34) – no response even at the beam

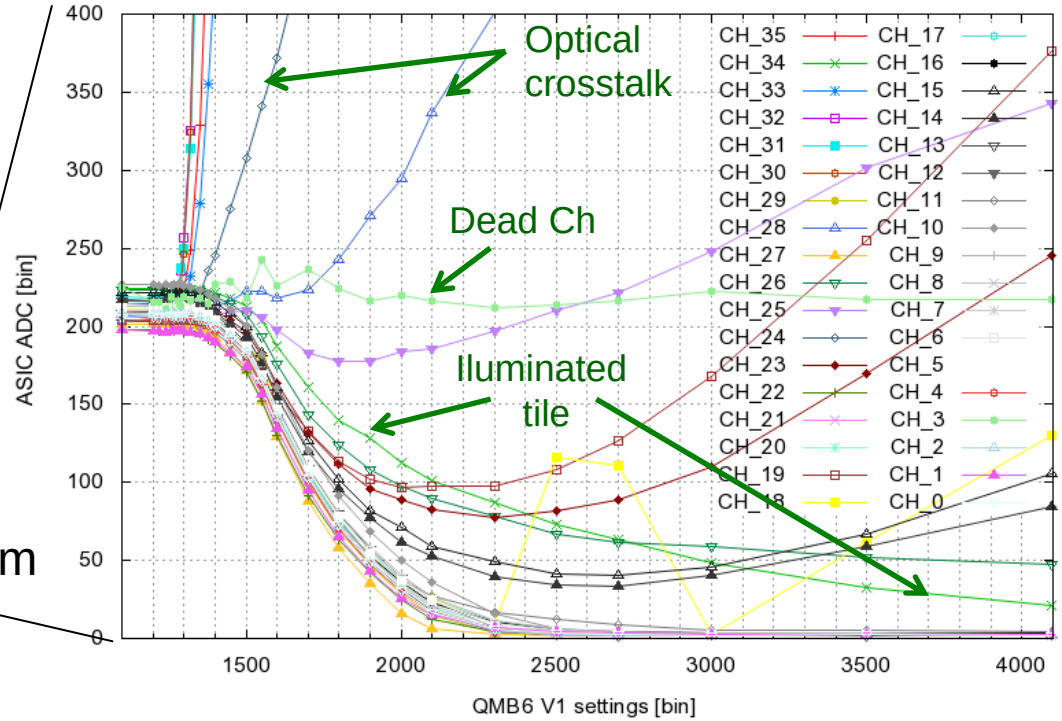
Large pedestal shift in High Gain mode

Data analysis in progress





zoom



1 row of cell iluminated:

Conclusions

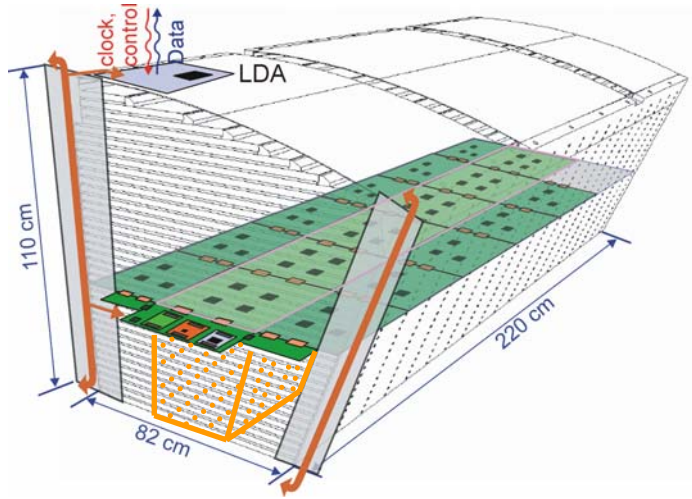
- prototypes are assembled and tested. All components delivered:
  - CALIB and POWER modules: available
  - Calibration multi-channel prototype: both options available
  - Mechanical structure: available
- Full system integration (electronics + mechanics) incorporating tiles and SiPMs from first user completed
- both EUDET modules (HBU) operated at DESY TB

➔ Trans-national access: 2 weeks test of Prague LED system (analysis ongoing)

Outlook

Next steps (within and beyond EUDET) :

- integration tests to full slab (2.2 m calorimeter layer)
- redesign of detector interface cards (on-going)
- test of a calorimeter tower (multi-layer operation)

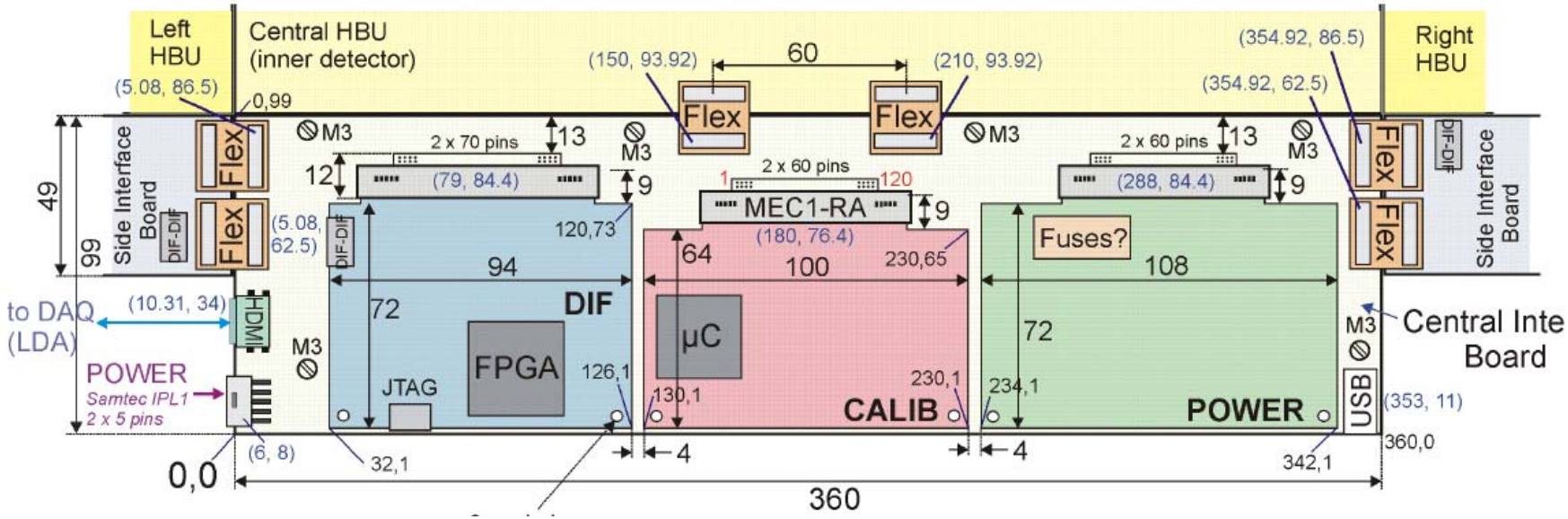


Full scale area integration (slab) requires redesign of HBU started

Multi-layer integration (tower) requires redesign of end-face components

DIF	started
CALIB, POWER	done
PCB support for all cards	done

Status of electronics redesign



X done

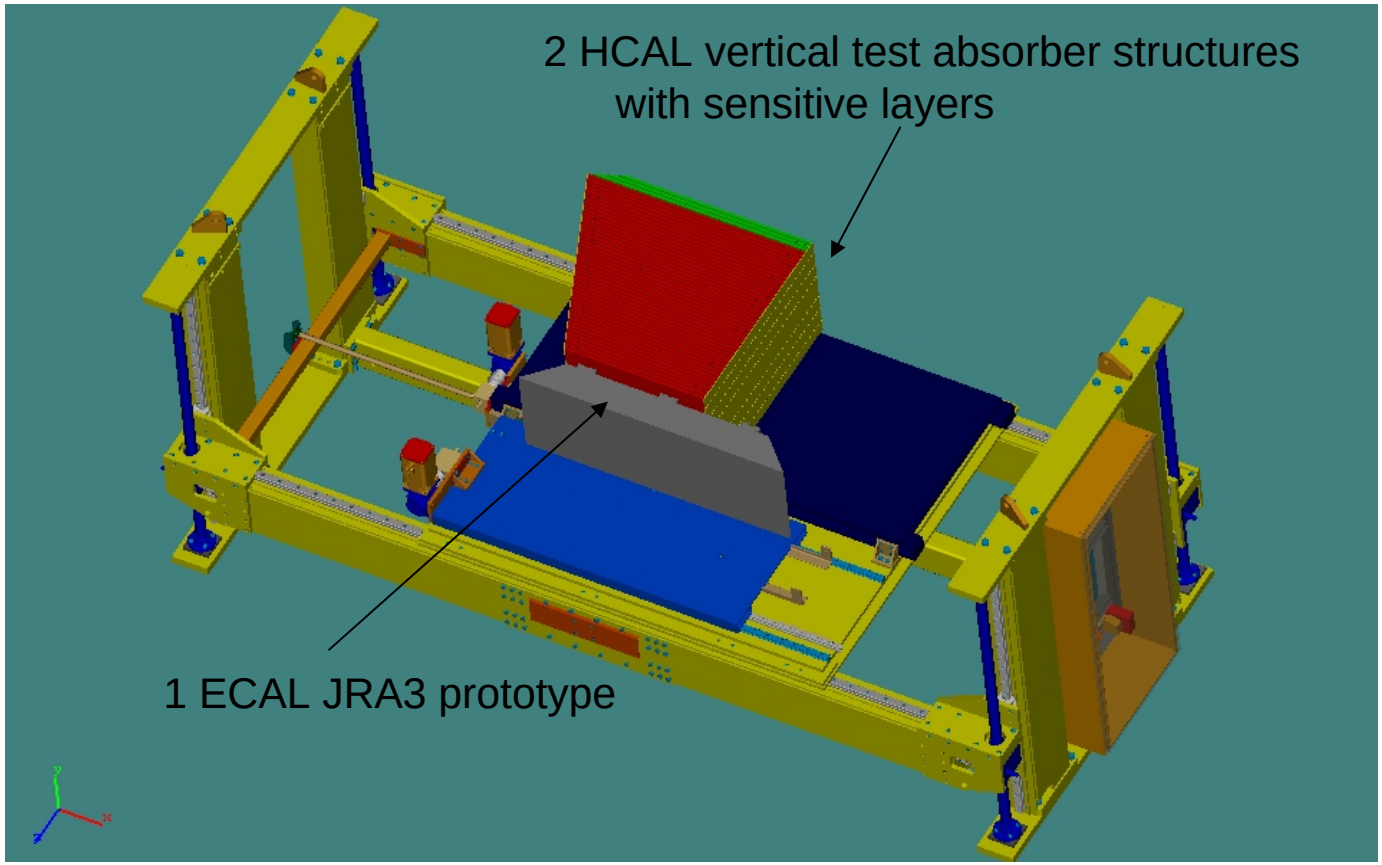
X in preparation

X not started yet

	DIF	CALIB2	POWER2	HBU2	CIB	SIB	Flexleads
concept dev., circuit design	X	X	X	X	X	X	X
schematic entry	NIU	X	X	X	X	X	X
Layout	NIU	X	X	X	X	X	X
Production	NIU	X	X	X	X	X	X

DESY Redesigns: module.
M. Zeribi, H. Wentzlaff,
M. Reinecke

Future HCAL project



- Mechanical structure assembled together with ECAL for test beam experiment
- Test in magnetic filed also under discussion