Progress on readout electronics for LumiCal detector

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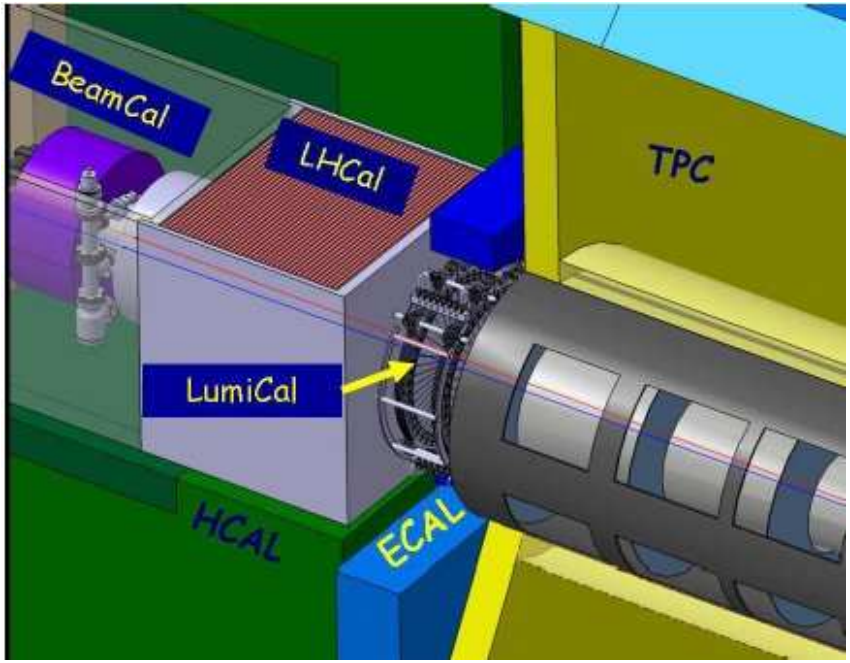
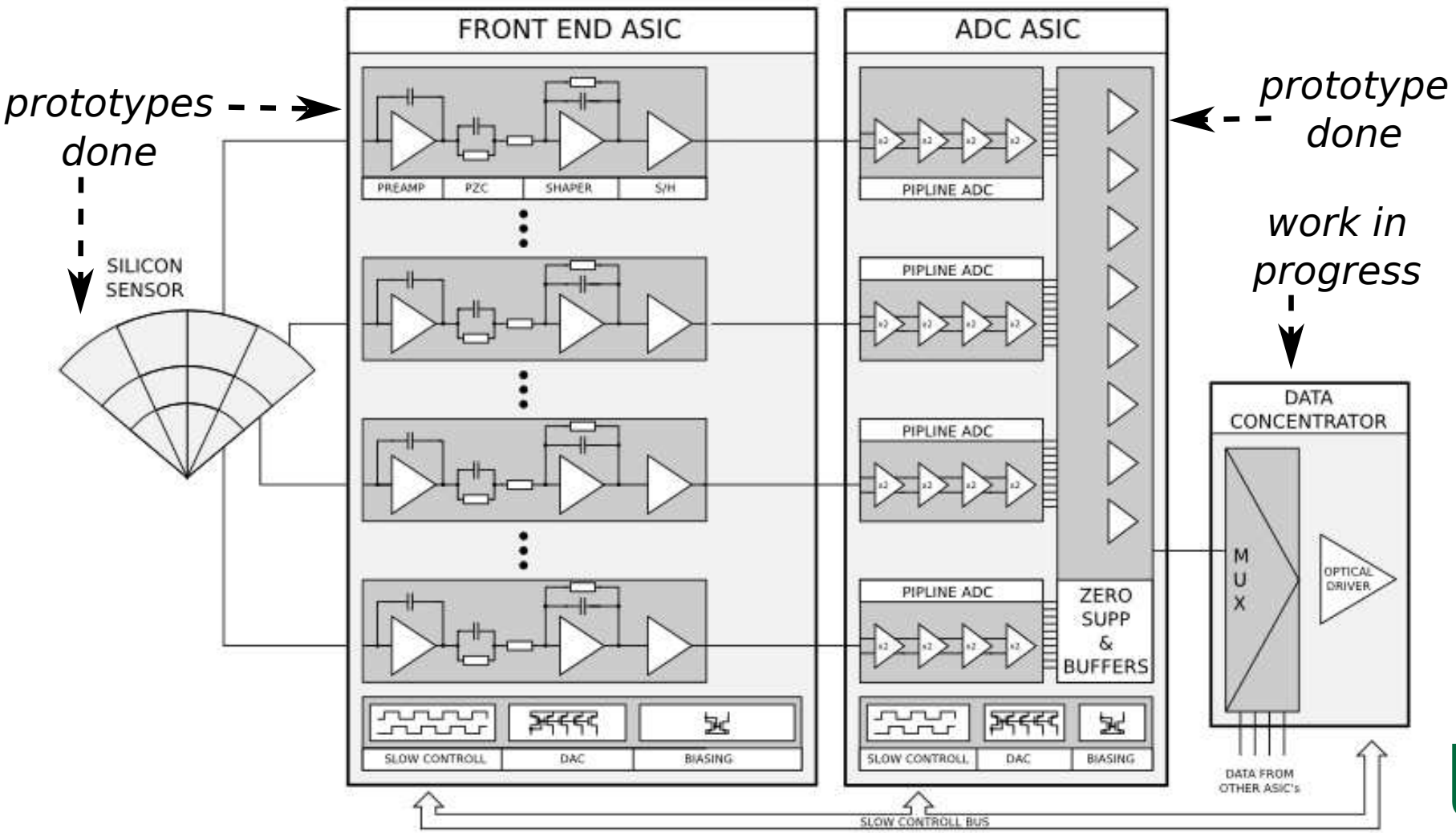
Outline

1. Front-end electronics
2. ADC prototypes
3. Other readout issues
4. Summary and future plans

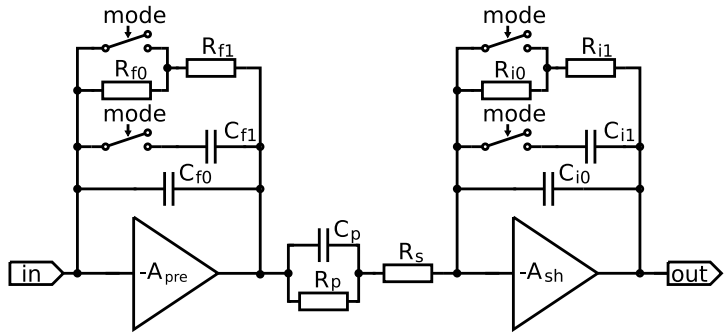


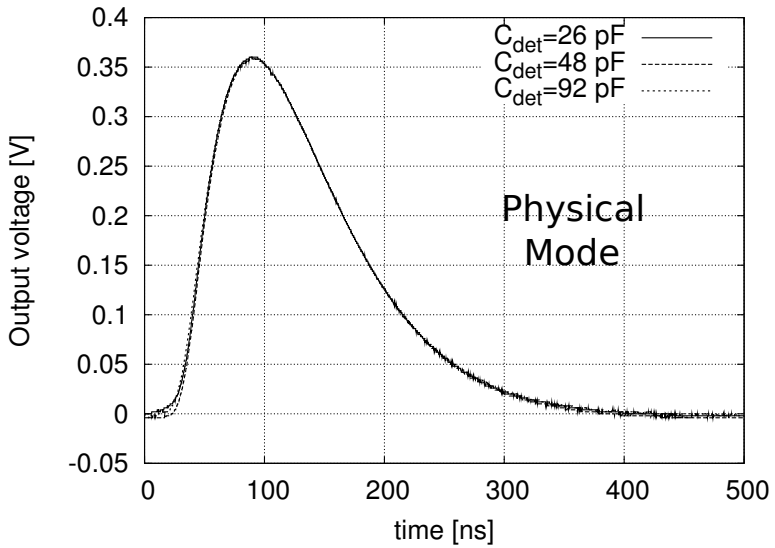
LumiCal readout architecture



Front-end electronics I

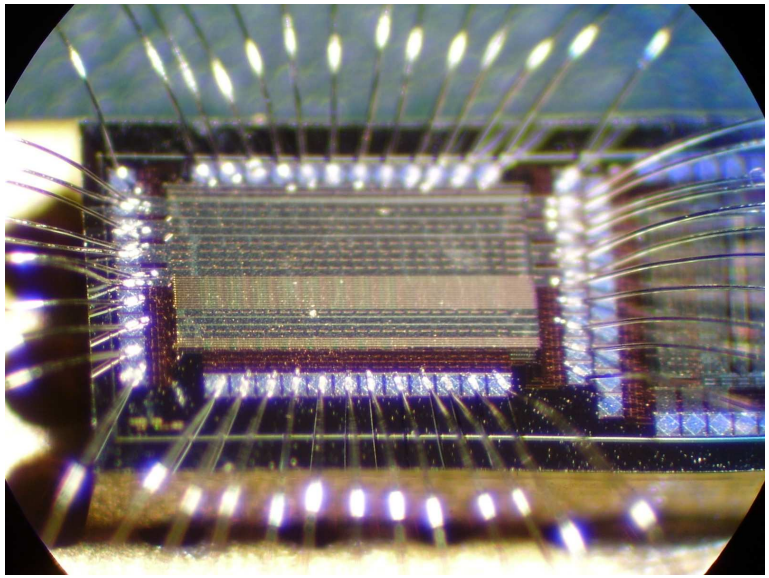
- $C_{det} \approx 0 \div 100$pF
- 1^{st} order shaper ($T_{peak} \approx 60$ ns)
- variable gain: MIP (calibration mode) and input charge up to 10 pC (physics mode)
- power: 8.9 mW/channel
- rate up to 3 MHz





Front-end electronics II

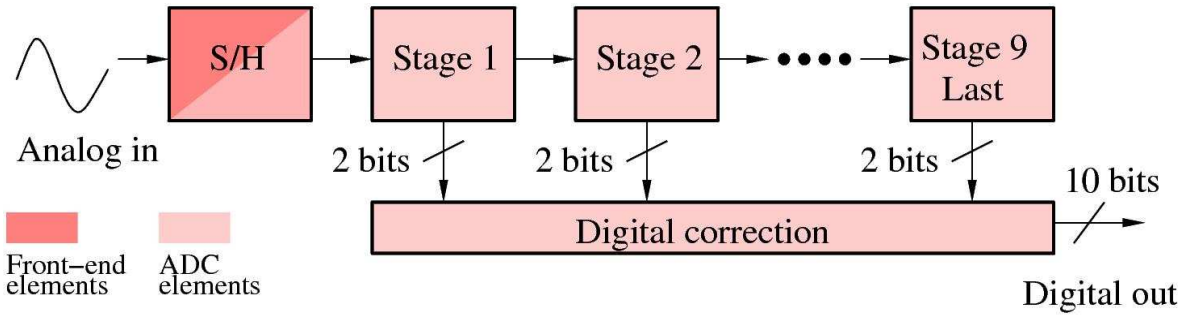
- ASIC contains 8 channels
- measured crosstalk < 1%
- prototypes fabricated and tested (tests completed)



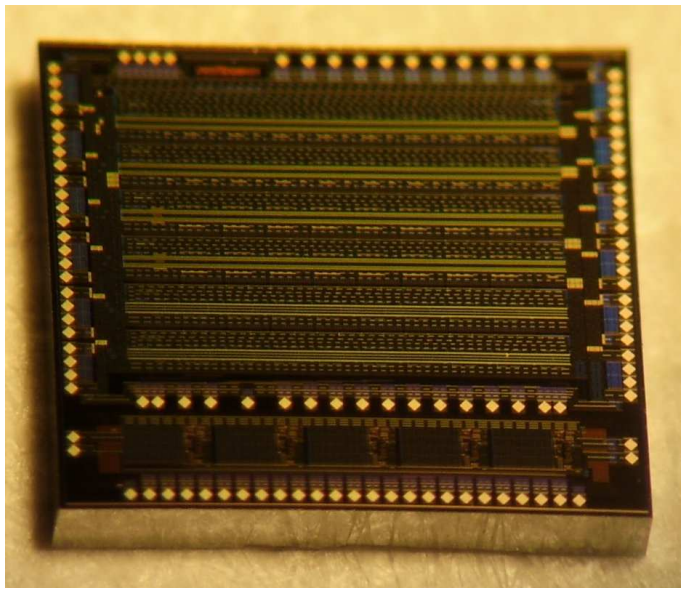
AMS 0.35 μm

- 4 front-end ASICs (32 channels) were used during first test

Single channel 10-bit pipeline ADC



- 1st prototype: only 8 stages (fully functional)
- 2nd prototype of complete ADC (photo)
  - 9 stages + S/H
  - digital correction
  - clock and power switching
  - external reference voltages
- 2nd prototype fully functional, tests completed



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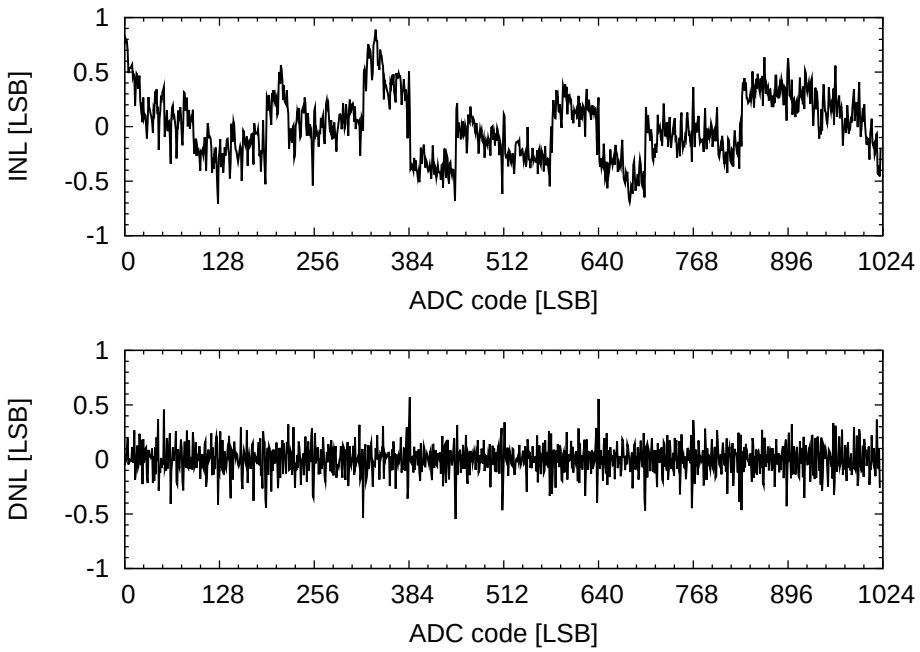
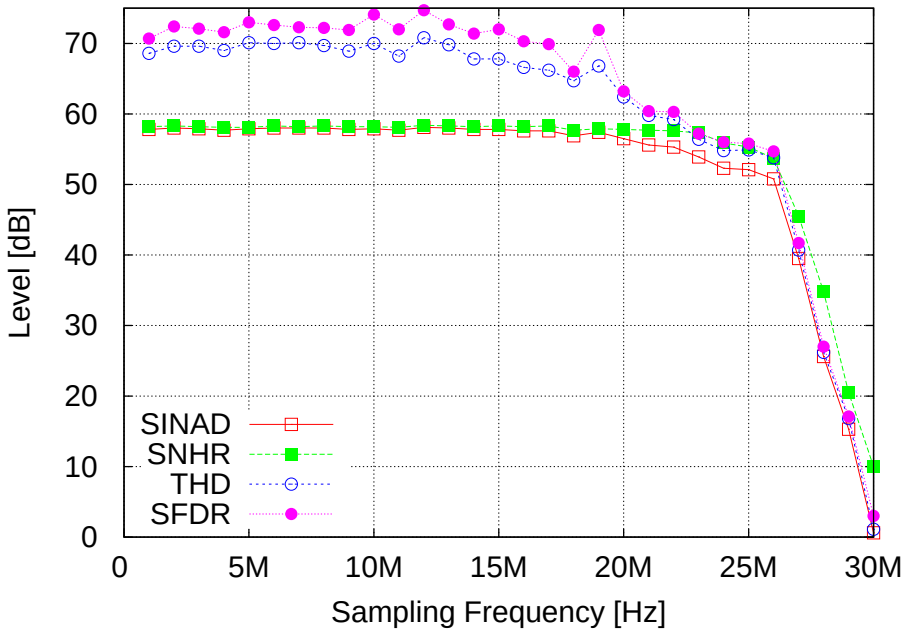
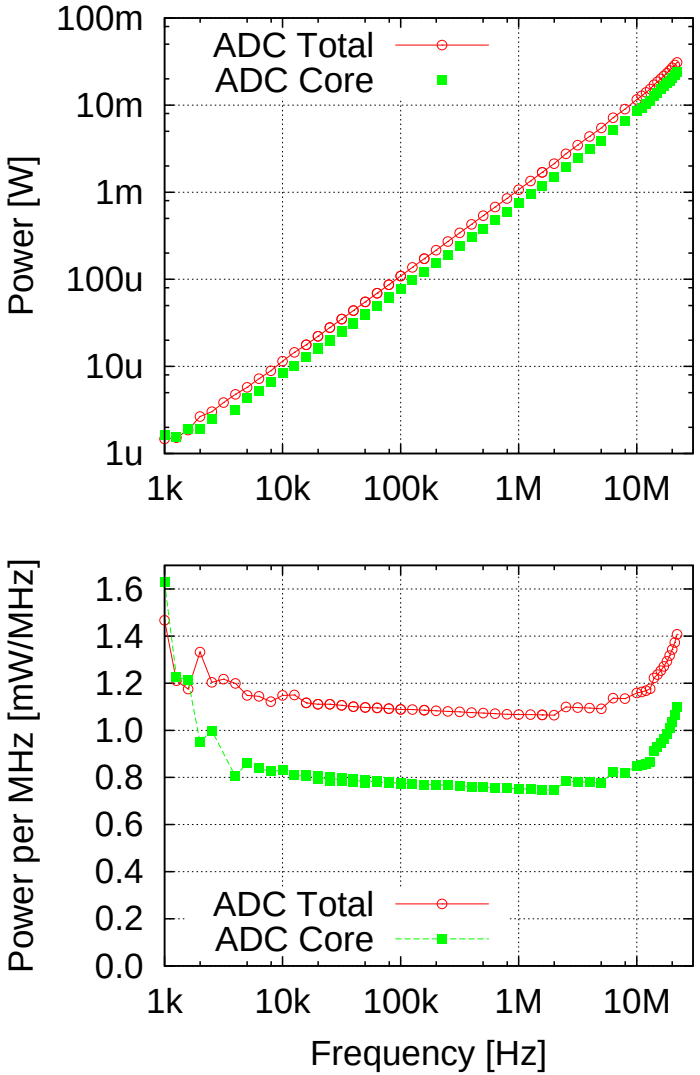
2nd ADC prototype — static and dynamic parameters





- static parameters
  - INL < 1 LSB
  - DNL < 0.5 LSB
- dynamic parameters
  - SINAD = 57.7 dB
  - ENOB = 9.3
- works well up to 25 MHz

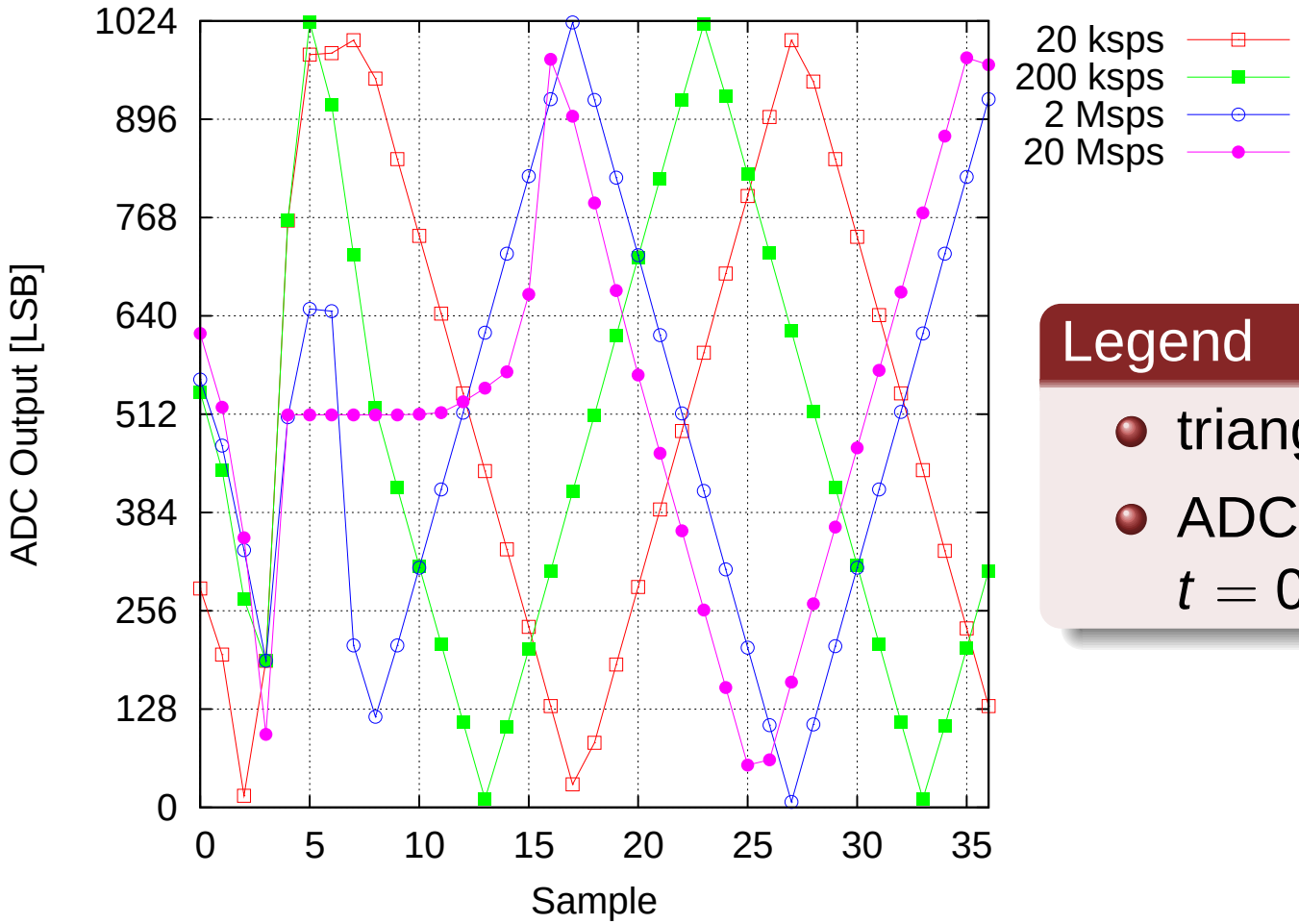
2nd ADC prototype — power scaling



- power consumption scales linearly in frequency range 3 k ÷ 10 MHz
  - 0.8 mW/MHz with supply 3.0 V (plot)
  - 0.6 mW/MHz with supply 2.6 V
- useful also for CLIC

Total includes also input/output buffers

2nd ADC prototype — power switching



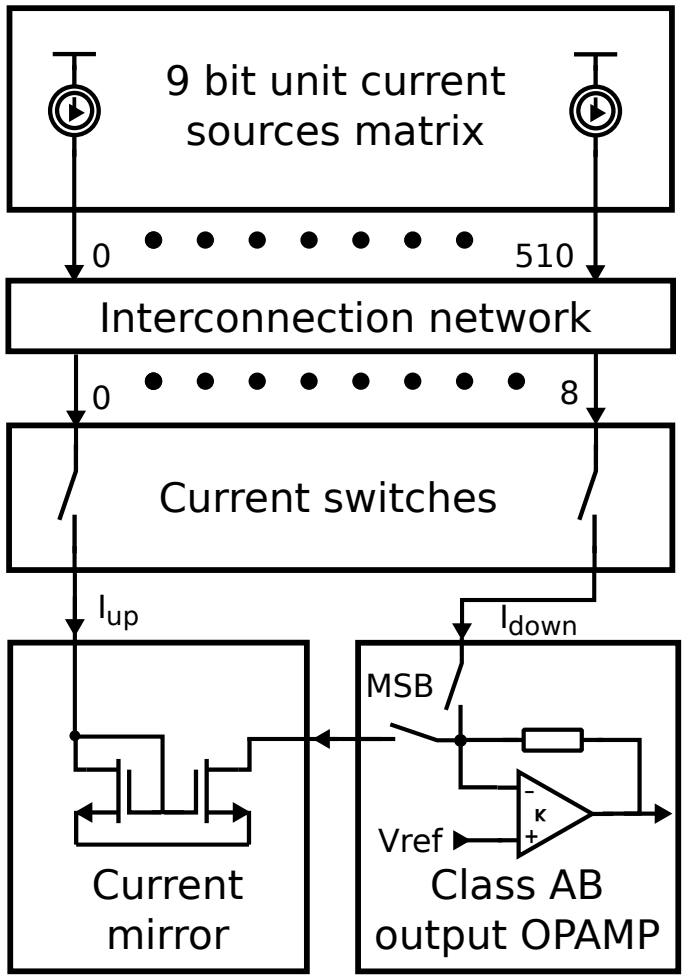
Legend

- triangle input signal
- ADC power ON at $t = 0$

- depending on sampling frequency 8 clock cycles or 800 ns (16 clk @ 20 MHz) needed to restart correct conversion

10-bit low power high swing DAC

- 10^{th} bit achieved by current reversing
- prototype fully functional, tests completed
- nonlinearities DNL & INL < 0.42 LSB
- ENOB = 9.8
- settling time 0.5 – 2 μm
- power consumption 0.6 mW



AMS 0.35 μm

Other readout peripheries

- bandgap based precise reference voltage source, prototype fully functional
- bandgap based temperature sensor, prototype fully functional
- fast LVDS driver and receiver (around 1 Gb/s), prototype fully functional
- first prototype of 1 GHz PLL based wire transceiver, prototype fully functional
- all prototypes were manufactured in AMS 0.35 technology

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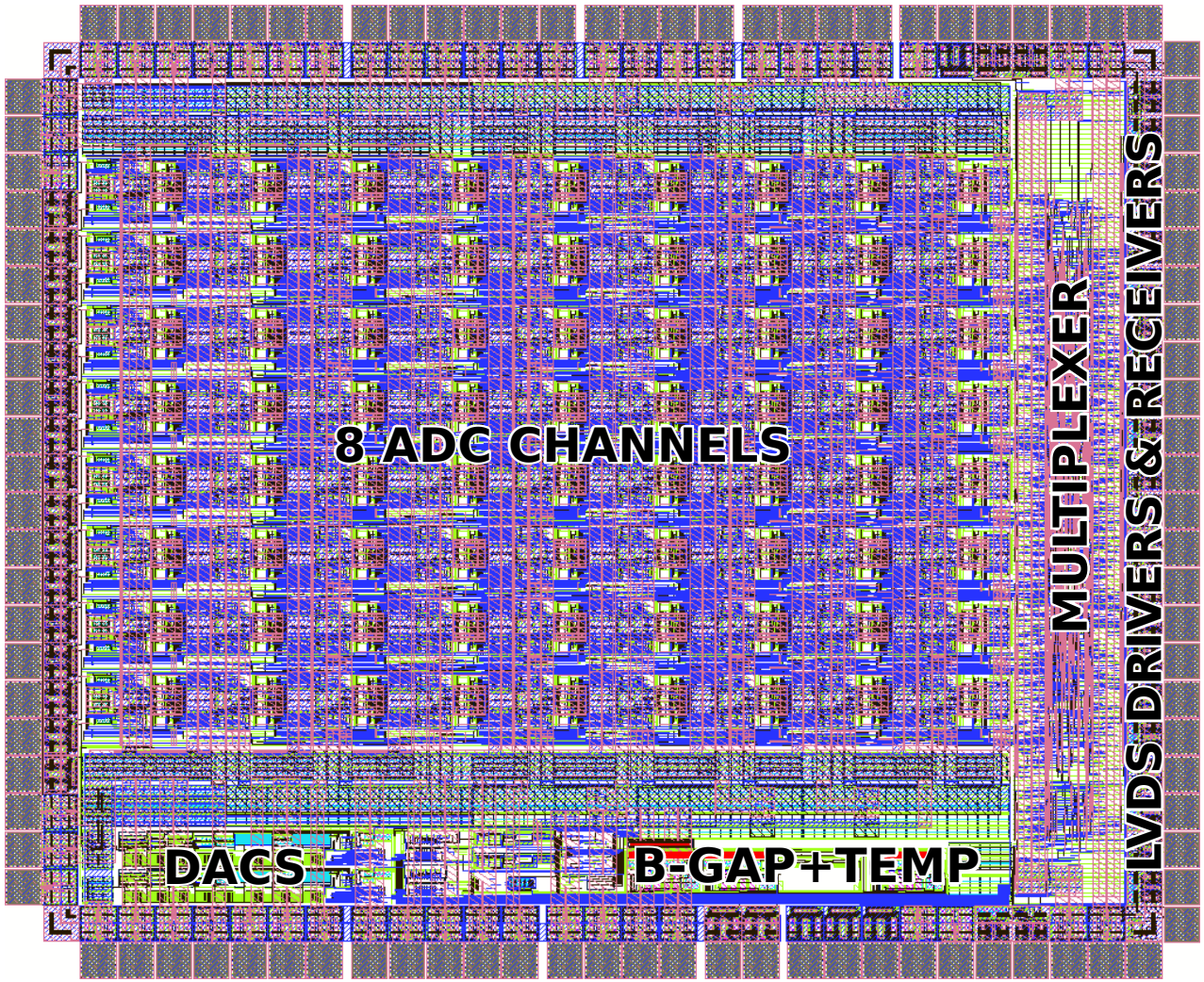
Multichannel ADC — layout



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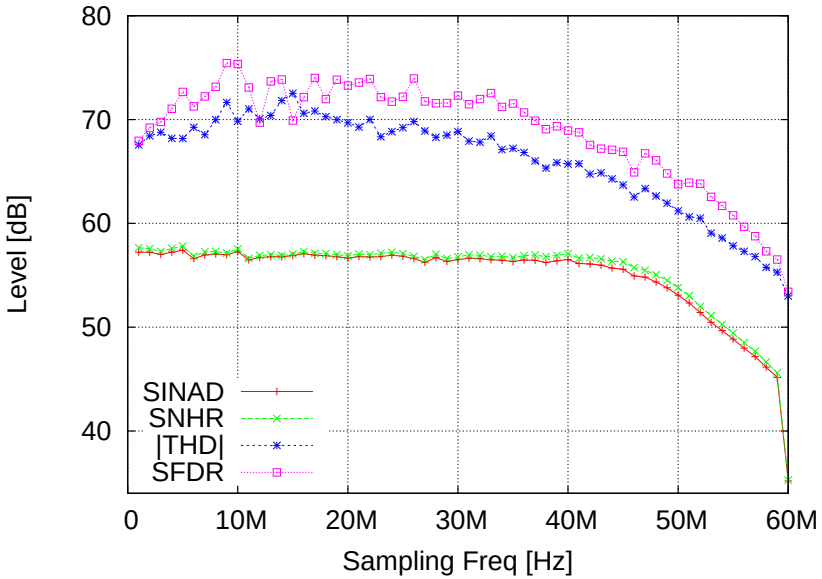
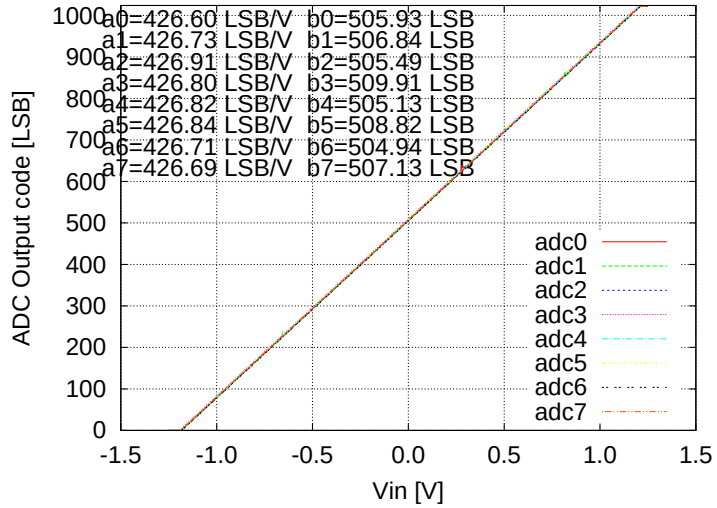
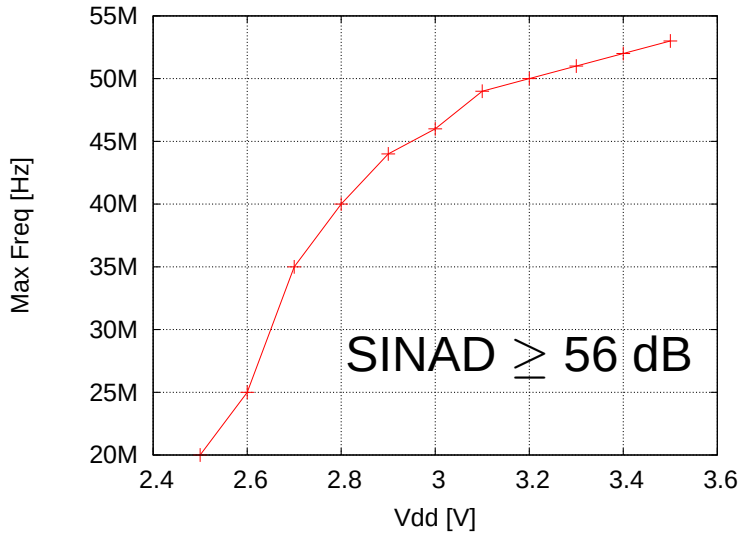
Multichannel ADC — preliminary results

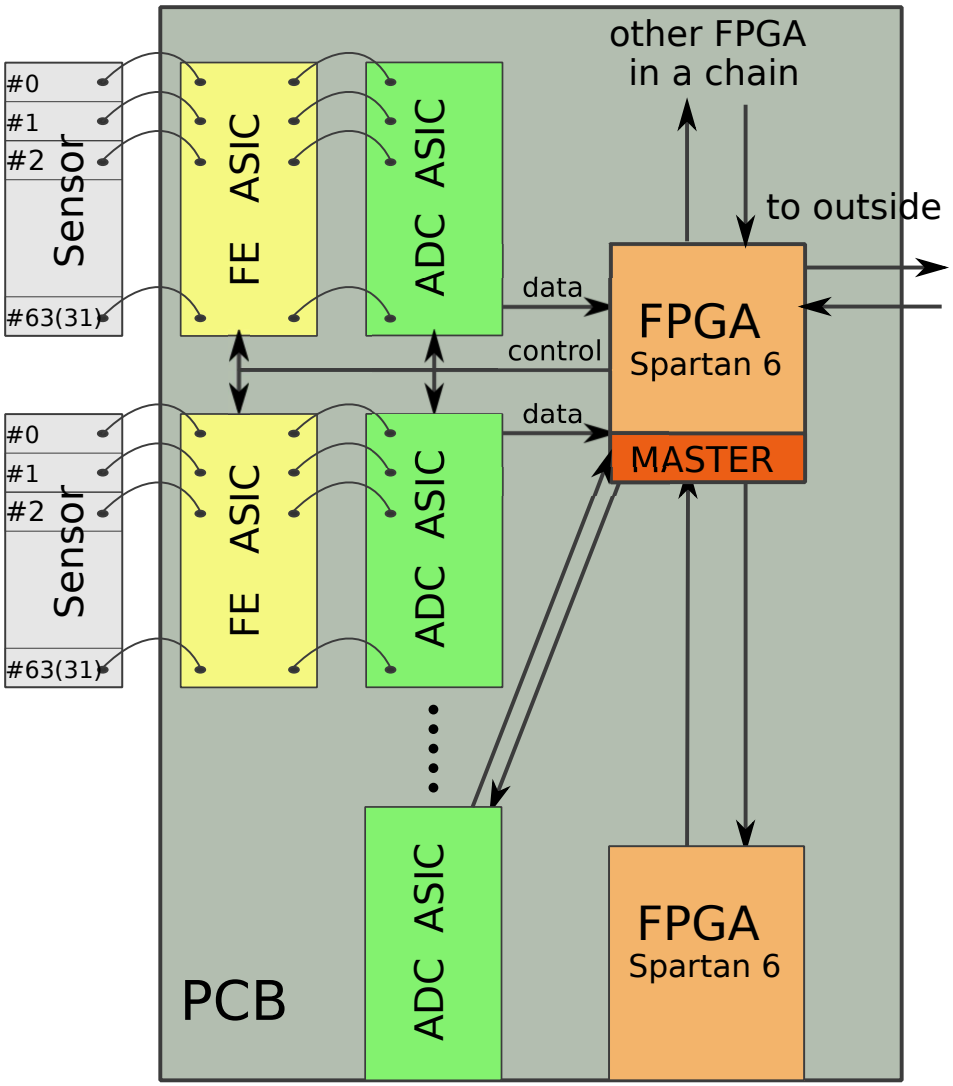
- gain & offset spread < 1%
- maximum sampling frequency about 45 MHz





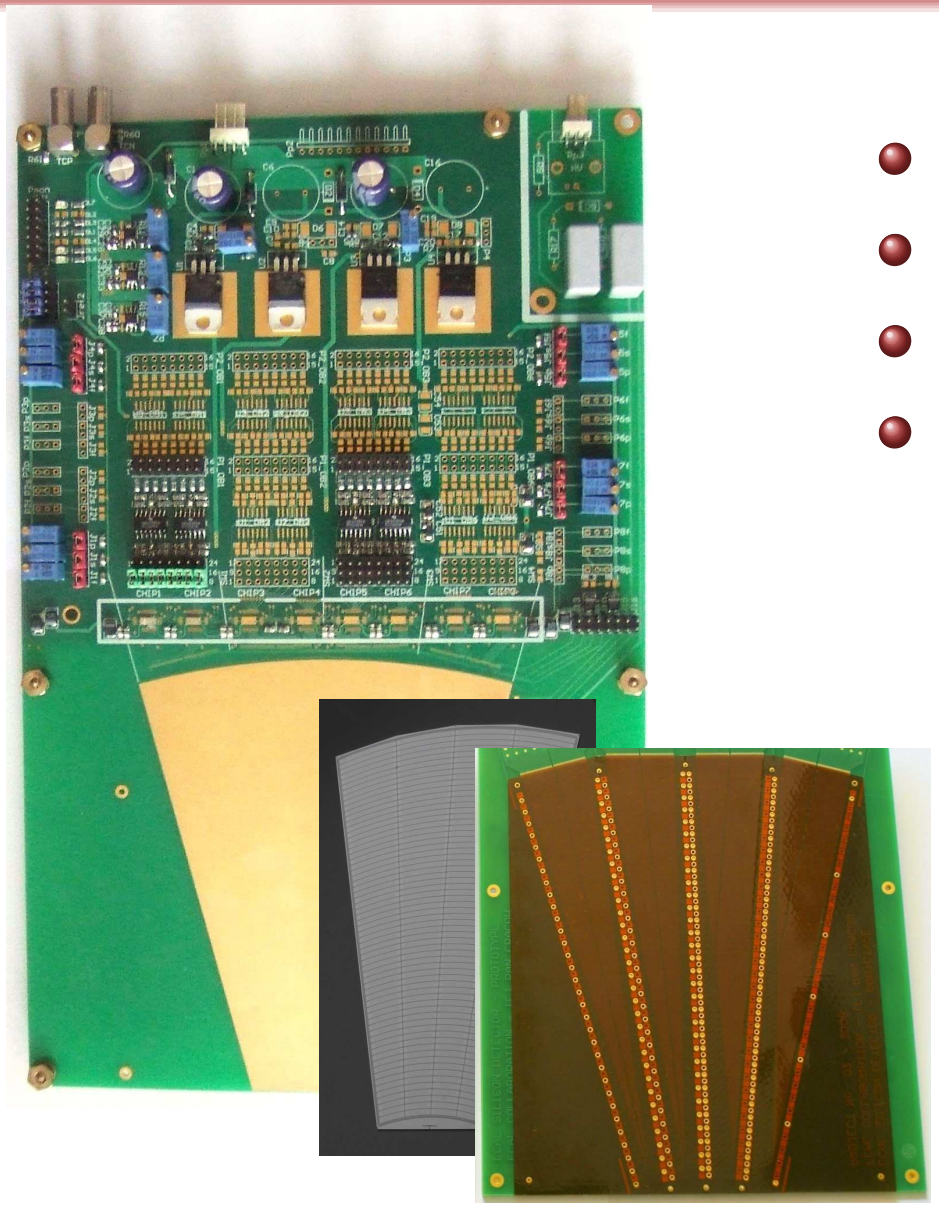


LumiCal data concentration

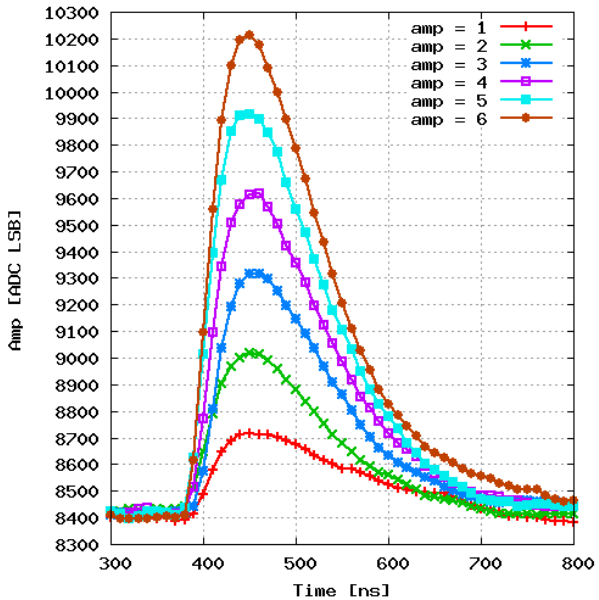


- one ADC for each FE channel
- one FPGA (or ASIC in the future) per sensor tail (256 channels — 4 or 8 ASICs)
- one master FPGA transmitting data out per detector half-layer
- master FPGA is connected to DIF — first level of standard DAQ

First tests on beam



- dedicated PCB
- LumiCal sensors with fanout
- 8 front-end ASICs (64 channels)
- external ADC (multichannel ASIC ready)



EUDET milestones, deliverable and more . . .

- EUDET milestones and deliverable
  - prototypes of two readout ASICs: front-end and ADC are produced, tested and ready
  - front-end functionality with fanout and sensors was confirmed during test beam
- more (in view of complete detector readout)
  - complex readout — multichannel ADC including: multiplexer, DACs, LVDS, bandgap based references and temperature sensor is in advance stage
  - works on PLL based 1 GHz wire transmitter on progress

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Future plans — AIDA

- re-design of front-end ASIC according to upgraded detector specification
- design a complete multichannel readout system (already started with multichannel ADC ASIC)
- proceed with data concentration and system powering
- continue the works on fast wire transmitter (already started with first PLL prototype)
- move some readout blocks to smaller size technology (promising candidate IBM 0.13 μm, works already started)

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Summary

- EUDET milestones and deliverable accomplished — prototypes of readout ASICs: front-end and ADC ready and fully working
- first test beam with sensor, fanout and front-end succeeded
- works on complete sensors readout in advanced stage (multichannel ADC, DAC, LVDS etc.)
- the goal is to have a prototype of multilayer detector at the end of AIDA

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